

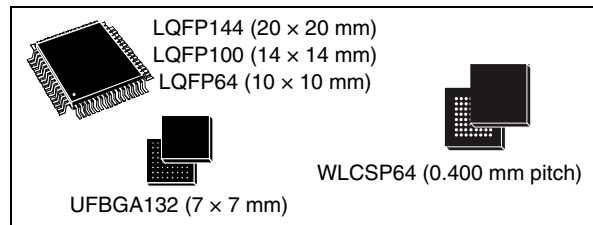


# STM32L151xC STM32L152xC

Ultralow power ARM-based 32-bit MCU with 256 KB Flash, RTC, LCD, USB, analog functions, 10 serial ports, memory I/F

## Features

- Operating conditions
  - Operating power supply range: 1.65 V to 3.6 V (without BOR) or 1.8 V to 3.6 V
- Low power features
  - 7 modes: Sleep, Low-power run (11  $\mu$ A at 32 kHz), Low-power sleep (4.4  $\mu$ A), Stop with RTC, Stop (650 nA), Standby with RTC, Standby (300 nA)
  - Dynamic core voltage scaling down to 233  $\mu$ A/MHz
  - Ultralow leakage per I/O: 50 nA max
  - Fast wakeup time from Stop: 8  $\mu$ s
  - Three wakeup pins
- Core: ARM 32-bit Cortex™-M3 CPU
  - 32 MHz maximum frequency, 33.3 DMIPS peak (Dhrystone 2.1)
  - Memory protection unit
- Reset and supply management
  - Low power, ultrasafe BOR (brownout reset)
  - Ultralow power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 1 to 24 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 16 MHz factory-trimmed RC
  - Internal 37 kHz low consumption RC
  - Internal multispeed low power RC, 65 kHz to 4.2 MHz
  - PLL for CPU clock and USB (48 MHz)
- Memories
  - 256 Kbytes of Flash memory with ECC
  - 8 Kbytes of data EEPROM with ECC
  - 32 Kbytes of RAM
- Low power calendar RTC
  - Alarm, periodic wakeup from Stop/Standby
- Up to 116 fast I/Os (102 of which are 5 V-tolerant)
- DMA: 12-channel DMA controller



- LCD 8 × 40 or 4 × 44 with step-up converter
- 2 operational amplifiers
- 12-bit ADC up to 1 Msps and 40 channels
  - Operational amplifier output, temperature sensor and internal voltage reference
  - Operates down to 1.8 V
- Two 12-bit DACs with output buffers
- Two ultralow power comparators
  - Window mode and wakeup capability
- 11 timers: one 32-bit and six 16-bit general-purpose timers, two 16-bit basic timers, two watchdog timers (independent and window)
- Up to 12 communication interfaces
  - Up to two I2C interfaces (SMBus/PMBus)
  - Up to three USARTs
  - Up to three SPIs (16 Mbit/s), two with I2S
  - USB 2.0 full-speed interface
- Up to 36 capacitive sensing channels supporting touch, proximity, linear and rotary sensors
- 32-bit CRC calculation unit, 96-bit unique ID

Table 1. Device summary

| Reference   | Part number  |
|-------------|--|
| STM32L151xC | STM32L151QC STM32L151RC<br>STM32L151VC STM32L151ZC |
| STM32L152xC | STM32L152QC STM32L152RC<br>STM32L152VC STM32L152ZC |

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the medium density plus STM32L151xC and STM32L152xC ultralow power ARM Cortex™-based microcontrollers product line. Medium density plus STM32L15xxC devices are microcontrollers with a Flash memory density of 256 Kbytes.

The medium density plus ultralow power STM32L15xxC family includes devices in 5 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the medium density plus ultralow power STM32L15xxC microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, Video intercom
- Utility metering

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the [www.arm.com](http://www.arm.com) website at the following address: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337g>.

*Figure 1* shows the general block diagram of the device family.

## 2 Description

The medium density plus ultralow power STM32L15xxC incorporates the connectivity power of the universal serial bus (USB) with the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 256 Kbytes and RAM up to 32 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All medium density plus devices offer two operational amplifiers, one 12-bit ADC, two DACs, two ultralow power comparators, one general-purpose 32-bit timer, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the medium density plus STM32L15xxC devices contain standard and advanced communication interfaces: up to two I<sup>2</sup>Cs, three SPIs, two I2S, three USARTs, and a USB. Up to 36 channels are available for capacitive sensing directly driven through GPIOs and general purpose timers.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller has a built-in LCD voltage generator that allows you to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The medium density plus ultralow power STM32L15xxC operates from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +85 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



## 2.1 Device overview

Table 2. Ultralow power STM32L15xxC device features and peripheral counts

| Peripheral  |                  | STM32L15xRC   | STM32L15xVC       | STM32L15xZC<br>STM32L15xQC |
|---|------------------|---|-------------------|----------------------------|
| Flash - Kbytes                                      |                  | 256   | 256               | 256                        |
| Data EEPROM   |                  | 8   | 8                 | 8                          |
| RAM - Kbytes  |                  | 32  | 32                | 32                         |
| Timers  | 32 bit           | 1   | 1                 | 1                          |
|   | General-purpose  | 6   | 6                 | 6                          |
|   | Basic            | 2   | 2                 | 2                          |
| Communication interfaces                            | SPI/(I2S)        | 3/(2)   | 3/(2)             | 3/(2)                      |
|   | I <sup>2</sup> C | 2   | 2                 | 2                          |
|   | USART            | 3   | 3                 | 3                          |
|   | USB              | 1   | 1                 | 1                          |
| GPIOs   |                  | 51  | 83                | 115 <sup>(1)</sup>         |
| Operation amplifiers                                |                  | 2   | 2                 | 2                          |
| 12-bit synchronized ADC<br>Number of channels       |                  | 1<br>21   | 1<br>25           | 1<br>40                    |
| 12-bit DAC<br>Number of channels                    |                  | 2<br>2  | 2<br>2            | 2<br>2                     |
| LCD <sup>(2)</sup><br>COM x SEG                     |                  | 1<br>4x32 or 8x28   | 1<br>4x44 or 8x40 | 1<br>4x44 or 8x40          |
| Comparators   |                  | 2   | 2                 | 2                          |
| Capacitive sensing<br>No. of channels/No. of groups |                  | 30/10   | 30/10             | 36/11                      |
| CPU frequency                                       |                  | 32 MHz  |                   |                            |
| Operating voltage                                   |                  | 1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option<br>1.65 V to 3.6 V without BOR option |                   |                            |
| Operating temperatures                              |                  | Ambient temperature: -40 to +85 °C<br>Junction temperature: -40 to + 105 °C                         |                   |                            |
| Packages  |                  | LQFP64, WLCSP64   | LQFP100           | LQFP144, BGA132            |

1. 109 GPIOs in BGA132 package

2. STM32L152xx devices only.

## 2.2 Ultralow power device continuum

The ultralow power STM32L15xxD, STM32L162xD, and STM32L15xxC are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultralow power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics 0.13 µm ultralow leakage process.

*Note: The ultralow power STM32L and general-purpose STM32Fxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.*

### 2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex™-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultralow power performance to range from 5 up to 33.3 DMIPs.

### 2.2.2 Shared peripherals

STM8L15xxx, STM32L15xxx, and STM32L162xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC, and comparators
- Digital peripherals: RTC and some communication interfaces

### 2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx, and STM32L162xx families use a common architecture:

- Same power supply range from 1.65 V to 3.6 V.
- Architecture optimized to reach ultralow consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

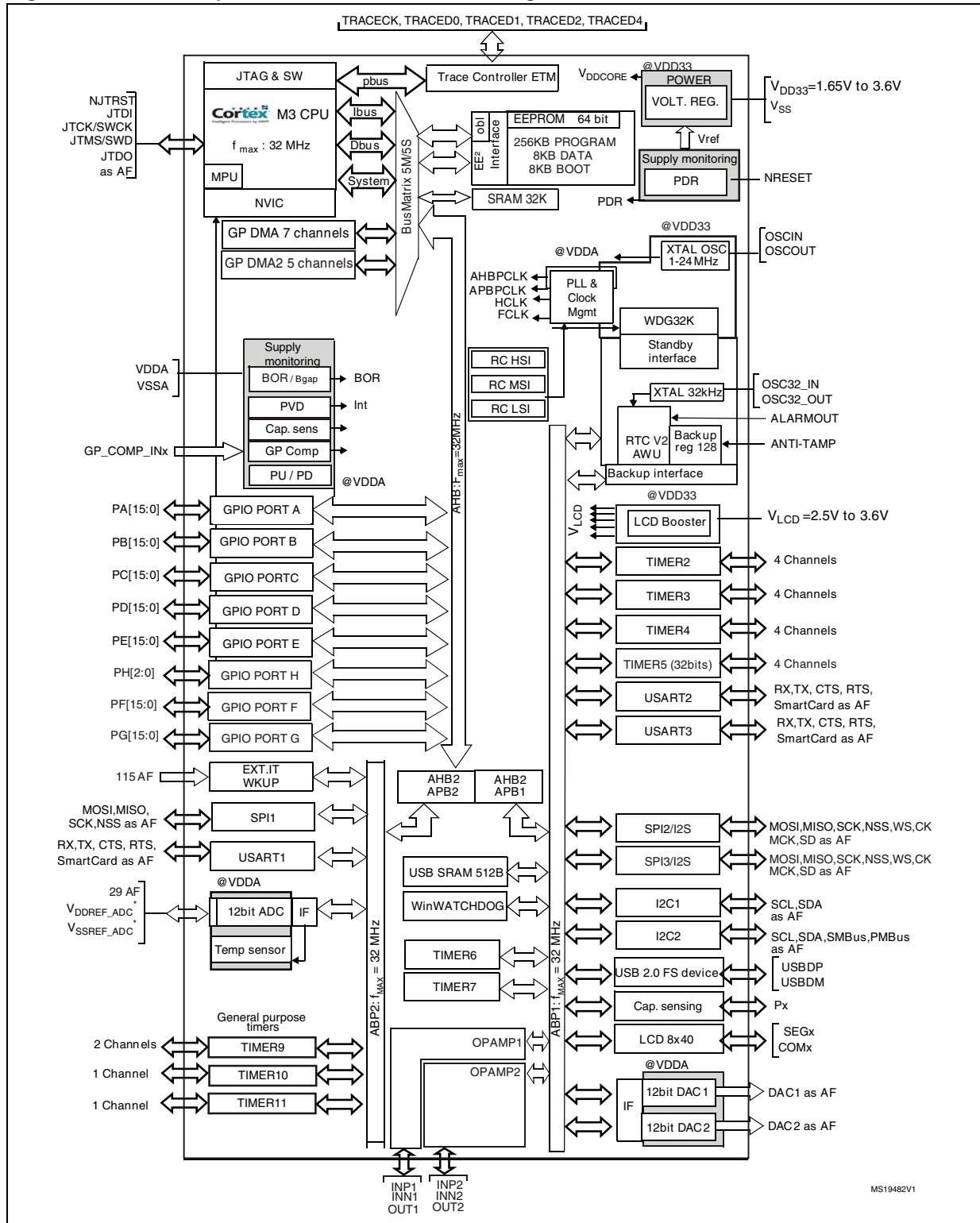
### 2.2.4 Features

ST ultralow power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 384 Kbytes

### 3 Functional overview

Figure 1. Ultralow power STM32L15xxC block diagram



1. Legend:
- AF: alternate function
  - ADC: analog-to-digital converter
  - BOR: brown out reset
  - DMA: direct memory access
  - DAC: digital-to-analog converter
  - I<sup>2</sup>C: inter-integrated circuit multimaster interface

### 3.1 Low power modes

The ultralow power STM32L15xxC supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 ( $V_{DD}$  range limited to 2.0-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full  $V_{DD}$  range), with a maximum CPU frequency of 16 MHz
- Range 3 (full  $V_{DD}$  range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source).

Seven low power modes are provided to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**  
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.
- **Low power run mode**  
This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (131 kHz), execution from SRAM or Flash memory, and internal regulator in low power mode to minimize the regulator's operating current. In Low power run mode, the clock frequency and the number of enabled peripherals are both limited.
- **Low power sleep mode**  
This mode is achieved by entering Sleep mode with the internal voltage regulator in Low power mode to minimize the regulator's operating current. In Low power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.  
When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.
- **Stop mode with RTC**  
Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the  $V_{CORE}$  domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low power mode.  
The device can be woken up from Stop mode by any of the EXTI line, in 8  $\mu$ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), It can be, the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event, the RTC wakeup.

- **Stop mode without RTC**

Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8  $\mu$ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.
- **Standby mode with RTC**

Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire  $V_{CORE}$  domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC\_CSR).

The device exits Standby mode in 60  $\mu$ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.
- **Standby mode without RTC**

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire  $V_{CORE}$  domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC\_CSR).

The device exits Standby mode in 60  $\mu$ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

*Note:* The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

## 3.2 ARM<sup>®</sup> Cortex<sup>™</sup>-M3 core with MPU

The ARM Cortex<sup>™</sup>-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex<sup>™</sup>-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L15xxC is compatible with all ARM tools and software.

### Nested vectored interrupt controller (NVIC)

The ultralow power STM32L15xxC embeds a nested vectored interrupt controller able to handle up to 53 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.3 Reset and supply management

### 3.3.1 Power supply schemes

- $V_{DD} = 1.65$  to  $3.6$  V: external power supply for I/Os and the internal regulator. Provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA} = 1.65$  to  $3.6$  V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to  $V_{DDA}$  is  $1.8$  V when the ADC is used).  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD}$  and  $V_{SS}$ , respectively.

### 3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between  $1.8$  V and  $3.6$  V.
- The other version without BOR at power up operates between  $1.65$  V and  $3.6$  V.

As the BOR can be activated and deactivated at run time, this distinction is important only for power-up phase.

When BOR is active at power-on, it ensures proper operation starting from  $1.8$  V whatever the power ramp-up phase before it reaches  $1.8$  V. When BOR is not active at power-up, the power ramp-up should guarantee that  $1.65$  V is reached on  $V_{DD}$  at least  $1$  ms after it exits the POR area.

After the  $V_{DD}$  threshold is reached ( $1.65$  V or  $1.8$  V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently: in this case, the  $V_{DD}$  min value at power down is  $1.65$  V.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage ( $V_{REFINT}$ ) in Stop mode. The device remains in reset mode when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$  or  $V_{BOR}$ , without the need for any external reset circuit.

*Note:* The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}/V_{DDA}$  power supply and compares it to the  $V_{PVD}$  threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when  $V_{DD}/V_{DDA}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}/V_{DDA}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low power run, Low power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wake-up logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC\_CSR).

### 3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot from Flash usually boots at the beginning of the Flash (bank 1). An additional boot mechanism is available through user option byte, to allow booting from bank 2 when bank 2 contains valid code. This dual boot capability can be used to easily implement a secure field software update mechanism.

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USART1 and USART2.

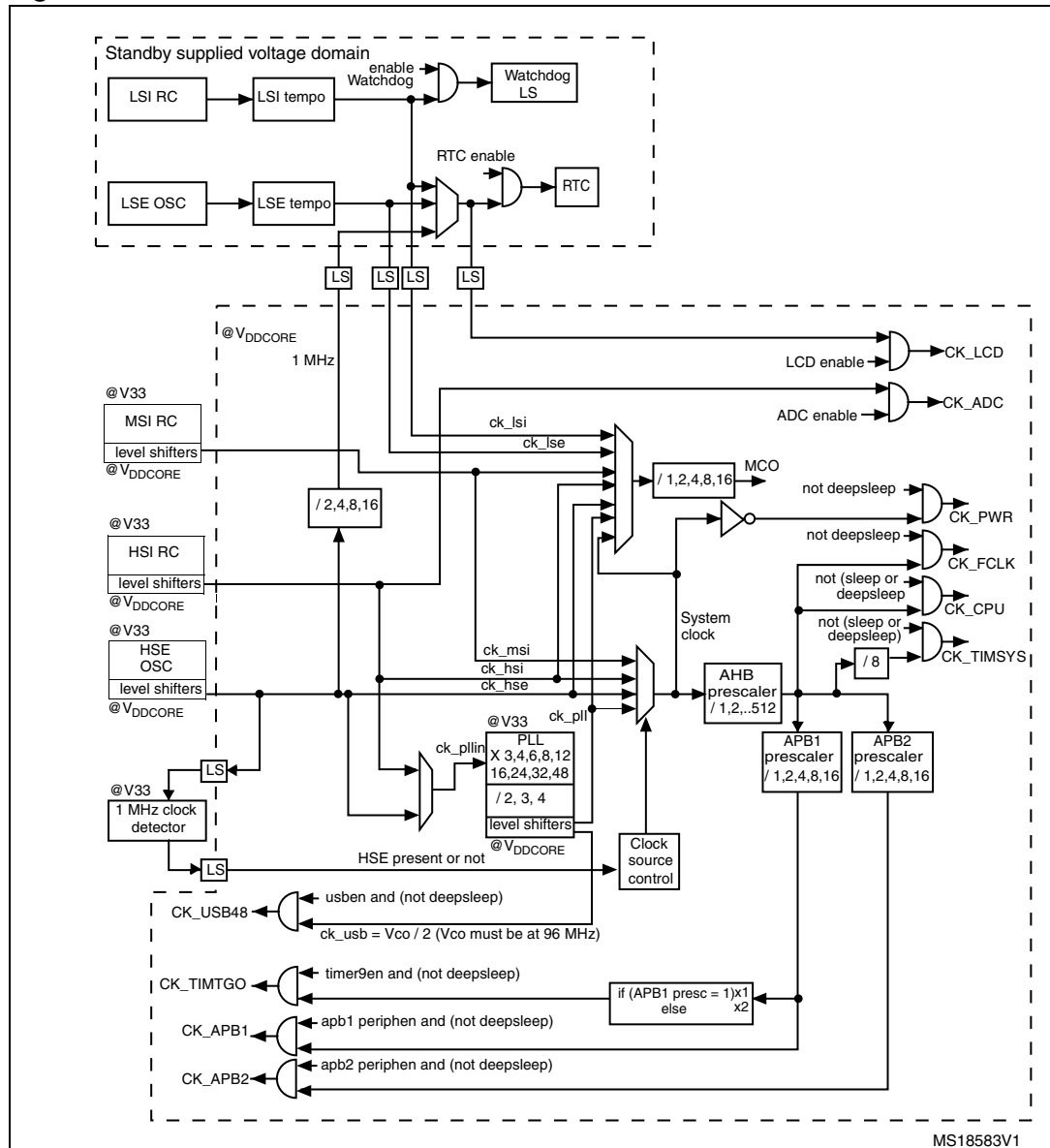
## 3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** three different clock sources can be used to drive the master clock SYSCLK:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a  $\pm 0.5\%$  accuracy.
- **Auxiliary clock source:** two ultralow power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

Figure 2. Clock tree



1. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 24 MHz or 32 MHz.

### 3.5 Low power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120  $\mu$ s to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

The RTC can also be automatically corrected with a 50/60Hz stable powerline.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronisation.

A time stamp can record an external event occurrence, and generates an interrupt.

There are thirty-two 32-bit backup registers provided to store 128 bytes of user application data. They are cleared in case of tamper detection.

Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

### 3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high-current-capable except for analog pins. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

#### External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 115 GPIOs can be connected to the 16 external interrupt lines. The 7 other lines are connected to RTC, PVD, USB or Comparator events.

## 3.7 Memories

The STM32L15xxC devices have the following features:

- 32 Kbyte of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 256 Kbyte of embedded Flash program memory
  - 8 Kbyte of data EEPROM
  - Options bytes

The options bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

## 3.8 DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I<sup>2</sup>C, USART, general-purpose timers, DAC, and ADC.

## 3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of  $V_{DD}$ . This converter can be deactivated, in which case the  $V_{LCD}$  pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

### 3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L15xxC devices with up to 40 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs with up to 29 external channel in a group.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

#### Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between  $1.8\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$ . The temperature sensor is internally connected to the ADC\_IN16 input channel.

#### Voltage reference

An internal precise voltage reference can be measured through the ADC. It enables accurate monitoring of the  $V_{\text{DD}}$  value (when no external voltage,  $V_{\text{REF+}}$ , is available for ADC).

### 3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- Up to 10-bit output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage  $V_{\text{REF+}}$

Eight DAC trigger inputs are used in the STM32L15xxC. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

### 3.12 Operational amplifier

The STM32L15xxC embeds two operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

The operational amplifiers feature:

- Low input bias current
- Low offset voltage
- Low power mode
- Rail-to-rail input

### 3.13 Ultralow power comparators and reference voltage

The STM32L15xxC embeds two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage ( $V_{REFINT}$ ) or a submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low power / low current output buffer (driving current capability of 1  $\mu$ A typical).

### 3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage  $V_{REFINT}$ .

### 3.15 Touch sensing

The STM32L15xxC devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In the STM32L15xxC, this acquisition is managed directly by the GPIOs, timers and analog I/O groups (see [Section 3.14: System configuration controller and routing interface](#)).

Reliable touch sensing solution can be quickly and easily implemented using the free STM32 touch sensing firmware library.

### 3.16 Timers and watchdogs

The ultralow power STM32L15xxC devices include seven general-purpose timers, two basic timers, and two watchdog timers.

[Table 3](#) compares the features of the general-purpose and basic timers.

**Table 3. Timer feature comparison**

| Timer            | Counter resolution | Counter type      | Prescaler factor                | DMA request generation | Capture/compare channels | Complementary outputs |
|------------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|-----------------------|
| TIM2, TIM3, TIM4 | 16-bit             | Up, down, up/down | Any integer between 1 and 65536 | Yes                    | 4                        | No                    |
| TIM5             | 32-bit             | Up, down, up/down | Any integer between 1 and 65536 | Yes                    | 4                        | No                    |
| TIM9             | 16-bit             | Up, down, up/down | Any integer between 1 and 65536 | No                     | 2                        | No                    |
| TIM10, TIM11     | 16-bit             | Up                | Any integer between 1 and 65536 | No                     | 1                        | No                    |
| TIM6, TIM7       | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 0                        | No                    |

### 3.16.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L15xxC devices (see [Table 3](#) for differences).

#### TIM2, TIM3, TIM4, TIM5

TIM2, TIM3, TIM4 are based on 16-bit auto-reload up/down counter. TIM5 is based on a 32-bit auto-reload up/down counter. They include a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures/output compares/PWMs on the largest packages.

TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

#### TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

### 3.16.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

### 3.16.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

### 3.16.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

### 3.16.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

## 3.17 Communication interfaces

### 3.17.1 I<sup>2</sup>C bus

Up to two I<sup>2</sup>C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

### 3.17.2 Universal synchronous/asynchronous receiver transmitter (USART)

The three USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability. The three USARTs provide hardware management of the CTS and RTS signals.

All USART interfaces can be served by the DMA controller.

### 3.17.3 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

### 3.17.4 Inter-integrated sound (I<sup>2</sup>S)

Two standard I<sup>2</sup>S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 96 kHz are supported. When either or both of the I<sup>2</sup>S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

### 3.17.5 Universal serial bus (USB)

The STM32L15xxC embeds a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

### 3.18 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 3.19 Development support

#### Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

#### Embedded Trace Macrocell™

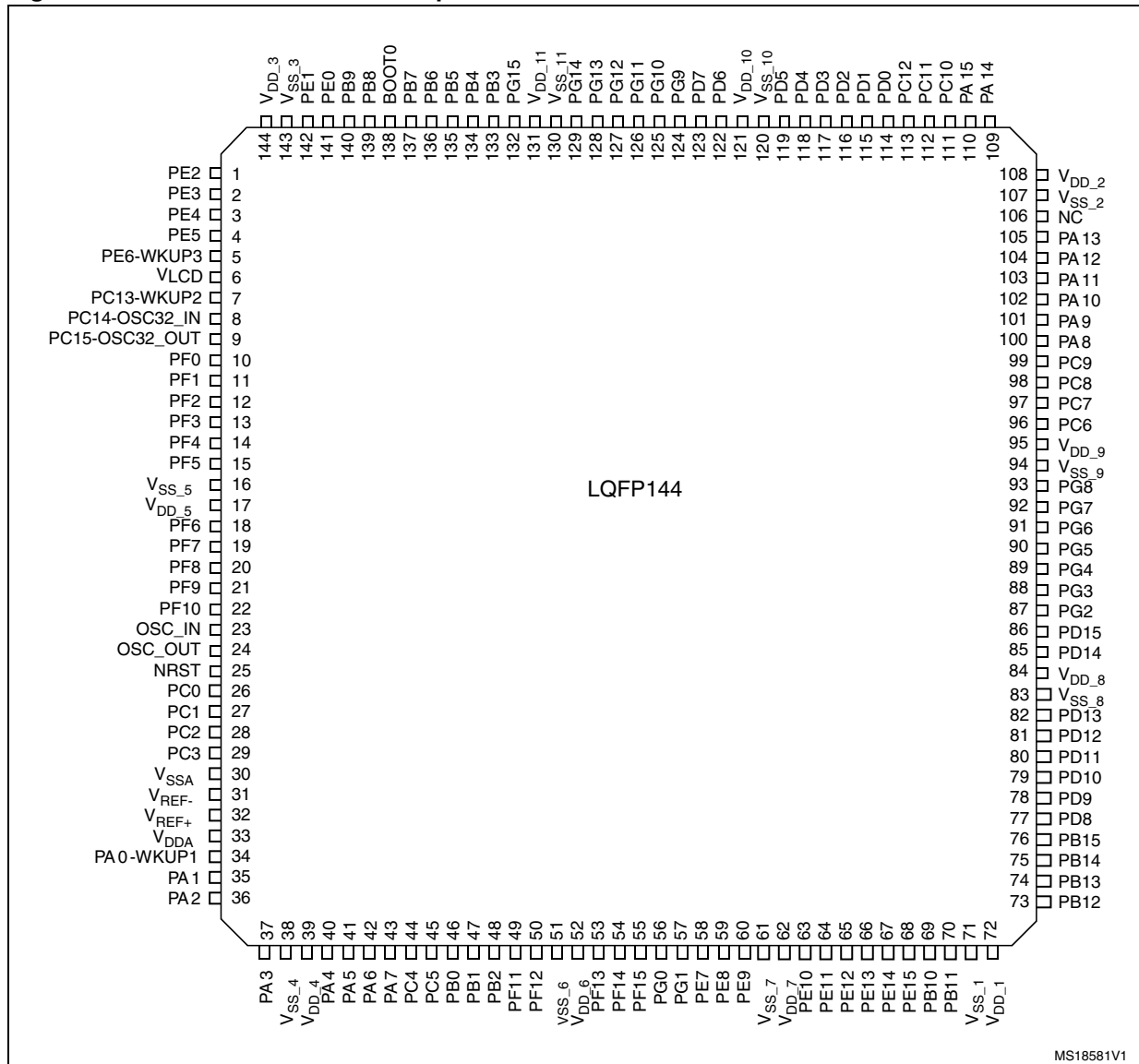
The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L15xxC through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

## 4 Pin descriptions

**Table 4. STM32L15xQC BGA132 ballout**

|          | 1                      | 2                 | 3                   | 4                   | 5   | 6                 | 7                  | 8    | 9    | 10   | 11                | 12                |
|----------|------------------------|-------------------|---------------------|---------------------|-----|-------------------|--------------------|------|------|------|-------------------|-------------------|
| <b>A</b> | PE3                    | PE1               | PB8                 | BOOT0               | PD7 | PD5               | PB4                | PB3  | PA15 | PA14 | PA13              | PA12              |
| <b>B</b> | PE4                    | PE2               | PB9                 | PB7                 | PB6 | PD6               | PD4                | PD3  | PD1  | PC12 | PC10              | PA11              |
| <b>C</b> | PC13-<br>WKUP2         | PE5               | PE0                 | V <sub>DD_3</sub>   | PB5 | PG14              | PG13               | PD2  | PD0  | PC11 | PH2               | PA10              |
| <b>D</b> | PC14-<br>OSC32<br>_IN  | PE6-<br>WKUP3     | V <sub>SS_3</sub>   | PF2                 | PF1 | PF0               | PG12               | PG10 | PG9  | PA9  | PA8               | PC9               |
| <b>E</b> | PC15-<br>OSC32<br>_OUT | VLCD              | V <sub>SS_6</sub>   | PF3                 |     |                   |                    |      | PG5  | PC8  | PC7               | PC6               |
| <b>F</b> | PH0<br>OSC_IN          | V <sub>SS_5</sub> | PF4                 | PF5                 |     | V <sub>SS_9</sub> | V <sub>SS_10</sub> |      | PG3  | PG4  | V <sub>SS_2</sub> | V <sub>SS_1</sub> |
| <b>G</b> | PH1<br>OSC_<br>OUT     | V <sub>DD_5</sub> | PF6                 | PF7                 |     | V <sub>DD_9</sub> | V <sub>DD_10</sub> |      | PG1  | PG2  | V <sub>DD_2</sub> | V <sub>DD_1</sub> |
| <b>H</b> | PC0                    | NRST              | V <sub>DD_6</sub>   | PF8                 |     |                   |                    |      | PG0  | PD15 | PD14              | PD13              |
| <b>J</b> | V <sub>SSA</sub>       | PC1               | PC2                 | PA4                 | PA7 | PF9               | PF12               | PF14 | PF15 | PD12 | PD11              | PD10              |
| <b>K</b> | NC                     | PC3               | PA2                 | PA5                 | PC4 | PF11              | PF13               | PD9  | PD8  | PB15 | PB14              | PB13              |
| <b>L</b> | V <sub>REF+</sub>      | PA0-<br>WKUP1     | PA3                 | PA6                 | PC5 | PB2               | PE8                | PE10 | PE12 | PB10 | PB11              | PB12              |
| <b>M</b> | V <sub>DDA</sub>       | PA1               | OPAM<br>P1_<br>VINM | OPAMP<br>2_<br>VINM | PB0 | PB1               | PE7                | PE9  | PE11 | PE13 | PE14              | PE15              |

Figure 3. STM32L15xZC LQFP144 pinout



MS18581V1

Figure 4. STM32L15xVC LQFP100 pinout

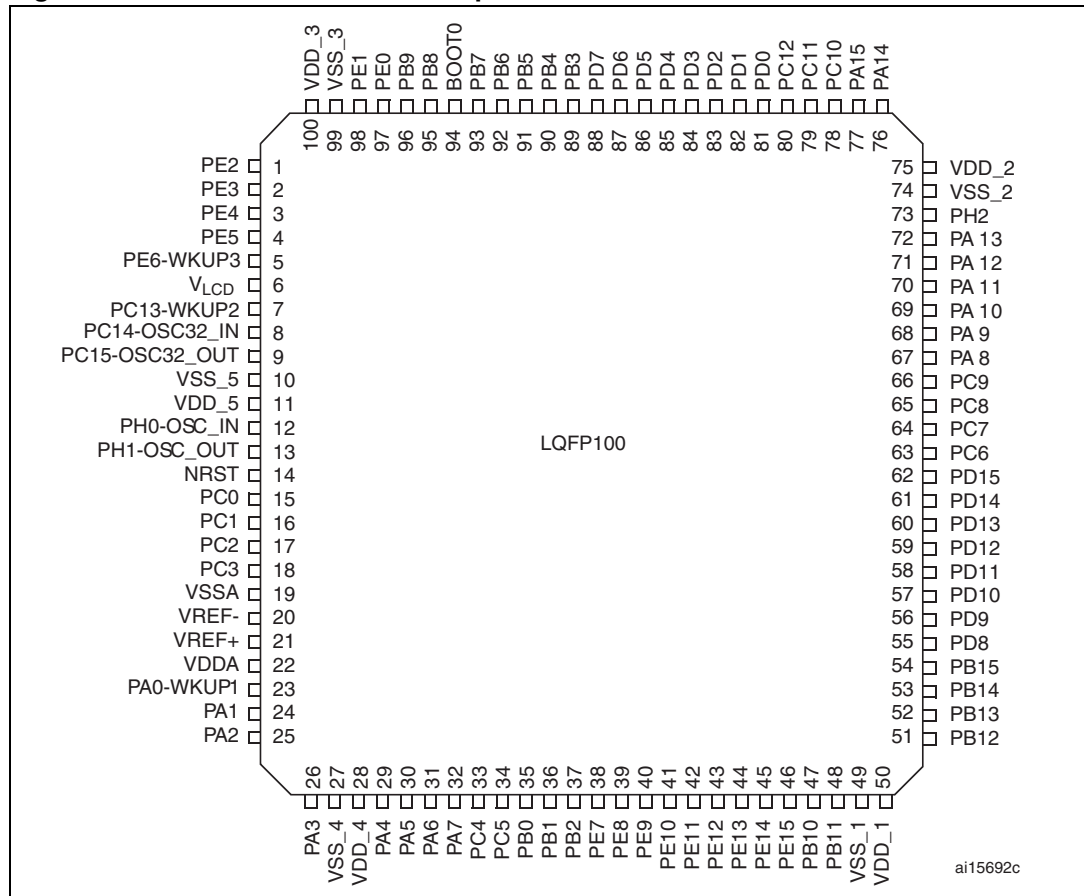


Figure 5. STM32L15xRC LQFP64 pinout

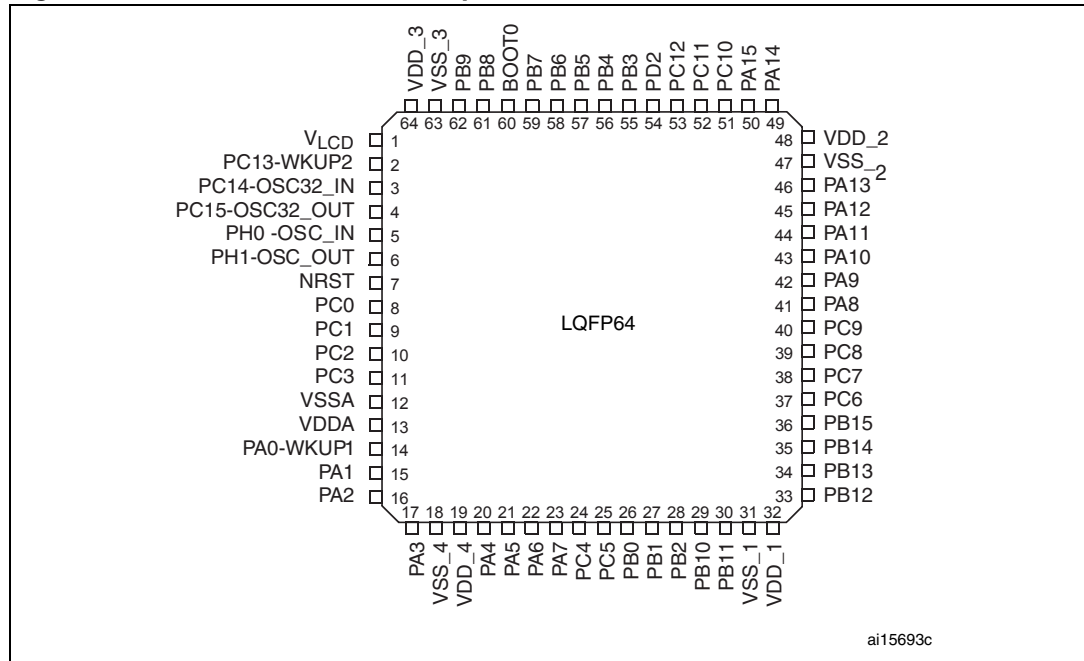


Table 5. STM32L15xRC WLCSP64 ballout

|          | 8                 | 7                  | 6                 | 5                 | 4    | 3    | 2                 | 1                 |
|----------|-------------------|--------------------|-------------------|-------------------|------|------|-------------------|-------------------|
| <b>A</b> | V <sub>DD_3</sub> | V <sub>SS_3</sub>  | BOOT0             | PB5               | PB3  | PD2  | PC10              | V <sub>DD_2</sub> |
| <b>B</b> | PC14-<br>OSC32_IN | PC15-<br>OSC32_OUT | PB9               | PB6               | PB4  | PC11 | PA14              | V <sub>SS_2</sub> |
| <b>C</b> | PC13-<br>WKUP2    | NRST               | V <sub>LCD</sub>  | PB7               | PC12 | PA15 | PA12              | PA11              |
| <b>D</b> | PH0-<br>OSC_IN    | PH1-<br>OSC_OUT    | PC2               | PB8               | PA13 | PA10 | PA9               | PC9               |
| <b>E</b> | PC0               | V <sub>SSA</sub>   | PA1               | PA5               | PA8  | PC8  | PC7               | PC6               |
| <b>F</b> | PC1               | PC3                | PA0-<br>WKUP1     | V <sub>SS_4</sub> | PB1  | PB11 | PB14              | PB15              |
| <b>G</b> | V <sub>DDA</sub>  | PA3                | V <sub>DD_4</sub> | PA6               | PA7  | PB10 | PB12              | PB13              |
| <b>H</b> | PA2               | PA4                | PC4               | PC5               | PB0  | PB2  | V <sub>SS_1</sub> | V <sub>DD_1</sub> |

Table 6. STM32L15xxC pin definitions

| Pins    |          |         |        |         | Pin name                         | Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Main function <sup>(3)</sup><br>(after reset) | Alternate functions            |
|---------|----------|---------|--------|---------|----------------------------------|---------------------|--------------------------|---|--------------------------------|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP64 |                                  |                     |                          |   |                                |
| 1       | B2       | 1       | -      | -       | PE2                              | I/O                 | FT                       | PE2   | TIM3_ETR/LCD_SEG38/TRACECK     |
| 2       | A1       | 2       | -      | -       | PE3                              | I/O                 | FT                       | PE3   | TIM3_CH1/LCD_SEG39/TRACED0     |
| 3       | B1       | 3       | -      | -       | PE4                              | I/O                 | FT                       | PE4   | TIM3_CH2/TRACED1               |
| 4       | C2       | 4       | -      | -       | PE5                              | I/O                 | FT                       | PE5   | TIM9_CH1/TRACED2               |
| 5       | D2       | 5       | -      | -       | PE6-<br>WKUP3                    | I/O                 | FT                       | PE6   | WKUP3/TAMPER3/TIM9_CH2/TRACED3 |
| 6       | E2       | 6       | 1      | C6      | V <sub>LCD</sub> <sup>(4)</sup>  | S                   |                          | V <sub>LCD</sub>                              |                                |
| 7       | C1       | 7       | 2      | C8      | PC13-WKUP2                       | I/O                 | FT                       | PC13  | WKUP2/TAMPER1/RTC_AF1          |
| 8       | D1       | 8       | 3      | B8      | PC14-<br>OSC32_IN <sup>(5)</sup> | I/O                 |                          | PC14  | OSC32_IN                       |
| 9       | E1       | 9       | 4      | B7      | PC15-<br>OSC32_OUT               | I/O                 |                          | PC15  | OSC32_OUT                      |
| 10      | D6       | -       | -      | -       | PF0                              | I/O                 | FT                       | PF0   |                                |
| 11      | D5       | -       | -      | -       | PF1                              | I/O                 | FT                       | PF1   |                                |
| 12      | D4       | -       | -      | -       | PF2                              | I/O                 | FT                       | PF2   |                                |
| 13      | E4       | -       | -      | -       | PF3                              | I/O                 | FT                       | PF3   |                                |
| 14      | F3       | -       | -      | -       | PF4                              | I/O                 | FT                       | PF4   |                                |
| 15      | F4       | -       | -      | -       | PF5                              | I/O                 | FT                       | PF5   |                                |
| 16      | F2       | 10      | -      | -       | V <sub>SS_5</sub>                | S                   |                          | V <sub>SS_5</sub>                             |                                |
| 17      | G2       | 11      | -      | -       | V <sub>DD_5</sub>                | S                   |                          | V <sub>DD_5</sub>                             |                                |
| 18      | G3       | -       | -      | -       | PF6                              | I/O                 | FT                       | PF6   | TIM5_CH1/TIM5_ETR/ADC_IN27     |
| 19      | G4       | -       | -      | -       | PF7                              | I/O                 | FT                       | PF7   | TIM5_CH2/ADC_IN28/COMP1_INP    |
| 20      | H4       | -       | -      | -       | PF8                              | I/O                 | FT                       | PF8   | TIM5_CH3/ADC_IN29/COMP1_INP    |
| 21      | J6       | -       | -      | -       | PF9                              | I/O                 | FT                       | PF9   | TIM5_CH4/ADC_IN30/COMP1_INP    |
| 22      | -        | -       | -      | -       | PF10                             | I/O                 | FT                       | PF10  | ADC_IN30/COMP1_INP             |
| 23      | F1       | 12      | 5      | D8      | PH0-OSC_IN <sup>(6)</sup>        | I                   |                          | PH0   | OSC_IN                         |
| 24      | G1       | 13      | 6      | D7      | PH1-<br>OSC_OUT <sup>(6)</sup>   | O                   |                          | PH1   | OSC_VOUT                       |
| 25      | H2       | 14      | 7      | C7      | NRST                             | I/O                 |                          | NRST  |                                |
| 26      | H1       | 15      | 8      | E8      | PC0                              | I/O                 | FT                       | PC0   | LCD_SEG18/ADC_IN10/COMP1_INP   |
| 27      | J2       | 16      | 9      | F8      | PC1                              | I/O                 | FT                       | PC1   | LCD_SEG19/ADC_IN11/COMP1_INP   |
| 28      | -        | 17      | 10     | D6      | PC2                              | I/O                 | FT                       | PC2   | LCD_SEG20/ADC_IN12/COMP1_INP   |
| -       | J3       | -       | -      | -       | PC2                              | I/O                 | FT                       | PC2   | LCD_SEG20/ADC_IN12/COMP1_INP   |
| -       | K1       | -       | -      | -       | NC                               | I                   |                          |   |                                |
| 29      | K2       | 18      | 11     | F7      | PC3                              | I/O                 |                          | PC3   | LCD_SEG21/ADC_IN13/COMP1_INP   |
| 30      | J1       | 19      | 12     | E7      | V <sub>SSA</sub>                 | S                   |                          | V <sub>SSA</sub>                              |                                |
| 31      | -        | 20      | -      | -       | V <sub>REF-</sub>                | S                   |                          | V <sub>REF-</sub>                             |                                |

Table 6. STM32L15xxC pin definitions (continued)

| Pins    |          |         |        |         | Pin name          | Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Main function <sup>(3)</sup><br>(after reset) | Alternate functions   |
|---------|----------|---------|--------|---------|-------------------|---------------------|--------------------------|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP64 |                   |                     |                          |   |   |
| 32      | L1       | 21      | -      | -       | V <sub>REF+</sub> | S                   |                          | V <sub>REF+</sub>                             |   |
| 33      | M1       | 22      | 13     | G8      | V <sub>DDA</sub>  | S                   |                          | V <sub>DDA</sub>                              |   |
| 34      | L2       | 23      | 14     | F6      | PA0-WKUP1         | I/O                 | FT                       | PA0   | WKUP1/TAMPER2/TIM2_CH1_ETR/TIM5_CH1/<br>USART2_CTS/ADC_IN0/COMP1_INP                |
| 35      | M2       | 24      | 15     | E6      | PA1               | I/O                 | FT                       | PA1   | TIM2_CH2/TIM5_CH2/<br>USART2_RTS/LCD_SEG0/<br>ADC_IN1/COMP1_INP/OPAMP1_VINP         |
| 36      | -        | 25      | 16     | H8      | PA2               | I/O                 | FT                       | PA2   | TIM2_CH3/TIM5_CH3/TIM9_CH1/USART2_TX/<br>LCD_SEG1/ADC_IN2/<br>COMP1_INP/OPAMP1_VINM |
| -       | K3       | -       | -      | -       | PA2               | I/O                 | FT                       | PA2   | TIM2_CH3/TIM5_CH3/TIM9_CH1/USART2_TX/<br>LCD_SEG1/ADC_IN2/COMP1_INP                 |
| -       | M3       | -       | -      | -       | OPAMP1_VINM       | I                   |                          | OPAMP1_VI<br>NM                               |   |
| 37      | L3       | 26      | 17     | G7      | PA3               | I/O                 |                          | PA3   | TIM2_CH4/TIM5_CH4/TIM9_CH2/USART2_RX/<br>LCD_SEG2/<br>ADC_IN3/COMP1_INP/OPAMP1_OUT  |
| 38      | -        | 27      | 18     | F5      | V <sub>SS_4</sub> | S                   |                          | V <sub>SS_4</sub>                             |   |
| 39      | -        | 28      | 19     | G6      | V <sub>DD_4</sub> | S                   |                          | V <sub>DD_4</sub>                             |   |
| 40      | J4       | 29      | 20     | H7      | PA4               | I/O                 |                          | PA4   | SPI1_NSS/SPI3_NSS/ I2S3_WS/USART2_CK/<br>ADC_IN4/DAC_OUT1/COMP1_INP                 |
| 41      | K4       | 30      | 21     | E5      | PA5               | I/O                 |                          | PA5   | TIM2_CH1_ETR/SPI1_SCK/ADC_IN5/DAC_OUT<br>2/<br>COMP1_INP                            |
| 42      | L4       | 31      | 22     | G5      | PA6               | I/O                 | FT                       | PA6   | TIM3_CH1/TIM10_CH1/SPI1_MISO/LCD_SEG3/<br>ADC_IN6/COMP1_INP/OPAMP2_VINP             |
| 43      | -        | 32      | 23     | G4      | PA7               | I/O                 | FT                       | PA7   | TIM3_CH2/TIM11_CH1/ SPI1_MOSI/LCD_SEG4/<br>ADC_IN7/COMP1_INP/OPAMP2_VINM            |
| -       | J5       | -       | -      | -       | PA7               | I/O                 | FT                       | PA7   | TIM3_CH2/TIM11_CH1/ SPI1_MOSI/LCD_SEG4/<br>ADC_IN7/COMP1_INP                        |
| -       | M4       | -       | -      | -       | OPAMP2_VINM       | I                   |                          | OPAMP2_VI<br>NM                               |   |
| 44      | K5       | 33      | 24     | H6      | PC4               | I/O                 | FT                       | PC4   | LCD_SEG22/ADC_IN14/COMP1_INP  |
| 45      | L5       | 34      | 25     | H5      | PC5               | I/O                 | FT                       | PC5   | LCD_SEG23/ADC_IN15/COMP1_INP  |
| 46      | M5       | 35      | 26     | H4      | PB0               | I/O                 |                          | PB0   | TIM3_CH3/LCD_SEG5/ADC_IN8/COMP1_INP/<br>VREF_OUT/ OPAMP2_VOUT                       |
| 47      | M6       | 36      | 27     | F4      | PB1               | I/O                 | FT                       | PB1   | TIM3_CH4/LCD_SEG6/ADC_IN9/COMP1_INP/<br>VREF_OUT                                    |
| 48      | L6       | 37      | 28     | H3      | PB2               | I/O                 | FT                       | PB2/BOOT1                                     | ADC_IN0b/COMP1_INP  |
| 49      | K6       | -       | -      | -       | PF11              | I/O                 | FT                       | PF11  | ADC_IN1b/COMP1_INP  |
| 50      | J7       | -       | -      | -       | PF12              | I/O                 | FT                       | PF12  | ADC_IN2b/COMP1_INP  |

Table 6. STM32L15xxC pin definitions (continued)

| Pins    |          |         |        |         | Pin name          | Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Main function <sup>(3)</sup><br>(after reset) | Alternate functions   |
|---------|----------|---------|--------|---------|-------------------|---------------------|--------------------------|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP64 |                   |                     |                          |   |   |
| 51      | E3       | -       | -      | -       | V <sub>SS_6</sub> | S                   |                          | V <sub>SS_6</sub>                             |   |
| 52      | H3       | -       | -      | -       | V <sub>DD_6</sub> | S                   |                          | V <sub>DD_6</sub>                             |   |
| 53      | K7       | -       | -      | -       | PF13              | I/O                 | FT                       | PF13  | ADC_IN3b/COMP1_INP  |
| 54      | J8       | -       | -      | -       | PF14              | I/O                 | FT                       | PF14  | ADC_IN6b/COMP1_INP  |
| 55      | J9       | -       | -      | -       | PF15              | I/O                 | FT                       | PF15  | ADC_IN7b/COMP1_INP  |
| 56      | H9       | -       | -      | -       | PG0               | I/O                 | FT                       | PG0   | ADC_IN8b/COMP1_INP  |
| 57      | G9       | -       | -      | -       | PG1               | I/O                 | FT                       | PG1   | ADC_IN9b/COMP1_INP  |
| 58      | M7       | 38      | -      | -       | PE7               | I/O                 |                          | PE7   | ADC_IN22/COMP1_INP  |
| 59      | L7       | 39      | -      | -       | PE8               | I/O                 |                          | PE8   | ADC_IN23/COMP1_INP  |
| 60      | M8       | 40      | -      | -       | PE9               | I/O                 |                          | PE9   | TIM2_CH1_ETR/ADC_IN24/COMP1_INP   |
| 61      | -        | -       | -      | -       | V <sub>SS_7</sub> | S                   |                          | V <sub>SS_7</sub>                             |   |
| 62      | -        | -       | -      | -       | V <sub>DD_7</sub> | S                   |                          | V <sub>DD_7</sub>                             |   |
| 63      | L8       | 41      | -      | -       | PE10              | I/O                 |                          | PE10  | TIM2_CH2/ADC_IN25/COMP1_INP   |
| 64      | M9       | 42      | -      | -       | PE11              | I/O                 | FT                       | PE11  | TIM2_CH3  |
| 65      | L9       | 43      | -      | -       | PE12              | I/O                 | FT                       | PE12  | TIM2_CH4/SPI1_NSS   |
| 66      | M10      | 44      | -      | -       | PE13              | I/O                 | FT                       | PE13  | SPI1_SCK  |
| 67      | M11      | 45      | -      | -       | PE14              | I/O                 | FT                       | PE14  | SPI1_MISO   |
| 68      | M12      | 46      | -      | -       | PE15              | I/O                 | FT                       | PE15  | SPI1_MOSI   |
| 69      | L10      | 47      | 29     | G3      | PB10              | I/O                 | FT                       | PB10  | TIM2_CH3/I2C2_SCL/USART3_TX/LCD_SEG10   |
| 70      | L11      | 48      | 30     | F3      | PB11              | I/O                 | FT                       | PB11  | TIM2_CH4/I2C2_SDA/ USART3_RX/LCD_SEG11  |
| 71      | F12      | 49      | 31     | H2      | V <sub>SS_1</sub> | S                   |                          | V <sub>SS_1</sub>                             |   |
| 72      | G12      | 50      | 32     | H1      | V <sub>DD_1</sub> | S                   |                          | V <sub>DD_1</sub>                             |   |
| 73      | L12      | 51      | 33     | G2      | PB12              | I/O                 | FT                       | PB12  | TIM10_CH1/I2C2_SMBA/SPI2_NSS/I2S2_WS/<br>USART3_CK/<br>LCD_SEG12/ADC_IN18/COMP1_INP |
| 74      | K12      | 52      | 34     | G1      | PB13              | I/O                 | FT                       | PB13  | TIM9_CH1/SPI2_SCK/ I2S2_CK/ USART3_CTS/<br>LCD_SEG13/ADC_IN19/COMP1_INP             |
| 75      | K11      | 53      | 35     | F2      | PB14              | I/O                 | FT                       | PB14  | TIM9_CH2/SPI2_MISO/<br>USART3_RTS/LCD_SEG14/<br>ADC_IN20/COMP1_INP                  |
| 76      | K10      | 54      | 36     | F1      | PB15              | I/O                 | FT                       | PB15  | TIM11_CH1/SPI2_MOSI/I2S2_SD/LCD_SEG15/<br>ADC_IN21/COMP1_INP/RTC_50_60Hz            |
| 77      | K9       | 55      | -      | -       | PD8               | I/O                 | FT                       | PD8   | USART3_TX/LCD_SEG28   |
| 78      | K8       | 56      | -      | -       | PD9               | I/O                 | FT                       | PD9   | USART3_RX/LCD_SEG29   |
| 79      | J12      | 57      | -      | -       | PD10              | I/O                 | FT                       | PD10  | USART3_CK/LCD_SEG30   |
| 80      | J11      | 58      | -      | -       | PD11              | I/O                 | FT                       | PD11  | USART3_CTS/LCD_SEG31  |
| 81      | J10      | 59      | -      | -       | PD12              | I/O                 | FT                       | PD12  | TIM4_CH1 / USART3_RTS/LCD_SEG32   |
| 82      | H12      | 60      | -      | -       | PD13              | I/O                 | FT                       | PD13  | TIM4_CH2/LCD_SEG33  |

Table 6. STM32L15xxC pin definitions (continued)

| Pins    |          |         |        |         | Pin name          | Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Main function <sup>(3)</sup><br>(after reset) | Alternate functions   |
|---------|----------|---------|--------|---------|-------------------|---------------------|--------------------------|---|---|
| LQFP144 | UFPGA132 | LQFP100 | LQFP64 | WLCSP64 |                   |                     |                          |   |   |
| 83      | -        | -       | -      | -       | V <sub>SS_8</sub> | S                   |                          | V <sub>SS_8</sub>                             |   |
| 84      | -        | -       | -      | -       | V <sub>DD_8</sub> | S                   |                          | V <sub>DD_8</sub>                             |   |
| 85      | H11      | 61      | -      | -       | PD14              | I/O                 | FT                       | PD14  | TIM4_CH3/LCD_SEG34  |
| 86      | H10      | 62      | -      | -       | PD15              | I/O                 | FT                       | PD15  | TIM4_CH4/LCD_SEG35  |
| 87      | G10      | -       | -      | -       | PG2               | I/O                 | FT                       | PG2   | ADC_IN10b/COMP1_INP   |
| 88      | F9       | -       | -      | -       | PG3               | I/O                 | FT                       | PG3   | ADC_IN11b/COMP1_INP   |
| 89      | F10      | -       | -      | -       | PG4               | I/O                 | FT                       | PG4   | ADC_IN12b/COMP1_INP   |
| 90      | E9       | -       | -      | -       | PG5               | I/O                 | FT                       | PG5   |   |
| 91      | -        | -       | -      | -       | PG6               | I/O                 | FT                       | PG6   |   |
| 92      | -        | -       | -      | -       | PG7               | I/O                 | FT                       | PG7   |   |
| 93      | -        | -       | -      | -       | PG8               | I/O                 | FT                       | PG8   |   |
| 94      | F6       | -       | -      | -       | V <sub>SS_9</sub> | S                   |                          | V <sub>SS_9</sub>                             |   |
| 95      | G6       | -       | -      | -       | V <sub>DD_9</sub> | S                   |                          | V <sub>DD_9</sub>                             |   |
| 96      | E12      | 63      | 37     | E1      | PC6               | I/O                 | FT                       | PC6   | TIM3_CH1/I2S2_MCK/LCD_SEG24                                   |
| 97      | E11      | 64      | 38     | E2      | PC7               | I/O                 | FT                       | PC7   | TIM3_CH2/I2S3_MCK/LCD_SEG25                                   |
| 98      | E10      | 65      | 39     | E3      | PC8               | I/O                 | FT                       | PC8   | TIM3_CH3/LCD_SEG26  |
| 99      | D12      | 66      | 40     | D1      | PC9               | I/O                 | FT                       | PC9   | TIM3_CH4/LCD_SEG27  |
| 100     | D11      | 67      | 41     | E4      | PA8               | I/O                 | FT                       | PA8   | USART1_CK/MCO/LCD_COM0  |
| 101     | D10      | 68      | 42     | D2      | PA9               | I/O                 | FT                       | PA9   | USART1_TX / LCD_COM1  |
| 102     | C12      | 69      | 43     | D3      | PA10              | I/O                 | FT                       | PA10  | USART1_RX / LCD_COM2  |
| 103     | B12      | 70      | 44     | C1      | PA11              | I/O                 | FT                       | PA11  | USART1_CTS/ USB_DM/SPI1_MISO                                  |
| 104     | A12      | 71      | 45     | C2      | PA12              | I/O                 | FT                       | PA12  | USART1_RTS/USB_DP/SPI1_MOSI                                   |
| 105     | A11      | 72      | 46     | D4      | PA13              | I/O                 | FT                       | JTMS-SWDIO                                    | PA13  |
| 106     | C11      | 73      | -      | -       | PH2               | I/O                 | FT                       | PH2   |   |
| 107     | F11      | 74      | 47     | B1      | V <sub>SS_2</sub> | S                   |                          | V <sub>SS_2</sub>                             |   |
| 108     | G11      | 75      | 48     | A1      | V <sub>DD_2</sub> | S                   |                          | V <sub>DD_2</sub>                             |   |
| 109     | A10      | 76      | 49     | B2      | PA14              | I/O                 | FT                       | JTCK-SWCLK                                    | PA14  |
| 110     | A9       | 77      | 50     | C3      | PA15              | I/O                 | FT                       | JTDI  | TIM2_CH1_ETR/ SPI1_NSS/SPI3_NSS/<br>I2S3_WS/LCD_SEG17         |
| 111     | B11      | 78      | 51     | A2      | PC10              | I/O                 | FT                       | PC10  | SPI3_SCK/I2S3_CK/USART3_TX/<br>LCD_SEG28/LCD_SEG40/LCD_COM4   |
| 112     | C10      | 79      | 52     | B3      | PC11              | I/O                 | FT                       | PC11  | SPI3_MISO/USART3_RX/<br>LCD_SEG29/LCD_SEG41/LCD_COM5/         |
| 113     | B10      | 80      | 53     | C4      | PC12              | I/O                 | FT                       | PC12  | SPI3_MOSI/I2S3_SD/USART3_CK/ LCD_SEG30/<br>LCD_SEG42/LCD_COM6 |
| 114     | C9       | 81      | -      | -       | PD0               | I/O                 | FT                       | PD0   | TIM9_CH1/SPI2_NSS/I2S2_WS                                     |

Table 6. STM32L15xxC pin definitions (continued)

| Pins    |          |         |        |         | Pin name           | Type <sup>(1)</sup> | I/O Level <sup>(2)</sup> | Main function <sup>(3)</sup><br>(after reset) | Alternate functions  |
|---------|----------|---------|--------|---------|--------------------|---------------------|--------------------------|---|--|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP64 |                    |                     |                          |   |  |
| 115     | B9       | 82      | -      | -       | PD1                | I/O                 | FT                       | PD1   | SPI2_SCK/I2S2_CK   |
| 116     | C8       | 83      | 54     | A3      | PD2                | I/O                 | FT                       | PD2   | TIM3_ETR/LCD_SEG31/LCD_SEG43/LCD_COM7                                      |
| 117     | B8       | 84      | -      | -       | PD3                | I/O                 | FT                       | PD3   | SPI2_MISO/USART2_CTS   |
| 118     | B7       | 85      | -      | -       | PD4                | I/O                 | FT                       | PD4   | SPI2_MOSI/I2S2_SD/<br>USART2_RTS   |
| 119     | A6       | 86      | -      | -       | PD5                | I/O                 | FT                       | PD5   | USART2_TX  |
| 120     | F7       | -       | -      | -       | V <sub>SS_10</sub> | S                   |                          | V <sub>SS_10</sub>                            |  |
| 121     | G7       | -       | -      | -       | V <sub>DD_10</sub> | S                   |                          | V <sub>DD_10</sub>                            |  |
| 122     | B6       | 87      | -      | -       | PD6                | I/O                 | FT                       | PD6   | USART2_RX  |
| 123     | A5       | 88      | -      | -       | PD7                | I/O                 | FT                       | PD7   | TIM9_CH2/USART2_CK   |
| 124     | D9       | -       | -      | -       | PG9                | I/O                 | FT                       | PG9   |  |
| 125     | D8       | -       | -      | -       | PG10               | I/O                 | FT                       | PG10  |  |
| 126     | -        | -       | -      | -       | PG11               | I/O                 | FT                       | PG11  |  |
| 127     | D7       | -       | -      | -       | PG12               | I/O                 | FT                       | PG12  |  |
| 128     | C7       | -       | -      | -       | PG13               | I/O                 | FT                       | PG13  |  |
| 129     | C6       | -       | -      | -       | PG14               | I/O                 | FT                       | PG14  |  |
| 130     | -        | -       | -      | -       | V <sub>SS_11</sub> | S                   |                          | V <sub>SS_11</sub>                            |  |
| 131     | -        | -       | -      | -       | V <sub>DD_11</sub> | S                   |                          | V <sub>DD_11</sub>                            |  |
| 132     | -        | -       | -      | -       | PG15               | I/O                 | FT                       | PG15  |  |
| 133     | A8       | 89      | 55     | A4      | PB3                | I/O                 | FT                       | JTDO  | TIM2_CH2/SPI1_SCK/SPI3_SCK/ I2S3_CK/<br>LCD_SEG7/COMP2_INM/TRACESWO        |
| 134     | A7       | 90      | 56     | B4      | PB4                | I/O                 | FT                       | NJTRST  | TIM3_CH1/ SPI1_MISO/SPI3_MISO/LCD_SEG8/<br>COMP2_INP                       |
| 135     | C5       | 91      | 57     | A5      | PB5                | I/O                 | FT                       | PB5   | TIM3_CH2<br>/I2C1_SMBAI/SPI1_MOSI/SPI3_MOSI/<br>I2S3_SD/LCD_SEG9/COMP2_INP |
| 136     | B5       | 92      | 58     | B5      | PB6                | I/O                 | FT                       | PB6   | TIM4_CH1/I2C1_SCL/USART1_TX/COMP2_INP                                      |
| 137     | B4       | 93      | 59     | C5      | PB7                | I/O                 | FT                       | PB7   | TIM4_CH2/I2C1_SDA/USART1_RX/PVD_IN/<br>COMP2_INP                           |
| 138     | A4       | 94      | 60     | A6      | BOOT0              | I                   |                          | BOOT0   |  |
| 139     | A3       | 95      | 61     | D5      | PB8                | I/O                 | FT                       | PB8   | TIM4_CH3/TIM10_CH1/I2C1_SCL/LCD_SEG16                                      |
| 140     | B3       | 96      | 62     | B6      | PB9                | I/O                 | FT                       | PB9   | TIM4_CH4/ TIM11_CH1/I2C1_SDA/LCD_COM3                                      |
| 141     | C3       | 97      | -      | -       | PE0                | I/O                 | FT                       | PE0   | TIM4_ETR/TIM10_CH1/LCD_SEG36   |
| 142     | A2       | 98      | -      | -       | PE1                | I/O                 | FT                       | PE1   | TIM11_CH1/LCD_SEG37  |
| 143     | D3       | 99      | 63     | A7      | V <sub>SS_3</sub>  | S                   |                          | V <sub>SS_3</sub>                             |  |
| 144     | C4       | 100     | 64     | A8      | V <sub>DD_3</sub>  | S                   |                          | V <sub>DD_3</sub>                             |  |

1. I = input, O = output, S = supply.

2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. Applicable to STM32L152xC devices only. In STM32L151xC devices, this pin should be connected to  $V_{DD}$ .
5. The PC14 and PC15 I/Os are only configured as OSC32\_IN/OSC32\_OUT when the LSE oscillator is ON (by setting the LSEON bit in the RCC\_CSR register). The LSE oscillator pins OSC32\_IN/OSC32\_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32\_IN/OSC32\_OUT pins as GPIO PC14/PC15 port pins section in the STM32L15xxx reference manual (RM0048).
6. The PH0 and PH1 I/Os are only configured as OSC\_IN/OSC\_OUT when the HSE oscillator is ON (by setting the HSEON bit in the RCC\_CR register). The HSE oscillator pins OSC\_IN/OSC\_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.



**Table 7. Alternate function input/output**

| Port name     | Digital alternate function number |               |          |            |        |           |                     |            |       |        |        |      |                                    |           |
|---------------|-----------------------------------|---------------|----------|------------|--------|-----------|---------------------|------------|-------|--------|--------|------|------------------------------------|-----------|
|               | AFIO0                             | AFIO1         | AFIO2    | AFIO3      | AFIO4  | AFIO5     | AFIO6               | AFIO7      | ..    | AFIO10 | AFIO11 | ..   | AFIO14                             | AFIO15    |
|               | Alternate function                |               |          |            |        |           |                     |            |       |        |        |      |                                    |           |
|               | SYSTEM                            | TIM2          | TIM3/4/5 | TIM9/10/11 | I2C1/2 | SPI1/2    | SPI3                | USART1/2/3 | USB   | LCD    |        | CPRI | SYSTEM                             |           |
| BOOT0         | BOOT0                             |               |          |            |        |           |                     |            |       |        |        |      |                                    | EVENT OUT |
| NRST          | NRST                              |               |          |            |        |           |                     |            |       |        |        |      |                                    |           |
| PA0-<br>WKUP1 | WKUP1/<br>TAMPER2                 | TIM2_CH1_ETR  | TIM5_CH1 |            |        |           |                     | USART2_CTS |       |        |        |      | COMP1_INP/<br>TIMx_IC1_0/<br>G1IO1 | EVENT OUT |
| PA1           |                                   | TIM2_CH2      | TIM5_CH2 |            |        |           |                     | USART2_RTS |       | SEG0   |        |      | COMP1_INP/<br>TIMx_IC2_0 G1IO2     | EVENT OUT |
| PA2           |                                   | TIM2_CH3      | TIM5_CH3 | TIM9_CH1   |        |           |                     | USART2_TX  |       | SEG1   |        |      | COMP1_INP/<br>TIMx_IC3_0/<br>G1IO3 | EVENT OUT |
| PA3           |                                   | TIM2_CH4      | TIM5_CH4 | TIM9_CH2   |        |           |                     | USART2_RX  |       | SEG2   |        |      | COMP1_INP/<br>TIMx_IC4_0/<br>G1IO4 | EVENT OUT |
| PA4           |                                   |               |          |            |        | SPI1_NSS  | SPI3_NSS<br>I2S3_WS | USART2_CK  |       |        |        |      | COMP1_INP/<br>TIMx_IC1_1           | EVENT OUT |
| PA5           |                                   | TIM2_CH1_ETR* |          |            |        | SPI1_SCK  |                     |            |       |        |        |      | COMP1_INP/<br>TIMx_IC2_1           | EVENT OUT |
| PA6           |                                   |               | TIM3_CH1 | TIM10_CH1  |        | SPI1_MISO |                     |            |       | SEG3   |        |      | COMP1_INP/<br>TIMx_IC3_1 G2IO1     | EVENT OUT |
| PA7           |                                   |               | TIM3_CH2 | TIM11_CH1  |        | SPI1_MOSI |                     |            |       | SEG4   |        |      | COMP1_INP/<br>TIMx_IC4_1/<br>G2IO2 | EVENT OUT |
| PA8           | MCO                               |               |          |            |        |           |                     | USART1_CK  |       | COM0   |        |      | TIMx_IC1_2/<br>G4IO1               | EVENT OUT |
| PA9           |                                   |               |          |            |        |           |                     | USART1_TX  |       | COM1   |        |      | TIMx_IC2_2/<br>G4IO2               | EVENT OUT |
| PA10          |                                   |               |          |            |        |           |                     | USART1_RX  |       | COM2   |        |      | TIMx_IC3_2/<br>G4IO3               | EVENT OUT |
| PA11          |                                   |               |          |            |        | SPI1_MISO |                     | USART1_CTS | USBDM |        |        |      | TIMx_IC4_2/<br>G4IO4               | EVENT OUT |

Table 7. Alternate function input/output (continued)

| Port name | Digital alternate function number |              |          |                |            |                     |                      |            |     |        |        |                      |           |        |
|-----------|-----------------------------------|--------------|----------|----------------|------------|---------------------|----------------------|------------|-----|--------|--------|----------------------|-----------|--------|
|           | AFIO0                             | AFIO1        | AFIO2    | AFIO3          | AFIO4      | AFIO5               | AFIO6                | AFIO7      | ..  | AFIO10 | AFIO11 | ..                   | AFIO14    | AFIO15 |
|           | Alternate function                |              |          |                |            |                     |                      |            |     |        |        |                      |           |        |
|           | SYSTEM                            | TIM2         | TIM3/4/5 | TIM9/<br>10/11 | I2C1/2     | SPI1/2              | SPI3                 | USART1/2/3 | USB | LCD    |        | CPRI                 | SYSTEM    |        |
| PA12      |                                   |              |          |                |            | SPI1_MOSI           |                      | USART1_RTS | USB | USBDP  |        | TIMx_IC1_3/          | EVENT OUT |        |
| PA13      | JTMS-SWDIO                        |              |          |                |            |                     |                      |            |     |        |        | TIMx_IC2_3/<br>G5IO1 | EVENT OUT |        |
| PA14      | JTCK-SWCLK                        |              |          |                |            |                     |                      |            |     |        |        | TIMx_IC3_3/<br>G5IO2 | EVEN TOUT |        |
| PA15      | JTDI                              | TIM2_CH1_ETR |          |                |            | SPI1_NSS            | SPI3_NSS<br>I2S3_WS  |            |     |        | SEG17  | TIMx_IC4_3/<br>G5IO3 | EVEN TOUT |        |
| PB0       |                                   |              | TIM3_CH3 |                |            |                     |                      |            |     |        | SEG5   | COMP1_INP/<br>G3IO1  | EVEN TOUT |        |
| PB1       |                                   |              | TIM3_CH4 |                |            |                     |                      |            |     |        | SEG6   | COMP1_INP/<br>G3IO2  | EVENT OUT |        |
| PB2       | BOOT1                             |              |          |                |            |                     |                      |            |     |        |        | COMP1_INP/<br>G3IO3  | EVENT OUT |        |
| PB3       | JTDO                              | TIM2_CH2     |          |                |            | SPI1_SCK            | SPI3_SCK<br>I2S3_CK  |            |     |        | SEG7   |                      | EVENT OUT |        |
| PB4       | JTRST                             |              | TIM3_CH1 |                |            | SPI1_MISO           | SPI3_MISO            |            |     |        | SEG8   | G6IO1                | EVENT OUT |        |
| PB5       |                                   |              | TIM3_CH2 |                | I2C1_ SMBA | SPI1_MOSI           | SPI3_MOSI<br>I2S3_SD |            |     |        | SEG9   | G6IO2                | EVENT OUT |        |
| PB6       |                                   |              | TIM4_CH1 |                | I2C1_SCL   |                     |                      | USART1_TX  |     |        |        | G6IO3                | EVENT OUT |        |
| PB7       |                                   |              | TIM4_CH2 |                | I2C1_SDA   |                     |                      | USART1_RX  |     |        |        | G6IO4                | EVENT OUT |        |
| PB8       |                                   |              | TIM4_CH3 | TIM10_ CH1     | I2C1_SCL   |                     |                      |            |     |        | SEG16  |                      | EVENT OUT |        |
| PB9       |                                   |              | TIM4_CH4 | TIM11_ CH1     | I2C1_SDA   |                     |                      |            |     |        | COM3   |                      | EVENT OUT |        |
| PB10      |                                   | TIM2_CH3     |          |                | I2C_SCL    |                     |                      | USART3_TX  |     |        | SEG10  |                      | EVENT OUT |        |
| PB11      |                                   | TIM2_CH4     |          |                | I2C_SDA    |                     |                      | USART3_RX  |     |        | SEG11  |                      | EVENT OUT |        |
| PB12      |                                   |              |          | TIM10_ CH1     | I2C_ SMBA  | SPI2_NSS<br>I2S2_WS |                      | USART3_CK  |     |        | SEG12  | COMP1_INP/<br>G7IO1  | EVENT OUT |        |



**Table 7. Alternate function input/output (continued)**

| Port name | Digital alternate function number |       |          |                |        |                      |          |            |     |        |        |                                    |           |        |
|-----------|-----------------------------------|-------|----------|----------------|--------|----------------------|----------|------------|-----|--------|--------|------------------------------------|-----------|--------|
|           | AFIO0                             | AFIO1 | AFIO2    | AFIO3          | AFIO4  | AFIO5                | AFIO6    | AFIO7      | ..  | AFIO10 | AFIO11 | ..                                 | AFIO14    | AFIO15 |
|           | Alternate function                |       |          |                |        |                      |          |            |     |        |        |                                    |           |        |
|           | SYSTEM                            | TIM2  | TIM3/4/5 | TIM9/<br>10/11 | I2C1/2 | SPI1/2               | SPI3     | USART1/2/3 | USB | LCD    |        | CPRI                               | SYSTEM    |        |
| PB13      |                                   |       |          | TIM9_<br>CH1   |        | SPI2_SCK<br>I2S2_CK  |          | USART3_CTS |     | SEG13  |        | COMP1_INP/<br>G7IO2                | EVENT OUT |        |
| PB14      |                                   |       |          | TIM9_<br>CH2   |        | SPI2_MISO            |          | USART3_RTS |     | SEG14  |        | COMP1_INP/<br>G7IO3                | EVENT OUT |        |
| PB15      | RTC 50/60 Hz                      |       |          | TIM11_<br>CH1  |        | SPI2_MOSII<br>2S2_SD |          |            |     | SEG15  |        | COMP1_INP/<br>G7IO4                | EVENT OUT |        |
| PC0       |                                   |       |          |                |        |                      |          |            |     | SEG18  |        | COMP1_INP/<br>TIMx_IC1_4/<br>G8IO1 | EVENT OUT |        |
| PC1       |                                   |       |          |                |        |                      |          |            |     | SEG19  |        | COMP1_INP/<br>TIMx_IC2_4/<br>G8IO2 | EVENT OUT |        |
| PC2       |                                   |       |          |                |        |                      |          |            |     | SEG20  |        | COMP1_INP/<br>TIMx_IC3_4/<br>G8IO3 | EVENT OUT |        |
| PC3       |                                   |       |          |                |        |                      |          |            |     | SEG21  |        | COMP1_INP/<br>TIMx_IC4_4/<br>G8IO4 | EVENT OUT |        |
| PC4       |                                   |       |          |                |        |                      |          |            |     | SEG22  |        | COMP1_INP/<br>TIMx_IC1_5/<br>G9IO1 | EVENT OUT |        |
| PC5       |                                   |       |          |                |        |                      |          |            |     | SEG23  |        | COMP1_INP/<br>TIMx_IC2_5/<br>G9IO2 | EVENT OUT |        |
| PC6       |                                   |       | TIM3_CH1 |                |        | I2S2_MCK             |          |            |     | SEG24  |        | TIMx_IC3_5/<br>G10IO1              | EVENT OUT |        |
| PC7       |                                   |       | TIM3_CH2 |                |        |                      | I2S3_MCK |            |     | SEG25  |        | TIMx_IC4_5/<br>G10IO2              | EVENT OUT |        |
| PC8       |                                   |       | TIM3_CH3 |                |        |                      |          |            |     | SEG26  |        | TIMx_IC1_6/<br>G10IO3              | EVENT OUT |        |
| PC9       |                                   |       | TIM3_CH4 |                |        |                      |          |            |     | SEG27  |        | TIMx_IC2_6/<br>G10IO4              | EVENT OUT |        |

Table 7. Alternate function input/output (continued)

| Port name             | Digital alternate function number                       |       |          |                |        |        |                      |            |            |        |                          |      |                      |           |
|-----------------------|---|-------|----------|----------------|--------|--------|----------------------|------------|------------|--------|--------------------------|------|----------------------|-----------|
|                       | AFIO0   | AFIO1 | AFIO2    | AFIO3          | AFIO4  | AFIO5  | AFIO6                | AFIO7      | ..         | AFIO10 | AFIO11                   | ..   | AFIO14               | AFIO15    |
|                       | Alternate function                                      |       |          |                |        |        |                      |            |            |        |                          |      |                      |           |
|                       | SYSTEM  | TIM2  | TIM3/4/5 | TIM9/<br>10/11 | I2C1/2 | SPI1/2 | SPI3                 | USART1/2/3 | USB        | LCD    |                          | CPRI | SYSTEM               |           |
| PC10                  |   |       |          |                |        |        | SPI3_SCK<br>I2S3_CK  | USART3_TX  |            |        | COM4/<br>SEG28/<br>SEG40 |      | TIMx_IC3_6/<br>G5IO4 | EVENT OUT |
| PC11                  |   |       |          |                |        |        | SPI3_MISO            | USART3_RX  |            |        | COM5/<br>SEG29<br>/SEG41 |      | TIMx_IC4_6           | EVENT OUT |
| PC12                  |   |       |          |                |        |        | SPI3_MOSI<br>I2S3_SD | USART3_CK  |            |        | COM6/<br>SEG30/<br>SEG42 |      | TIMx_IC1_7           | EVENT OUT |
| PC13-<br>WKUP2        | WKUP2/<br>TAMPER1/<br>TIMESTAMP/<br>ALARM_OUT/51<br>2Hz |       |          |                |        |        |                      |            |            |        |                          |      | TIMx_IC2_7           | EVENT OUT |
| PC14<br>OSC32_IN      | OSC32_IN  |       |          |                |        |        |                      |            |            |        |                          |      | TIMx_IC3_7           | EVENT OUT |
| PC15<br>OSC32_<br>OUT | OSC32_OUT   |       |          |                |        |        |                      |            |            |        |                          |      | TIMx_IC4_7           | EVENT OUT |
| PD0                   |   |       |          | TIM9_CH1       |        |        | SPI2_NSS<br>I2S2_WS  |            |            |        |                          |      | TIMx_IC1_8           | EVENT OUT |
| PD1                   |   |       |          |                |        |        | SPI2_SCK<br>I2S2_CK  |            |            |        |                          |      | TIMx_IC2_8           | EVENT OUT |
| PD2                   |   |       |          |                |        |        |                      |            |            |        | COM7/<br>SEG31/<br>SEG43 |      | TIMx_IC3_8           | EVENT OUT |
| PD3                   |   |       |          |                |        |        | SPI2_MISO            |            | USART2_CTS |        |                          |      | TIMx_IC4_8           | EVENT OUT |
| PD4                   |   |       |          |                |        |        | SPI2_MOSI<br>I2S2_SD |            | USART2_RTS |        |                          |      | TIMx_IC1_9           | EVENT OUT |
| PD5                   |   |       |          |                |        |        |                      |            | USART2_TX  |        |                          |      | TIMx_IC2_9           | EVENT OUT |
| PD6                   |   |       |          |                |        |        |                      |            | USART2_RX  |        |                          |      | TIMx_IC3_9           | EVENT OUT |
| PD7                   |   |       |          |                |        |        |                      |            | USART2_CK  |        |                          |      | TIMx_IC4_9           | EVENT OUT |



**Table 7. Alternate function input/output (continued)**

| Port name     | Digital alternate function number |              |          |                |        |        |            |            |        |        |                           |           |        |        |
|---------------|-----------------------------------|--------------|----------|----------------|--------|--------|------------|------------|--------|--------|---------------------------|-----------|--------|--------|
|               | AFIO0                             | AFIO1        | AFIO2    | AFIO3          | AFIO4  | AFIO5  | AFIO6      | AFIO7      | ..     | AFIO10 | AFIO11                    | ..        | AFIO14 | AFIO15 |
|               | Alternate function                |              |          |                |        |        |            |            |        |        |                           |           |        |        |
|               | SYSTEM                            | TIM2         | TIM3/4/5 | TIM9/<br>10/11 | I2C1/2 | SPI1/2 | SPI3       | USART1/2/3 | USB    | LCD    |                           | CPRI      | SYSTEM |        |
| PD8           |                                   |              |          |                |        |        | USART3_TX  |            | SEG28  |        | TIMx_IC1_10               | EVENT OUT |        |        |
| PD9           |                                   |              |          |                |        |        | USART3_RX  |            | SEG29  |        | TIMx_IC2_10               | EVENT OUT |        |        |
| PD10          |                                   |              |          |                |        |        | USART3_CK  |            | SEG30  |        | TIMx_IC3_10               | EVENT OUT |        |        |
| PD11          |                                   |              |          |                |        |        | USART3_CTS |            | SEG31  |        | TIMx_IC4_10               | EVENT OUT |        |        |
| PD12          |                                   |              | TIM4_CH1 |                |        |        | USART3_RTS |            | SEG32  |        | TIMx_IC1_11               | EVENT OUT |        |        |
| PD13          |                                   |              | TIM4_CH2 |                |        |        |            |            | SEG33  |        | TIMx_IC2_11               | EVENT OUT |        |        |
| PD14          |                                   |              | TIM4_CH3 |                |        |        |            |            | SEG34  |        | TIMx_IC3_11               | EVENT OUT |        |        |
| PD15          |                                   |              | TIM4_CH4 |                |        |        |            |            | SEG35  |        | TIMx_IC4_11               | EVENT OUT |        |        |
| PE0           |                                   |              | TIM4_ETR | TIM10_CH1      |        |        |            |            | SEG36  |        | TIMx_IC1_12               | EVENT OUT |        |        |
| PE1           |                                   |              |          | TIM11_CH1      |        |        |            |            | SEG37  |        | TIMx_IC2_12               | EVENT OUT |        |        |
| PE2           | TRACECK                           |              | TIM3_ETR |                |        |        |            |            | SEG 38 |        | TIMx_IC3_12               | EVENT OUT |        |        |
| PE3           | TRACED0                           |              | TIM3_CH1 |                |        |        |            |            | SEG 39 |        | TIMx_IC4_12               | EVENT OUT |        |        |
| PE4           | TRACED1                           |              | TIM3_CH2 |                |        |        |            |            |        |        | TIMx_IC1_13               | EVENT OUT |        |        |
| PE5           | TRACED2                           |              |          | TIM9_CH1       |        |        |            |            |        |        | TIMx_IC2_13               | EVENT OUT |        |        |
| PE6-<br>WKUP3 | WKUP3/<br>TAMPER3 /<br>TRACED3    |              |          | TIM9_CH2       |        |        |            |            |        |        | TIMx_IC3_13               | EVENT OUT |        |        |
| PE7           |                                   |              |          |                |        |        |            |            |        |        | COMP1_INP/<br>TIMx_IC4_13 | EVENT OUT |        |        |
| PE8           |                                   |              |          |                |        |        |            |            |        |        | COMP1_INP/<br>TIMx_IC1_14 | EVENT OUT |        |        |
| PE9           |                                   | TIM2_CH1_ETR |          |                |        |        |            |            |        |        | COMP1_INP/<br>TIMx_IC2_14 | EVENT OUT |        |        |
| PE10          |                                   | TIM2_CH2     |          |                |        |        |            |            |        |        | COMP1_INP/<br>TIMx_IC3_14 | EVENT OUT |        |        |
| PE11          |                                   | TIM2_CH3     |          |                |        |        |            |            |        |        | TIMx_IC4_14               | EVENT OUT |        |        |



Table 7. Alternate function input/output (continued)

| Port name | Digital alternate function number |          |              |                |        |           |       |            |     |        |        |      |                     |           |
|-----------|-----------------------------------|----------|--------------|----------------|--------|-----------|-------|------------|-----|--------|--------|------|---------------------|-----------|
|           | AFIO0                             | AFIO1    | AFIO2        | AFIO3          | AFIO4  | AFIO5     | AFIO6 | AFIO7      | ..  | AFIO10 | AFIO11 | ..   | AFIO14              | AFIO15    |
|           | Alternate function                |          |              |                |        |           |       |            |     |        |        |      |                     |           |
|           | SYSTEM                            | TIM2     | TIM3/4/5     | TIM9/<br>10/11 | I2C1/2 | SPI1/2    | SPI3  | USART1/2/3 | USB | LCD    |        | CPRI | SYSTEM              |           |
| PE12      |                                   | TIM2_CH4 |              |                |        | SPI1_NSS  |       |            |     |        |        |      | TIMx_IC1_15         | EVENT OUT |
| PE13      |                                   |          |              |                |        | SPI1_SCK  |       |            |     |        |        |      | TIMx_IC2_15         | EVENT OUT |
| PE14      |                                   |          |              |                |        | SPI1_MISO |       |            |     |        |        |      | TIMx_IC3_15         | EVENT OUT |
| PE15      |                                   |          |              |                |        | SPI1_MOSI |       |            |     |        |        |      | TIMx_IC4_15         | EVENT OUT |
| PF0       |                                   |          |              |                |        |           |       |            |     |        |        |      |                     | EVENT OUT |
| PF1       |                                   |          |              |                |        |           |       |            |     |        |        |      |                     | EVENT OUT |
| PF2       |                                   |          |              |                |        |           |       |            |     |        |        |      |                     | EVENT OUT |
| PF3       |                                   |          |              |                |        |           |       |            |     |        |        |      |                     | EVENT OUT |
| PF4       |                                   |          |              |                |        |           |       |            |     |        |        |      |                     | EVENT OUT |
| PF5       |                                   |          |              |                |        |           |       |            |     |        |        |      |                     | EVENT OUT |
| PF6       |                                   |          | TIM5_CH1_ETR |                |        |           |       |            |     |        |        |      | COMP1_INP<br>G11IO1 | EVENT OUT |
| PF7       |                                   |          | TIM5_CH2     |                |        |           |       |            |     |        |        |      | COMP1_INP<br>G11IO2 | EVENT OUT |
| PF8       |                                   |          | TIM5_CH3     |                |        |           |       |            |     |        |        |      | COMP1_INP<br>G11IO3 | EVENT OUT |
| PF9       |                                   |          | TIM5_CH4     |                |        |           |       |            |     |        |        |      | COMP1_INP<br>G11IO4 | EVENT OUT |
| PF10      |                                   |          |              |                |        |           |       |            |     |        |        |      | COMP1_INP<br>G11IO5 | EVENT OUT |
| PF11      |                                   |          |              |                |        |           |       |            |     |        |        |      | COMP1_INP<br>G3IO4  | EVENT OUT |
| PF12      |                                   |          |              |                |        |           |       |            |     |        |        |      | G3IO5               | EVENT OUT |
| PF13      |                                   |          |              |                |        |           |       |            |     |        |        |      | G9IO3               | EVENT OUT |
| PF14      |                                   |          |              |                |        |           |       |            |     |        |        |      | G9IO4               | EVENT OUT |
| PF15      |                                   |          |              |                |        |           |       |            |     |        |        |      | G2IO3               | EVENT OUT |
| PG0       |                                   |          |              |                |        |           |       |            |     |        |        |      | G2IO4               | EVENT OUT |



**Table 7. Alternate function input/output (continued)**

| Port name  | Digital alternate function number |       |          |                |        |        |       |            |     |        |        |      |        |           |
|------------|-----------------------------------|-------|----------|----------------|--------|--------|-------|------------|-----|--------|--------|------|--------|-----------|
|            | AFIO0                             | AFIO1 | AFIO2    | AFIO3          | AFIO4  | AFIO5  | AFIO6 | AFIO7      | ..  | AFIO10 | AFIO11 | ..   | AFIO14 | AFIO15    |
|            | Alternate function                |       |          |                |        |        |       |            |     |        |        |      |        |           |
|            | SYSTEM                            | TIM2  | TIM3/4/5 | TIM9/<br>10/11 | I2C1/2 | SPI1/2 | SPI3  | USART1/2/3 | USB | LCD    |        | CPRI | SYSTEM |           |
| PG1        |                                   |       |          |                |        |        |       |            |     |        |        |      | G2IO5  | EVENT OUT |
| PG2        |                                   |       |          |                |        |        |       |            |     |        |        |      | G7IO5  | EVENT OUT |
| PG3        |                                   |       |          |                |        |        |       |            |     |        |        |      | G7IO6  | EVENT OUT |
| PG4        |                                   |       |          |                |        |        |       |            |     |        |        |      | G7IO7  | EVENT OUT |
| PG5        |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG6        |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG7        |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG8        |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG9        |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG10       |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG11       |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG12       |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG13       |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG14       |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PG15       |                                   |       |          |                |        |        |       |            |     |        |        |      |        | EVENT OUT |
| PH0OSC_IN  | OSC_IN                            |       |          |                |        |        |       |            |     |        |        |      |        |           |
| PH1OSC_OUT | OSC_OUT                           |       |          |                |        |        |       |            |     |        |        |      |        |           |
| PH2        |                                   |       |          |                |        |        |       |            |     |        |        |      |        |           |



## 6 Electrical characteristics

### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ °C}$  and  $T_A = T_{A\text{max}}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean} \pm 3\sigma$ ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ °C}$ ,  $V_{DD} = 3.6\text{ V}$  (for the  $1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ( $\text{mean} \pm 2\sigma$ ).

#### 6.1.3 Typical curves

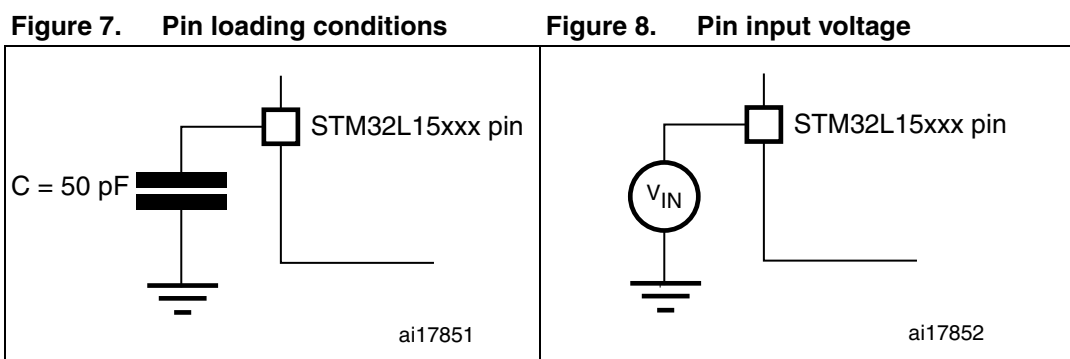
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 7](#).

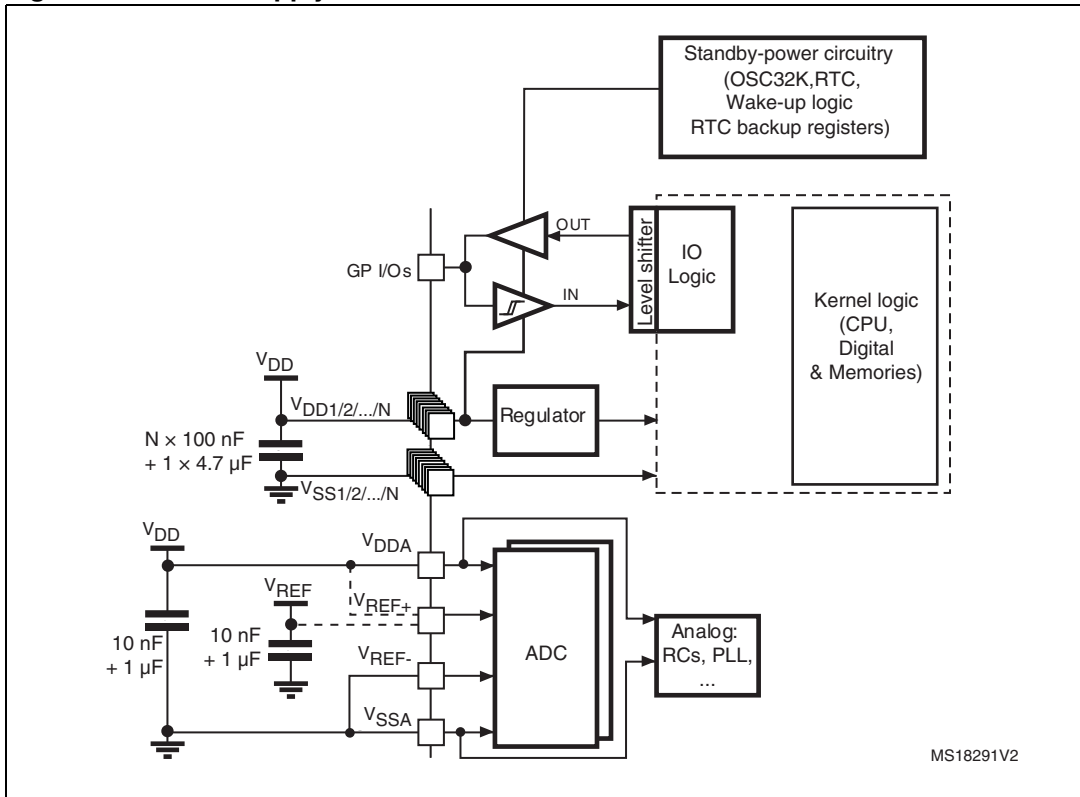
#### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 8](#).



### 6.1.6 Power supply scheme

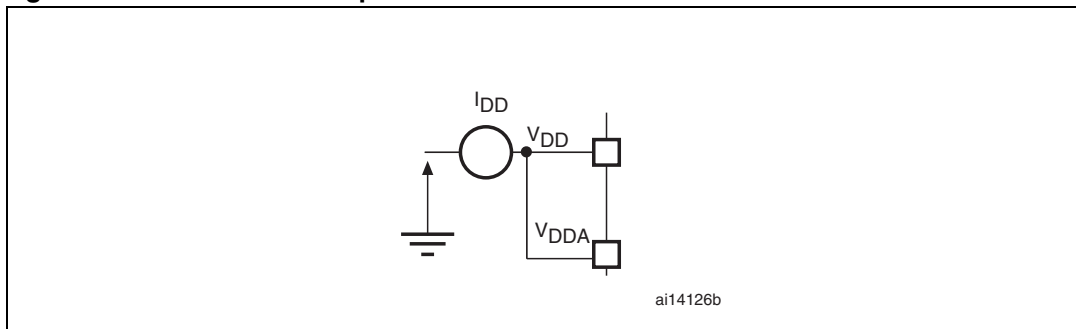
Figure 9. Power supply scheme



**Caution:** In this figure, the  $4.7\text{ }\mu\text{F}$  capacitor must be connected to  $V_{DD2}$ .

### 6.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 8: Voltage characteristics](#), [Table 9: Current characteristics](#), and [Table 10: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 8. Voltage characteristics**

| Symbol             | Ratings   | Min                                | Max          | Unit |
|--------------------|---|------------------------------------|--------------|------|
| $V_{DD}-V_{SS}$    | External main supply voltage (including $V_{DDA}$ and $V_{DD}$ ) <sup>(1)</sup> | -0.3                               | 4.0          | V    |
| $V_{IN}^{(2)}$     | Input voltage on five-volt tolerant pin   | $V_{SS}-0.3$                       | $V_{DD}+4.0$ |      |
|                    | Input voltage on any other pin  | $V_{SS}-0.3$                       | 4.0          |      |
| $ \Delta V_{DDX} $ | Variations between different $V_{DD}$ power pins                                |                                    | 50           | mV   |
| $ V_{SSX}-V_{SS} $ | Variations between all different ground pins                                    |                                    | 50           |      |
| $V_{ESD(HBM)}$     | Electrostatic discharge voltage (human body model)                              | see <a href="#">Section 6.3.10</a> |              |      |

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2.  $V_{IN}$  maximum must always be respected. Refer to [Table 9](#) for maximum allowed injected current values.

**Table 9. Current characteristics**

| Symbol                | Ratings   | Max.   | Unit |
|-----------------------|---|--------|------|
| $I_{VDD}$             | Total current into $V_{DD}/V_{DDA}$ power lines (source) <sup>(1)</sup> | 80     | mA   |
| $I_{VSS}$             | Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>        | 80     |      |
| $I_{IO}$              | Output current sunk by any I/O and control pin                          | 25     |      |
|                       | Output current sourced by any I/O and control pin                       | - 25   |      |
| $I_{INJ(PIN)}^{(2)}$  | Injected current on five-volt tolerant I/O <sup>(3)</sup>               | +0 /-5 |      |
|                       | Injected current on any other pin <sup>(4)</sup>                        | ± 5    |      |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) <sup>(5)</sup> | ± 25   |      |

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in [Section 6.3.16](#).
3. Positive current injection is not possible on these I/Os. A negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 8](#) for maximum allowed input voltage values.
4. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 8: Voltage characteristics](#) for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 10. Thermal characteristics

| Symbol    | Ratings                      | Value       | Unit |
|-----------|------------------------------|-------------|------|
| $T_{STG}$ | Storage temperature range    | -65 to +150 | °C   |
| $T_J$     | Maximum junction temperature | 150         | °C   |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

Table 11. General operating conditions

| Symbol          | Parameter                                       | Conditions                                  | Min  | Max | Unit |
|-----------------|---|---|------|-----|------|
| $f_{HCLK}$      | Internal AHB clock frequency                    |   | 0    | 32  | MHz  |
| $f_{PCLK1}$     | Internal APB1 clock frequency                   |   | 0    | 32  |      |
| $f_{PCLK2}$     | Internal APB2 clock frequency                   |   | 0    | 32  |      |
| $V_{DD}$        | Standard operating voltage                      | BOR detector disabled                       | 1.65 | 3.6 | V    |
|                 |   | BOR detector enabled, at power on           | 1.8  | 3.6 |      |
|                 |   | BOR detector disabled, after power on       | 1.65 | 3.6 |      |
| $V_{DDA}^{(1)}$ | Analog operating voltage (ADC and DAC not used) | Must be the same voltage as $V_{DD}^{(2)}$  | 1.65 | 3.6 | V    |
|                 | Analog operating voltage (ADC or DAC used)      |   | 1.8  | 3.6 |      |
| $P_D$           | Power dissipation at $T_A = 85\text{ °C}^{(3)}$ |   |      | 290 | mW   |
| $T_A$           | Temperature range                               | Maximum power dissipation                   | -40  | 85  | °C   |
|                 |   | Low power dissipation <sup>(4)</sup>        | -40  | 105 |      |
| $T_J$           | Junction temperature range                      | $-40\text{ °C} \leq T_A \leq 105\text{ °C}$ | -40  | 105 | °C   |

1. When the ADC is used, refer to [Table 51: ADC characteristics](#).
2. It is recommended to power  $V_{DD}$  and  $V_{DDA}$  from the same source. A maximum difference of 300 mV between  $V_{DD}$  and  $V_{DDA}$  can be tolerated during power-up and operation.
3. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_J$  max (see [Table 65: Thermal characteristics on page 105](#)).
4. In low power dissipation state,  $T_A$  can be extended to this range as long as  $T_J$  does not exceed  $T_J$  max (see [Table 65: Thermal characteristics on page 105](#)).

**Table 12. Functionalities depending on the operating power supply range**

| Operating power supply range    | Functionalities depending on the operating power supply range |                           |                             |   |                            |
|---------------------------------|---|---------------------------|-----------------------------|---|----------------------------|
|                                 | DAC and ADC operation   | USB                       | V <sub>CORE</sub>           | Maximum CPU frequency (f <sub>CPU max</sub> ) | I/O operation              |
| V <sub>DD</sub> = 1.65 to 1.8 V | Not functional  | Not functional            | Range 2 or range 3          | 16 MHz (1ws)<br>8MHz (0ws)                    | Degraded speed performance |
| V <sub>DD</sub> = 1.8 to 2.0 V  | Conversion time up to 500 Ksps                                | Not functional            | Range 2 or range 3          | 16 MHz (1ws)<br>8MHz (0ws)                    | Degraded speed performance |
| V <sub>DD</sub> = 2.0 to 2.4 V  | Conversion time up to 500 Ksps                                | Functional <sup>(1)</sup> | Range 1, range 2 or range 3 | 32 MHz (1ws)<br>16MHz (0ws)                   | Full speed operation       |
| V <sub>DD</sub> = 2.4 to 3.6 V  | Conversion time up to 1 Msps                                  | Functional <sup>(1)</sup> | Range 1, range 2 or range 3 | 32 MHz (1ws)<br>16MHz (0ws)                   | Full speed operation       |

1. To be USB compliant from the IO voltage standpoint, the minimum V<sub>DD</sub> is 3.0 V.

### 6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in [Table 11](#).

**Table 13. Embedded reset and power control block characteristics**

| Symbol                               | Parameter                      | Conditions                           | Min | Typ | Max  | Unit |
|--------------------------------------|--------------------------------|--------------------------------------|-----|-----|------|------|
| t <sub>VDD</sub> <sup>(1)</sup>      | V <sub>DD</sub> rise time rate | BOR detector enabled                 | 0   |     | ∞    | μs/V |
|                                      |                                | BOR detector disabled                | 0   |     | 1000 |      |
|                                      | V <sub>DD</sub> fall time rate | BOR detector enabled                 | 20  |     | ∞    |      |
|                                      |                                | BOR detector disabled                | 0   |     | 1000 |      |
| T <sub>RSTTEMPO</sub> <sup>(1)</sup> | Reset temporization            | V <sub>DD</sub> rising, BOR enabled  |     | 2   | 3.3  | ms   |
|                                      |                                | V <sub>DD</sub> rising, BOR disabled | 0.4 | 0.7 | 1.6  |      |

Table 13. Embedded reset and power control block characteristics (continued)

| Symbol        | Parameter                                 | Conditions                                | Min  | Typ  | Max  | Unit |
|---------------|---|---|------|------|------|------|
| $V_{POR/PDR}$ | Power on/power down reset threshold       | Falling edge                              | 1    | 1.5  | 1.65 | V    |
|               |   | Rising edge                               | 1.3  | 1.5  | 1.65 |      |
| $V_{BOR0}$    | Brown-out reset threshold 0               | Falling edge                              | 1.67 | 1.7  | 1.74 |      |
|               |   | Rising edge                               | 1.69 | 1.76 | 1.8  |      |
| $V_{BOR1}$    | Brown-out reset threshold 1               | Falling edge                              | 1.87 | 1.93 | 1.97 |      |
|               |   | Rising edge                               | 1.96 | 2.03 | 2.07 |      |
| $V_{BOR2}$    | Brown-out reset threshold 2               | Falling edge                              | 2.22 | 2.30 | 2.35 |      |
|               |   | Rising edge                               | 2.31 | 2.41 | 2.44 |      |
| $V_{BOR3}$    | Brown-out reset threshold 3               | Falling edge                              | 2.45 | 2.55 | 2.60 |      |
|               |   | Rising edge                               | 2.54 | 2.66 | 2.7  |      |
| $V_{BOR4}$    | Brown-out reset threshold 4               | Falling edge                              | 2.68 | 2.8  | 2.85 |      |
|               |   | Rising edge                               | 2.78 | 2.9  | 2.95 |      |
| $V_{PVD0}$    | Programmable voltage detector threshold 0 | Falling edge                              | 1.8  | 1.85 | 1.88 |      |
|               |   | Rising edge                               | 1.88 | 1.94 | 1.99 |      |
| $V_{PVD1}$    | PVD threshold 1                           | Falling edge                              | 1.98 | 2.04 | 2.09 |      |
|               |   | Rising edge                               | 2.08 | 2.14 | 2.18 |      |
| $V_{PVD2}$    | PVD threshold 2                           | Falling edge                              | 2.20 | 2.24 | 2.28 |      |
|               |   | Rising edge                               | 2.28 | 2.34 | 2.38 |      |
| $V_{PVD3}$    | PVD threshold 3                           | Falling edge                              | 2.39 | 2.44 | 2.48 |      |
|               |   | Rising edge                               | 2.47 | 2.54 | 2.58 |      |
| $V_{PVD4}$    | PVD threshold 4                           | Falling edge                              | 2.57 | 2.64 | 2.69 |      |
|               |   | Rising edge                               | 2.68 | 2.74 | 2.79 |      |
| $V_{PVD5}$    | PVD threshold 5                           | Falling edge                              | 2.77 | 2.83 | 2.88 |      |
|               |   | Rising edge                               | 2.87 | 2.94 | 2.99 |      |
| $V_{PVD6}$    | PVD threshold 6                           | Falling edge                              | 2.97 | 3.05 | 3.09 |      |
|               |   | Rising edge                               | 3.08 | 3.15 | 3.20 |      |
| $V_{hyst}$    | Hysteresis voltage                        | BOR0 threshold                            |      | 40   |      | mV   |
|               |   | All BOR and PVD thresholds excepting BOR0 |      | 100  |      |      |

1. Guaranteed by characterisation, not tested in production.

### 6.3.3 Embedded internal reference voltage

The parameters given in [Table 14](#) are based on characterization results, unless otherwise specified.

**Table 14. Embedded internal reference voltage**

| Symbol                    | Parameter  | Conditions   | Min   | Typ   | Max     | Unit              |
|---------------------------|--|--|-------|-------|---------|-------------------|
| $V_{REFINT\_out}^{(1)}$   | Internal reference voltage   | $-40\text{ °C} < T_J < +105\text{ °C}$                           | 1.202 | 1.224 | 1.242   | V                 |
| $I_{REFINT}$              | Internal reference current consumption                               |  |       | 1.4   | 2.3     | $\mu\text{A}$     |
| $T_{VREFINT}$             | Internal reference startup time                                      |  |       | 2     | 3       | ms                |
| $V_{VREF\_MEAS}$          | $V_{DDA}$ and $V_{REF+}$ voltage during $V_{REFINT}$ factory measure |  | 2.99  | 3     | 3.01    | V                 |
| $A_{VREF\_MEAS}$          | Accuracy of factory-measured $V_{REF}$ value <sup>(2)</sup>          | Including uncertainties due to ADC and $V_{DDA}/V_{REF+}$ values |       |       | $\pm 5$ | mV                |
| $T_{Coeff}^{(3)}$         | Temperature coefficient  | $-40\text{ °C} < T_J < +105\text{ °C}$                           |       | 20    | 50      | ppm/°C            |
|                           |  | $0\text{ °C} < T_J < +50\text{ °C}$                              |       |       | 20      |                   |
| $A_{Coeff}^{(3)}$         | Long-term stability  | 1000 hours, $T = 25\text{ °C}$                                   |       |       | 1000    | ppm               |
| $VDDCoeff^{(3)}$          | Voltage coefficient  | $3.0\text{ V} < V_{DDA} < 3.6\text{ V}$                          |       |       | 2000    | ppm/V             |
| $T_{S\_vrefint}^{(3)(4)}$ | ADC sampling time when reading the internal reference voltage        |  |       | 5     | 10      | $\mu\text{s}$     |
| $T_{ADC\_BUF}^{(3)}$      | Startup time of reference voltage buffer for ADC                     |  |       |       | 10      | $\mu\text{s}$     |
| $I_{BUF\_ADC}^{(3)}$      | Consumption of reference voltage buffer for ADC                      |  |       | 13.5  | 25      | $\mu\text{A}$     |
| $I_{VREF\_OUT}^{(3)}$     | $VREF\_OUT$ output current <sup>(5)</sup>                            |  |       |       | 1       | $\mu\text{A}$     |
| $C_{VREF\_OUT}^{(3)}$     | $VREF\_OUT$ output load  |  |       |       | 50      | pF                |
| $I_{LPBUF}^{(3)}$         | Consumption of reference voltage buffer for $VREF\_OUT$ and COMP     |  |       | 730   | 1200    | nA                |
| $V_{REFINT\_DIV1}^{(3)}$  | 1/4 reference voltage  |  | 24    | 25    | 26      | %<br>$V_{REFINT}$ |
| $V_{REFINT\_DIV2}^{(3)}$  | 1/2 reference voltage  |  | 49    | 50    | 51      |                   |
| $V_{REFINT\_DIV3}^{(3)}$  | 3/4 reference voltage  |  | 74    | 75    | 76      |                   |

1. Tested in production;
2. The internal  $V_{REF}$  value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by design, not tested in production.
4. Shortest sampling time can be determined in the application by multiple iterations.
5. To guarantee less than 1%  $VREF\_OUT$  deviation.

### 6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in [Figure 10: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

#### Maximum current consumption

The MCU is placed under the following conditions:

- $V_{DD} = 3.6\text{ V}$
- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted depending on  $f_{HCLK}$  frequency and voltage range
- Prefetch and 64-bit access are enabled in configurations with 1 wait state

The parameters given in [Table 15](#), [Table 11](#) and [Table 13](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 11](#).

**Table 15. Current consumption in Run mode, code with data processing running from Flash**

| Symbol                       | Parameter  | Conditions   |  | $f_{HCLK}$   | Typ     | Max <sup>(1)</sup> |       |        | Unit          |             |
|------------------------------|--|--|--|--|---------|--------------------|-------|--------|---------------|-------------|
|                              |  |  |  |  |         | 55 °C              | 85 °C | 105 °C |               |             |
| $I_{DD}$<br>(Run from Flash) | Supply current in Run mode, code executed from Flash | $f_{HSE} = f_{HCLK}$ up to 16 MHz, included<br>$f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON) <sup>(2)</sup> | Range 3,<br>$V_{CORE}=1.2\text{ V}$<br>$VOS[1:0] = 11$ | 1 MHz  | 360     | 500                | 500   | 500    | $\mu\text{A}$ |             |
|                              |  |  |  | 2 MHz  | 620     | 750                | 750   | 750    |               |             |
|                              |  |  |  | 4 MHz  | 1070    | 1200               | 1200  | 1200   |               |             |
|                              |  |  |  | Range 2,<br>$V_{CORE}=1.5\text{ V}$<br>$VOS[1:0] = 10$ | 4 MHz   | 1.30               | 1.6   | 1.6    | 1.6           | $\text{mA}$ |
|                              |  |  |  | 8 MHz  | 2.4     | 2.9                | 2.9   | 2.9    |               |             |
|                              |  |  |  | 16 MHz   | 4.6     | 5.2                | 5.2   | 5.2    |               |             |
|                              |  |  |  | Range 1,<br>$V_{CORE}=1.8\text{ V}$<br>$VOS[1:0] = 01$ | 8 MHz   | 2.9                | 3.5   | 3.5    | 3.5           |             |
|                              |  |  |  | 16 MHz   | 5.7     | 6.5                | 6.5   | 6.5    |               |             |
|                              |  |  |  | 32 MHz   | 10.4    | 12                 | 12    | 12     |               |             |
|                              |  |  | HSI clock source (16 MHz)                              | Range 2,<br>$V_{CORE}=1.5\text{ V}$<br>$VOS[1:0] = 10$ | 16 MHz  | 4.5                | 5.2   | 5.2    | 5.2           |             |
|                              |  |  |  | Range 1,<br>$V_{CORE}=1.8\text{ V}$<br>$VOS[1:0] = 01$ | 32 MHz  | 10.9               | 12.3  | 12.3   | 12.3          |             |
|                              |  |  | MSI clock, 65 kHz                                      | Range 3,<br>$V_{CORE}=1.2\text{ V}$<br>$VOS[1:0] = 11$ | 65 kHz  | 0.05               | 0.079 | 0.092  | 0.13          |             |
|                              |  |  | MSI clock, 524 kHz                                     |  | 524 kHz | 0.17               | 0.2   | 0.21   | 0.25          |             |
|                              | MSI clock, 4.2 MHz                                   | 4.2 MHz  | 1.0  |  | 1.1     | 1.1                | 1.2   |        |               |             |

1. Based on characterization, not tested in production, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).

**Table 16. Current consumption in Run mode, code with data processing running from RAM**

| Symbol                            | Parameter  | Conditions  |   | f <sub>HCLK</sub>                                     | Typ     | Max <sup>(1)</sup> |       |                     | Unit |    |
|-----------------------------------|--|---|---|---|---------|--------------------|-------|---------------------|------|----|
|                                   |  |   |   |   |         | 55 °C              | 85 °C | 105 °C              |      |    |
| I <sub>DD</sub><br>(Run from RAM) | Supply current in Run mode, code executed from RAM, Flash switched off | f <sub>HSE</sub> = f <sub>HCLK</sub> up to 16 MHz, included<br>f <sub>HSE</sub> = f <sub>HCLK</sub> /2 above 16 MHz (PLL ON) <sup>(2)</sup> | Range 3,<br>V <sub>CORE</sub> =1.2 V<br>VOS[1:0] = 11 | 1 MHz   | 310     | 470                | 470   | 470                 | μA   |    |
|                                   |  |   |   | 2 MHz   | 590     | 780                | 780   | 780                 |      |    |
|                                   |  |   |   | 4 MHz   | 1030    | 1200               | 1200  | 1200 <sup>(3)</sup> |      |    |
|                                   |  |   |   | Range 2,<br>V <sub>CORE</sub> =1.5 V<br>VOS[1:0] = 10 | 4 MHz   | 1.2                | 1.5   | 1.5                 | 1.5  | mA |
|                                   |  |   |   | 8 MHz   | 2.3     | 3                  | 3     | 3                   |      |    |
|                                   |  |   |   | 16 MHz  | 4.3     | 5                  | 5     | 5                   |      |    |
|                                   |  |   |   | Range 1,<br>V <sub>CORE</sub> =1.8 V<br>VOS[1:0] = 01 | 8 MHz   | 2.7                | 3.5   | 3.5                 | 3.5  |    |
|                                   |  |   |   | 16 MHz  | 5.0     | 5.55               | 5.55  | 5.55                |      |    |
|                                   |  |   |   | 32 MHz  | 9.8     | 10.9               | 10.9  | 10.9                |      |    |
|                                   |  |   | HSI clock source (16 MHz)                             | Range 2,<br>V <sub>CORE</sub> =1.5 V<br>VOS[1:0] = 10 | 16 MHz  | 4.3                | 4.8   | 4.8                 | 4.8  |    |
|                                   |  |   |   | Range 1,<br>V <sub>CORE</sub> =1.8 V<br>VOS[1:0] = 01 | 32 MHz  | 10.1               | 11.7  | 11.7                | 11.7 |    |
|                                   |  |   | MSI clock, 65 kHz                                     | Range 3,<br>V <sub>CORE</sub> =1.2 V<br>VOS[1:0] = 11 | 65 kHz  | 40                 | 48.5  | 63                  | 100  | μA |
|                                   |  |   | MSI clock, 524 kHz                                    |   | 524 kHz | 148                | 175   | 183                 | 215  |    |
|                                   |  |   | MSI clock, 4.2 MHz                                    |   | 4.2 MHz | 990                | 1032  | 1034                | 1100 |    |

1. Based on characterization, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).
3. Tested in production.

Table 17. Current consumption in Sleep mode

| Symbol                     | Parameter  | Conditions  |   | f <sub>HCLK</sub>                               | Typ    | Max <sup>(1)</sup> |       |                    | Unit |
|----------------------------|--|---|---|---|--------|--------------------|-------|--------------------|------|
|                            |  |   |   |   |        | 55 °C              | 85 °C | 105 °C             |      |
| I <sub>DD</sub><br>(Sleep) | Supply current in Sleep mode, code executed from RAM, Flash switched OFF | f <sub>HSE</sub> = f <sub>HCLK</sub> up to 16 MHz, included<br>f <sub>HSE</sub> = f <sub>HCLK</sub> /2 above 16 MHz (PLL ON) <sup>(2)</sup> | Range 3, V <sub>CORE</sub> =1.2 V VOS[1:0] = 11 | 1 MHz   | 180    | 220                | 220   | 220                | μA   |
|                            |  |   |   | 2 MHz   | 225    | 300                | 300   | 300                |      |
|                            |  |   |   | 4 MHz   | 300    | 380                | 380   | 380 <sup>(3)</sup> |      |
|                            |  |   | Range 2, V <sub>CORE</sub> =1.5 V VOS[1:0] = 10 | 4 MHz   | 360    | 500                | 500   | 500                |      |
|                            |  |   |   | 8 MHz   | 570    | 700                | 700   | 700                |      |
|                            |  |   |   | 16 MHz  | 990    | 1100               | 1100  | 1100               |      |
|                            |  |   | Range 1, V <sub>CORE</sub> =1.8 V VOS[1:0] = 01 | 8 MHz   | 675    | 800                | 800   | 800                |      |
|                            |  |   |   | 16 MHz  | 1150   | 1250               | 1250  | 1250               |      |
|                            |  |   |   | 32 MHz  | 2300   | 2700               | 2700  | 2700               |      |
|                            |  | HSI clock source (16 MHz)   | Range 2, V <sub>CORE</sub> =1.5 V VOS[1:0] = 10 | 16 MHz  | 1025   | 1100               | 1100  | 1100               |      |
|                            |  |   |   | Range 1, V <sub>CORE</sub> =1.8 V VOS[1:0] = 01 | 32 MHz | 2460               | 2700  | 2700               |      |
|                            |  | MSI clock, 65 kHz   | Range 3, V <sub>CORE</sub> =1.2 V VOS[1:0] = 11 | 65 kHz  | 30     | 36                 | 46    | 72                 |      |
|                            |  | MSI clock, 524 kHz  |   | 524 kHz   | 50     | 58                 | 67    | 92                 |      |
|                            |  | MSI clock, 4.2 MHz  |   | 4.2 MHz   | 210    | 245                | 251   | 273                |      |
| I <sub>DD</sub><br>(Sleep) | Supply current in Sleep mode, code executed from Flash                   | HSE = 16 MHz <sup>(2)</sup> (PLL ON for f <sub>HCLK</sub> above 16 MHz)   | Range 3, V <sub>CORE</sub> =1.2 V VOS[1:0] = 11 | 1 MHz   | 190    | 250                | 250   | 250                | μA   |
|                            |  |   |   | 2 MHz   | 235    | 300                | 300   | 300                |      |
|                            |  |   |   | 4 MHz   | 315    | 380                | 380   | 380                |      |
|                            |  |   | Range 2, V <sub>CORE</sub> =1.5 V VOS[1:0] = 10 | 4 MHz   | 390    | 500                | 500   | 500                |      |
|                            |  |   |   | 8 MHz   | 600    | 700                | 700   | 700                |      |
|                            |  |   |   | 16 MHz  | 1000   | 1120               | 1120  | 1120               |      |
|                            |  |   | Range 1, V <sub>CORE</sub> =1.8 V VOS[1:0] = 01 | 8 MHz   | 690    | 800                | 800   | 800                |      |
|                            |  |   |   | 16 MHz  | 1160   | 1300               | 1300  | 1300               |      |
|                            |  |   |   | 32 MHz  | 2310   | 2700               | 2700  | 2700               |      |
|                            |  | HSI clock source (16 MHz)   | Range 2, V <sub>CORE</sub> =1.5 V VOS[1:0] = 10 | 16 MHz  | 1040   | 1160               | 1160  | 1160               |      |
|                            |  |   |   | Range 1, V <sub>CORE</sub> =1.8 V VOS[1:0] = 01 | 32 MHz | 2500               | 2800  | 2800               |      |
| I <sub>DD</sub><br>(Sleep) | Supply current in Sleep mode, code executed from Flash                   | MSI clock, 65 kHz   | Range 3, V <sub>CORE</sub> =1.2V VOS[1:0] = 11  | 65 kHz  | 42     | 50                 | 60    | 90                 | μA   |
|                            |  | MSI clock, 524 kHz  |   | 524 kHz   | 63     | 72                 | 82    | 110                |      |
|                            |  | MSI clock, 4.2 MHz  |   | 4.2 MHz   | 230    | 263                | 265   | 290                |      |

1. Based on characterization, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register)
3. Tested in production.

**Table 18. Current consumption in Low power run mode**

| Symbol                    | Parameter                                 | Conditions   |  |                           | Typ | Max (1) | Unit    |
|---------------------------|---|--|--|---------------------------|-----|---------|---------|
| $I_{DD}$<br>(LP Run)      | Supply current in Low power run mode      | All peripherals OFF, code executed from RAM, Flash switched OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz<br>$f_{HCLK} = 32$ kHz   | $T_A = -40$ °C to $25$ °C | 11  | 14      | $\mu A$ |
|                           |   |  |  | $T_A = 85$ °C             | 26  | 32      |         |
|                           |   |  |  | $T_A = 105$ °C            | 53  | 72      |         |
|                           |   |  | MSI clock, 65 kHz<br>$f_{HCLK} = 65$ kHz   | $T_A = -40$ °C to $25$ °C | 18  | 21      |         |
|                           |   |  |  | $T_A = 85$ °C             | 33  | 40      |         |
|                           |   |  |  | $T_A = 105$ °C            | 60  | 78      |         |
|                           |   |  | MSI clock, 131 kHz<br>$f_{HCLK} = 131$ kHz | $T_A = -40$ °C to $25$ °C | 36  | 41      |         |
|                           |   |  |  | $T_A = 55$ °C             | 39  | 44      |         |
|                           |   |  |  | $T_A = 85$ °C             | 50  | 58      |         |
|                           |   | All peripherals OFF, code executed from Flash, $V_{DD}$ from 1.65 V to 3.6 V                   | MSI clock, 65 kHz<br>$f_{HCLK} = 32$ kHz   | $T_A = -40$ °C to $25$ °C | 36  | 40.5    |         |
|                           |   |  |  | $T_A = 85$ °C             | 53  | 60      |         |
|                           |   |  |  | $T_A = 105$ °C            | 81  | 100     |         |
|                           |   |  | MSI clock, 65 kHz<br>$f_{HCLK} = 65$ kHz   | $T_A = -40$ °C to $25$ °C | 44  | 49      |         |
|                           |   |  |  | $T_A = 85$ °C             | 61  | 67      |         |
|                           |   |  |  | $T_A = 105$ °C            | 89  | 107     |         |
|                           |   |  | MSI clock, 131 kHz<br>$f_{HCLK} = 131$ kHz | $T_A = -40$ °C to $25$ °C | 64  | 71      |         |
|                           |   |  |  | $T_A = 55$ °C             | 68  | 73      |         |
|                           |   |  |  | $T_A = 85$ °C             | 80  | 88      |         |
|                           |   |  |  | $T_A = 105$ °C            | 101 | 110     |         |
| $I_{DD\ max}$<br>(LP Run) | Max allowed current in Low power run mode | $V_{DD}$ from 1.65 V to 3.6 V  |  |                           |     | 200     |         |

1. Based on characterization, not tested in production, unless otherwise specified.

**Table 19. Current consumption in Low power sleep mode**

| Symbol                                     | Parameter                                   | Conditions   |  | Typ                                      | Max (1)                   | Unit |         |      |
|--|---|--|--|--|---------------------------|------|---------|------|
| $I_{DD}$ (LP Sleep)                        | Supply current in Low power sleep mode      | All peripherals OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz<br>$f_{HCLK} = 32$ kHz<br>Flash OFF            | $T_A = -40$ °C to $25$ °C                | 4.4                       |      | $\mu A$ |      |
|  |   |  | MSI clock, 65 kHz<br>$f_{HCLK} = 32$ kHz<br>Flash ON             | $T_A = -40$ °C to $25$ °C                | 18                        | 21   |         |      |
|  |   |  |  | $T_A = 85$ °C                            | 24                        | 27   |         |      |
|  |   |  |  | $T_A = 105$ °C                           | 35                        | 43   |         |      |
|  |   |  | MSI clock, 65 kHz<br>$f_{HCLK} = 65$ kHz,<br>Flash ON            | $T_A = -40$ °C to $25$ °C                | 18.6                      | 21   |         |      |
|  |   |  |  | $T_A = 85$ °C                            | 24.5                      | 28   |         |      |
|  |   |  |  | $T_A = 105$ °C                           | 35                        | 42   |         |      |
|  |   |  | MSI clock, 131 kHz<br>$f_{HCLK} = 131$ kHz,<br>Flash ON          | $T_A = -40$ °C to $25$ °C                | 22                        | 25   |         |      |
|  |   |  |  | $T_A = 55$ °C                            | 23.5                      | 26   |         |      |
|  |   |  |  | $T_A = 85$ °C                            | 28.5                      | 31   |         |      |
|  |   |  | TIM9 and USART1 enabled, Flash ON, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz<br>$f_{HCLK} = 32$ kHz | $T_A = -40$ °C to $25$ °C | 18   |         | 20.5 |
|  |   |  |  |  | $T_A = 85$ °C             | 24   |         | 27   |
|  |   | $T_A = 105$ °C                                     |  |  | 35                        | 43   |         |      |
|  |   | MSI clock, 65 kHz<br>$f_{HCLK} = 65$ kHz           |  | $T_A = -40$ °C to $25$ °C                | 18.6                      | 21   |         |      |
|  |   |  |  | $T_A = 85$ °C                            | 24.5                      | 28   |         |      |
|  |   |  |  | $T_A = 105$ °C                           | 35                        | 42   |         |      |
| MSI clock, 131 kHz<br>$f_{HCLK} = 131$ kHz | $T_A = -40$ °C to $25$ °C                   | 22   |  | 25                                       |                           |      |         |      |
|  | $T_A = 55$ °C                               | 23.5   |  | 26                                       |                           |      |         |      |
|  | $T_A = 85$ °C                               | 28.5   |  | 31                                       |                           |      |         |      |
|  | $T_A = 105$ °C                              | 39   | 45   |  |                           |      |         |      |
|  |   |  |  |  |                           |      |         |      |
|  |   |  |  |  |                           |      |         |      |
| $I_{DD}$ max (LP Sleep)                    | Max allowed current in Low power Sleep mode | $V_{DD}$ from 1.65 V to 3.6 V                      |  |  | 200                       |      |         |      |

1. Based on characterization, not tested in production, unless otherwise specified.

Table 20. Typical and maximum current consumptions in Stop mode

| Symbol  | Parameter   | Conditions  |                                     | Typ   | Max <sup>(1)</sup> | Unit |               |
|---|---|---|-------------------------------------|---|--------------------|------|---------------|
| $I_{DD}$<br>(Stop with RTC)                                 | Supply current in Stop mode with RTC enabled        | RTC clocked by LSI, regulator in LP mode, HSI and HSE OFF (no independent watchdog)                             | LCD OFF                             | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$ | 1.7                | 4    | $\mu\text{A}$ |
|   |   |   |                                     | $T_A = 55^{\circ}\text{C}$                          | 2.7                | 6    |               |
|   |   |   |                                     | $T_A = 85^{\circ}\text{C}$                          | 7                  | 10   |               |
|   |   |   |                                     | $T_A = 105^{\circ}\text{C}$                         | 15                 | 23   |               |
|   |   |   | LCD ON (static duty) <sup>(2)</sup> | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$ | 3.8                | 6    |               |
|   |   |   |                                     | $T_A = 55^{\circ}\text{C}$                          | 4.7                | 7    |               |
|   |   |   |                                     | $T_A = 85^{\circ}\text{C}$                          | 9                  | 12   |               |
|   |   |   |                                     | $T_A = 105^{\circ}\text{C}$                         | 19                 | 27   |               |
|   |   |   | LCD ON (1/8 duty) <sup>(3)</sup>    | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$ | 7.8                | 10   |               |
|   |   |   |                                     | $T_A = 55^{\circ}\text{C}$                          | 8.5                | 11   |               |
|   |   |   |                                     | $T_A = 85^{\circ}\text{C}$                          | 13                 | 16   |               |
|   |   |   |                                     | $T_A = 105^{\circ}\text{C}$                         | 26                 | 44   |               |
|   |   | RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog) | LCD OFF                             | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$ | TBD                | TBD  |               |
|   |   |   |                                     | $T_A = 55^{\circ}\text{C}$                          | TBD                | TBD  |               |
|   |   |   |                                     | $T_A = 85^{\circ}\text{C}$                          | TBD                | TBD  |               |
|   |   |   |                                     | $T_A = 105^{\circ}\text{C}$                         | TBD                | TBD  |               |
|   |   |   | LCD ON (static duty) <sup>(2)</sup> | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$ | TBD                | TBD  |               |
|   |   |   |                                     | $T_A = 55^{\circ}\text{C}$                          | TBD                | TBD  |               |
|   |   |   |                                     | $T_A = 85^{\circ}\text{C}$                          | TBD                | TBD  |               |
|   |   |   |                                     | $T_A = 105^{\circ}\text{C}$                         | TBD                | TBD  |               |
| LCD ON (1/8 duty) <sup>(3)</sup>                            | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$ |   | TBD                                 | TBD   |                    |      |               |
|   | $T_A = 55^{\circ}\text{C}$                          |   | TBD                                 | TBD   |                    |      |               |
|   | $T_A = 85^{\circ}\text{C}$                          |   | TBD                                 | TBD   |                    |      |               |
|   | $T_A = 105^{\circ}\text{C}$                         |   | TBD                                 | TBD   |                    |      |               |
| RTC clocked by LSE (no independent watchdog) <sup>(4)</sup> | LCD OFF   | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$<br>$V_{DD} = 1.8\text{V}$                                   | TBD                                 |   |                    |      |               |
|   |   | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$<br>$V_{DD} = 3.0\text{V}$                                   | TBD                                 |   |                    |      |               |
|   |   | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$<br>$V_{DD} = 3.6\text{V}$                                   | TBD                                 |   |                    |      |               |
| $I_{DD}$<br>(Stop)  | Supply current in Stop mode (RTC disabled)          | Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled                                     |                                     | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$ | 1.6                | 2.2  | $\mu\text{A}$ |
|   |   | Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)  |                                     | $T_A = -40^{\circ}\text{C}$ to $25^{\circ}\text{C}$ | 0.65               | 1    |               |
|   |   |   | $T_A = 55^{\circ}\text{C}$          | 1.6   | 3                  |      |               |
|   |   |   | $T_A = 85^{\circ}\text{C}$          | 6   | 9                  |      |               |
|   |   |   | $T_A = 105^{\circ}\text{C}$         | 14  | 22 <sup>(5)</sup>  |      |               |

**Table 20. Typical and maximum current consumptions in Stop mode (continued)**

| Symbol                            | Parameter                                   | Conditions     | Typ                            | Max <sup>(1)</sup> | Unit |
|-----------------------------------|---|----------------|--------------------------------|--------------------|------|
| I <sub>DD</sub><br>(WU from Stop) | Supply current during wakeup from Stop mode | MSI = 4.2 MHz  | T <sub>A</sub> = -40°C to 25°C | TBD                | mA   |
|                                   |   | MSI = 1.05 MHz |                                | TBD                |      |
|                                   |   | MSI = 65 kHz   |                                | TBD                |      |

1. Based on characterization, not tested in production, unless otherwise specified
2. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected
3. LCD enabled with external VLCD, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
5. Tested in production.

**Table 21. Typical and maximum current consumptions in Standby mode**

| Symbol                                | Parameter                                       | Conditions  | Typ                              | Max <sup>(1)</sup>               | Unit               |     |
|---------------------------------------|---|---|----------------------------------|----------------------------------|--------------------|-----|
| I <sub>DD</sub><br>(Standby with RTC) | Supply current in Standby mode with RTC enabled | RTC clocked by LSI (no independent watchdog)                | T <sub>A</sub> = -40 °C to 25 °C | 1.3                              | 1.9                | µA  |
|                                       |   |   | T <sub>A</sub> = 55 °C           | 1.5                              | 2.2                |     |
|                                       |   |   | T <sub>A</sub> = 85 °C           | 2.15                             | 4                  |     |
|                                       |   |   | T <sub>A</sub> = 105 °C          | 3.8                              | 8.3 <sup>(2)</sup> |     |
|                                       |   | RTC clocked by LSE (no independent watchdog) <sup>(3)</sup> | T <sub>A</sub> = -40 °C to 25 °C | TBD                              |                    |     |
|                                       |   |   | T <sub>A</sub> = 55 °C           | TBD                              |                    |     |
|                                       |   |   | T <sub>A</sub> = 85 °C           | TBD                              |                    |     |
|                                       |   |   | T <sub>A</sub> = 105 °C          | TBD                              |                    |     |
| I <sub>DD</sub><br>(Standby)          | Supply current in Standby mode (RTC disabled)   | Independent watchdog and LSI enabled                        | T <sub>A</sub> = -40 °C to 25 °C | 1.3                              | 1.7                |     |
|                                       |   |   | Independent watchdog and LSI OFF | T <sub>A</sub> = -40 °C to 25 °C | 0.35               | 0.6 |
|                                       |   | T <sub>A</sub> = 55 °C                                      |                                  | 0.47                             | 0.9                |     |
|                                       |   | T <sub>A</sub> = 85 °C                                      |                                  | 1.2                              | 2.75               |     |
|                                       |   | T <sub>A</sub> = 105 °C                                     | 2.9                              | 7 <sup>(2)</sup>                 |                    |     |
| I <sub>DD</sub><br>(WU from Standby)  | Supply current during wakeup from Standby mode  |   | T <sub>A</sub> = -40 °C to 25 °C | TBD                              |                    |     |

1. Based on characterization, not tested in production, unless otherwise specified
2. Tested in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

**Wakeup time from low-power mode**

The wakeup times given in the following table are measured with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Stop mode
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 11](#).

**Table 22. Typical and maximum timings in Low power modes**

| Symbol                           | Parameter   | Conditions  | Typ  | Max <sup>(1)</sup> | Unit |
|----------------------------------|---|---|------|--------------------|------|
| t <sub>WUSLEEP</sub>             | Wakeup from Sleep mode  | f <sub>HCLK</sub> = 32 MHz  | 0.4  |                    | μs   |
| t <sub>WUSLEEP_LP</sub>          | Wakeup from Low power sleep mode<br>f <sub>HCLK</sub> = 262 kHz | f <sub>HCLK</sub> = 262 kHz<br>Flash enabled                            | 46   |                    |      |
|                                  |   | f <sub>HCLK</sub> = 262 kHz<br>Flash switched OFF                       | 46   |                    |      |
| t <sub>WUSTOP</sub>              | Wakeup from Stop mode, regulator in Run mode                    | f <sub>HCLK</sub> = f <sub>MSI</sub> = 4.2 MHz                          | TBD  |                    |      |
|                                  |   | f <sub>HCLK</sub> = f <sub>MSI</sub> = 4.2 MHz<br>Voltage range 1 and 2 | 7.7  | 8.9                |      |
|                                  | Wakeup from Stop mode, regulator in low power mode              | f <sub>HCLK</sub> = f <sub>MSI</sub> = 4.2 MHz<br>Voltage range 3       | 8.2  | 13.1               |      |
|                                  |   | f <sub>HCLK</sub> = f <sub>MSI</sub> = 2.1 MHz                          | 10.2 | 13.4               |      |
|                                  |   | f <sub>HCLK</sub> = f <sub>MSI</sub> = 1.05 MHz                         | 16   | 20                 |      |
|                                  |   | f <sub>HCLK</sub> = f <sub>MSI</sub> = 524 kHz                          | 31   | 37                 |      |
|                                  |   | f <sub>HCLK</sub> = f <sub>MSI</sub> = 262 kHz                          | 57   | 66                 |      |
|                                  |   | f <sub>HCLK</sub> = f <sub>MSI</sub> = 131 kHz                          | 112  | 123                |      |
| f <sub>HCLK</sub> = MSI = 65 kHz | 221   | 236   |      |                    |      |
| t <sub>WUSTDBY</sub>             | Wakeup from Standby mode<br>FWU bit = 1                         | f <sub>HCLK</sub> = MSI = 2.1 MHz                                       | 58   | 104                |      |
|                                  | Wakeup from Standby mode<br>FWU bit = 0                         | f <sub>HCLK</sub> = MSI = 2.1 MHz                                       | 2.6  | 3.25               | ms   |

1. Based on characterization, not tested in production, unless otherwise specified

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

### 6.3.5 External clock source characteristics

#### High-speed external user clock generated from an external source

**Table 23. High-speed external user clock characteristics<sup>(1)</sup>**

| Symbol                       | Parameter                            | Conditions                       | Min         | Typ | Max         | Unit    |
|------------------------------|--------------------------------------|----------------------------------|-------------|-----|-------------|---------|
| $f_{HSE\_ext}$               | User external clock source frequency |                                  | 1           | 8   | 32          | MHz     |
| $V_{HSEH}$                   | OSC_IN input pin high level voltage  |                                  | $0.7V_{DD}$ |     | $V_{DD}$    | V       |
| $V_{HSEL}$                   | OSC_IN input pin low level voltage   |                                  | $V_{SS}$    |     | $0.3V_{DD}$ |         |
| $t_{w(HSE)}$<br>$t_{w(HSE)}$ | OSC_IN high or low time              |                                  | 12          |     |             | ns      |
| $t_{r(HSE)}$<br>$t_{f(HSE)}$ | OSC_IN rise or fall time             |                                  |             |     | 20          |         |
| $C_{in(HSE)}$                | OSC_IN input capacitance             |                                  |             | 2.6 |             | pF      |
| $DuCy_{(HSE)}$               | Duty cycle                           |                                  | 45          |     | 55          | %       |
| $I_L$                        | OSC_IN Input leakage current         | $V_{SS} \leq V_{IN} \leq V_{DD}$ |             |     | $\pm 1$     | $\mu A$ |

1. Guaranteed by design, not tested in production.

**Low-speed external user clock generated from an external source**

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 11](#).

**Table 24. Low-speed external user clock characteristics<sup>(1)</sup>**

| Symbol                       | Parameter                             | Conditions                       | Min         | Typ    | Max         | Unit    |
|------------------------------|---------------------------------------|----------------------------------|-------------|--------|-------------|---------|
| $f_{LSE\_ext}$               | User external clock source frequency  |                                  | 1           | 32.768 | 1000        | kHz     |
| $V_{LSEH}$                   | OSC32_IN input pin high level voltage |                                  | $0.7V_{DD}$ |        | $V_{DD}$    | V       |
| $V_{LSEL}$                   | OSC32_IN input pin low level voltage  |                                  | $V_{SS}$    |        | $0.3V_{DD}$ |         |
| $t_{w(LSE)}$<br>$t_{w(LSE)}$ | OSC32_IN high or low time             |                                  | TBD         |        |             | ns      |
| $t_{r(LSE)}$<br>$t_{f(LSE)}$ | OSC32_IN rise or fall time            |                                  |             |        | TBD         |         |
| $C_{IN(LSE)}$                | OSC32_IN input capacitance            |                                  |             | 0.6    |             | pF      |
| $DuCy_{(LSE)}$               | Duty cycle                            |                                  | TBD         |        | TBD         | %       |
| $I_L$                        | OSC32_IN Input leakage current        | $V_{SS} \leq V_{IN} \leq V_{DD}$ |             |        | $\pm 1$     | $\mu A$ |

1. Guaranteed by design, not tested in production

**Figure 11. Low-speed external clock source AC timing diagram**

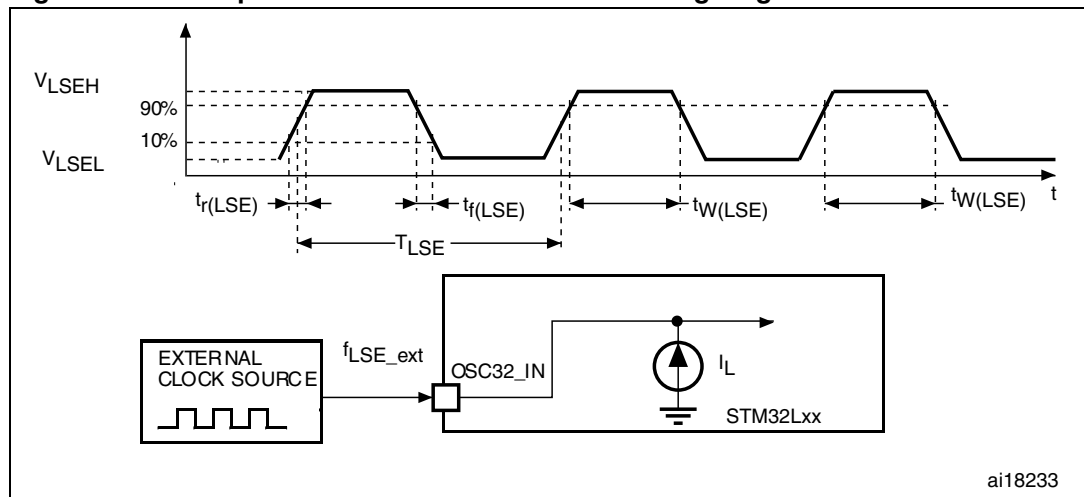
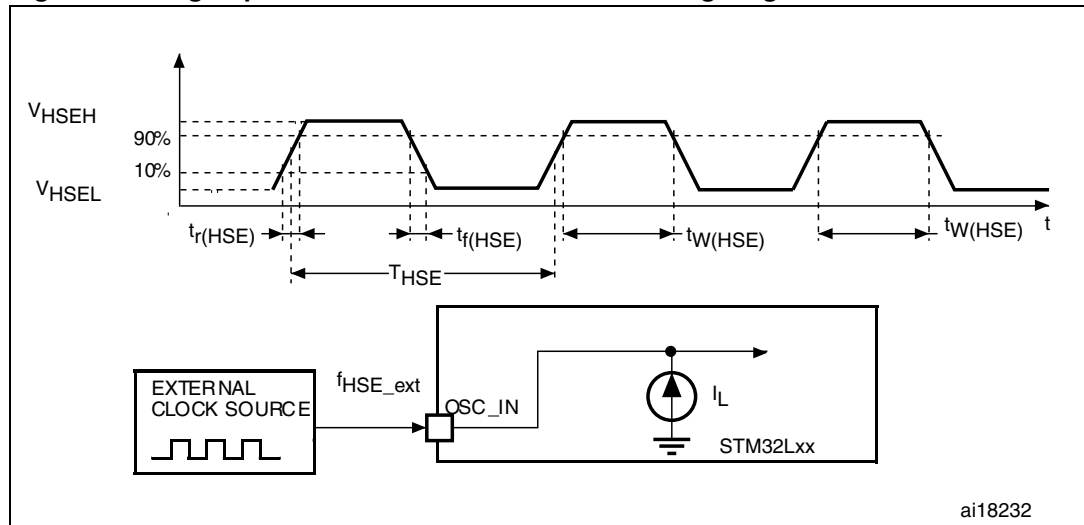


Figure 12. High-speed external clock source AC timing diagram



**High-speed external clock generated from a crystal/ceramic resonator**

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 25](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

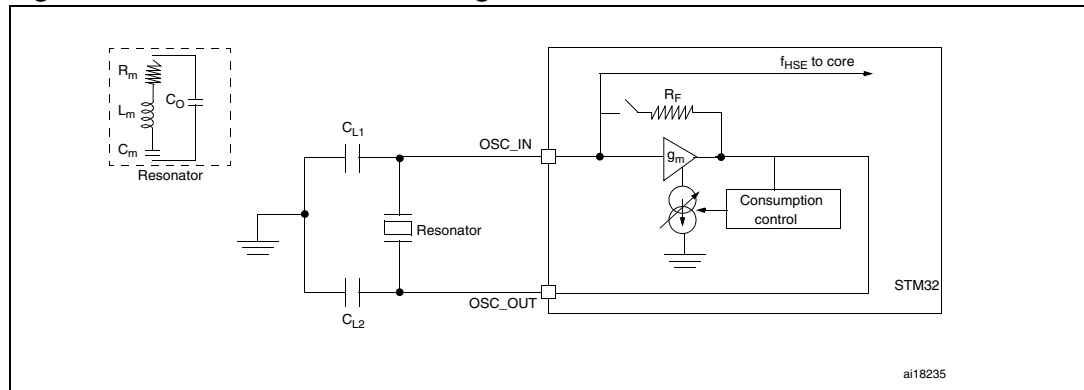
**Table 25. HSE 1-24 MHz oscillator characteristics<sup>(1)(2)</sup>**

| Symbol                      | Parameter  | Conditions  | Min | Typ | Max                                | Unit     |
|-----------------------------|--|---|-----|-----|------------------------------------|----------|
| f <sub>OSC_IN</sub>         | Oscillator frequency   |   | 1   |     | 24                                 | MHz      |
| R <sub>F</sub>              | Feedback resistor  |   |     | 200 |                                    | kΩ       |
| C                           | Recommended load capacitance versus equivalent serial resistance of the crystal (R <sub>S</sub> ) <sup>(3)</sup> | R <sub>S</sub> = 30 Ω   |     | 20  |                                    | pF       |
| I <sub>HSE</sub>            | HSE driving current  | V <sub>DD</sub> = 3.3 V, V <sub>IN</sub> = V <sub>SS</sub><br>with 30 pF load |     |     | 3                                  | mA       |
| I <sub>DD(HSE)</sub>        | HSE oscillator power consumption   | C = 20 pF<br>f <sub>OSC</sub> = 16 MHz  |     |     | 2.5 (startup)<br>0.7 (stabilized)  | mA       |
|                             |  | C = 10 pF<br>f <sub>OSC</sub> = 16 MHz  |     |     | 2.5 (startup)<br>0.46 (stabilized) |          |
| g <sub>m</sub>              | Oscillator transconductance  | Startup   | 3.5 |     |                                    | mA<br>/V |
| t <sub>SU(HSE)</sub><br>(4) | Startup time   | V <sub>DD</sub> is stabilized   |     | 1   |                                    | ms       |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. t<sub>SU(HSE)</sub> is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C<sub>L1</sub> and C<sub>L2</sub>, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 13](#)). C<sub>L1</sub> and C<sub>L2</sub> are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C<sub>L1</sub> and C<sub>L2</sub>. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C<sub>L1</sub> and C<sub>L2</sub>. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website [www.st.com](http://www.st.com).

Figure 13. HSE oscillator circuit diagram



1.  $R_{EXT}$  value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 26](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 26. LSE oscillator characteristics ( $f_{LSE} = 32.768 \text{ kHz}$ )<sup>(1)</sup>

| Symbol                 | Parameter  | Conditions                                | Min | Typ    | Max | Unit |
|------------------------|--|---|-----|--------|-----|------|
| $f_{LSE}$              | Low speed external oscillator frequency  |   |     | 32.768 |     | kHz  |
| $R_F$                  | Feedback resistor  |   |     | 1.2    |     | MΩ   |
| $C^{(2)}$              | Recommended load capacitance versus equivalent serial resistance of the crystal ( $R_S$ ) <sup>(3)</sup> | $R_S = 30 \text{ k}\Omega$                |     | 8      |     | pF   |
| $I_{LSE}$              | LSE driving current  | $V_{DD} = 3.3 \text{ V}, V_{IN} = V_{SS}$ |     |        | 1.1 | μA   |
| $I_{DD} \text{ (LSE)}$ | LSE oscillator current consumption   | $V_{DD} = 1.8 \text{ V}$                  |     | 450    |     | nA   |
|                        |  | $V_{DD} = 3.0 \text{ V}$                  |     | 600    |     |      |
|                        |  | $V_{DD} = 3.6 \text{ V}$                  |     | 750    |     |      |
| $g_m$                  | Oscillator transconductance  |   | 3   |        |     | μA/V |
| $t_{SU(LSE)}^{(4)}$    | Startup time   | $V_{DD}$ is stabilized                    |     | 1      |     | s    |

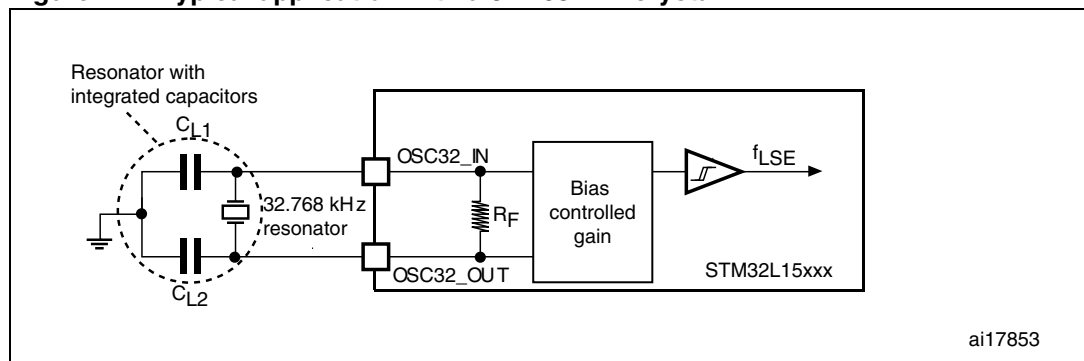
1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small  $R_S$  value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details;
4.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

**Note:** For  $C_{L1}$  and  $C_{L2}$ , it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 14).  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . Load capacitance  $C_L$  has the following formula:  $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$  where  $C_{stray}$  is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

**Caution:** To avoid exceeding the maximum value of  $C_{L1}$  and  $C_{L2}$  (15 pF) it is strongly recommended to use a resonator with a load capacitance  $C_L \leq 7$  pF. Never use a resonator with a load capacitance of 12.5 pF.

**Example:** if you choose a resonator with a load capacitance of  $C_L = 6$  pF and  $C_{stray} = 2$  pF, then  $C_{L1} = C_{L2} = 8$  pF.

**Figure 14. Typical application with a 32.768 kHz crystal**



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### 6.3.6 Internal clock source characteristics

The parameters given in [Table 27](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 11](#).

#### High-speed internal (HSI) RC oscillator

**Table 27. HSI oscillator characteristics**

| Symbol              | Parameter   | Conditions   | Min        | Typ       | Max       | Unit          |
|---------------------|---|--|------------|-----------|-----------|---------------|
| $f_{HSI}$           | Frequency   | $V_{DD} = 3.0\text{ V}$  |            | 16        |           | MHz           |
| $TRIM^{(1)(2)}$     | HSI user-trimmed resolution                       | Trimming code is not a multiple of 16  |            | $\pm 0.4$ | 0.7       | %             |
|                     |   | Trimming code is a multiple of 16  |            |           | $\pm 1.5$ | %             |
| $ACC_{HSI}^{(2)}$   | Accuracy of the factory-calibrated HSI oscillator | $V_{DDA} = 3.0\text{ V}, T_A = 25\text{ }^\circ\text{C}$                                     | $-1^{(3)}$ |           | $1^{(3)}$ | %             |
|                     |   | $V_{DDA} = 3.0\text{ V}, T_A = 0\text{ to }55\text{ }^\circ\text{C}$                         | -1.5       |           | 1.5       | %             |
|                     |   | $V_{DDA} = 3.0\text{ V}, T_A = -10\text{ to }70\text{ }^\circ\text{C}$                       | -2         |           | 2         | %             |
|                     |   | $V_{DDA} = 3.0\text{ V}, T_A = -10\text{ to }85\text{ }^\circ\text{C}$                       | -2.5       |           | 2         | %             |
|                     |   | $V_{DDA} = 3.0\text{ V}, T_A = -10\text{ to }105\text{ }^\circ\text{C}$                      | -4         |           | 2         | %             |
|                     |   | $V_{DDA} = 1.65\text{ V to }3.6\text{ V}$<br>$T_A = -40\text{ to }105\text{ }^\circ\text{C}$ | -4         |           | 3         | %             |
| $t_{SU(HSI)}^{(2)}$ | HSI oscillator startup time                       |  |            | 3.7       | 6         | $\mu\text{s}$ |
| $I_{DD(HSI)}^{(2)}$ | HSI oscillator power consumption                  |  |            | 100       | 140       | $\mu\text{A}$ |

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Based on characterization, not tested in production.
3. Tested in production.

#### Low-speed internal (LSI) RC oscillator

**Table 28. LSI oscillator characteristics**

| Symbol              | Parameter  | Min | Typ | Max | Unit          |
|---------------------|--|-----|-----|-----|---------------|
| $f_{LSI}^{(1)}$     | LSI frequency  | 26  | 38  | 56  | kHz           |
| $D_{LSI}^{(2)}$     | LSI oscillator frequency drift<br>$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | -10 |     | 4   | %             |
| $t_{SU(LSI)}^{(3)}$ | LSI oscillator startup time  |     |     | 200 | $\mu\text{s}$ |
| $I_{DD(LSI)}^{(3)}$ | LSI oscillator power consumption   |     | 400 | 510 | nA            |

1. Tested in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design, not tested in production.

**Multi-speed internal (MSI) RC oscillator**

**Table 29. MSI oscillator characteristics**

| Symbol                | Parameter  | Condition   | Typ       | Max         | Unit          |  |     |
|-----------------------|--|-------------|-----------|-------------|---------------|--|-----|
| $f_{MSI}$             | Frequency after factory calibration, done at $V_{DD}= 3.3\text{ V}$ and $T_A = 25\text{ °C}$           | MSI range 0 | 65.5      |             | kHz           |  |     |
|                       |  | MSI range 1 | 131       |             |               |  |     |
|                       |  | MSI range 2 | 262       |             |               |  |     |
|                       |  |             |           | MSI range 3 | 524           |  | MHz |
|                       |  |             |           | MSI range 4 | 1.05          |  |     |
|                       |  |             |           | MSI range 5 | 2.1           |  |     |
|                       |  |             |           | MSI range 6 | 4.2           |  |     |
| $ACC_{MSI}$           | Frequency error after factory calibration  |             | $\pm 0.5$ |             | %             |  |     |
| $D_{TEMP(MSI)}^{(1)}$ | MSI oscillator frequency drift<br>$0\text{ °C} \leq T_A \leq 85\text{ °C}$                             |             | $\pm 3$   |             | %             |  |     |
| $D_{VOLT(MSI)}^{(1)}$ | MSI oscillator frequency drift<br>$1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $T_A = 25\text{ °C}$ |             |           | 2.5         | %/V           |  |     |
| $I_{DD(MSI)}^{(2)}$   | MSI oscillator power consumption   | MSI range 0 | 0.75      |             | $\mu\text{A}$ |  |     |
|                       |  | MSI range 1 | 1         |             |               |  |     |
|                       |  | MSI range 2 | 1.5       |             |               |  |     |
|                       |  | MSI range 3 | 2.5       |             |               |  |     |
|                       |  | MSI range 4 | 4.5       |             |               |  |     |
|                       |  | MSI range 5 | 8         |             |               |  |     |
|                       |  | MSI range 6 | 15        |             |               |  |     |

**Table 29. MSI oscillator characteristics (continued)**

| Symbol                                | Parameter                          | Condition                          | Typ | Max | Unit |
|---------------------------------------|------------------------------------|------------------------------------|-----|-----|------|
| t <sub>SU(MSI)</sub>                  | MSI oscillator startup time        | MSI range 0                        | 30  |     | μs   |
|                                       |                                    | MSI range 1                        | 20  |     |      |
|                                       |                                    | MSI range 2                        | 15  |     |      |
|                                       |                                    | MSI range 3                        | 10  |     |      |
|                                       |                                    | MSI range 4                        | 6   |     |      |
|                                       |                                    | MSI range 5                        | 5   |     |      |
|                                       |                                    | MSI range 6, Voltage range 1 and 2 | 3.5 |     |      |
|                                       |                                    | MSI range 6, Voltage range 3       | 5   |     |      |
| t <sub>STAB(MSI)</sub> <sup>(2)</sup> | MSI oscillator stabilization time  | MSI range 0                        |     | 40  | μs   |
|                                       |                                    | MSI range 1                        |     | 20  |      |
|                                       |                                    | MSI range 2                        |     | 10  |      |
|                                       |                                    | MSI range 3                        |     | 4   |      |
|                                       |                                    | MSI range 4                        |     | 2.5 |      |
|                                       |                                    | MSI range 5                        |     | 2   |      |
|                                       |                                    | MSI range 6, Voltage range 1 and 2 |     | 2   |      |
|                                       |                                    | MSI range 3, Voltage range 3       |     | 3   |      |
| f <sub>OVER(MSI)</sub>                | MSI oscillator frequency overshoot | Any range to range 5               |     | 4   | MHz  |
|                                       |                                    | Any range to range 6               |     | 6   |      |

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Based on characterization, not tested in production.

### 6.3.7 PLL characteristics

The parameters given in [Table 30](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 11](#).

**Table 30. PLL characteristics**

| Symbol                 | Parameter   | Value |     |                    | Unit |
|------------------------|---|-------|-----|--------------------|------|
|                        |   | Min   | Typ | Max <sup>(1)</sup> |      |
| f <sub>PLL_IN</sub>    | PLL input clock <sup>(2)</sup>                                    | 2     |     | 24                 | MHz  |
|                        | PLL input clock duty cycle  | 45    |     | 55                 | %    |
| f <sub>PLL_OUT</sub>   | PLL output clock  | 2     |     | 32                 | MHz  |
| t <sub>LOCK</sub>      | Worst case PLL lock time<br>PLL input = 2 MHz<br>PLL VCO = 96 MHz |       | 100 | 130                | μs   |
| Jitter                 | Cycle-to-cycle jitter   |       |     | ±600               | ps   |
| I <sub>DDA</sub> (PLL) | Current consumption on V <sub>DDA</sub>                           |       | 220 | 450                | μA   |
| I <sub>DD</sub> (PLL)  | Current consumption on V <sub>DD</sub>                            |       | 120 | 150                |      |

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f<sub>PLL\_OUT</sub>.

### 6.3.8 Memory characteristics

The characteristics are given at T<sub>A</sub> = -40 to 105 °C unless otherwise specified.

#### RAM memory

**Table 31. RAM and hardware registers**

| Symbol | Parameter                          | Conditions           | Min  | Typ | Max | Unit |
|--------|------------------------------------|----------------------|------|-----|-----|------|
| VRM    | Data retention mode <sup>(1)</sup> | STOP mode (or RESET) | 1.65 |     |     | V    |

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory

Table 32. Flash memory characteristics

| Symbol            | Parameter  | Conditions                                      | Min  | Typ  | Max <sup>(1)</sup> | Unit |
|-------------------|--|---|------|------|--------------------|------|
| V <sub>DD</sub>   | Operating voltage<br>Read / Write / Erase  |   | 1.65 |      | 3.6                | V    |
| t <sub>prog</sub> | Programming time for<br>word or half-page  | Erasing   |      | 3.28 | 3.94               | ms   |
|                   |  | Programming                                     |      | 3.28 | 3.94               |      |
| I <sub>DD</sub>   | Average current during<br>the whole programming /<br>erase operation               | T <sub>A</sub> = 25 °C, V <sub>DD</sub> = 3.6 V |      | 600  | TBD                | μA   |
|                   | Maximum current (peak)<br>during the whole pro-<br>gramming / erase opera-<br>tion |   |      | 1.5  | TBD                | mA   |

1. Guaranteed by design, not tested in production.

Table 33. Flash memory endurance and data retention

| Symbol                          | Parameter   | Conditions                          | Value              |     |     | Unit    |
|---------------------------------|---|-------------------------------------|--------------------|-----|-----|---------|
|                                 |   |                                     | Min <sup>(1)</sup> | Typ | Max |         |
| N <sub>CYC</sub> <sup>(2)</sup> | Cycling (erase / write )<br>Program memory  | T <sub>A</sub> = -40°C to<br>105 °C | 10                 |     |     | kcycles |
|                                 | Cycling (erase / write )<br>EEPROM data memory                                      |                                     | 300                |     |     |         |
| t <sub>RET</sub> <sup>(2)</sup> | Data retention (program memory) after<br>10 kcycles at T <sub>A</sub> = 85 °C       | T <sub>RET</sub> = +85 °C           | 30                 |     |     | years   |
|                                 | Data retention (EEPROM data memory)<br>after 300 kcycles at T <sub>A</sub> = 85 °C  |                                     | 30                 |     |     |         |
|                                 | Data retention (program memory) after<br>10 kcycles at T <sub>A</sub> = 105 °C      | T <sub>RET</sub> = +105 °C          | 10                 |     |     |         |
|                                 | Data retention (EEPROM data memory)<br>after 300 kcycles at T <sub>A</sub> = 105 °C |                                     | 10                 |     |     |         |

1. Based on characterization not tested in production.

2. Characterization is done according to JEDEC JESD22-A117.

### 6.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 34](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 34. EMS characteristics**

| Symbol     | Parameter   | Conditions  | Level/Class |
|------------|---|---|-------------|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance  | $V_{DD} = 3.3\text{ V}$ , LQFP100, $T_A = +25\text{ °C}$ ,<br>$f_{HCLK} = 32\text{ MHz}$<br>conforms to IEC 61000-4-2 | 2B          |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$ , LQFP100, $T_A = +25\text{ °C}$ ,<br>$f_{HCLK} = 32\text{ MHz}$<br>conforms to IEC 61000-4-4 | 4A          |

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

**Prequalification trials**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 35. EMI characteristics**

| Symbol           | Parameter  | Conditions   | Monitored frequency band | Max vs. frequency range |                        |                        | Unit |
|------------------|------------|--|--------------------------|-------------------------|------------------------|------------------------|------|
|                  |            |  |                          | 4 MHz voltage range 3   | 16 MHz voltage range 2 | 32 MHz voltage range 1 |      |
| S <sub>EMI</sub> | Peak level | V <sub>DD</sub> = 3.3 V,<br>T <sub>A</sub> = 25 °C,<br>LQFP100 package<br>compliant with IEC 61967-2 | 0.1 to 30 MHz            | 3                       | -6                     | -5                     | dBμV |
|                  |            |  | 30 to 130 MHz            | 18                      | 4                      | -7                     |      |
|                  |            |  | 130 MHz to 1GHz          | 15                      | 5                      | -7                     |      |
|                  |            |  | SAE EMI Level            | 2.5                     | 2                      | 1                      | -    |

**6.3.10 Absolute maximum ratings (electrical sensitivity)**

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 36. ESD absolute maximum ratings**

| Symbol                | Ratings   | Conditions   | Class | Maximum value <sup>(1)</sup> | Unit |
|-----------------------|---|--|-------|------------------------------|------|
| V <sub>ESD(HBM)</sub> | Electrostatic discharge voltage (human body model)    | T <sub>A</sub> = +25 °C, conforming to JESD22-A114 | 2     | 2000                         | V    |
| V <sub>ESD(CDM)</sub> | Electrostatic discharge voltage (charge device model) | T <sub>A</sub> = +25 °C, conforming to JESD22-C101 | II    | 500                          |      |

1. Based on characterization results, not tested in production.

**Static latch-up**

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 37. Electrical sensitivities**

| Symbol | Parameter             | Conditions                                     | Class      |
|--------|-----------------------|--|------------|
| LU     | Static latch-up class | T <sub>A</sub> = +105 °C conforming to JESD78A | II level A |

**6.3.11 I/O current injection characteristics**

As a general rule, current injection to the I/O pins, due to external voltage below V<sub>SS</sub> or above V<sub>DD</sub> (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

**Functional susceptibility to I/O current injection**

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

**Table 38. I/O current injection susceptibility**

| Symbol           | Description                                    | Functional susceptibility |                    | Unit |
|------------------|--|---------------------------|--------------------|------|
|                  |  | Negative injection        | Positive injection |      |
| I <sub>INJ</sub> | Injected current on true open-drain pins       | -5                        | +0                 | mA   |
|                  | Injected current on all 5 V tolerant (FT) pins | -5                        | +0                 |      |
|                  | Injected current on any other pin              | -5                        | +5                 |      |

### 6.3.12 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 39](#) are derived from tests performed under the conditions summarized in [Table 11](#). All I/Os are CMOS and TTL compliant.

**Table 39. I/O static characteristics**

| Symbol    | Parameter  | Conditions  | Min                   | Typ  | Max               | Unit       |
|-----------|--|---|-----------------------|------|-------------------|------------|
| $V_{IL}$  | Input low level voltage  | TTL ports<br>$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$             | $V_{SS} - 0.3$        |      | 0.8               | V          |
| $V_{IH}$  | Standard I/O input high level voltage                          |   | $2^{(1)}$             |      | $V_{DD} + 0.3$    |            |
|           | FT <sup>(2)</sup> I/O input high level voltage                 |   |                       | 5.5V |                   |            |
| $V_{IL}$  | Input low level voltage  | CMOS ports<br>$1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$           | -0.3                  |      | $0.3V_{DD}^{(3)}$ | V          |
| $V_{IH}$  | Standard I/O Input high level voltage                          | CMOS ports<br>$1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$           | $0.7 V_{DD}^{(3)(4)}$ |      | $V_{DD} + 0.3$    |            |
|           | FT <sup>(5)</sup> I/O input high level voltage                 | CMOS ports<br>$1.65\text{ V} \leq V_{DD} \leq 2.0\text{ V}$           |                       |      | 5.25              |            |
|           |  | CMOS ports<br>$2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$            |                       |      | 5.5               |            |
| $V_{hys}$ | Standard I/O Schmitt trigger voltage hysteresis <sup>(6)</sup> |   | $10\% V_{DD}^{(7)}$   |      |                   |            |
| $I_{Ikg}$ | Input leakage current <sup>(8)(3)</sup>                        | $V_{SS} \leq V_{IN} \leq V_{DD}$<br>I/Os with LCD                     |                       |      | $\pm 50$          | nA         |
|           |  | $V_{SS} \leq V_{IN} \leq V_{DD}$<br>I/Os with analog switches         |                       |      | $\pm 50$          |            |
|           |  | $V_{SS} \leq V_{IN} \leq V_{DD}$<br>I/Os with analog switches and LCD |                       |      | $\pm 50$          |            |
|           |  | $V_{SS} \leq V_{IN} \leq V_{DD}$<br>I/Os with USB                     |                       |      | TBD               |            |
|           |  | $V_{SS} \leq V_{IN} \leq V_{DD}$<br>Standard I/Os                     |                       |      | $\pm 50$          |            |
| $R_{PU}$  | Weak pull-up equivalent resistor <sup>(9)(3)</sup>             | $V_{IN} = V_{SS}$   | 30                    | 45   | 60                | k $\Omega$ |
| $R_{PD}$  | Weak pull-down equivalent resistor <sup>(9)(3)</sup>           | $V_{IN} = V_{DD}$   | 30                    | 45   | 60                | k $\Omega$ |
| $C_{IO}$  | I/O pin capacitance  |   |                       | 5    |                   | pF         |

1. Guaranteed by design.
2. FT = 5V tolerant. To sustain a voltage higher than  $V_{DD} + 0.5$  the internal pull-up/pull-down resistors must be disabled.
3. Tested in production
4.  $0.7V_{DD}$  for 5V-tolerant receiver
5. FT = Five-volt tolerant.
6. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
7. With a minimum of 200 mV. Based on characterization, not tested in production.

- 8. The max. value may be exceeded if negative current is injected on adjacent pins.
- 9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

**Output driving current**

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA with the non-standard  $V_{OL}/V_{OH}$  specifications given in [Table 40](#).

in the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $I_{VDD}$  (see [Table 9](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $I_{VSS}$  (see [Table 9](#)).

**Output voltage levels**

Unless otherwise specified, the parameters given in [Table 40](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 11](#). All I/Os are CMOS and TTL compliant.

**Table 40. Output voltage characteristics**

| Symbol            | Parameter   | Conditions  | Min           | Max  | Unit |
|-------------------|---|---|---------------|------|------|
| $V_{OL}^{(1)(2)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time     | $I_{IO} = +8 \text{ mA}$<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$  |               | 0.4  | V    |
| $V_{OH}^{(3)(2)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time |   | 2.4           |      |      |
| $V_{OL}^{(1)(4)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time     | $I_{IO} = +4 \text{ mA}$<br>$1.65 \text{ V} < V_{DD} < 2.7 \text{ V}$ |               | 0.45 |      |
| $V_{OH}^{(3)(4)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time |   | $V_{DD}-0.45$ |      |      |
| $V_{OL}^{(1)(4)}$ | Output low level voltage for an I/O pin when 4 pins are sunk at same time     | $I_{IO} = +20 \text{ mA}$<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ |               | 1.3  |      |
| $V_{OH}^{(3)(4)}$ | Output high level voltage for an I/O pin when 4 pins are sourced at same time |   | $V_{DD}-1.3$  |      |      |

1. The  $I_{IO}$  current sunk by the device must always respect the absolute maximum rating specified in [Table 9](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
2. Tested in production.
3. The  $I_{IO}$  current sourced by the device must always respect the absolute maximum rating specified in [Table 9](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VDD}$ .
4. Based on characterization data, not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 15](#) and [Table 41](#), respectively.

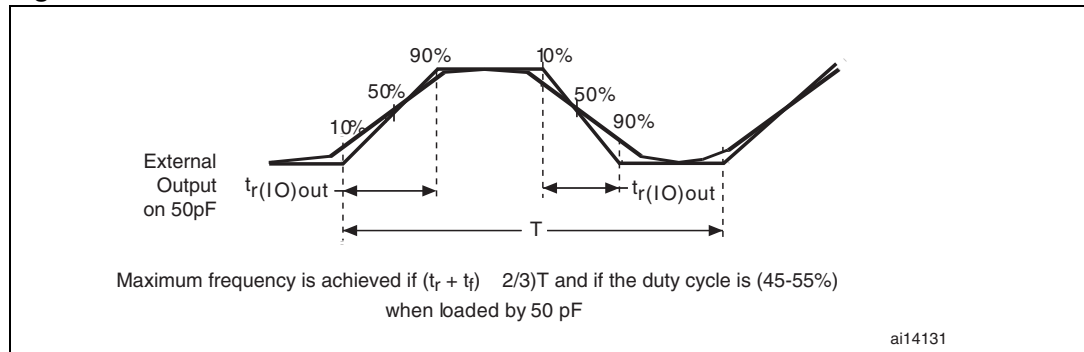
Unless otherwise specified, the parameters given in [Table 41](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 11](#).

**Table 41. I/O AC characteristics<sup>(1)</sup>**

| OSPEEDRx [1:0] bit value <sup>(1)</sup> | Symbol   | Parameter   | Conditions   | Min | Max <sup>(2)</sup> | Unit |
|---|--|---|--|-----|--------------------|------|
| 00                                      | $f_{\max(\text{IO})\text{out}}$                              | Maximum frequency <sup>(3)</sup>                                | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$  |     | 400                | kHz  |
|   |  |   | $C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$ |     | TBD                |      |
|   | $t_{f(\text{IO})\text{out}}$<br>$t_{r(\text{IO})\text{out}}$ | Output rise and fall time                                       | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$  |     | 625                | ns   |
|   |  |   | $C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$ |     | TBD                |      |
| 01                                      | $f_{\max(\text{IO})\text{out}}$                              | Maximum frequency <sup>(3)</sup>                                | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$  |     | 2                  | MHz  |
|   |  |   | $C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$ |     | 1                  |      |
|   | $t_{f(\text{IO})\text{out}}$<br>$t_{r(\text{IO})\text{out}}$ | Output rise and fall time                                       | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$  |     | 125                | ns   |
|   |  |   | $C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$ |     | TBD                |      |
| 10                                      | $F_{\max(\text{IO})\text{out}}$                              | Maximum frequency <sup>(3)</sup>                                | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$  |     | 10                 | MHz  |
|   |  |   | $C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$ |     | 2                  |      |
|   | $t_{f(\text{IO})\text{out}}$<br>$t_{r(\text{IO})\text{out}}$ | Output rise and fall time                                       | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$  |     | 25                 | ns   |
|   |  |   | $C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$ |     | TBD                |      |
| 11                                      | $F_{\max(\text{IO})\text{out}}$                              | Maximum frequency <sup>(3)</sup>                                | $C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$  |     | 50                 | MHz  |
|   |  |   | $C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$ |     | 8                  |      |
|   | $t_{f(\text{IO})\text{out}}$<br>$t_{r(\text{IO})\text{out}}$ | Output rise and fall time                                       | $C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$  |     | 5                  | ns   |
|   |  |   | $C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$ |     | TBD                |      |
| -                                       | $t_{\text{EXTI}pw}$  | Pulse width of external signals detected by the EXTI controller |  | 8   |                    | ns   |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32L15xxx reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design. Not tested in production.
3. The maximum frequency is defined in [Figure 15](#).

Figure 15. I/O AC characteristics definition



### 6.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology.

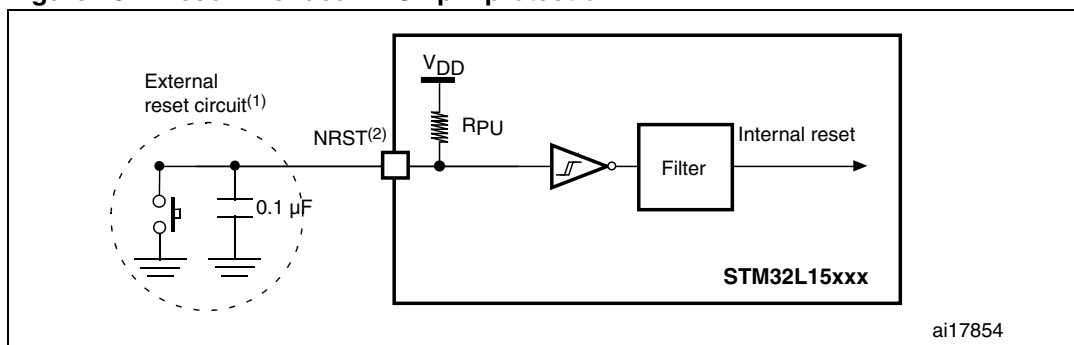
Unless otherwise specified, the parameters given in [Table 42](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 11](#).

Table 42. NRST pin characteristics

| Symbol                | Parameter                                       | Conditions   | Min                | Typ | Max      | Unit       |
|-----------------------|---|--|--------------------|-----|----------|------------|
| $V_{IL(NRST)}^{(1)}$  | NRST input low level voltage                    |  | $V_{SS}$           |     | 0.8      | V          |
| $V_{IH(NRST)}^{(1)}$  | NRST input high level voltage                   |  | 1.4                |     | $V_{DD}$ |            |
| $V_{OL(NRST)}^{(1)}$  | NRST output low level voltage                   | $I_{OL} = 2 \text{ mA}$<br>$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$    |                    |     | 0.4      |            |
|                       |   | $I_{OL} = 1.5 \text{ mA}$<br>$1.65 \text{ V} < V_{DD} < 2.7 \text{ V}$ |                    |     |          |            |
| $V_{hys(NRST)}^{(1)}$ | NRST Schmitt trigger voltage hysteresis         |  | $10\%V_{DD}^{(2)}$ |     |          | mV         |
| $R_{PU}$              | Weak pull-up equivalent resistor <sup>(3)</sup> | $V_{IN} = V_{SS}$  | 30                 | 45  | 60       | k $\Omega$ |
| $V_{F(NRST)}^{(1)}$   | NRST input filtered pulse                       |  |                    |     | 50       | ns         |
| $V_{NF(NRST)}^{(1)}$  | NRST input not filtered pulse                   |  | 350                |     |          | ns         |

1. Guaranteed by design, not tested in production.
2. 200 mV minimum value
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Figure 16. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 42](#). Otherwise the reset will not be taken into account by the device.

### 6.3.14 TIM timer characteristics

The parameters given in the following table are guaranteed by design.

Refer to [Section 6.3.11: I/O current injection characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 43. TIMx<sup>(1)</sup> characteristics

| Symbol           | Parameter  | Conditions                     | Min    | Max                  | Unit          |
|------------------|--|--------------------------------|--------|----------------------|---------------|
| $t_{res(TIM)}$   | Timer resolution time  |                                | 1      |                      | $t_{TIMxCLK}$ |
|                  |  | $f_{TIMxCLK} = 32 \text{ MHz}$ | 31.25  |                      | ns            |
| $f_{EXT}$        | Timer external clock frequency on CH1 to CH4   |                                | 0      | $f_{TIMxCLK}/2$      | MHz           |
|                  |  | $f_{TIMxCLK} = 32 \text{ MHz}$ | 0      | 16                   | MHz           |
| $Res_{TIM}$      | Timer resolution   |                                |        | 16                   | bit           |
| $t_{COUNTER}$    | 16-bit counter clock period when internal clock is selected (timer's prescaler disabled) |                                | 1      | 65536                | $t_{TIMxCLK}$ |
|                  |  | $f_{TIMxCLK} = 32 \text{ MHz}$ | 0.0312 | 2048                 | $\mu\text{s}$ |
| $t_{MAX\_COUNT}$ | Maximum possible count   |                                |        | $65536 \times 65536$ | $t_{TIMxCLK}$ |
|                  |  | $f_{TIMxCLK} = 32 \text{ MHz}$ |        | 134.2                | s             |

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

### 6.3.15 Communications interfaces

#### I<sup>2</sup>C interface characteristics

Unless otherwise specified, the parameters given in [Table 44](#) are derived from tests performed under ambient temperature,  $f_{PCLK1}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 11](#).

The product line I<sup>2</sup>C interface meets the requirements of the standard I<sup>2</sup>C communication protocol with the following restrictions: SDA and SCL are not “true” open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and  $V_{DD}$  is disabled, but is still present.

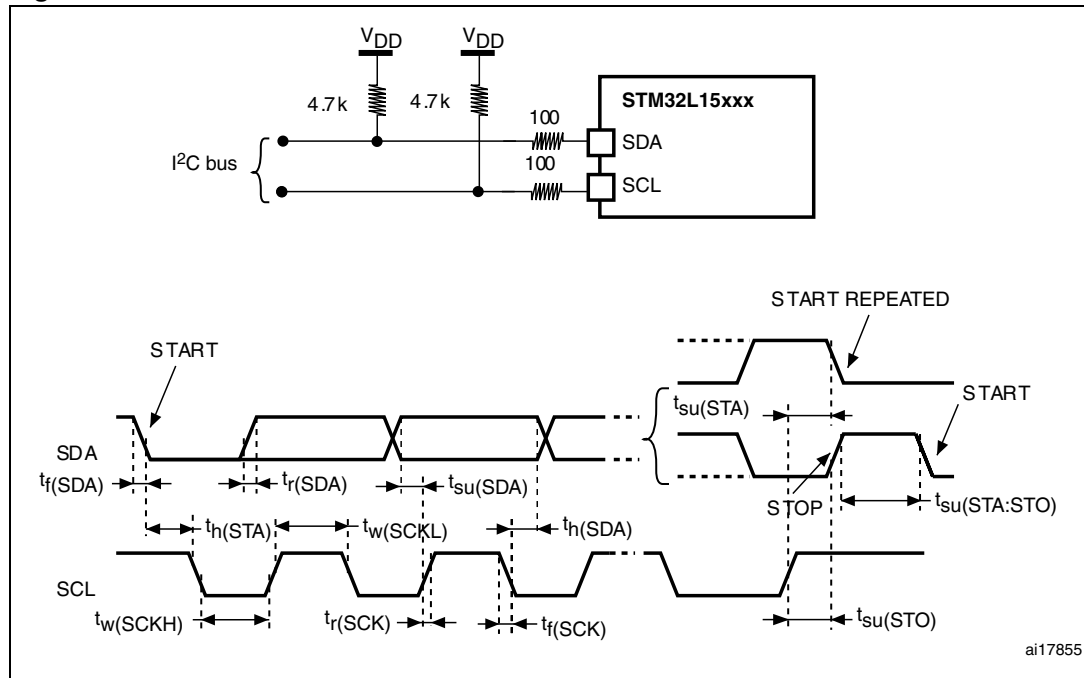
The I<sup>2</sup>C characteristics are described in [Table 44](#). Refer also to [Section 6.3.11: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 44. I<sup>2</sup>C characteristics**

| Symbol                   | Parameter                               | Standard mode I <sup>2</sup> C <sup>(1)</sup> |      | Fast mode I <sup>2</sup> C <sup>(1)(2)</sup> |                    | Unit    |
|--------------------------|---|---|------|--|--------------------|---------|
|                          |   | Min   | Max  | Min  | Max                |         |
| $t_{w(SCLL)}$            | SCL clock low time                      | 4.7   |      | 1.3  |                    | $\mu$ s |
| $t_{w(SCLH)}$            | SCL clock high time                     | 4.0   |      | 0.6  |                    |         |
| $t_{su(SDA)}$            | SDA setup time                          | 250   |      | 100  |                    | ns      |
| $t_h(SDA)$               | SDA data hold time                      | 0 <sup>(3)</sup>                              |      | 0 <sup>(4)</sup>                             | 900 <sup>(3)</sup> |         |
| $t_r(SDA)$<br>$t_r(SCL)$ | SDA and SCL rise time                   |   | 1000 | $20 + 0.1C_b$                                | 300                |         |
| $t_f(SDA)$<br>$t_f(SCL)$ | SDA and SCL fall time                   |   | 300  |  | 300                |         |
| $t_h(STA)$               | Start condition hold time               | 4.0   |      | 0.6  |                    | $\mu$ s |
| $t_{su(STA)}$            | Repeated Start condition setup time     | 4.7   |      | 0.6  |                    |         |
| $t_{su(STO)}$            | Stop condition setup time               | 4.0   |      | 0.6  |                    | $\mu$ s |
| $t_w(STO:STA)$           | Stop to Start condition time (bus free) | 4.7   |      | 1.3  |                    | $\mu$ s |
| $C_b$                    | Capacitive load for each bus line       |   | 400  |  | 400                | pF      |

1. Guaranteed by design, not tested in production.
2.  $f_{PCLK1}$  must be higher than 2 MHz to achieve standard mode I<sup>2</sup>C frequencies. It must be higher than 4 MHz to achieve fast mode I<sup>2</sup>C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I<sup>2</sup>C fast mode clock.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 17. I<sup>2</sup>C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: 0.3V<sub>DD</sub> and 0.7V<sub>DD</sub>.

Table 45. SCL frequency (f<sub>PCLK1</sub>= 32 MHz, V<sub>DD</sub> = 3.3 V)<sup>(1)(2)</sup>

| f <sub>SCL</sub> (kHz) | I2C_CCR value           |
|------------------------|-------------------------|
|                        | R <sub>P</sub> = 4.7 kΩ |
| 400                    | 0x801B                  |
| 300                    | 0x8024                  |
| 200                    | 0x8035                  |
| 100                    | 0x00A0                  |
| 50                     | 0x0140                  |
| 20                     | 0x0320                  |

1. R<sub>P</sub> = External pull-up resistance, f<sub>SCL</sub> = I<sup>2</sup>C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

**SPI characteristics**

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 11](#).

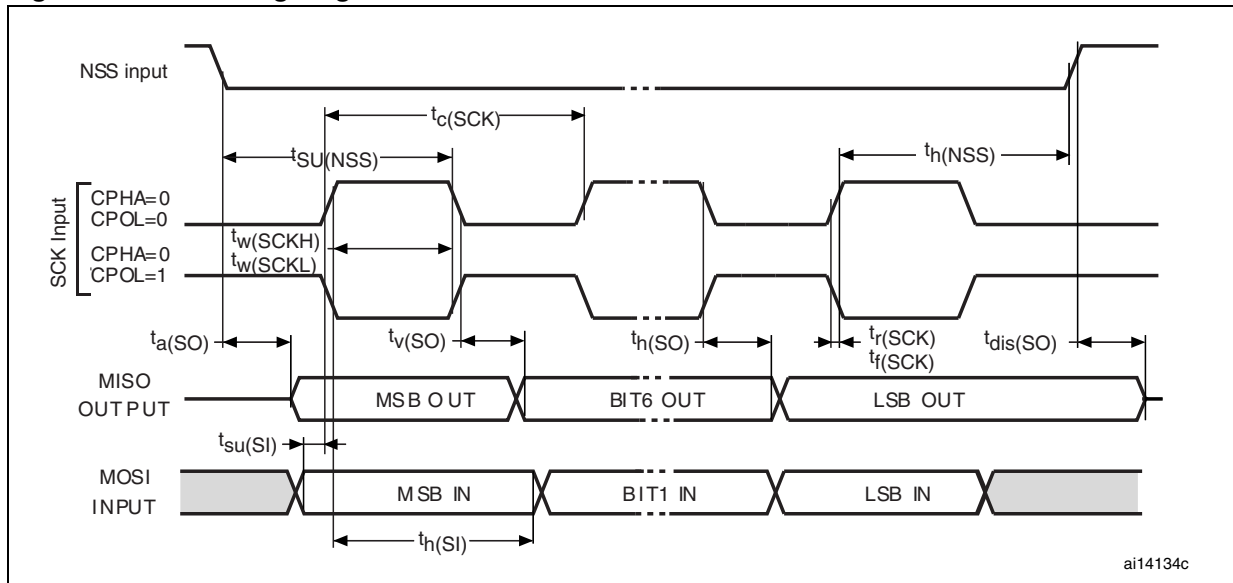
Refer to [Section 6.3.11: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 46. SPI characteristics<sup>(1)</sup>**

| Symbol                                 | Parameter                        | Conditions                                  | Min         | Max <sup>(2)</sup> | Unit |
|--|----------------------------------|---|-------------|--------------------|------|
| $f_{SCK}$<br>$1/t_{c(SCK)}$            | SPI clock frequency              | Master mode                                 |             | 16                 | MHz  |
|  |                                  | Slave mode                                  |             | 16                 |      |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$           | SPI clock rise and fall time     | Capacitive load: C = 30 pF                  |             | TBD                | ns   |
| DuCy(SCK)                              | SPI slave input clock duty cycle | Slave mode                                  | 30          | 70                 | %    |
| $t_{su(NSS)}$                          | NSS setup time                   | Slave mode                                  | $4t_{PCLK}$ |                    | ns   |
| $t_{h(NSS)}$                           | NSS hold time                    | Slave mode                                  | $2t_{PCLK}$ |                    |      |
| $t_{w(SCKH)}$<br>$t_{w(SCKL)}$         | SCK high and low time            | Master mode, $f_{PCLK} = 16$ MHz, presc = 4 | TBD         | TBD                |      |
| $t_{su(MI)}$<br>$t_{su(SI)}$           | Data input setup time            | Master mode                                 | 5           |                    |      |
|  |                                  | Slave mode                                  | 5           |                    |      |
| $t_{h(MI)}$<br>$t_{h(SI)}$             | Data input hold time             | Master mode                                 | 5           |                    |      |
|  |                                  | Slave mode                                  | 4           |                    |      |
| $t_{a(SO)}^{(3)}$                      | Data output access time          | Slave mode, $f_{PCLK} = 20$ MHz             | 0           | $3t_{PCLK}$        |      |
| $t_{dis(SO)}^{(4)}$                    | Data output disable time         | Slave mode                                  | TBD         | TBD                |      |
| $t_{v(SO)}^{(2)}$                      | Data output valid time           | Slave mode (after enable edge)              |             | TBD                |      |
| $t_{v(MO)}^{(2)}$                      | Data output valid time           | Master mode (after enable edge)             |             | TBD                |      |
| $t_{h(SO)}^{(2)}$<br>$t_{h(MO)}^{(2)}$ | Data output hold time            | Slave mode (after enable edge)              | TBD         |                    |      |
|  |                                  | Master mode (after enable edge)             | TBD         |                    |      |

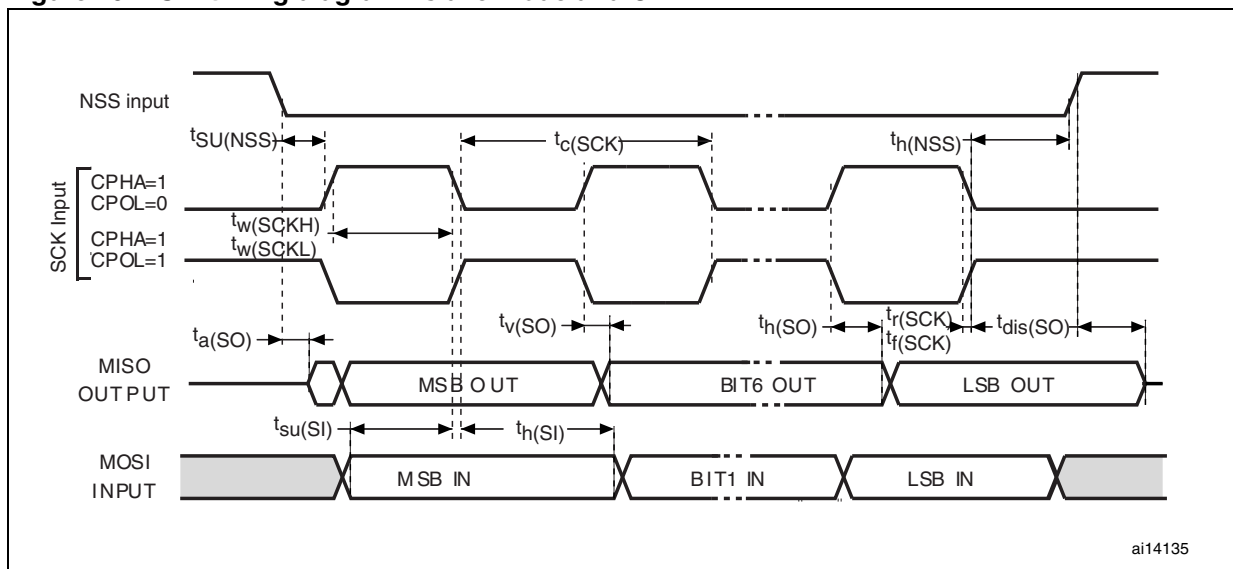
1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

Figure 18. SPI timing diagram - slave mode and CPHA = 0



ai14134c

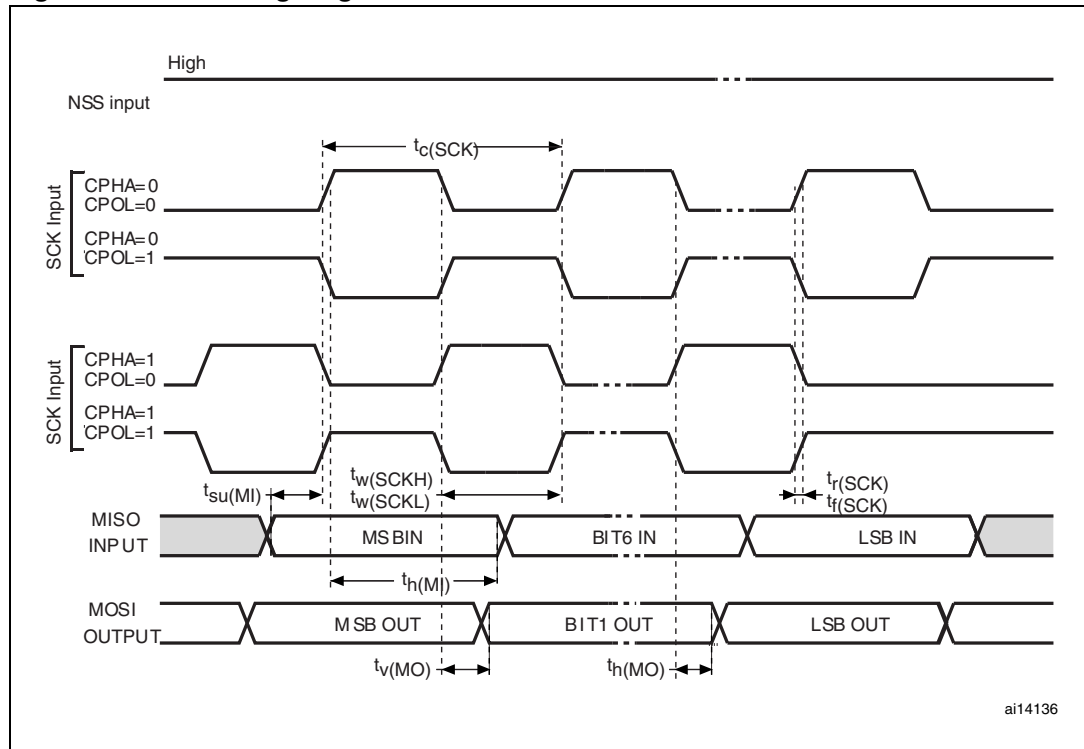
Figure 19. SPI timing diagram - slave mode and CPHA = 1<sup>(1)</sup>



ai14135

1. Measurement points are done at CMOS levels: 0.3V<sub>DD</sub> and 0.7V<sub>DD</sub>.

Figure 20. SPI timing diagram - master mode<sup>(1)</sup>



1. Measurement points are done at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

### USB characteristics

The USB interface is USB-IF certified (full speed).

Table 47. USB startup time

| Symbol              | Parameter                    | Max | Unit    |
|---------------------|------------------------------|-----|---------|
| $t_{STARTUP}^{(1)}$ | USB transceiver startup time | 1   | $\mu s$ |

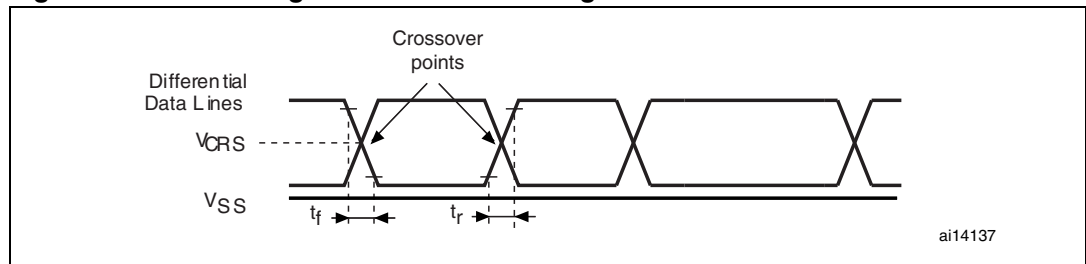
1. Guaranteed by design, not tested in production.

**Table 48. USB DC electrical characteristics**

| Symbol                         | Parameter                       | Conditions  | Min. <sup>(1)</sup> | Max. <sup>(1)</sup> | Unit |
|--------------------------------|---------------------------------|---|---------------------|---------------------|------|
| <b>Input levels</b>            |                                 |   |                     |                     |      |
| V <sub>DD</sub>                | USB operating voltage           |   | 3.0                 | 3.6                 | V    |
| V <sub>DI</sub> <sup>(2)</sup> | Differential input sensitivity  | I(USBDP, USBDM)   | 0.2                 |                     | V    |
| V <sub>CM</sub> <sup>(2)</sup> | Differential common mode range  | Includes V <sub>DI</sub> range                            | 0.8                 | 2.5                 |      |
| V <sub>SE</sub> <sup>(2)</sup> | Single ended receiver threshold |   | 1.3                 | 2.0                 |      |
| <b>Output levels</b>           |                                 |   |                     |                     |      |
| V <sub>OL</sub> <sup>(3)</sup> | Static output level low         | R <sub>L</sub> of 1.5 kΩ to 3.6 V <sup>(4)</sup>          |                     | 0.3                 | V    |
| V <sub>OH</sub> <sup>(3)</sup> | Static output level high        | R <sub>L</sub> of 15 kΩ to V <sub>SS</sub> <sup>(4)</sup> | 2.8                 | 3.6                 |      |

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization, not tested in production.
3. Tested in production.
4. R<sub>L</sub> is the load connected on the USB drivers.

**Figure 21. USB timings: definition of data signal rise and fall time**



**Table 49. USB: full speed electrical characteristics**

| Driver characteristics <sup>(1)</sup> |                                 |                                |     |     |      |
|---------------------------------------|---------------------------------|--------------------------------|-----|-----|------|
| Symbol                                | Parameter                       | Conditions                     | Min | Max | Unit |
| t <sub>r</sub>                        | Rise time <sup>(2)</sup>        | C <sub>L</sub> = 50 pF         | 4   | 20  | ns   |
| t <sub>f</sub>                        | Fall Time <sup>(2)</sup>        | C <sub>L</sub> = 50 pF         | 4   | 20  | ns   |
| t <sub>rfm</sub>                      | Rise/ fall time matching        | t <sub>r</sub> /t <sub>f</sub> | 90  | 110 | %    |
| V <sub>CRS</sub>                      | Output signal crossover voltage |                                | 1.3 | 2.0 | V    |

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 51](#) are guaranteed by design.

Table 50. ADC clock frequency

| Symbol           | Parameter           | Conditions          |                                      | Min   | Max   | Unit |     |
|------------------|---------------------|---------------------|--------------------------------------|---|-------|------|-----|
| f <sub>ADC</sub> | ADC clock frequency | Voltage range 1 & 2 | 2.4 V ≤ V <sub>DDA</sub> ≤ 3.6 V     | V <sub>REF+</sub> = V <sub>DDA</sub>                              | 0.480 | 16   | MHz |
|                  |                     |                     |                                      | V <sub>REF+</sub> < V <sub>DDA</sub><br>V <sub>REF+</sub> > 2.4 V |       | 8    |     |
|                  |                     |                     | 1.8 V ≤ V <sub>DDA</sub> ≤ 2.4 V     | V <sub>REF+</sub> < V <sub>DDA</sub><br>V <sub>REF+</sub> ≥ 2.4 V |       | 4    |     |
|                  |                     |                     |                                      | V <sub>REF+</sub> = V <sub>DDA</sub>                              |       | 8    |     |
|                  |                     | Voltage range 3     | V <sub>REF+</sub> < V <sub>DDA</sub> | 4   |       |      |     |
|                  |                     |                     |                                      | 4   |       |      |     |

Table 51. ADC characteristics

| Symbol                           | Parameter                                 | Conditions   | Min                | Typ              | Max               | Unit |
|----------------------------------|---|--|--------------------|------------------|-------------------|------|
| V <sub>DDA</sub>                 | Power supply                              |  | 1.8                |                  | 3.6               | V    |
| V <sub>REF+</sub>                | Positive reference voltage                | 2.4 V ≤ V <sub>DDA</sub> ≤ 3.6 V<br>V <sub>REF+</sub> must be below or equal to V <sub>DDA</sub> | 1.8 <sup>(1)</sup> |                  | V <sub>DDA</sub>  |      |
| V <sub>REF-</sub>                | Negative reference voltage                |  |                    | V <sub>SSA</sub> |                   |      |
| I <sub>VDDA</sub>                | Current on the V <sub>DDA</sub> input pin |  |                    | 1000             | 1450              | μA   |
| I <sub>VREF</sub> <sup>(2)</sup> | Current on the V <sub>REF</sub> input pin | Peak   |                    | 400              | 700               |      |
|                                  |   | Average  |                    |                  | 450               |      |
| V <sub>AIN</sub>                 | Conversion voltage range <sup>(3)</sup>   |  | 0 <sup>(4)</sup>   |                  | V <sub>REF+</sub> | V    |
| f <sub>S</sub>                   | 12-bit sampling rate                      | Direct channels  | 0.03               |                  | 1                 | Msps |
|                                  |   | Multiplexed channels   | 0.03               |                  | 0.76              |      |
|                                  | 10-bit sampling rate                      | Direct channels  | 0.03               |                  | 1.07              | Msps |
|                                  |   | Multiplexed channels   | 0.03               |                  | 0.8               |      |
|                                  | 8-bit sampling rate                       | Direct channels  | 0.03               |                  | 1.23              | Msps |
|                                  |   | Multiplexed channels   | 0.03               |                  | 0.89              |      |
|                                  | 6-bit sampling rate                       | Direct channels  | 0.03               |                  | 1.54              | Msps |
|                                  |   | Multiplexed channels   | 0.03               |                  | 1                 |      |

**Table 51. ADC characteristics (continued)**

| Symbol                          | Parameter  | Conditions   | Min   | Typ | Max                  | Unit               |
|---------------------------------|--|--|---|-----|----------------------|--------------------|
| t <sub>S</sub>                  | Sampling time                                      | Direct channels<br>2.4 V ≤ V <sub>DDA</sub> ≤ 3.6 V      | 0.25 <sup>(5)</sup>                                       |     |                      | μs                 |
|                                 |  | Multiplexed channels<br>2.4 V ≤ V <sub>DDA</sub> ≤ 3.6 V | 0.56 <sup>(5)</sup>                                       |     |                      |                    |
|                                 |  | Direct channels<br>1.8 V ≤ V <sub>DDA</sub> ≤ 2.4 V      | 0.56 <sup>(5)</sup>                                       |     |                      |                    |
|                                 |  | Multiplexed channels<br>1.8 V ≤ V <sub>DDA</sub> ≤ 2.4 V | 1 <sup>(5)</sup>  |     |                      |                    |
|                                 |  |  |   | 4   |                      | 384                |
| t <sub>CONV</sub>               | Total conversion time<br>(including sampling time) | f <sub>ADC</sub> = 16 MHz                                | 1   |     | 24.75                | μs                 |
|                                 |  |  | 4 to 384 (sampling phase) + 12 (successive approximation) |     |                      | 1/f <sub>ADC</sub> |
| C <sub>ADC</sub>                | Internal sample and hold capacitor                 | Direct channels  |   | 16  |                      | pF                 |
|                                 |  | Multiplexed channels                                     |   |     |                      |                    |
| f <sub>TRIG</sub>               | External trigger frequency<br>Regular sequencer    | 12-bit conversions                                       |   |     | T <sub>conv</sub> +1 | 1/f <sub>ADC</sub> |
|                                 |  | 6/8/10-bit conversions                                   |   |     | T <sub>conv</sub>    | 1/f <sub>ADC</sub> |
| f <sub>TRIG</sub>               | External trigger frequency<br>Injected sequencer   | 12-bit conversions                                       |   |     | T <sub>conv</sub> +2 | 1/f <sub>ADC</sub> |
|                                 |  | 6/8/10-bit conversions                                   |   |     | T <sub>conv</sub> +1 | 1/f <sub>ADC</sub> |
| R <sub>AIN</sub> <sup>(6)</sup> | External input impedance                           |  |   |     | 50                   | kΩ                 |
|                                 |  |  |   |     | 0.5                  |                    |
| t <sub>lat</sub>                | Injection trigger conversion latency               | f <sub>ADC</sub> = 16 MHz                                | 219   |     | 281                  | ns                 |
|                                 |  |  | 3.5   |     | 4.5                  | 1/f <sub>ADC</sub> |
| t <sub>latr</sub>               | Regular trigger conversion latency                 | f <sub>ADC</sub> = 16 MHz                                | 156   |     | 219                  | ns                 |
|                                 |  |  | 2.5   |     | 3.5                  | 1/f <sub>ADC</sub> |
| t <sub>STAB</sub>               | Power-up time                                      |  |   |     | 3.5                  | μs                 |

- The Vref+ input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
- The current consumption through VREF is composed of two parameters:
  - one constant (max 300 μA)
  - one variable (max 400 μA), only during sampling time + 2 first conversion pulses.
 So, peak consumption is 300+400 = 700 μA and average consumption is 300 + [(4 sampling + 2) / 16] x 400 = 450 μA at 1Msps
- V<sub>REF+</sub> can be internally connected to V<sub>DDA</sub> and V<sub>REF-</sub> can be internally connected to V<sub>SSA</sub>, depending on the package. Refer to [Section 4: Pin descriptions](#) for further details.
- V<sub>SSA</sub> or V<sub>REF-</sub> must be tied to ground.
- Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ
- For 1 Msps, maximum Rext is 0.5 kΩ

Table 52. ADC accuracy<sup>(1)(2)</sup>

| Symbol | Parameter                            | Test conditions   | Min <sup>(3)</sup> | Typ | Max <sup>(3)</sup> | Unit |
|--------|--------------------------------------|---|--------------------|-----|--------------------|------|
| ET     | Total unadjusted error               | $2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$<br>$2.4\text{ V} \leq V_{REF+} \leq 3.6\text{ V}$<br>$f_{ADC} = 8\text{ MHz}$ , $R_{AIN} = 50\ \Omega$<br>$T_A = -40\text{ to }105\text{ }^\circ\text{C}$ | -                  | 2   | 4                  | LSB  |
| EO     | Offset error                         |   | -                  | 1   | 2                  |      |
| EG     | Gain error                           |   | -                  | 1.5 | 3.5                |      |
| ED     | Differential linearity error         |   | -                  | 1   | 2                  |      |
| EL     | Integral linearity error             |   | -                  | 1.7 | 3                  |      |
| ENOB   | Effective number of bits             | $2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$   | 9.2                | 10  | -                  | bits |
| SINAD  | Signal-to-noise and distortion ratio | $V_{DDA} = V_{REF+}$<br>$f_{ADC} = 16\text{ MHz}$ , $R_{AIN} = 50\ \Omega$<br>$T_A = -40\text{ to }105\text{ }^\circ\text{C}$<br>$1\text{ kHz} \leq F_{input} \leq 100\text{ kHz}$                      | 57.5               | 62  | -                  | dB   |
| SNR    | Signal-to-noise ratio                |   | 57.5               | 62  | -                  |      |
| THD    | Total harmonic distortion            |   | -74                | -75 | -                  |      |
| ET     | Total unadjusted error               |   | -                  | 4   | 6.5                |      |
| EO     | Offset error                         | $2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$<br>$1.8\text{ V} \leq V_{REF+} \leq 2.4\text{ V}$<br>$f_{ADC} = 4\text{ MHz}$ , $R_{AIN} = 50\ \Omega$<br>$T_A = -40\text{ to }105\text{ }^\circ\text{C}$ | -                  | 2   | 4                  | LSB  |
| EG     | Gain error                           |   | -                  | 4   | 6                  |      |
| ED     | Differential linearity error         |   | -                  | 1   | 2                  |      |
| EL     | Integral linearity error             |   | -                  | 1.5 | 3                  |      |
| ET     | Total unadjusted error               |   | -                  | 2   | 3                  |      |
| EO     | Offset error                         | $1.8\text{ V} \leq V_{DDA} \leq 2.4\text{ V}$<br>$1.8\text{ V} \leq V_{REF+} \leq 2.4\text{ V}$<br>$f_{ADC} = 4\text{ MHz}$ , $R_{AIN} = 50\ \Omega$<br>$T_A = -40\text{ to }105\text{ }^\circ\text{C}$ | -                  | 1   | 1.5                | LSB  |
| EG     | Gain error                           |   | -                  | 1.5 | 2                  |      |
| ED     | Differential linearity error         |   | -                  | 1   | 2                  |      |
| EL     | Integral linearity error             |   | -                  | 1   | 1.5                |      |
| ET     | Total unadjusted error               |   | -                  | 2   | 3                  |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative injection current: injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 6.3.11](#) does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

Figure 22. ADC accuracy characteristics

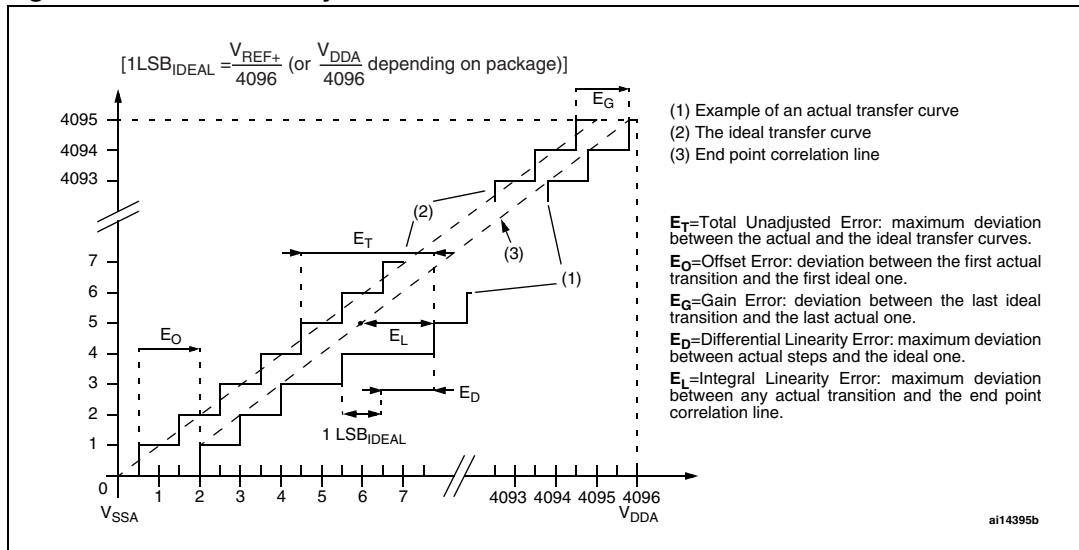
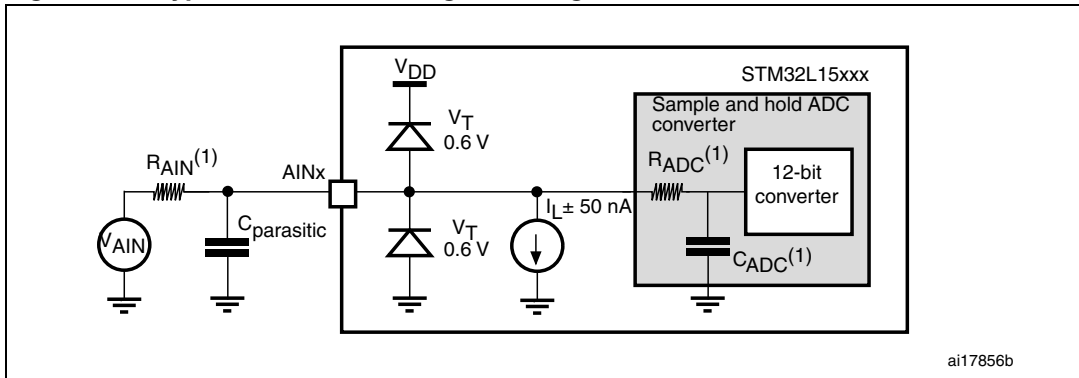
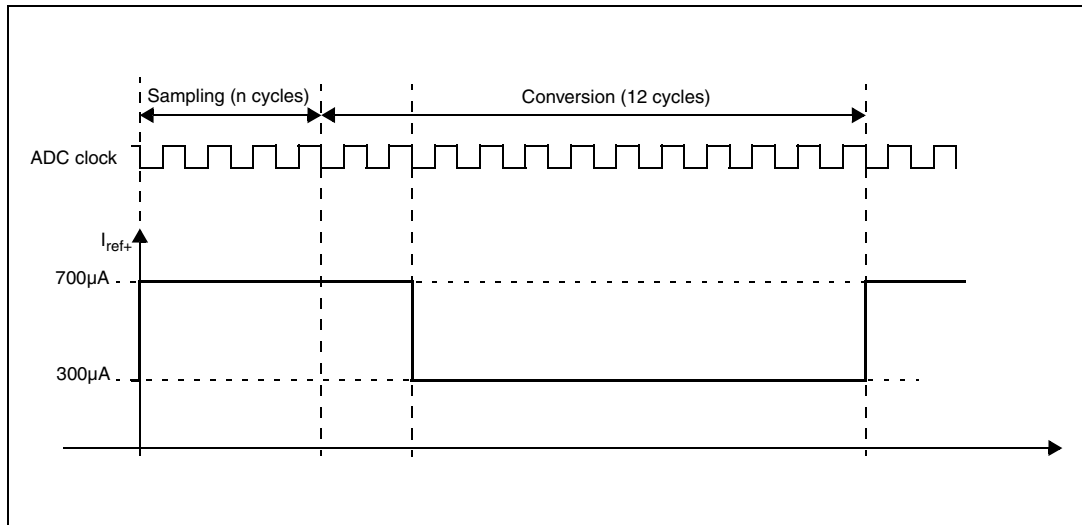


Figure 23. Typical connection diagram using the ADC



1. Refer to [Table 51](#) for the values of  $R_{AIN}$ ,  $R_{ADC}$  and  $C_{ADC}$ .
2.  $C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{parasitic}$  value will downgrade conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced.

**Figure 24. Maximum dynamic current consumption on V<sub>REF+</sub> supply pin during ADC conversion**



**Table 53. R<sub>AIN</sub> max for f<sub>ADC</sub> = 16 MHz<sup>(1)</sup>**

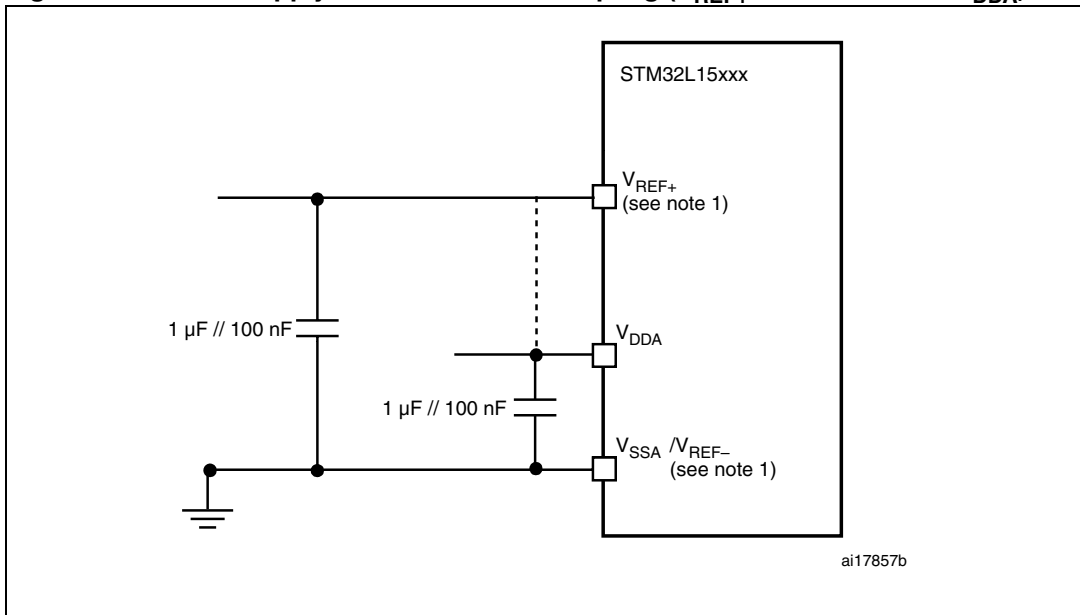
| Ts (cycles) | Ts (µs) | R <sub>AIN</sub> max (kΩ)        |                                  |                                  |                                  |
|-------------|---------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
|             |         | Multiplexed channels             |                                  | Direct channels                  |                                  |
|             |         | 2.4 V < V <sub>DDA</sub> < 3.6 V | 1.8 V < V <sub>DDA</sub> < 2.4 V | 2.4 V < V <sub>DDA</sub> < 3.3 V | 1.8 V < V <sub>DDA</sub> < 2.4 V |
| 4           | 0.25    | Not allowed                      | Not allowed                      | 0.7                              | Not allowed                      |
| 9           | 0.5625  | 0.8                              | Not allowed                      | 2.0                              | 1.0                              |
| 16          | 1       | 2.0                              | 0.8                              | 4.0                              | 3.0                              |
| 24          | 1.5     | 3.0                              | 1.8                              | 6.0                              | 4.5                              |
| 48          | 3       | 6.8                              | 4.0                              | 15.0                             | 10.0                             |
| 96          | 6       | 15.0                             | 10.0                             | 30.0                             | 20.0                             |
| 192         | 12      | 32.0                             | 25.0                             | 50.0                             | 40.0                             |
| 384         | 24      | 50.0                             | 50.0                             | 50.0                             | 50.0                             |

1. Guaranteed by design, not tested in production.

**General PCB design guidelines**

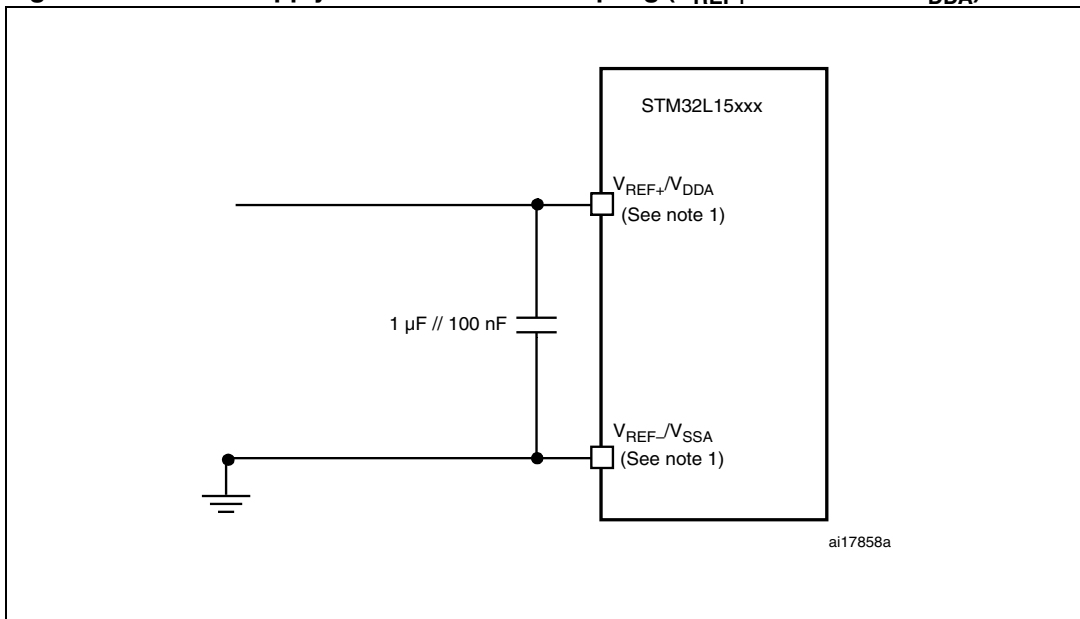
Power supply decoupling should be performed as shown in [Figure 25](#) or [Figure 26](#), depending on whether V<sub>REF+</sub> is connected to V<sub>DDA</sub> or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

**Figure 25. Power supply and reference decoupling ( $V_{REF+}$  not connected to  $V_{DDA}$ )**



1.  $V_{REF+}$  and  $V_{REF-}$  inputs are available only on 100-pin packages.

**Figure 26. Power supply and reference decoupling ( $V_{REF+}$  connected to  $V_{DDA}$ )**



1.  $V_{REF+}$  and  $V_{REF-}$  inputs are available only on 100-pin packages.

### 6.3.17 DAC electrical specifications

Data guaranteed by design, not tested in production, unless otherwise specified.

**Table 54. DAC characteristics**

| Symbol                 | Parameter   | Conditions  | Min       | Typ       | Max                      | Unit             |
|------------------------|---|---|-----------|-----------|--------------------------|------------------|
| $V_{DDA}$              | Analog supply voltage   |   | 1.8       |           | 3.6                      | V                |
| $V_{REF+}$             | Reference supply voltage  | $V_{REF+}$ must always be below $V_{DDA}$                                     | 1.8       |           | 3.6                      |                  |
| $V_{REF-}$             | Lower reference voltage   |   | $V_{SSA}$ |           |                          |                  |
| $I_{DDVREF+}^{(1)}$    | Current consumption on $V_{REF+}$ supply<br>$V_{REF+} = 3.3\text{ V}$ | No load, middle code (0x800)  |           | 130       | 220                      | $\mu\text{A}$    |
|                        |   | No load, worst code (0x000)   |           | 220       | 350                      |                  |
| $I_{DDA}^{(1)}$        | Current consumption on $V_{DDA}$ supply<br>$V_{DDA} = 3.3\text{ V}$   | No load, middle code (0x800)  |           | 210       | 320                      |                  |
|                        |   | No load, worst code (0xF1C)   |           | 320       | 520                      |                  |
| $R_L^{(2)}$            | Resistive load  | DAC output buffer ON  | 5         |           |                          | $\text{k}\Omega$ |
| $C_L^{(2)}$            | Capacitive load   |   |           |           | 50                       | $\text{pF}$      |
| $R_O$                  | Output impedance  | DAC output buffer OFF   | 6         | 8         | 10                       | $\text{k}\Omega$ |
| $V_{DAC\_OUT}$         | Voltage on DAC_OUT output   | DAC output buffer ON  | 0.2       |           | $V_{DDA} - 0.2$          | V                |
|                        |   | DAC output buffer OFF   | 0.5       |           | $V_{REF+} - 1\text{LSB}$ | mV               |
| $\text{DNL}^{(1)}$     | Differential non linearity <sup>(3)</sup>                             | $C_L \leq 50\text{ pF}$ , $R_L \geq 5\text{ k}\Omega$<br>DAC output buffer ON |           | 1.5       | 3                        | LSB              |
|                        |   | No $R_{LOAD}$ , $C_L \leq 50\text{ pF}$<br>DAC output buffer OFF              |           | 1.5       | 3                        |                  |
| $\text{INL}^{(1)}$     | Integral non linearity <sup>(4)</sup>                                 | $C_L \leq 50\text{ pF}$ , $R_L \geq 5\text{ k}\Omega$<br>DAC output buffer ON |           | 2         | 4                        |                  |
|                        |   | No $R_{LOAD}$ , $C_L \leq 50\text{ pF}$<br>DAC output buffer OFF              |           | 2         | 4                        |                  |
| Offset <sup>(1)</sup>  | Offset error at code 0x800 <sup>(5)</sup>                             | $C_L \leq 50\text{ pF}$ , $R_L \geq 5\text{ k}\Omega$<br>DAC output buffer ON |           | $\pm 10$  | $\pm 25$                 |                  |
|                        |   | No $R_{LOAD}$ , $C_L \leq 50\text{ pF}$<br>DAC output buffer OFF              |           | $\pm 5$   | $\pm 8$                  |                  |
| Offset1 <sup>(1)</sup> | Offset error at code 0x001 <sup>(6)</sup>                             | No $R_{LOAD}$ , $C_L \leq 50\text{ pF}$<br>DAC output buffer OFF              |           | $\pm 1.5$ | $\pm 5$                  |                  |

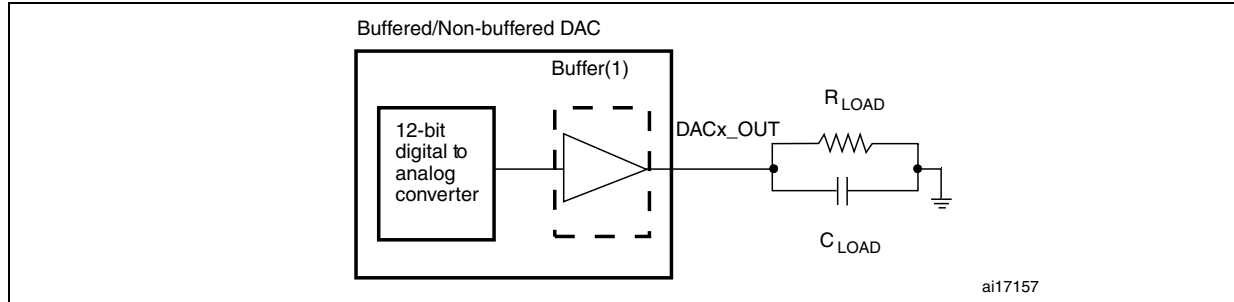
Table 54. DAC characteristics (continued)

| Symbol                    | Parameter  | Conditions  | Min | Typ          | Max          | Unit  |
|---------------------------|--|---|-----|--------------|--------------|-------|
| dOffset/dT <sup>(1)</sup> | Offset error temperature coefficient (code 0x800)  | V <sub>DDA</sub> = 3.3V<br>V <sub>REF+</sub> = 3.0V<br>T <sub>A</sub> = 0 to 50 °C<br>DAC output buffer OFF | -20 | -10          | 0            | μV/°C |
|                           |  | V <sub>DDA</sub> = 3.3V<br>V <sub>REF+</sub> = 3.0V<br>T <sub>A</sub> = 0 to 50 °C<br>DAC output buffer ON  | 0   | 20           | 50           |       |
| Gain <sup>(1)</sup>       | Gain error <sup>(7)</sup>  | C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ<br>DAC output buffer ON                                       |     | +0.1 / -0.2% | +0.2 / -0.5% | %     |
|                           |  | No R <sub>LOAD</sub> , C <sub>L</sub> ≤ 50 pF<br>DAC output buffer OFF                                      |     | +0 / -0.2%   | +0 / -0.4%   |       |
| dGain/dT <sup>(1)</sup>   | Gain error temperature coefficient   | V <sub>DDA</sub> = 3.3V<br>V <sub>REF+</sub> = 3.0V<br>T <sub>A</sub> = 0 to 50 °C<br>DAC output buffer OFF | -10 | -2           | 0            | μV/°C |
|                           |  | V <sub>DDA</sub> = 3.3V<br>V <sub>REF+</sub> = 3.0V<br>T <sub>A</sub> = 0 to 50 °C<br>DAC output buffer ON  | -40 | -8           | 0            |       |
| TUE <sup>(1)</sup>        | Total unadjusted error   | C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ<br>DAC output buffer ON                                       |     | 12           | 30           | LSB   |
|                           |  | No R <sub>LOAD</sub> , C <sub>L</sub> ≤ 50 pF<br>DAC output buffer OFF                                      |     | 8            | 12           |       |
| t <sub>SETTLING</sub>     | Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB) | C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ   |     | 7            | 12           | μs    |
| Update rate               | Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code   | C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ   |     |              | 1            | MSPS  |
| t <sub>WAKEUP</sub>       | Wakeup time from off state (setting the ENx bit in the DAC Control register) <sup>(8)</sup>  | C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ   |     | 9            | 15           | μs    |
| PSRR+                     | V <sub>DDA</sub> supply rejection ratio (static DC measurement)  | C <sub>L</sub> ≤ 50 pF, R <sub>L</sub> ≥ 5 kΩ   |     | -60          | -35          | dB    |

1. Data based on characterization results.
2. Connected between DAC\_OUT and V<sub>SSA</sub>.
3. Difference between two consecutive codes - 1 LSB.
4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.

5. Difference between the value measured at Code (0x800) and the ideal value =  $V_{REF+}/2$ .
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFFF when buffer is OFF, and from code giving 0.2 V and  $(V_{DDA} - 0.2)$  V when buffer is ON.
8. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 27. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

### 6.3.18 Operational amplifier characteristics

Table 55. Operational amplifier characteristics

| Symbol                 | Parameter                    |                           | Condition <sup>(1)</sup> | Min <sup>(2)</sup> | Typ | Max <sup>(2)</sup> | Unit              |
|------------------------|------------------------------|---------------------------|--------------------------|--------------------|-----|--------------------|-------------------|
| CMIR                   | Common mode input range      |                           |                          | 0                  |     | $V_{DD}$           |                   |
| $V_{I\_OFFSET}$        | Input offset voltage         | Maximum calibration range |                          |                    |     | $\pm 15$           | mV                |
|                        |                              | After offset calibration  |                          |                    |     | $\pm 1.5$          |                   |
| $\Delta V_{I\_OFFSET}$ | Input offset voltage drift   | Normal mode               |                          |                    |     | $\pm 40$           | $\mu V/^{\circ}C$ |
|                        |                              | Low power mode            |                          |                    |     | $\pm 80$           |                   |
| $I_{IB}$               | Input current bias           | Dedicated input           | 75 °C                    |                    |     | 1                  | nA                |
|                        |                              | General purpose input     |                          |                    |     | 10                 |                   |
| $I_{LOAD}$             | Drive current                | Normal mode               |                          |                    |     | 500                | $\mu A$           |
|                        |                              | Low power mode            |                          |                    |     | 100                |                   |
| $I_{DD}$               | Consumption                  | Normal mode               | No load, quiescent mode  |                    | 100 | 220                | $\mu A$           |
|                        |                              | Low power mode            |                          |                    | 30  | 60                 |                   |
| CMRR                   | Common mode rejection ration | Normal mode               |                          |                    | -85 |                    | dB                |
|                        |                              | Low power mode            |                          |                    | -90 |                    |                   |
| PSRR                   | Power supply rejection ratio | Normal mode               | DC                       |                    | -85 |                    | dB                |
|                        |                              | Low power mode            |                          |                    | -90 |                    |                   |

**Table 55. Operational amplifier characteristics (continued)**

| Symbol               | Parameter   |                | Condition <sup>(1)</sup>  | Min <sup>(2)</sup> | Typ  | Max <sup>(2)</sup> | Unit |  |
|----------------------|---|----------------|---|--------------------|------|--------------------|------|--|
| GBW                  | Bandwidth   | Normal mode    | $V_{DD} > 2.4\text{ V}$   | 400                | 1000 | 3000               | kHz  |  |
|                      |   | Low power mode |   | 150                | 300  | 800                |      |  |
|                      |   | Normal mode    | $V_{DD} < 2.4\text{ V}$   | 200                | 500  | 2200               |      |  |
|                      |   | Low power mode |   | 70                 | 150  | 800                |      |  |
| SR                   | Slew rate   | Normal mode    | $V_{DD} > 2.4\text{ V}$<br>(between 0.1 V and $V_{DD} - 0.1\text{ V}$ ) |                    | 700  |                    | V/ms |  |
|                      |   | Low power mode | $V_{DD} > 2.4\text{ V}$   |                    | 100  |                    |      |  |
|                      |   | Normal mode    | $V_{DD} < 2.4\text{ V}$   |                    | 300  |                    |      |  |
|                      |   | Low power mode |   |                    | 50   |                    |      |  |
| AO                   | Open loop gain  | Normal mode    |   | 55                 | 100  |                    | dB   |  |
|                      |   | Low power mode |   | 65                 | 110  |                    |      |  |
| R <sub>LOAD</sub>    | Resistive load  | Normal mode    | $V_{DD} < 2.4\text{ V}$   | 4                  |      |                    | kΩ   |  |
|                      |   | Low power mode |   | 20                 |      |                    |      |  |
| C <sub>LOAD</sub>    | Capacitive load   |                |   |                    |      | 50                 | pF   |  |
| V <sub>OH</sub> SAT  | High saturation voltage   | Normal mode    | $I_{LOAD} = \text{max or}$<br>$R_{LOAD} = \text{min}$                   | $V_{DD} - 100$     |      |                    | mV   |  |
|                      |   | Low power mode |   | $V_{DD} - 50$      |      |                    |      |  |
| V <sub>OL</sub> SAT  | Low saturation voltage  | Normal mode    |   |                    |      | 100                |      |  |
|                      |   | low power mode |   |                    |      | 50                 |      |  |
| φ <sub>m</sub>       | Phase margin  |                |   |                    | 60   |                    | °    |  |
| GM                   | Gain margin   |                |   |                    | -12  |                    | dB   |  |
| t <sub>OFFTRIM</sub> | Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy |                |   |                    | 1    |                    | ms   |  |
| t <sub>WAKEUP</sub>  | Wakeup time   | Normal mode    | $C_{LOAD} \leq 50\text{ pf,}$<br>$R_{LOAD} \geq 4\text{ k}\Omega$       |                    | 10   |                    | μs   |  |
|                      |   | Low power mode | $C_{LOAD} \leq 50\text{ pf,}$<br>$R_{LOAD} \geq 20\text{ k}\Omega$      |                    | 30   |                    |      |  |

1. Operating conditions are limited to junction temperature (0 °C to 105 °C) when  $V_{DD}$  is below 2 V. Otherwise, the operating temperature range is 105 °C to -40 °C.
2. Data based on characterization results, not tested in production.

### 6.3.19 Temperature sensor characteristics

**Table 56. TS characteristics**

| Symbol                   | Parameter                                       | Min | Typ     | Max     | Unit            |
|--------------------------|---|-----|---------|---------|-----------------|
| $T_L^{(1)}$              | $V_{SENSE}$ linearity with temperature          |     | $\pm 1$ | $\pm 2$ | $^{\circ}C$     |
| Avg_Slope <sup>(1)</sup> | Average slope                                   | TBD | 1.66    | TBD     | mV/ $^{\circ}C$ |
| $V_{110}$                | Voltage at 110 $^{\circ}C \pm 5^{\circ}C^{(2)}$ | 612 | 626.8   | 641.5   | mV              |
| $I_{DDA(TEMP)^{(3)}}$    | Current consumption                             |     | 3.4     | 6       | $\mu A$         |
| $t_{START}^{(3)}$        | Startup time                                    |     |         | 10      | $\mu s$         |
| $T_{S\_temp}^{(4)(3)}$   | ADC sampling time when reading the temperature  |     | 5       | 10      |                 |

1. Guaranteed by characterization, not tested in production.
2. Measured at  $V_{DD} = 3 V \pm 10 mV$ .  $V_{110}$  ADC conversion result is stored in the TS\_Factory\_CONV\_V110 byte.
3. Guaranteed by design, not tested in production.
4. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.20 Comparator

**Table 57. Comparator 1 characteristics**

| Symbol           | Parameter  | Conditions   | Min <sup>(1)</sup> | Typ     | Max <sup>(1)</sup> | Unit       |
|------------------|--|--|--------------------|---------|--------------------|------------|
| $V_{DDA}$        | Analog supply voltage  |  | 1.65               |         | 3.6                | V          |
| $R_{400K}$       | $R_{400K}$ value   |  |                    | 400     |                    | k $\Omega$ |
| $R_{10K}$        | $R_{10K}$ value  |  |                    | 10      |                    |            |
| $V_{IN}$         | Comparator 1 input voltage range                               |  | 0.6                |         | $V_{DDA}$          | V          |
| $t_{START}$      | Comparator startup time  |  |                    | 7       | 10                 | $\mu s$    |
| $t_d$            | Propagation delay <sup>(2)</sup>                               |  |                    | 3       | 10                 |            |
| Voffset          | Comparator offset  |  |                    | $\pm 3$ | $\pm 10$           | mV         |
| $d_{Voffset}/dt$ | Comparator offset variation in worst voltage stress conditions | $V_{DDA} = 3.6 V$<br>$V_{IN+} = 0 V$<br>$V_{IN-} = V_{REFINT}$<br>$T_A = 25^{\circ} C$ | 0                  | 1.5     | 10                 | mV/1000 h  |
| $I_{COMP1}$      | Current consumption <sup>(3)</sup>                             |  |                    | 160     | 260                | nA         |

1. Based on characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

**Table 58. Comparator 2 characteristics**

| Symbol                 | Parameter                                     | Conditions  | Min  | Typ     | Max <sup>(1)</sup> | Unit                  |
|------------------------|---|---|------|---------|--------------------|-----------------------|
| $V_{DDA}$              | Analog supply voltage                         |   | 1.65 |         | 3.6                | V                     |
| $V_{IN}$               | Comparator 2 input voltage range              |   | 0    |         | $V_{DDA}$          | V                     |
| $t_{START}$            | Comparator startup time                       | Fast mode   |      | 15      | 20                 | $\mu$ s               |
|                        |   | Slow mode   |      | 20      | 25                 |                       |
| $t_{d\ slow}$          | Propagation delay <sup>(2)</sup> in slow mode | $1.65\text{ V} \leq V_{DDA} \leq 2.7\text{ V}$  |      | 1.8     | 3.5                |                       |
|                        |   | $2.7\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$   |      | 2.5     | 6                  |                       |
| $t_{d\ fast}$          | Propagation delay <sup>(2)</sup> in fast mode | $1.65\text{ V} \leq V_{DDA} \leq 2.7\text{ V}$  |      | 0.8     | 2                  |                       |
|                        |   | $2.7\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$   |      | 1.2     | 4                  |                       |
| $V_{offset}$           | Comparator offset error                       |   |      | $\pm 4$ | $\pm 20$           | mV                    |
| $d\text{Threshold}/dt$ | Threshold voltage temperature coefficient     | $V_{DDA} = 3.3\text{ V}$<br>$T_A = 0\text{ to }50\text{ }^\circ\text{C}$<br>$V_- = V_{REF+}, 3/4 V_{REF+},$<br>$1/2 V_{REF+}, 1/4 V_{REF+}$ |      | 15      | 30                 | ppm/ $^\circ\text{C}$ |
| $I_{COMP2}$            | Current consumption <sup>(3)</sup>            | Fast mode   |      | 3.5     | 5                  | $\mu$ A               |
|                        |   | Slow mode   |      | 0.5     | 2                  |                       |

1. Based on characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

### 6.3.21 LCD controller

The embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the  $V_{DD}$  voltage. An external capacitor  $C_{ext}$  must be connected to the  $V_{LCD}$  pin to decouple this converter.

**Table 59. LCD controller characteristics**

| Symbol                | Parameter  | Min  | Typ           | Max       | Unit             |
|-----------------------|--|------|---------------|-----------|------------------|
| $V_{LCD}$             | LCD external voltage   |      |               | 3.6       | V                |
| $V_{LCD0}$            | LCD internal reference voltage 0   |      | 2.6           |           |                  |
| $V_{LCD1}$            | LCD internal reference voltage 1   |      | 2.73          |           |                  |
| $V_{LCD2}$            | LCD internal reference voltage 2   |      | 2.86          |           |                  |
| $V_{LCD3}$            | LCD internal reference voltage 3   |      | 2.98          |           |                  |
| $V_{LCD4}$            | LCD internal reference voltage 4   |      | 3.12          |           |                  |
| $V_{LCD5}$            | LCD internal reference voltage 5   |      | 3.26          |           |                  |
| $V_{LCD6}$            | LCD internal reference voltage 6   |      | 3.4           |           |                  |
| $V_{LCD7}$            | LCD internal reference voltage 7   |      | 3.55          |           |                  |
| $C_{ext}$             | $V_{LCD}$ external capacitance   | 0.1  |               | 2         | $\mu\text{F}$    |
| $I_{LCD}^{(1)}$       | Supply current at $V_{DD} = 2.2\text{ V}$  |      | 3.3           |           | $\mu\text{A}$    |
|                       | Supply current at $V_{DD} = 3.0\text{ V}$  |      | 3.1           |           |                  |
| $R_{Htot}^{(2)}$      | Low drive resistive network overall value  | 5.28 | 6.6           | 7.92      | $\text{M}\Omega$ |
| $R_L^{(2)}$           | High drive resistive network total value   | 192  | 240           | 288       | $\text{k}\Omega$ |
| $V_{44}$              | Segment/Common highest level voltage   |      |               | $V_{LCD}$ | V                |
| $V_{34}$              | Segment/Common 3/4 level voltage   |      | $3/4 V_{LCD}$ |           | V                |
| $V_{23}$              | Segment/Common 2/3 level voltage   |      | $2/3 V_{LCD}$ |           |                  |
| $V_{12}$              | Segment/Common 1/2 level voltage   |      | $1/2 V_{LCD}$ |           |                  |
| $V_{13}$              | Segment/Common 1/3 level voltage   |      | $1/3 V_{LCD}$ |           |                  |
| $V_{14}$              | Segment/Common 1/4 level voltage   |      | $1/4 V_{LCD}$ |           |                  |
| $V_0$                 | Segment/Common lowest level voltage  | 0    |               |           |                  |
| $\Delta V_{xx}^{(3)}$ | Segment/Common level voltage error<br>$T_A = -40\text{ to }85\text{ }^\circ\text{C}$ |      |               | $\pm 50$  | mV               |

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected
2. Guaranteed by design, not tested in production.
3. Based on characterization, not tested in production.

## 7 Package characteristics

### 7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 28. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline

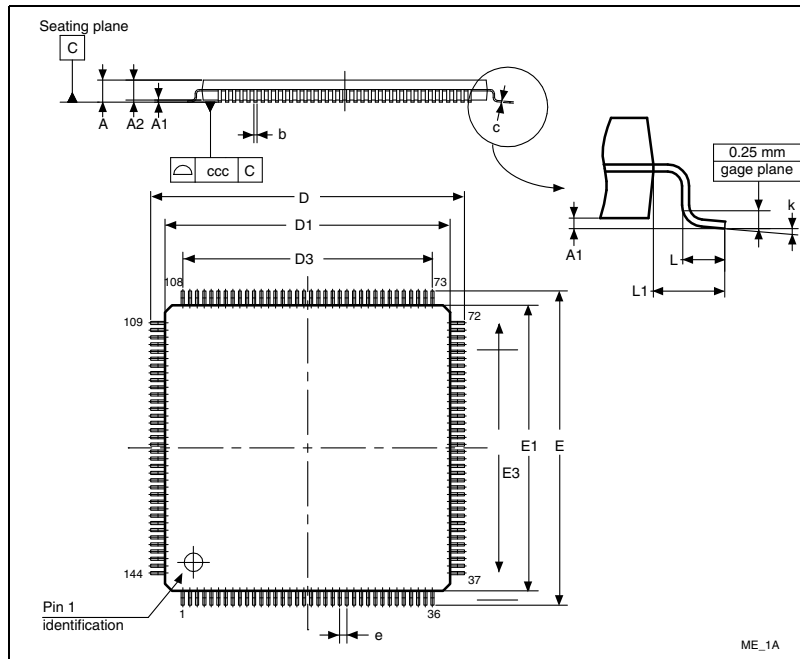
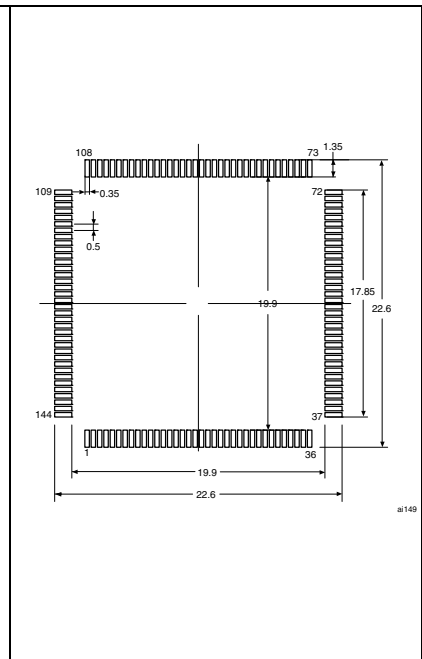


Figure 29. Recommended footprint



1. Drawing is not to scale. Dimensions are in millimeters.

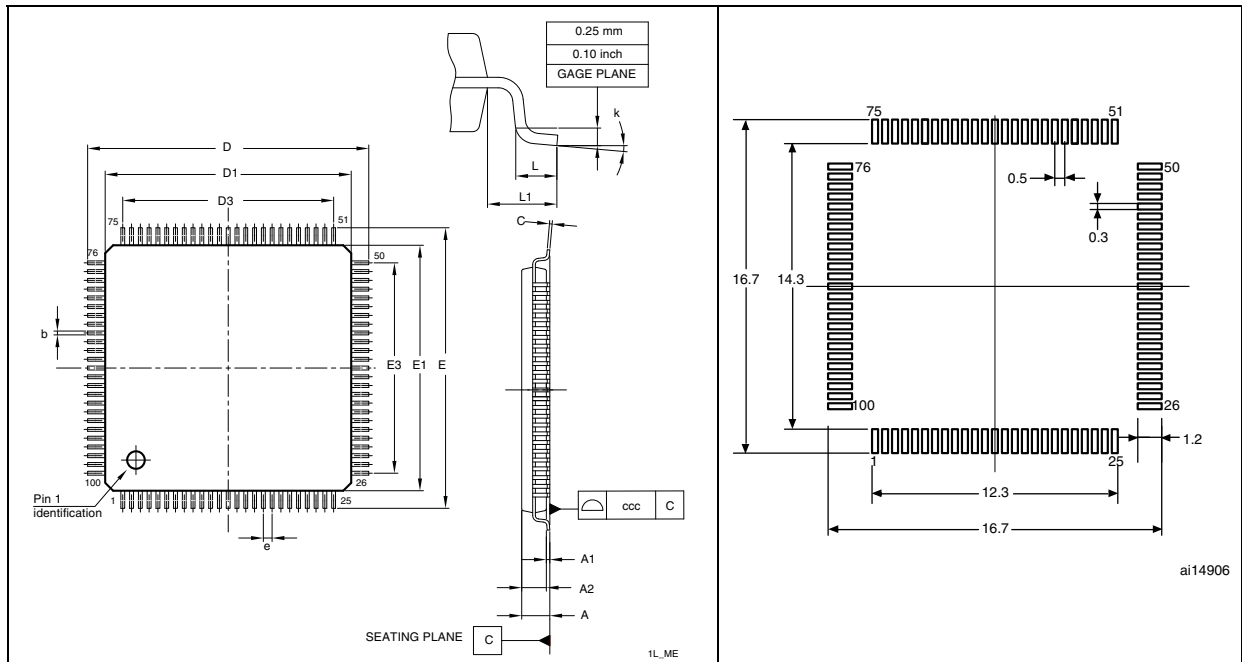
Table 60. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

| Symbol | millimeters |       |       | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|-------|-----------------------|--------|--------|
|        | Min         | Typ   | Max   | Min                   | Typ    | Max    |
| A      |             |       | 1.60  |                       |        | 0.063  |
| A1     | 0.05        |       | 0.15  | 0.002                 |        | 0.0059 |
| A2     | 1.35        | 1.40  | 1.45  | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.17        | 0.22  | 0.27  | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.09        |       | 0.20  | 0.0035                |        | 0.0079 |
| D      | 21.80       | 22.00 | 22.20 | 0.8583                | 0.8661 | 0.874  |
| D1     | 19.80       | 20.00 | 20.20 | 0.7795                | 0.7874 | 0.7953 |
| D3     |             | 17.50 |       |                       | 0.689  |        |
| E      | 21.80       | 22.00 | 22.20 | 0.8583                | 0.8661 | 0.874  |
| E1     | 19.80       | 20.00 | 20.20 | 0.7795                | 0.7874 | 0.7953 |
| E3     |             | 17.50 |       |                       | 0.689  |        |
| e      |             | 0.50  |       |                       | 0.0197 |        |
| L      | 0.45        | 0.60  | 0.75  | 0.0177                | 0.0236 | 0.0295 |
| L1     |             | 1.00  |       |                       | 0.0394 |        |
| k      | 0°          | 3.5°  | 7°    | 0°                    | 3.5°   | 7°     |
| ccc    | 0.08        |       |       | 0.0031                |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 30. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline

Figure 31. Recommended footprint



1. Drawing is not to scale. Dimensions are in millimeters.

Table 61. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

| Symbol | millimeters |      |      | inches <sup>(1)</sup> |        |        |
|--------|-------------|------|------|-----------------------|--------|--------|
|        | Min         | Typ  | Max  | Min                   | Typ    | Max    |
| A      |             |      | 1.6  |                       |        | 0.063  |
| A1     | 0.05        |      | 0.15 | 0.002                 |        | 0.0059 |
| A2     | 1.35        | 1.4  | 1.45 | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.17        | 0.22 | 0.27 | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.09        |      | 0.2  | 0.0035                |        | 0.0079 |
| D      | 15.8        | 16   | 16.2 | 0.622                 | 0.6299 | 0.6378 |
| D1     | 13.8        | 14   | 14.2 | 0.5433                | 0.5512 | 0.5591 |
| D3     |             | 12   |      |                       | 0.4724 |        |
| E      | 15.8        | 16   | 16.2 | 0.622                 | 0.6299 | 0.6378 |
| E1     | 13.8        | 14   | 14.2 | 0.5433                | 0.5512 | 0.5591 |
| E3     |             | 12   |      |                       | 0.4724 |        |
| e      |             | 0.5  |      |                       | 0.0197 |        |
| L      | 0.45        | 0.6  | 0.75 | 0.0177                | 0.0236 | 0.0295 |
| L1     |             | 1    |      |                       | 0.0394 |        |
| k      | 0.0°        | 3.5° | 7.0° | 0.0°                  | 3.5°   | 7.0°   |
| ccc    | 0.08        |      |      | 0.0031                |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 32. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline

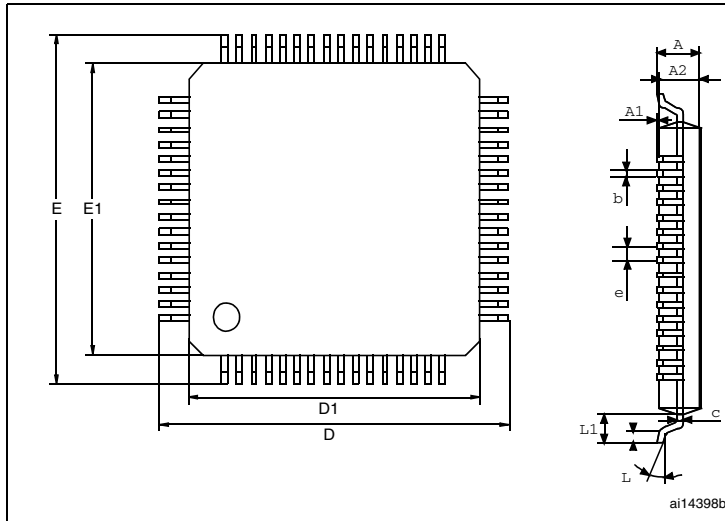
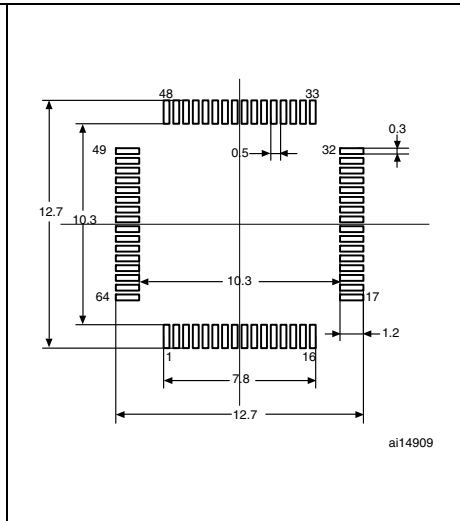


Figure 33. Recommended footprint



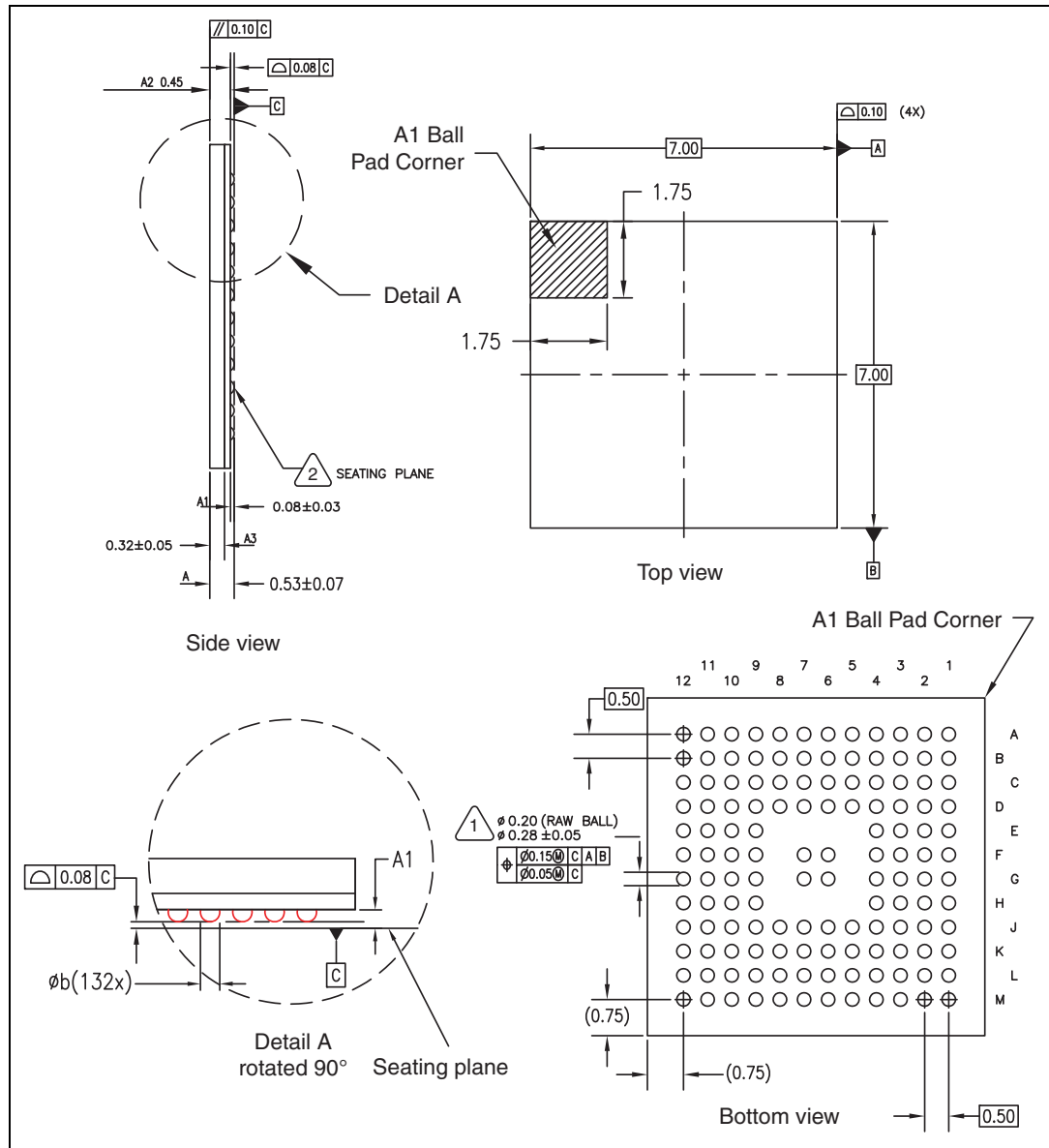
1. Drawing is not to scale. Dimensions are in millimeters.

Table 62. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

| Symbol | millimeters           |       |      | inches <sup>(1)</sup> |        |        |
|--------|-----------------------|-------|------|-----------------------|--------|--------|
|        | Min                   | Typ   | Max  | Min                   | Typ    | Max    |
| A      |                       |       | 1.60 |                       |        | 0.0630 |
| A1     | 0.05                  |       | 0.15 | 0.0020                |        | 0.0059 |
| A2     | 1.35                  | 1.40  | 1.45 | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.17                  | 0.22  | 0.27 | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.09                  |       | 0.20 | 0.0035                |        | 0.0079 |
| D      |                       | 12.00 |      |                       | 0.4724 |        |
| D1     |                       | 10.00 |      |                       | 0.3937 |        |
| E      |                       | 12.00 |      |                       | 0.4724 |        |
| E1     |                       | 10.00 |      |                       | 0.3937 |        |
| e      |                       | 0.50  |      |                       | 0.0197 |        |
| θ      | 0°                    | 3.5°  | 7°   | 0°                    | 3.5°   | 7°     |
| L      | 0.45                  | 0.60  | 0.75 | 0.0177                | 0.0236 | 0.0295 |
| L1     |                       | 1.00  |      |                       | 0.0394 |        |
| N      | <b>Number of pins</b> |       |      |                       |        |        |
|        | 64                    |       |      |                       |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package outline



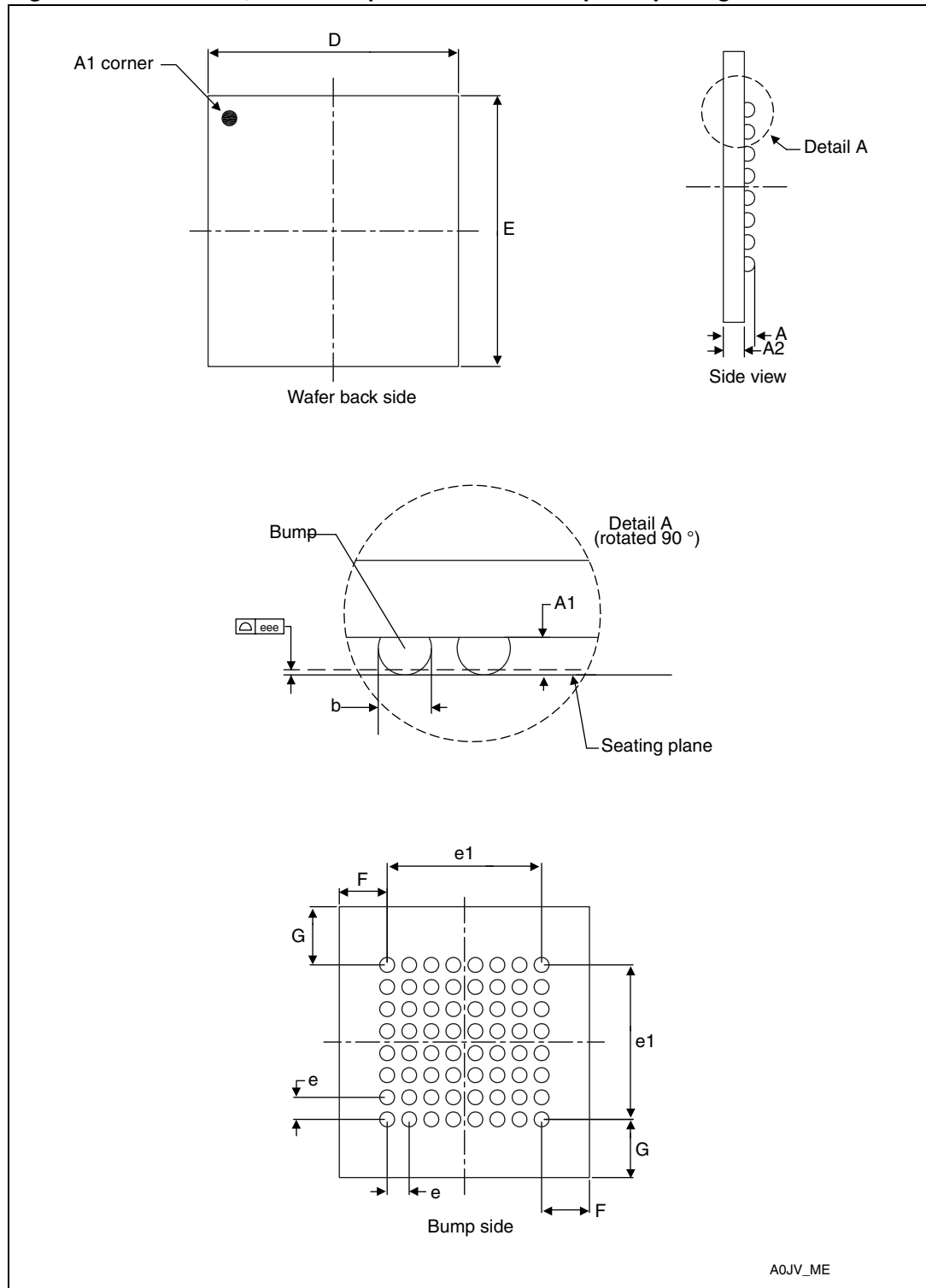
1. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.

Table 63. UFBGA132 package mechanical data

| Symbol | millimeters |      |      | inches <sup>(1)</sup> |        |        |
|--------|-------------|------|------|-----------------------|--------|--------|
|        | Min         | Typ  | Max  | Min                   | Typ    | Max    |
| A      | 0.46        | 0.53 | 0.60 | 0.0181                | 0.0209 | 0.0236 |
| A1     | 0.05        | 0.08 | 0.11 | 0.0020                | 0.0032 | 0.0043 |
| A2     | 0.40        | 0.45 | 0.50 | 0.0157                | 0.0177 | 0.0197 |
| b      | 0.17        | 0.28 | 0.33 | 0.0067                | 0.0110 | 0.0130 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. WLCSP64, 0.400 mm pitch wafer level chip size package outline



A0JV\_ME

**Table 64. WLCSP64, 0.400 mm pitch wafer level chip size package mechanical data**

| Symbol | millimeters |       |       | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|-------|-----------------------|--------|--------|
|        | Min         | Typ   | Max   | Min                   | Typ    | Max    |
| A      | 0.520       | 0.570 | 0.620 | 0.0205                | 0.0224 | 0.0244 |
| A1     | 0.170       | 0.190 | 0.210 | 0.0067                | 0.0075 | 0.0083 |
| A2     | 0.350       | 0.380 | 0.410 | 0.0138                | 0.0150 | 0.0161 |
| b      | 0.240       | 0.270 | 0.300 | 0.0094                | 0.0106 | 0.0118 |
| D      | 4.519       | 4.539 | 4.559 | 0.1779                | 0.1787 | 0.1795 |
| E      | 4.891       | 4.911 | 4.931 | 0.1926                | 0.1933 | 0.1941 |
| e      |             | 0.400 |       |                       | 0.0157 |        |
| e1     |             | 2.800 |       |                       | 0.1102 |        |
| F      |             | 0.870 |       |                       | 0.0342 |        |
| G      |             | 1.056 |       |                       | 0.0416 |        |
| eee    |             | 0.050 |       |                       | 0.0020 |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 7.2 Thermal characteristics

The maximum chip-junction temperature,  $T_J \text{ max}$ , in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$  is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$  is the sum of  $P_{INT \text{ max}}$  and  $P_{I/O \text{ max}}$  ( $P_D \text{ max} = P_{INT \text{ max}} + P_{I/O \text{ max}}$ ),
- $P_{INT \text{ max}}$  is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O \text{ max}}$  represents the maximum power dissipation on output pins where:

$$P_{I/O \text{ max}} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL} / I_{OL}$  and  $V_{OH} / I_{OH}$  of the I/Os at low and high level in the application.

**Table 65. Thermal characteristics**

| Symbol        | Parameter  | Value | Unit |
|---------------|--|-------|------|
| $\Theta_{JA}$ | Thermal resistance junction-ambient<br>LQFP144 - 20 x 20 mm / 0.5 mm pitch | 40    | °C/W |
|               | Thermal resistance junction-ambient<br>BGA132 - 7 x 7 mm                   | 60    |      |
|               | Thermal resistance junction-ambient<br>LQFP100 - 14 x 14 mm / 0.5 mm pitch | 43    |      |
|               | Thermal resistance junction-ambient<br>LQFP64 - 10 x 10 mm / 0.5 mm pitch  | 46    |      |

### 7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org).

## 8 Ordering information scheme

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

**Table 66. STM32L15xxC ordering information scheme**

| Example:  | STM32 | L | 151 | R | C | T | 6 | D | xxx |
|---|-------|---|-----|---|---|---|---|---|-----|
| <b>Device family</b><br>STM32 = ARM-based 32-bit microcontroller  |       |   |     |   |   |   |   |   |     |
| <b>Product type</b><br>L = Low power  |       |   |     |   |   |   |   |   |     |
| <b>Device subfamily</b><br>151: Devices without LCD<br>152: Devices with LCD  |       |   |     |   |   |   |   |   |     |
| <b>Pin count</b><br>R = 64 pins<br>V = 100 pins<br>Z = 144 pins<br>Q = 132 pins   |       |   |     |   |   |   |   |   |     |
| <b>Flash memory size</b><br>C = 256 Kbytes of Flash memory  |       |   |     |   |   |   |   |   |     |
| <b>Package</b><br>H = BGA<br>T = LQFP<br>Y = WLCSP  |       |   |     |   |   |   |   |   |     |
| <b>Temperature range</b><br>6 = Industrial temperature range, -40 to 85 °C  |       |   |     |   |   |   |   |   |     |
| <b>Options</b><br>No character = V <sub>DD</sub> range: 1.8 to 3.6 V and BOR enabled<br>D = V <sub>DD</sub> range: 1.65 to 3.6 V and BOR disabled |       |   |     |   |   |   |   |   |     |
| <b>Packing</b><br>TR = tape and reel<br>No character = tray or tube   |       |   |     |   |   |   |   |   |     |

## 9 Revision history

**Table 67. Document revision history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 21-Feb-2012 | 1        | Initial release. |

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