



# STMPE801

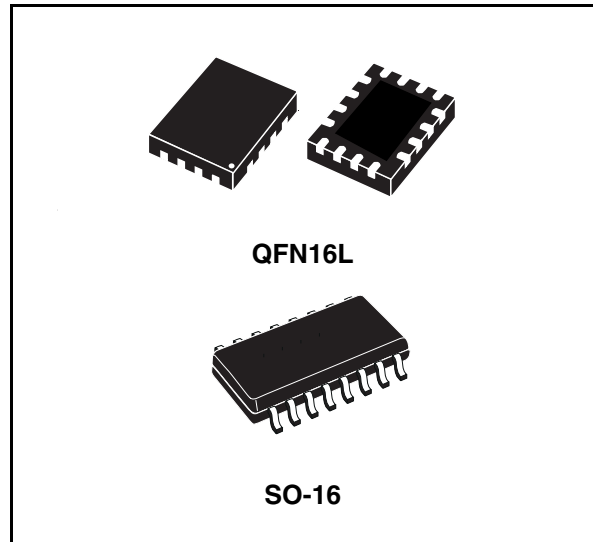
8-bit port expander  
Xpander logic

## Features

- 8 GPIO
- Operating voltage 1.65V - 3.6V
- I/O voltage 1.65V-3.6V
- Interrupt output pin
- Reset input pin
- Wake up feature on each I/O
- Up to 2 devices sharing the same bus (1 address line)
- <1µA suspend current

## Application

- Portable media player, Game console
- Mobile phone, Smart phone



## Description

The STMPE801 is a GPIO (General Purpose Input / Output) port expander able to interface a main digital ASIC via the two-line bidirectional bus (I<sup>2</sup>C); separate GPIO Expander IC is often used in Mobile-Multimedia platforms to solve the problems of the limited amounts of GPIOs usually available on the Digital Engine.

The STMPE801 offers great flexibility as each I/Os is configurable as input, output. This device has been designed very low quiescent current, and includes wake up feature for each I/O, to optimize the power consumption of the IC.

Table 1. Device summary

| Order codes | Package                | Packaging                     |
|-------------|------------------------|-------------------------------|
| STMPE801QTR | QFN16L (2.6mm x 1.8mm) | Tape and reel (3000 per reel) |
| STMPE801MTR | SO-16                  | Tape and reel (2500 per reel) |

# Contents

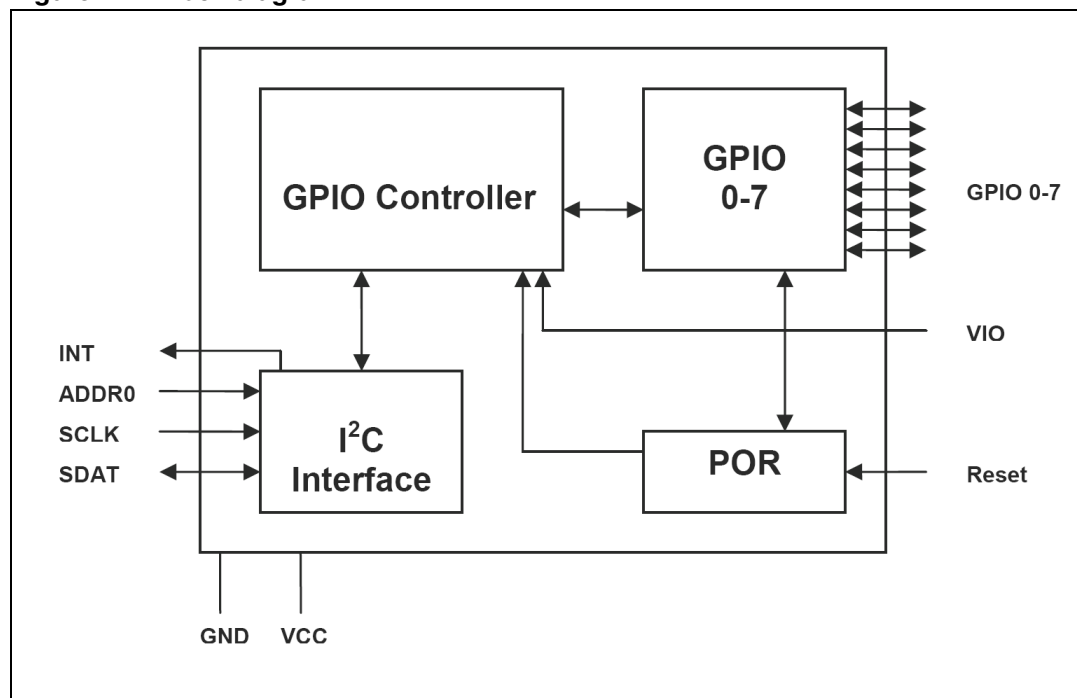
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# 1 Block diagram

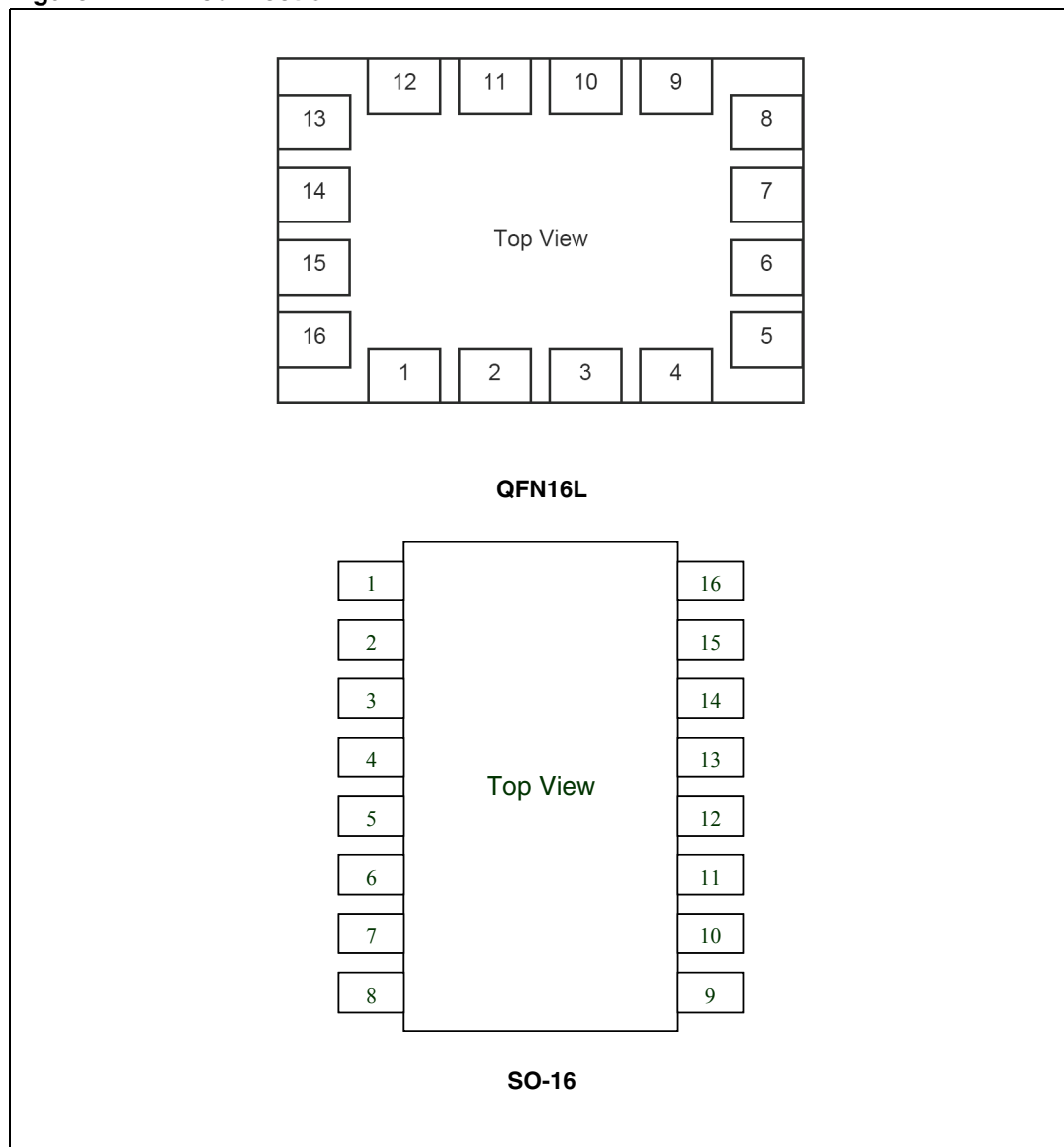
Figure 1. Block diagram



## 2 Pin settings

### 2.1 Pin connection

Figure 2. Pin connection



## 2.2 Pin assignment

Table 2. Pin assignment

| Pin N° |        | Name    | Function   |
|--------|--------|---------|--|
| SO-16  | QFN16L |         |  |
| 11     | 1      | INT     | INT output   |
| 12     | 2      | Reset   | Reset Input (Active Low)   |
| 13     | 3      | CLOCK   | I <sup>2</sup> C Clock   |
| 14     | 4      | Address | I <sup>2</sup> C Address   |
| 15     | 5      | DATA    | I <sup>2</sup> C Data  |
| 16     | 6      | VCC     | Supply voltage for I <sup>2</sup> C block  |
| 1      | 7      | VIO     | Supply voltage for GPO and GPIO Controller<br>(Note: V <sub>IO</sub> must be ≥ V <sub>CC</sub> ) |
| 2      | 8      | GND     | GND  |
| 3      | 9      | GPIO_0  | GPIO 0   |
| 4      | 10     | GPIO_1  | GPIO 1   |
| 5      | 11     | GPIO_2  | GPIO 2   |
| 6      | 12     | GPIO_3  | GPIO 3   |
| 7      | 13     | GPIO_4  | GPIO 4   |
| 8      | 14     | GPIO_5  | GPIO 5   |
| 9      | 15     | GPIO_6  | GPIO 6   |
| 10     | 16     | GPIO_7  | GPIO 7   |

### 3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

#### 3.1 Absolute maximum rating

Table 3. Absolute maximum rating

| Symbol          | Parameter                      | Value | Unit |
|-----------------|--------------------------------|-------|------|
| V <sub>CC</sub> | Supply voltage                 | 4.5   | V    |
| V <sub>IO</sub> | GPO supply voltage             | 4.5   | V    |
| VESD (HBM)      | ESD protection on each GPO pin | 2     | KV   |

#### 3.2 Thermal data

Table 4. Thermal data

| Symbol           | Parameter                     | Value |     |     | Unit |
|------------------|-------------------------------|-------|-----|-----|------|
|                  |                               | Min   | Typ | Max |      |
| T <sub>A</sub>   | Operating ambient temperature | -40   |     | +85 | °C   |
| T <sub>STG</sub> | Operating storage temperature | -65   |     | 155 | °C/W |

## 4 Electrical specification

### 4.1 DC electrical characteristics

Table 5. DC electrical characteristics

| Symbol            | Parameter                                     | Test conditions  | Value          |     |               | Unit    |
|-------------------|---|--|----------------|-----|---------------|---------|
|                   |   |  | Min            | Typ | Max           |         |
| $V_{CC}$          | Core supply voltage                           |  | 1.65           | -   | 3.6           | V       |
| $V_{IO}$          | IO suppli voltage                             |  | 1.65           | -   | 3.6           | V       |
| $I_{pd}$          | Power down current                            |  |                |     | 1             | $\mu$ A |
| $I_{cc\ Max}$     | Operating current<br>(No peripheral activity) | I <sup>2</sup> C running at 400KHz<br>100% traffic density |                | 0.2 | 0.5           | mA      |
| $I_{cc\ Normal}$  | Operating current<br>(No peripheral activity) | I <sup>2</sup> C running at 400KHz<br>1% traffic density   |                | 10  | 15            | $\mu$ A |
| $I_{CC\ Suspend}$ | Operating current<br>(No peripheral activity) | No I <sup>2</sup> C activity                               |                | 0.5 | 1             | $\mu$ A |
| $V_{IL}$          | Input voltage low state                       | $V_{IO} = 1.8-3.3V$  | -0.3V          |     | $0.30V_{IO}$  | V       |
| $V_{IH}$          | Input voltage high state                      | $V_{IO} = 1.8-3.3V$  | $0.70V_{IO}$   |     | $V_{IO}+0.3V$ | V       |
| $V_{OL}$          | Output voltage low state                      | $V_{IO} = 1.8-3.3V, I_{OL}=8mA$                            | -0.3V          |     | $0.25V_{IO}$  | V       |
| $V_{OH}$          | Output voltage high state                     | $V_{IO}=1.8-3.3V, I_{OL}=8mA$                              | $0.75V_{IO}$   |     | $V_{IO}+0.3V$ | V       |
| $V_{OL} (I^2C)$   | Output voltage low state                      | $V_{CC}=1.8-3.3V, I_{OL}=8mA$                              | -0.3V          |     | $0.25V_{CC}$  | V       |
| $V_{OH} (I^2C)$   | Output voltage high state                     | $V_{CC}=1.8-3.3V, I_{OL}=8mA$                              | $0.75V_{c\ c}$ |     | $V_{CC}+0.3V$ | V       |

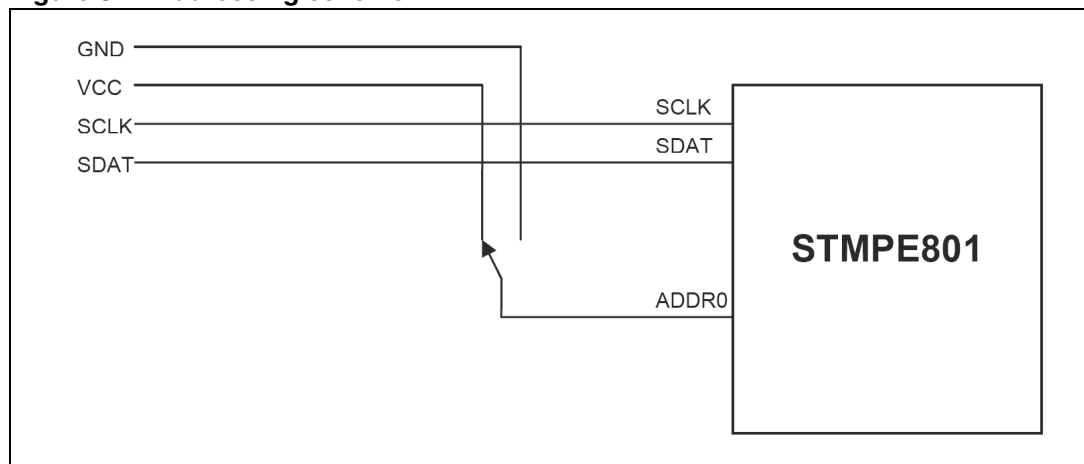
## 5 I<sup>2</sup>C module

STMPE801 is interface to the main processor using an I2C bus.

### 5.1 I<sup>2</sup>C address

Addressing scheme of STMPE801 is designed to allow up to 2 devices to be connected to the same I<sup>2</sup>C bus.

**Figure 3. Addressing scheme**



**Table 6. Addresses**

| ADDR0 | Address | Note |
|-------|---------|------|
| 0     | 0x82    |      |
| 1     | 0x88    |      |

For the bus master to communicate to the slave device, the bus master must initiate a Start condition and followed by the slave device address. Accompanying the slave device address, there is a Read/Write bit ( $R/\overline{W}$ ). The bit is set to 1 for Read and 0 for write operation.

If a match occurs on the slave device address, the corresponding device gives an acknowledge on the SDA during the 9<sup>th</sup> bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

Figure 4. I<sup>2</sup>C timing

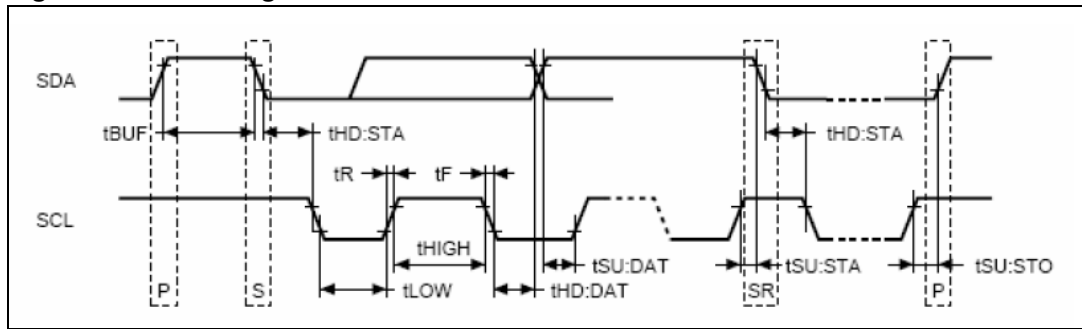


Table 7. I<sup>2</sup>C address

| Symbol       | Parameter   | Min | Typ | Max | Unit    |
|--------------|---|-----|-----|-----|---------|
| $f_{SCL}$    | SCL clock frequency   | 0   |     | 400 | kHz     |
| $t_{LOW}$    | Clock low period  | 1.3 |     |     | $\mu$ s |
| $t_{HIGH}$   | Clock high period   | 600 |     |     | ns      |
| $t_F$        | SDA and SCL fall time   |     |     | 300 | ns      |
| $t_{HD:STA}$ | START condition hold time<br>(After this period the first clock is generated) | 600 |     |     | ns      |
| $t_{SU:STA}$ | START condition setup time<br>(Only relevant for a repeated start period)     | 600 |     |     | ns      |
| $t_{SU:DAT}$ | Data setup time   | 100 |     |     | ns      |
| $t_{HD:DAT}$ | Data hold time  | 0   |     |     | $\mu$ s |
| $t_{SU:STO}$ | STOP condition setup time   | 600 |     |     | ns      |
| $t_{BUF}$    | Time the bust must be free before a new trasmission can start                 | 1.3 |     |     | $\mu$ s |

## 5.2 I<sup>2</sup>C features

The features that are supported by the I<sup>2</sup>C interface are as below:

- I<sup>2</sup>C slave device
- Operates at 1.8V
- Compliant to Philips I<sup>2</sup>C specification version 2.1
- Supports standard (uo to 100Kbps) and fast (up to 400Kbps) modes

### 5.3 Start condition

A Start condition is identified by a falling edge of SDATA while SCLK is stable at high state. A Start condition must precede any data/command transfer. The device continuously monitors for a Start condition and will not respond to any transaction unless one is encountered.

### 5.4 Stop condition

A Stop condition is identified by a rising edge of SDATA while SCLK is stable at high state. A Stop condition terminates communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a Stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I<sup>2</sup>C transaction. A Stop condition at the end of a write command stops the write operation to registers.

### 5.5 Acknowledge bit

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDATA after sending eight bits of data. During the ninth bit, the receiver pulls the SDATA low to acknowledge the receipt of the eight bits of data. The receiver may leave the SDATA in high state if it would to not acknowledge the receipt of the data.

### 5.6 Data input

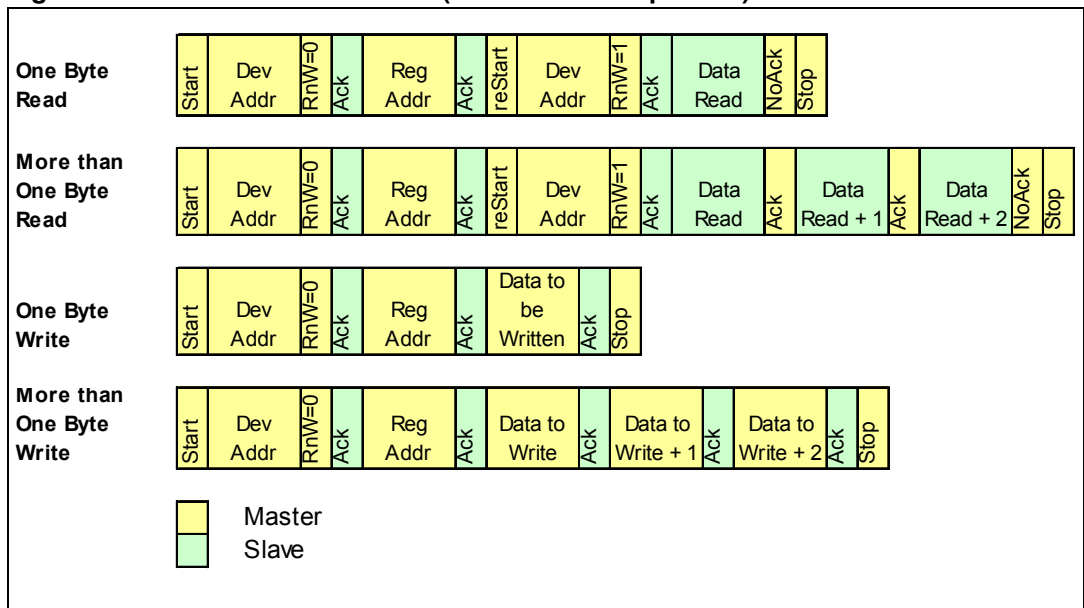
The device samples the data input on SDATA on the rising edge of the SCLK. The SDATA signal must be stable during the rising edge of SCLK and the SDATA signal must change only when SCLK is driven low.

## 5.7 Operation modes

Table 8. Operation modes

| Mode  | Bytes | Programming Sequence   |
|-------|-------|--|
| Read  | ≥1    | START, Device Address, R/W = 0, Register Address to be read  |
|       |       | RESTART, Device Address, R/W = 1, Data Read, STOP  |
|       |       | If no STOP is issued, the Data Read can be continuously preformed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being read. For register address that falls within a non-incremental address range, the address will be kept static throughout the entire read operations. Refer to the Memory Map table for the address ranges that are auto and non-increment.         |
| Write | ≥1    | START, Device Address, R/W = 0, Register Address to be written, Data Write, STOP   |
|       |       | If no STOP is issued, the Data Write can be continuously performed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being written in. For register address that falls within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the Memory Map table for the address ranges that are auto and non-increment. |

Figure 5. Read and write modes (random and sequential)



## 5.8 Read operation

A write is first performed to load the register address into the Address Counter but without sending a Stop condition. Then, the bus master sends a reStart condition and repeats the Device Address with the R/W bit set to 1. The slave device acknowledges and outputs the content of the addressed byte. If no more data is to be read, the bus master must not acknowledge the byte and terminates the transfer with a Stop condition.

If the bus master acknowledges the data byte, then it can continue to perform the data reading. To terminate the stream of data byte, the bus master must not acknowledge the last output byte and follow by a Stop condition. If the address of the register written into the Address Counter falls within the range of addresses that has the auto-increment function, the data being read will be coming from consecutive addresses, with the internal Address Counter automatically increments after each byte output. After the last memory address, the Address Counter 'rolls-over' and the device continue to output data from the memory address of 0x00. Similarly, for the address of register that falls within non-increment range of addresses, the output data byte comes from the same address (which is the address pointed by the Address Counter).

## 5.9 Acknowledgement in read operation

For the above read command, the slave device waits, after each byte read, for an acknowledgement during the ninth bit time. If the bus master does not drive the SDA to low state, then the slave device terminates and switches back to its idle mode, waiting for the next command.

## 5.10 Write operations

A write is first performed to load the register address into the Address Counter without sending a Stop condition. After the bus master receives an acknowledgement from the slave device, it may start to send a data byte to the register (pointed by the Address Counter). The slave device again acknowledges and the bus master terminates the transfer with a Stop condition.

If the bus master would like to continue to write more data, it can just continue write operation without issuing the Stop condition. Whether the Address Counter auto-increments or not after each data byte write, depends on the address of the register written into the Address Counter. After the bus master writes the last data byte and the slave device acknowledges the receipt of the last data, the bus master may terminates the write operation by sending a Stop condition. When the Address Counter reaches the last memory address, it 'rolls-over' on the next data byte write.

## 5.11 General call

A general call address is a transaction with the slave address of 0x00 and  $R/\overline{W} = 0$ . When a general call address is made, the device responds to this transaction with an acknowledgement and behaves as a slave-receiver mode. The meaning of a general call address is defined in the second byte sent by the master-transmitter.

**Table 9. General call**

| R/ $\overline{W}$ | Second Byte Value | Definition  |
|-------------------|-------------------|---|
| 0                 | 0x06              | 2-byte transaction in which the second byte tells the slave device to reset and write (or latch in) the 1-bit programmable part of the slave address.     |
| 0                 | 0x04              | 2-byte transaction in which the second byte tells the slave device not to reset and write (or latch in) the 1-bit programmable part of the slave address. |
| 0                 | 0x00              | Not allowed as second byte.   |

*Note:* All other second byte value will be ignored.

## 6 Turning I<sup>2</sup>C block OFF and ON

STMPE801 operates entirely on the I<sup>2</sup>C clock. When there are no activity on the I<sup>2</sup>C bus, current consumption of the device is extremely low. However, when there are activity on the I<sup>2</sup>C bus, current consumption increases, even if the I<sup>2</sup>C traffic is not directed to the assigned address.

Host system may choose to shut-down the I<sup>2</sup>C block in the STMPE801, if no access to the registers are required. This feature allows the current consumption to drop to the minimum. Host system turns OFF the I<sup>2</sup>C block by writing '1' into the I<sup>2</sup>C\_SHDN bit. The I<sup>2</sup>C block will shut down on the next valid clock edge of the I<sup>2</sup>C clock signal. In this state, the device CANNOT be accessed by I<sup>2</sup>C, as the I<sup>2</sup>C has shut down completely.

To turn ON the I<sup>2</sup>C block, system host must reset the STMPE801 in order to re-activate the I<sup>2</sup>C block. This could be done by hardware assertion of the RESET pin.

## 7 Register map

**Table 10. Register map**

| Address | Register Name | Size (bit) | Function                        |
|---------|---------------|------------|---------------------------------|
| 0x00    | Chip ID       | 16         | 0x0801                          |
| 0x02    | Version ID    | 8          | Revision number                 |
| 0x04    | SystemControl | 8          | Reset and interrupt control     |
| 0x08    | IEGPIOR       | 8          | GPIO interrupt enable register  |
| 0x09    | ISGPIOR       | 8          | GPIO interrupt status register  |
| 0x10    | GPMR          | 8          | GPIO monitor pin state register |
| 0x11    | GPSR          | 8          | GPIO set pin state register     |
| 0x12    | GPDR          | 8          | GPIO set pin direction register |

### 7.1 System and identification registers

**Table 11. System and identification registers**

| Register name | Size (bit) | Function   |
|---------------|------------|--|
| Chip ID       | 16         | 0x0801   |
| Version ID    | 8          | Revision number:<br>0x01 (Engineering)<br>0x02 (Final silicon) |
| Systemcontrol | 8          |  |

### 7.2 System control register

**Table 12. System control register**

| Bit | Reset | Name        | Description   |
|-----|-------|-------------|---|
| 7   | 0     | SoftReset   | Writing '1' to this bit causes a soft reset                                   |
| 6   | 0     | I2C_SHDN    | Writing '1' to this bit shuts down the I2C block on the next valid I2C clock. |
| 5   | 0     |             |   |
| 4   | 0     |             |   |
| 3   | 0     |             |   |
| 2   | 0     | INT_Enable  | '1' to enable, '0' to disable INT output                                      |
| 1   | 0     |             |   |
| 0   | 0     | INTPolarity | '1' for active HI, '0' for active LOW   |

## 8 Interrupt, power supply & reset

STMPE801 could be configured to generate an interrupt when there is a logic transition of any of the GPIO configured as input.

### 8.1 Interrupt enable GPIO mask register (IEGPIOR)

IEGPIOR register is used to enable the interruption from a particular GPIO interrupt source to the host. The IEG[7:0] bits are the interrupt enable mask bits correspond to the GPIO[7:0] pins.

|             |  | IEGPIOR |      |      |      |      |      |      |      |
|-------------|--|---------|------|------|------|------|------|------|------|
| Bit         |  | 7       | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|             |  | IEG7    | IEG6 | IEG5 | IEG4 | IEG3 | IEG2 | IEG1 | IEG0 |
| R/W         |  | RW      | RW   | RW   | RW   | RW   | RW   | RW   | RW   |
| Reset Value |  | 0       | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**Table 13. Register**

| Bits | Name   | Description   |
|------|--------|---|
| 7:0  | IEG[x] | Interrupt Enable GPIO Mask (where x = 7 to 0)<br>Writing a '1' to the IE[x] bit will enable the interruption to the host. |

## 8.2 Interrupt status GPIO register (ISGPIOR)

ISGPIOR register monitors the status of the interruption from a particular GPIO pin interrupt source to the host. Regardless whether the IEGPIOR bits are enabled or not, the ISGPIOR bits are still updated. The ISG[9:0] bits are the interrupt status bits correspond to the GPIO[7:0] pins.

| ISGPIOR     |      |      |      |      |      |      |      |      |
|-------------|------|------|------|------|------|------|------|------|
| Bit         | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|             | ISG7 | ISG6 | ISG5 | ISG4 | ISG3 | ISG2 | ISG1 | ISG0 |
| R/W         | RW   | RW   | RW   | RW   | RW   | RW   | RW   | RW   |
| Reset Value | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**Table 14. Register**

| Bits | Name   | Description  |
|------|--------|--|
| 7:0  | ISG[x] | Interrupt Status GPIO (where x = 7 to 0)<br><b>Read:</b><br>Interrupt Status of the GPIO[x]. Reading the register will clear any bits that has been set to '1'<br><b>Write:</b><br>Writing to this register has no effects |

## 8.3 GPIO controller

A total of 8 GPIOs are available in the STMPE801 port expander IC. The GPIO controller contains the registers that allow the host system to configure each of the pins as input or output. Unused GPIOs should be configured as outputs to minimize the power consumption.

A group of registers are used to control the exact function of each of the 8 GPIO. The registers and their respective address is listed in the following table.

**Table 15. Register**

| Address | Register Name | Description                     | Auto-Increment (during sequential R/W) |
|---------|---------------|---------------------------------|--|
| 0x10    | GPMR          | GPIO monitor pin state register | Yes                                    |
| 0x11    | GPSR          | GPIO set pin state register     | Yes                                    |
| 0x12    | GPDR          | GPIO set pin direction register | Yes                                    |

All GPIO registers are named as GPxx, where Xxx represents the functional group

|      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|
| Bit  | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| GPxx | IO-7 | IO-6 | IO-5 | IO-4 | IO-3 | IO-2 | IO-1 | IO-0 |

The function of each bit is shown in the following table:

**Table 16. Pin function**

| Register Name          | Function  |
|------------------------|---|
| GPIO Monitor Pin State | Reading this bit yields the current state of the bit. Writing has no effect.  |
| GPIO Set Pin State     | Writing '1' to this bit causes the corresponding GPIO to go to '1' state. Writing '0' to this bit causes the corresponding GPIO to go to '0' state. |
| GPIO Set Pin Direction | '0' sets the corresponding GPIO to input state, and '1' sets it to output state. All bits are '0' on reset.   |

On power-up reset, all GPIO are set as input.

## 8.4 Power supply

STMPE801 GPIO operates from a separate supply pin ( $V_{IO}$ ). This dedicated supply pin provides a level-shifting feature to the STMPE801.

GPIO will remain valid until  $V_{IO}$  is removed.

The host system may choose to turn off  $V_{CC}$  supply while keeping  $V_{IO}$  supplied. However it is not allowed to turn off supply to  $V_{IO}$ , while keeping the  $V_{CC}$  supplied.

## 8.5 Reset

STMPE801 is equipped with an internal POR circuit that holds the device in reset state, until the  $V_{IO}$  supply input is valid. The internal POR is tied to the  $V_{IO}$  supply pin.

The reset pin allows the host to reset the STMPE801 directly. Minimum pulse width of reset signal is 100µs.

During the period when reset pin is asserted, all GPIO default to inputs.

## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Table 17. QFN16L mechanical data

| Dim. | mm.  |      |      | inch  |       |       |
|------|------|------|------|-------|-------|-------|
|      | Min  | Typ  | Max  | Min   | Typ   | Max   |
| A    | 0.45 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1   |      | 0.02 | 0.05 |       | 0.001 | 0.002 |
| b    | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D    | 2.50 | 2.60 | 2.70 | 0.098 | 0.102 | 0.106 |
| E    | 1.70 | 1.80 | 1.90 | 0.067 | 0.071 | 0.075 |
| e    |      | 0.40 |      |       | 0.016 |       |
| L    | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |

Figure 6. Package dimensions

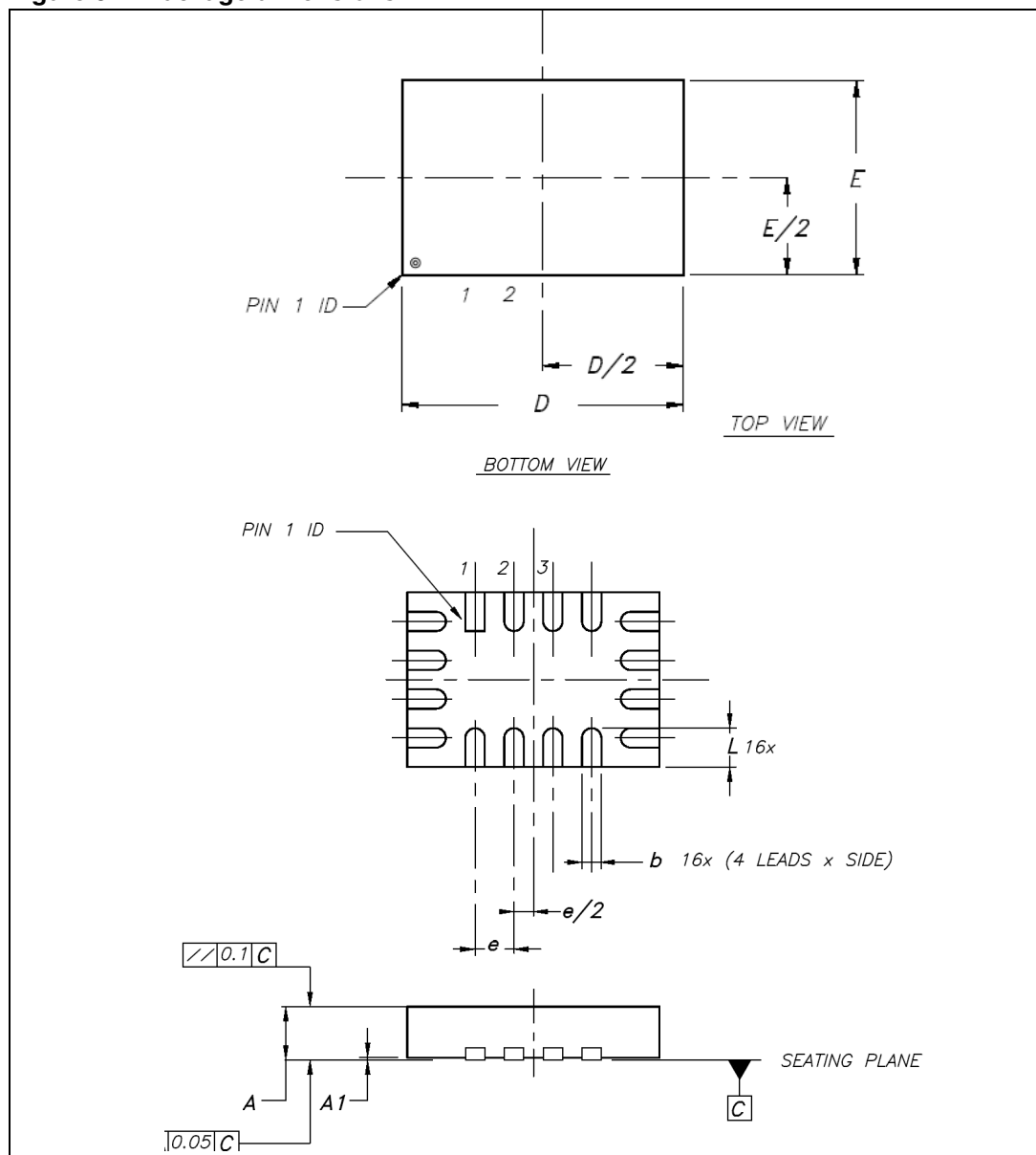


Figure 7. Footprint recommendation

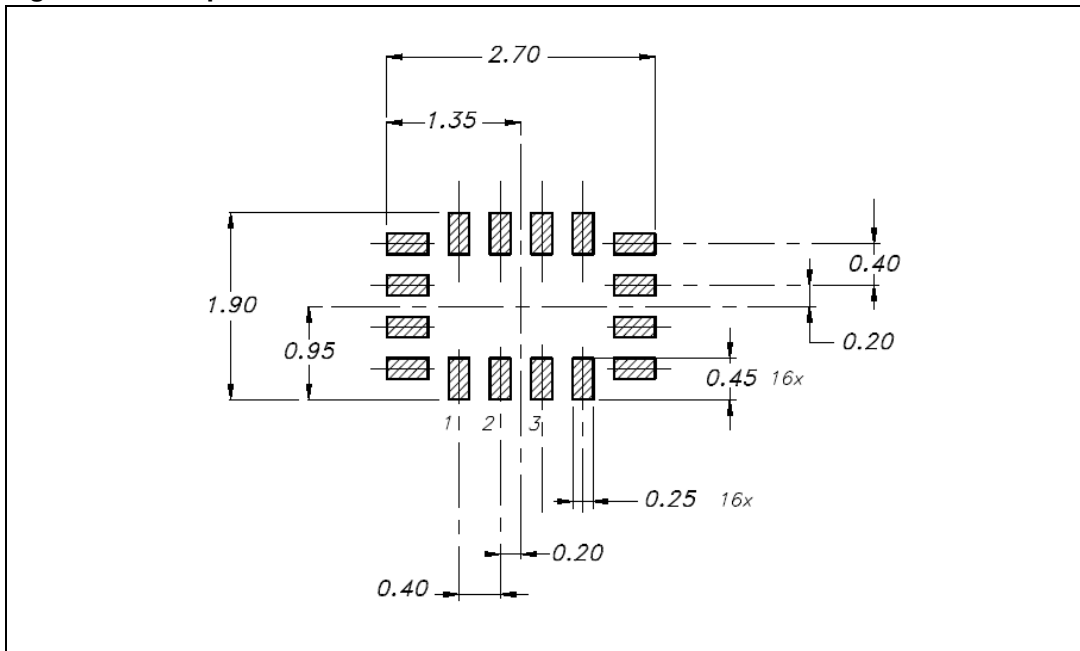


Figure 8. Marking

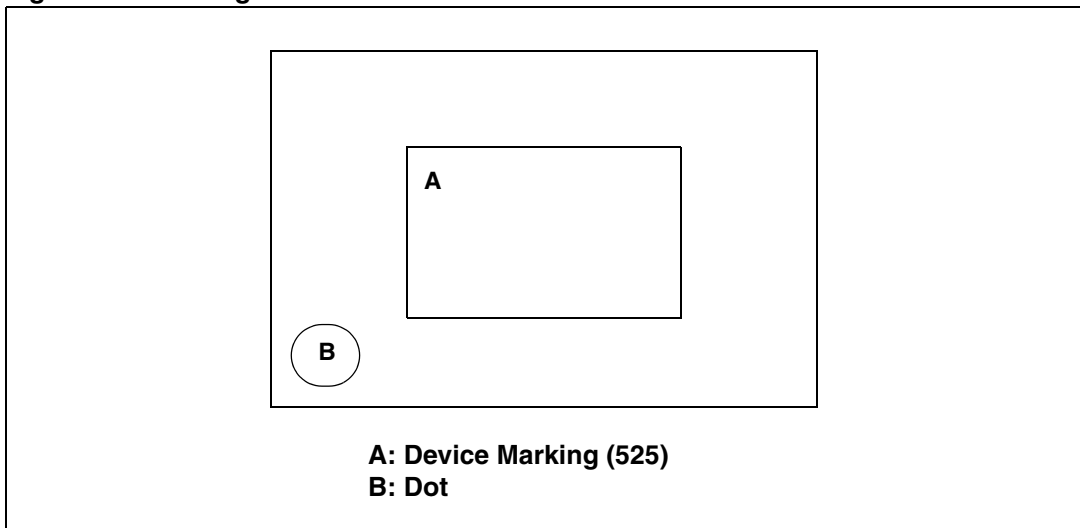


Figure 9. QFN16L tape and reel information

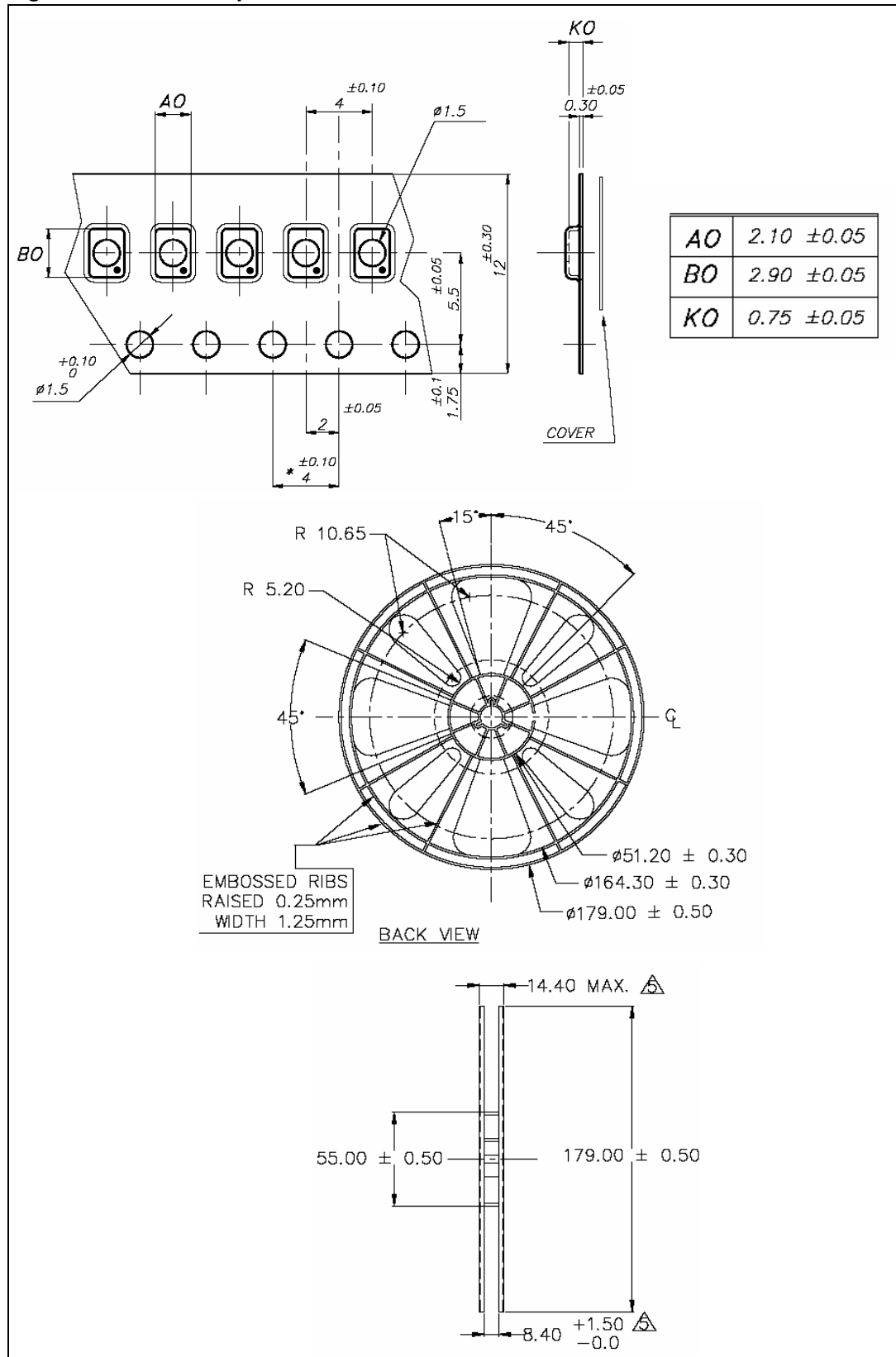


Figure 10. QFN16L tape and reel information (continued)

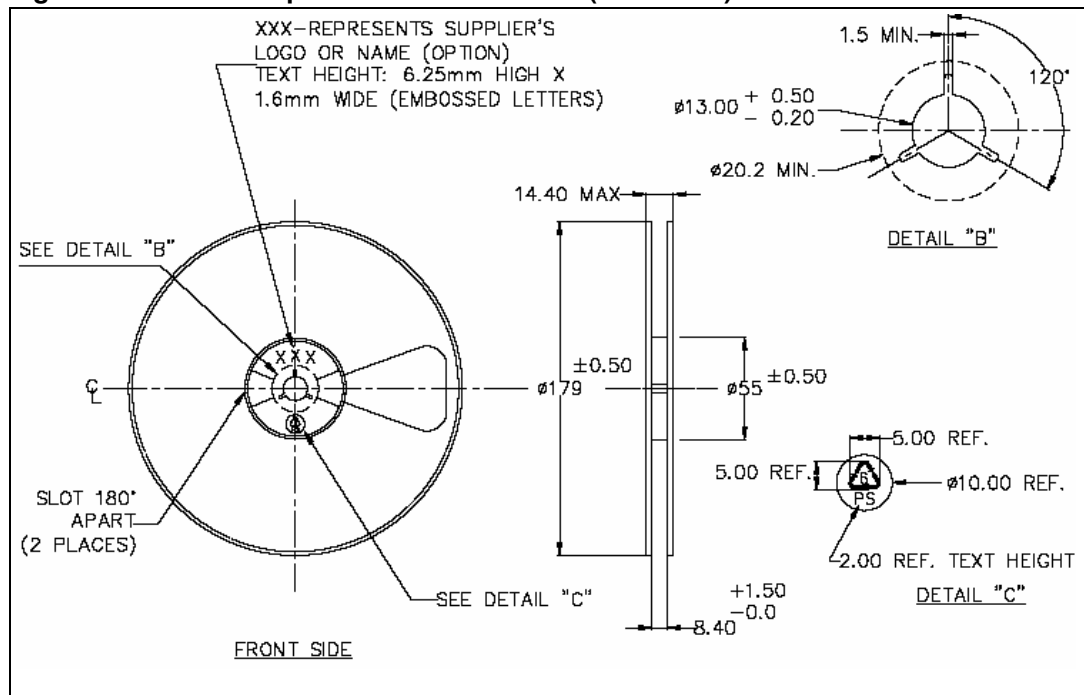
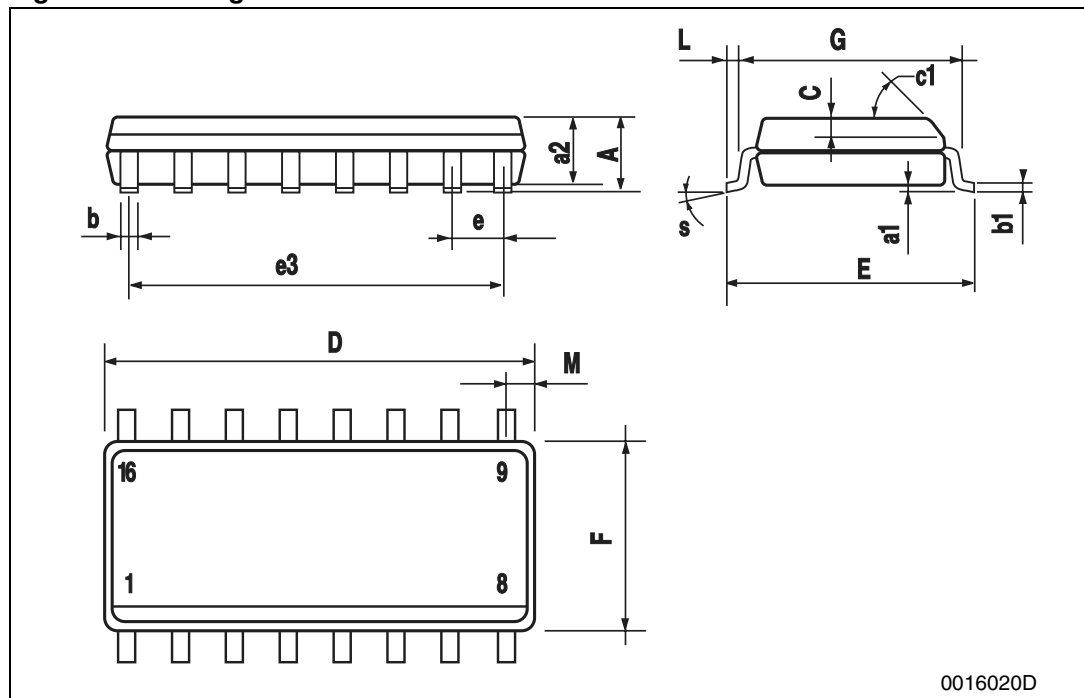


Table 18. SO-16 mechanical data

| Dim. | mm.        |      |      | inch  |       |       |
|------|------------|------|------|-------|-------|-------|
|      | Min.       | Typ  | Max. | Min.  | Typ.  | Max.  |
| A    |            |      | 1.75 |       |       | 0.068 |
| a1   | 0.1        |      | 0.25 | 0.004 |       | 0.010 |
| a2   |            |      | 1.64 |       |       | 0.063 |
| b    | 0.35       |      | 0.46 | 0.013 |       | 0.018 |
| b1   | 0.19       |      | 0.25 | 0.007 |       | 0.010 |
| C    |            | 0.5  |      |       | 0.019 |       |
| c1   | 45° (typ.) |      |      |       |       |       |
| D    | 9.8        |      | 10   | 0.385 |       | 0.393 |
| E    | 5.8        |      | 6.2  | 0.228 |       | 0.244 |
| e    |            | 1.27 |      |       | 0.050 |       |
| e3   |            | 8.89 |      |       | 0.350 |       |
| F    | 3.8        |      | 4.0  | 0.149 |       | 0.157 |
| G    | 4.6        |      | 5.3  | 0.181 |       | 0.208 |
| L    | 0.5        |      | 1.27 | 0.019 |       | 0.050 |
| M    |            |      | 0.62 |       |       | 0.024 |
| S    | 8° (max.)  |      |      |       |       |       |

Figure 11. Package dimensions



## 10 Revision history

**Table 19. Revision history**

| <b>Date</b> | <b>Revision</b> | <b>Changes</b>   |
|-------------|-----------------|--|
| 07-Dec-2006 | 1               | Initial release  |
| 22-Jan-2007 | 2               | Added Marking and Reel information   |
| 27-Apr-2007 | 3               | Updated <a href="#">Chapter 8.4</a> and <a href="#">Chapter 8.5 on page 18</a> |
| 02-Jul-2007 | 4               | Coverpage QFN package drawing updated  |

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