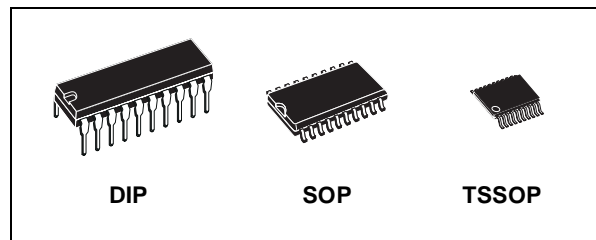




M74HCT373

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT NON INVERTING

- HIGH SPEED:
 $t_{PD} = 19\text{ns}$ (TYP.) at $V_{CC} = 4.5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}$ (MAX.) at $T_A=25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS :
 $V_{IH} = 2\text{V}$ (MIN.) $V_{IL} = 0.8\text{V}$ (MAX)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 6\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 373



ORDER CODES

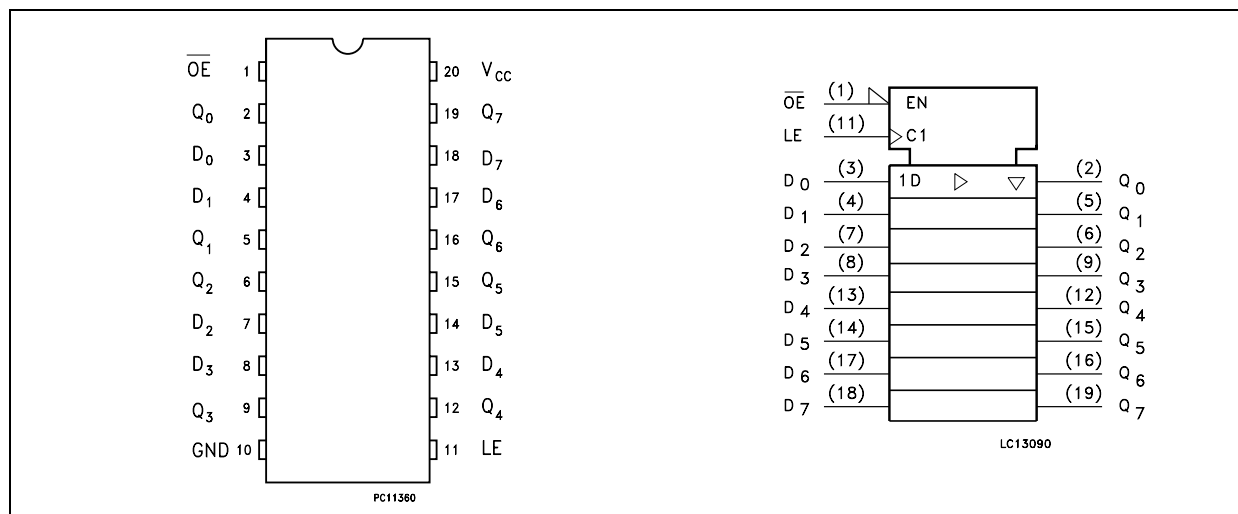
| PACKAGE | TUBE | T & R |
|---------|--------------|-----------------|
| DIP | M74HCT373B1R | |
| SOP | M74HCT373M1R | M74HCT373RM13TR |
| TSSOP | | M74HCT373TTR |

DESCRIPTION

The M74HCT373 is an high speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with sub-micron silicon gate C²MOS technology. This 8-BIT D-Type latches is controlled by a latch enable input (LE) and output enable input (\overline{OE}). While the LE input is held at a high level, the Q outputs will follow the data input. When the LE is taken low, the Q outputs will be latched at the logic level of D input data. While the \overline{OE} input is at low level, the eight outputs will be in a normal logic state (high or low logic

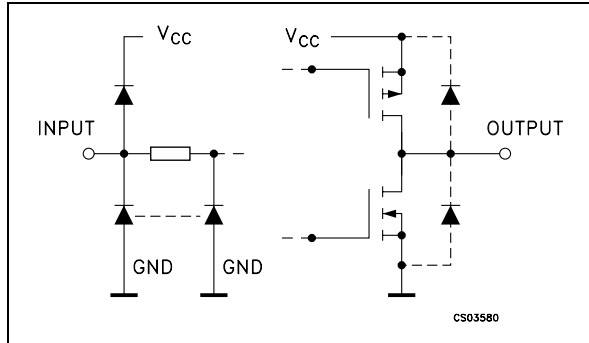
level) and when \overline{OE} is in high level the outputs will be in a high impedance state. The 3-State output configuration and the wide choice of outline make bus organized system simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



M74HCT373

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

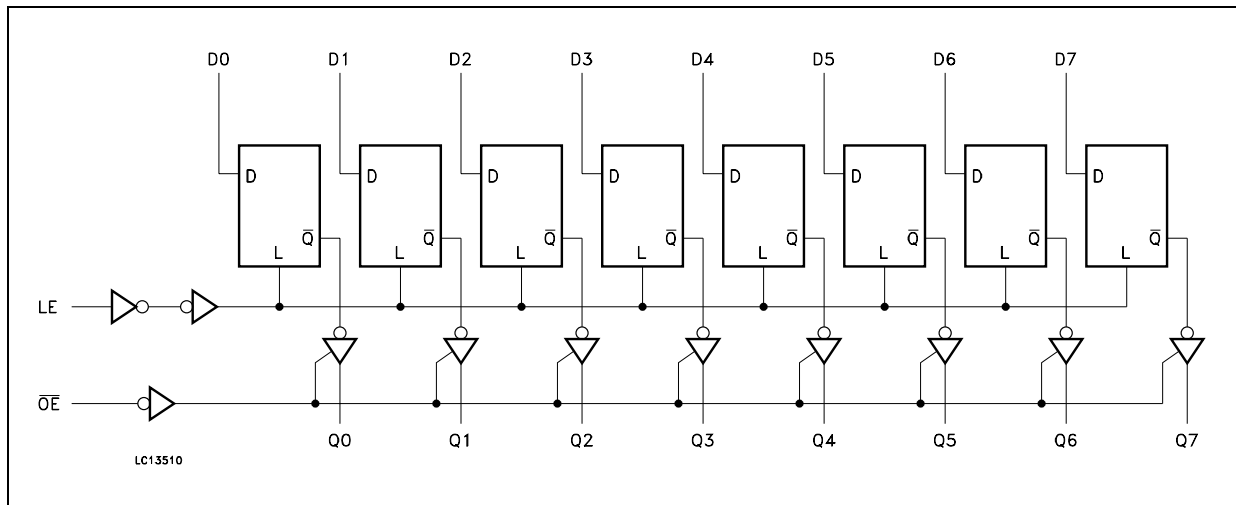
| PIN No | SYMBOL | NAME AND FUNCTION |
|----------------------------|-----------------|--|
| 1 | \overline{OE} | 3 State Output Enable Input (Active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0 to Q7 | 3 State Outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0 to D7 | Data Inputs |
| 11 | LE | Latch Enable Input |
| 10 | GND | Ground (0V) |
| 20 | V _{CC} | Positive Supply Voltage |

TRUTH TABLE

| INPUTS | | | OUTPUTS |
|-----------------|----|---|---------------|
| \overline{OE} | LE | D | Q |
| H | X | X | Z |
| L | L | X | NO CHANGE (*) |
| L | H | L | L |
| L | H | H | H |

X: Don't Care
 Z: High Impedance
 (*): Q Outputs are latched at the time when the LE input is taken low logic level.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|-------------------------------|------------------------|------|
| V_{CC} | Supply Voltage | -0.5 to +7 | V |
| V_I | DC Input Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| V_O | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | ± 20 | mA |
| I_{OK} | DC Output Diode Current | ± 20 | mA |
| I_O | DC Output Current | ± 35 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current | ± 70 | mA |
| P_D | Power Dissipation | 500(*) | mW |
| T_{stg} | Storage Temperature | -65 to +150 | °C |
| T_L | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|------------|---|---------------|------|
| V_{CC} | Supply Voltage | 4.5 to 5.5 | V |
| V_I | Input Voltage | 0 to V_{CC} | V |
| V_O | Output Voltage | 0 to V_{CC} | V |
| T_{op} | Operating Temperature | -55 to 125 | °C |
| t_r, t_f | Input Rise and Fall Time ($V_{CC} = 4.5$ to $5.5V$) | 0 to 500 | ns |

DC SPECIFICATIONS

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|-------------------|---------------------------------------|------------------------|---|-----------------------|------|-------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V _{IH} | High Level Input Voltage | 4.5 to 5.5 | | 2.0 | | | 2.0 | | 2.0 | | V |
| V _{IL} | Low Level Input Voltage | 4.5 to 5.5 | | | | 0.8 | | 0.8 | | 0.8 | V |
| V _{OH} | High Level Output Voltage | 4.5 | I _O = -20 μA | 4.4 | 4.5 | | 4.4 | | 4.4 | | V |
| | | | I _O = -6.0 mA | 4.18 | 4.31 | | 4.13 | | 4.10 | | |
| V _{OL} | Low Level Output Voltage | 4.5 | I _O = 20 μA | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | | I _O = 6.0 mA | | 0.17 | 0.26 | | 0.33 | | 0.40 | |
| I _I | Input Leakage Current | 5.5 | V _I = V _{CC} or GND | | | ± 0.1 | | ± 1 | | ± 1 | μA |
| I _{OZ} | High Impedance Output Leakage Current | 5.5 | V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND | | | ± 0.5 | | ± 5 | | ± 10 | μA |
| I _{CC} | Quiescent Supply Current | 5.5 | V _I = V _{CC} or GND | | | 4 | | 40 | | 80 | μA |
| Δ I _{CC} | Additional Worst Case Supply Current | 5.5 | Per Input pin V _I = 0.5V or V _I = 2.4V Other Inputs at V _{CC} or GND I _O = 0 | | | 2.0 | | 2.9 | | 3.0 | mA |

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

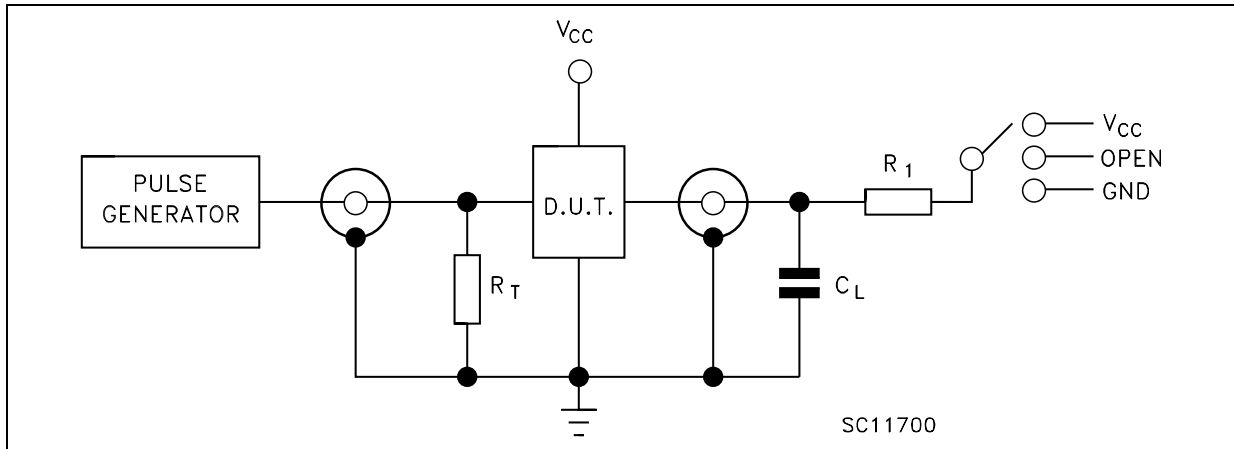
| Symbol | Parameter | Test Condition | | | Value | | | | | | Unit | |
|---------------------|------------------------------------|-----------------|---------------|--------------------------|--------------------------|------|------|-----------------------------|------|------------------------------|------|------|
| | | V_{CC} (V) | C_L (pF) | | $T_A = 25^\circ\text{C}$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| t_{TLH} t_{THL} | Output Transition Time | 4.5 | 50 | | | 7 | 12 | | 15 | | 18 | ns |
| t_{PLH} t_{PHL} | Propagation Delay Time (LE - Q) | 4.5 | 50 | | | 20 | 30 | | 38 | | 45 | ns |
| | | | 150 | | | 24 | 37 | | 46 | | 56 | |
| t_{PLH} t_{PHL} | Propagation Delay Time (D - Q) | 4.5 | 50 | | | 19 | 30 | | 38 | | 45 | ns |
| | | | 150 | | | 23 | 36 | | 45 | | 54 | |
| t_{PZL} t_{PZH} | High Impedance Output Enable Time | 4.5 | 50 | $R_L = 1\text{ K}\Omega$ | | 20 | 30 | | 38 | | 45 | ns |
| | | | 150 | | | 24 | 37 | | 46 | | 56 | |
| t_{PLZ} t_{PHZ} | High Impedance Output Disable Time | 4.5 | 50 | $R_L = 1\text{ K}\Omega$ | | 20 | 30 | | 38 | | 45 | ns |
| $t_{W(H)}$ | Minimum Pulse Width (LE) | 4.5 | 50 | | | 8 | 15 | | 19 | | 22 | ns |
| t_s | Minimum Set-up Time | 4.5 | 50 | | | 4 | 10 | | 13 | | 15 | ns |
| t_h | Minimum Hold Time | 4.5 | 50 | | | | 5 | | 5 | | 8 | ns |

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|----------|--|-----------------|--|--------------------------|------|------|-----------------------------|------|------------------------------|------|------|
| | | V_{CC} (V) | | $T_A = 25^\circ\text{C}$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| C_{IN} | Input Capacitance | | | | 5 | 10 | | 10 | | 10 | pF |
| C_{PD} | Power Dissipation Capacitance (note 1) | | | | 66 | | | | | | pF |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per Flip Flop) and the C_{PD} when n pcs of Flip Flop operate, can be gained by the following equation: $C_{PD(TOTAL)} = 32 + 34 \times n$ (pF)

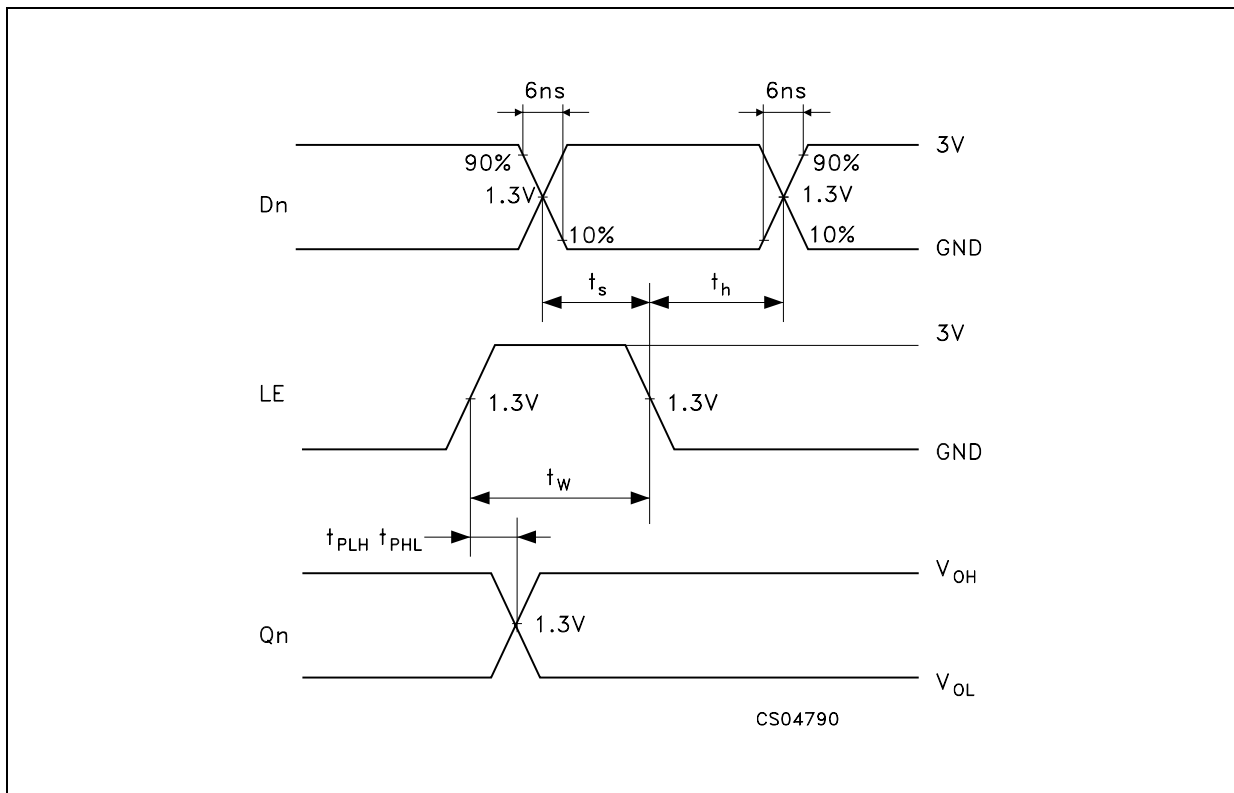
TEST CIRCUIT



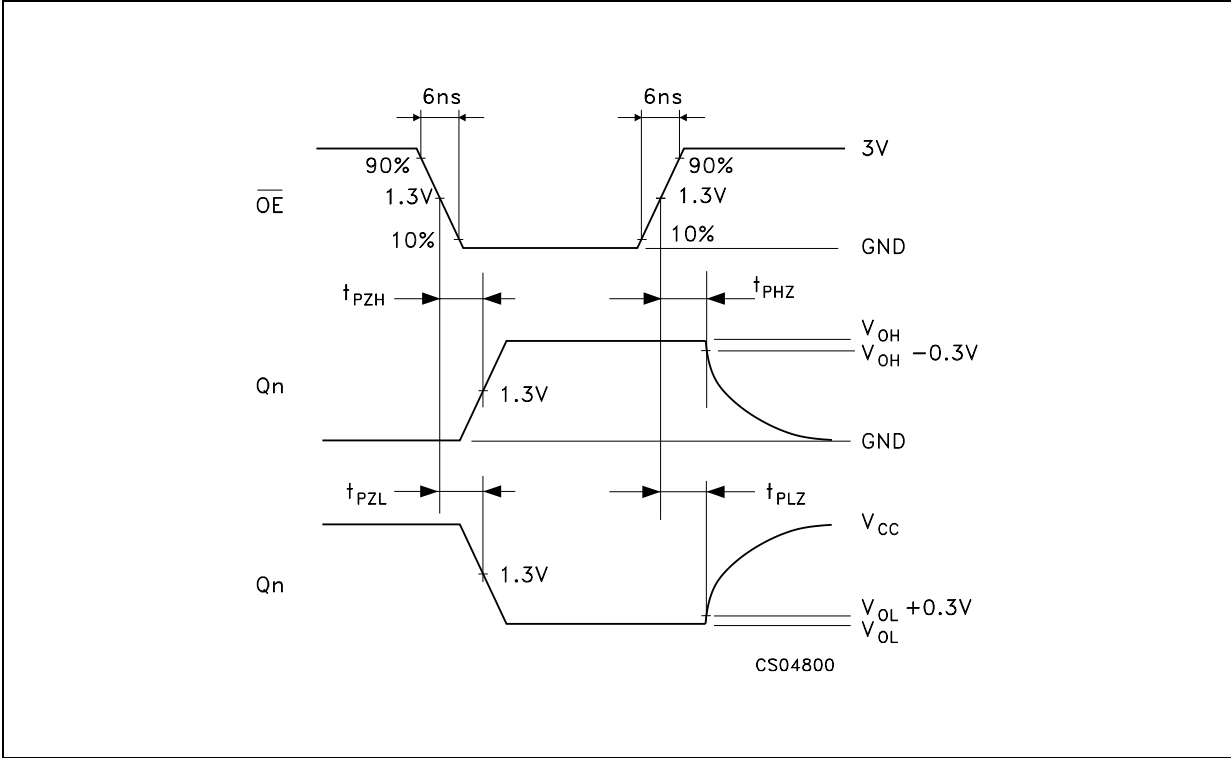
| TEST | SWITCH |
|-----------------------|----------|
| t_{PLH} , t_{PHL} | Open |
| t_{PZL} , t_{PLZ} | V_{CC} |
| t_{PZH} , t_{PHZ} | GND |

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
 R_1 = 1K Ω or equivalent
 R_T = Z_{OUT} of pulse generator (typically 50 Ω)

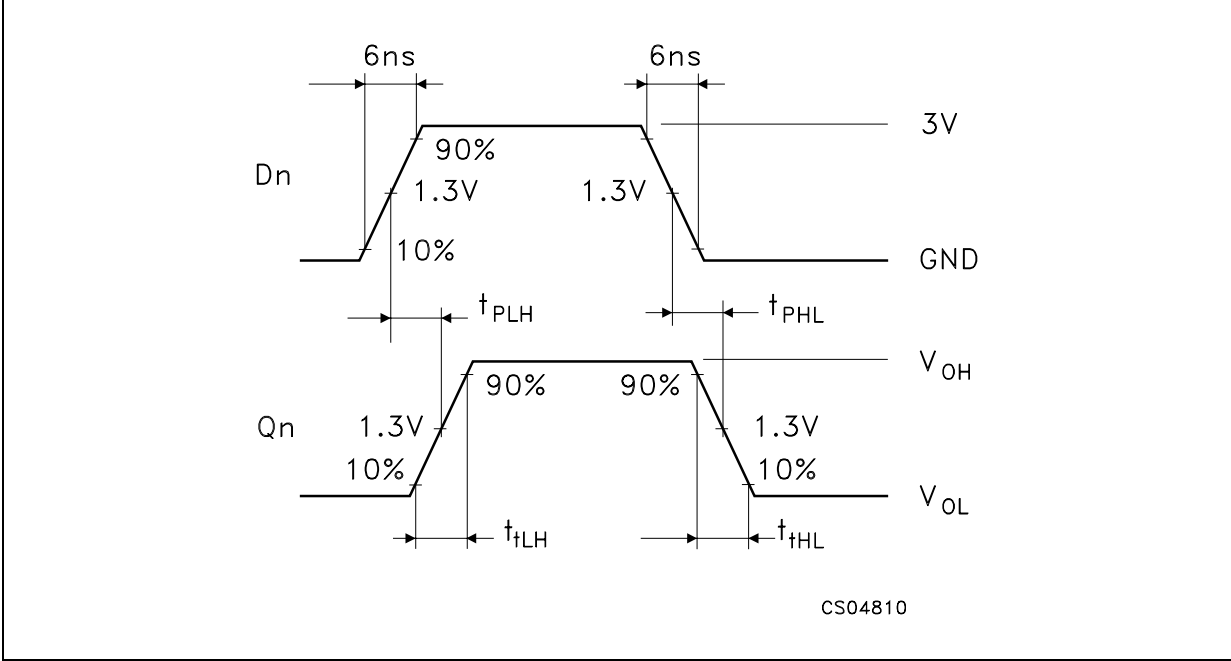
WAVEFORM 1: LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)

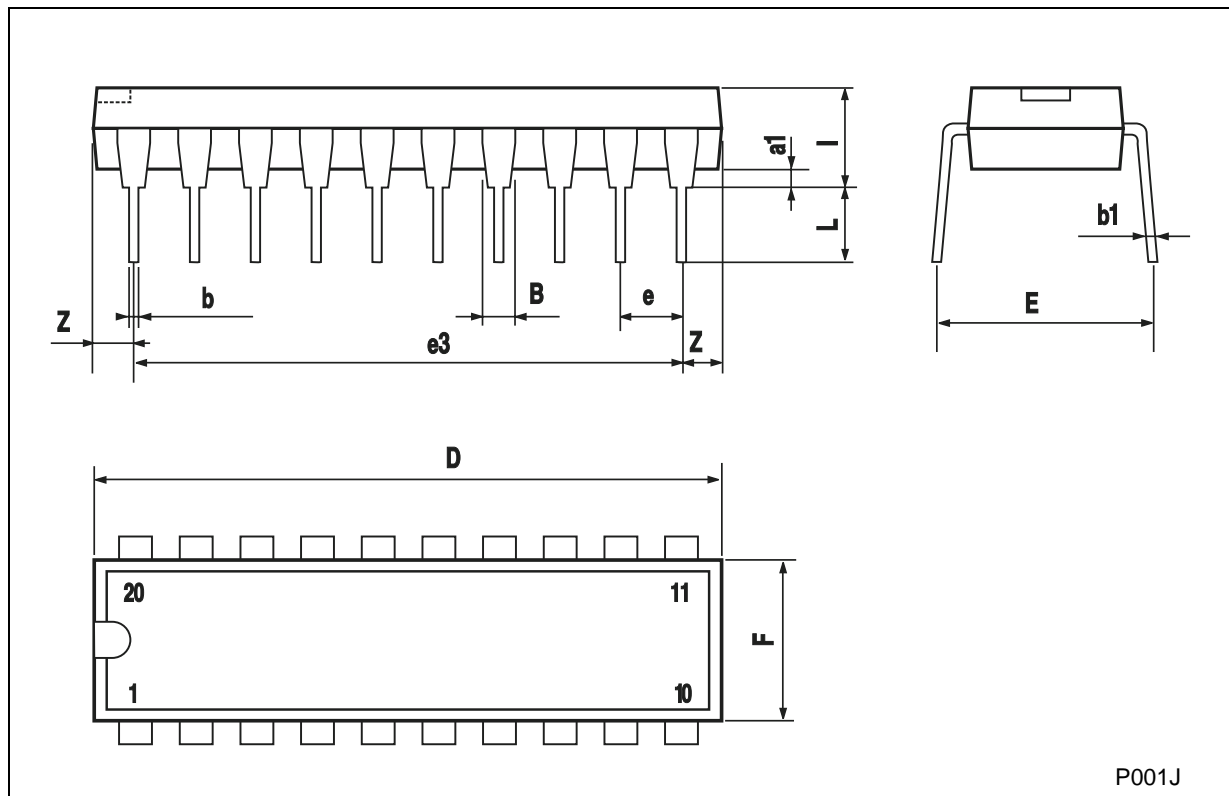


WAVEFORM 3: PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



Plastic DIP-20 (0.25) MECHANICAL DATA

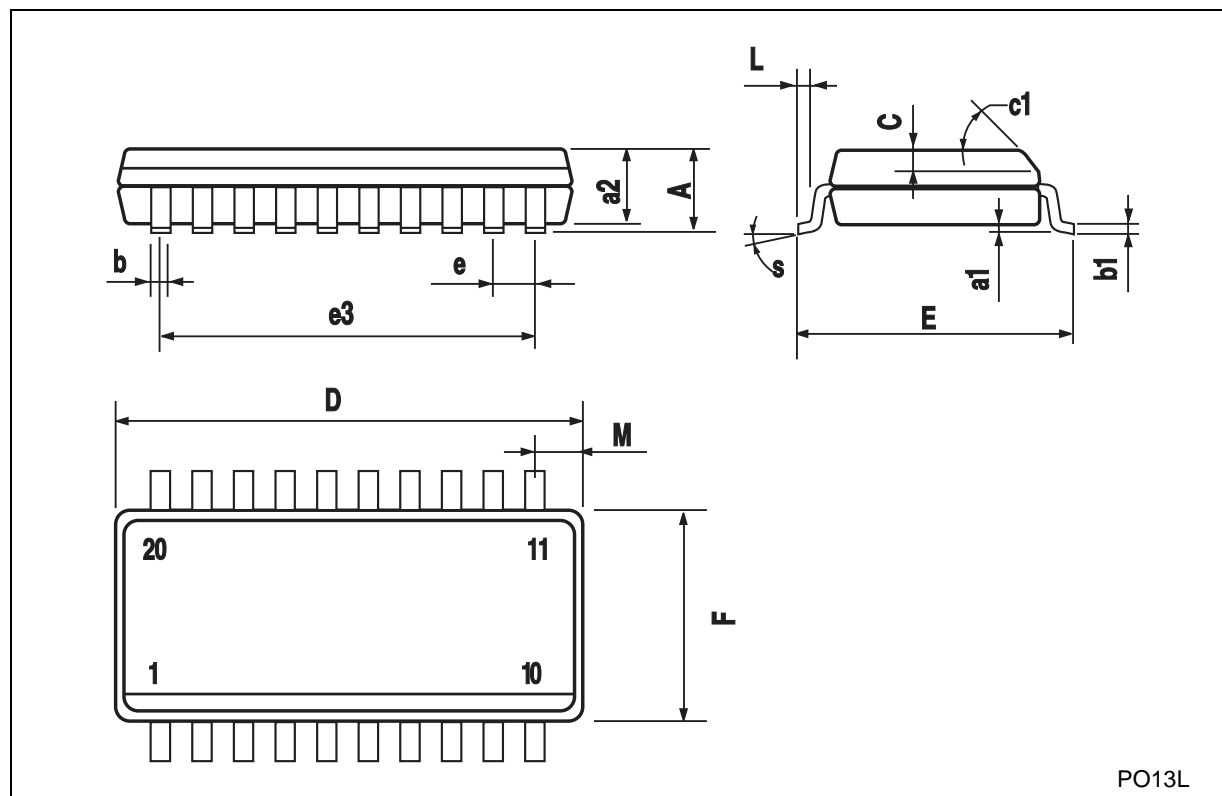
| DIM. | mm. | | | inch | | |
|------|-------|-------|------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.254 | | | 0.010 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.45 | | | 0.018 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 25.4 | | | 1.000 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 22.86 | | | 0.900 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 3.93 | | | 0.155 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.34 | | | 0.053 |



P001J

SO-20 MECHANICAL DATA

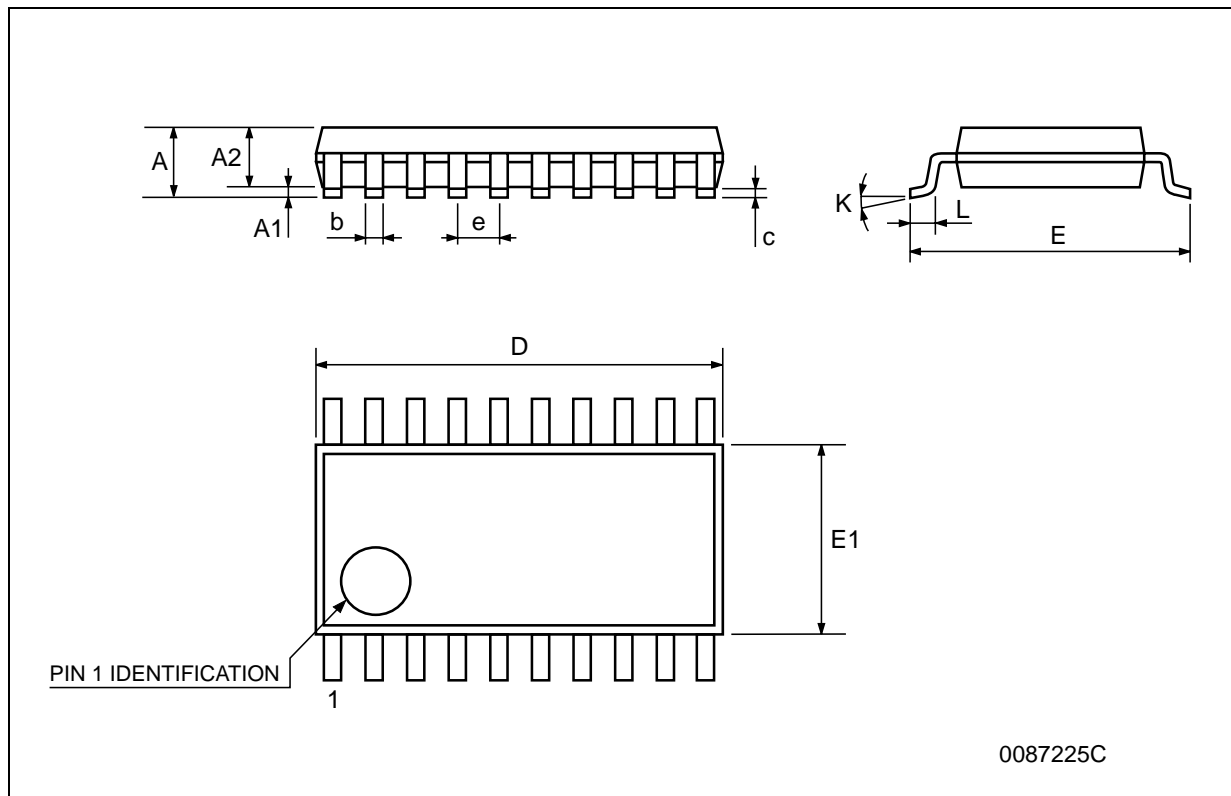
| DIM. | mm. | | | inch | | |
|------|------------|-------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 12.60 | | 13.00 | 0.496 | | 0.512 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 11.43 | | | 0.450 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.300 |
| L | 0.50 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8° (max.) | | | | | |



PO13L

TSSOP20 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|----------|------|-------|------------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 6.4 | 6.5 | 6.6 | 0.252 | 0.256 | 0.260 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



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