USBULC1606-4M8

Ultra low capacitance ESD protection for enhanced mini USB interface

Features

- Diode array topology
- D+/D- and ID lines protection with 6.8 V low voltage diodes (LV)
- V_{BUS} line protection with 14.6 V high voltage diodes (HV)
- Ultra low capacitance 0.5 pF on low voltage diodes
- 5 GHz bandwidth at -3 dB
- 1.35 mm width and 0.5 mm height package
- Lead-free package
- Low capacitance between lines to ground for optimized data integrity
- Low PCB space consumption: 2.3 mm² max foot print
- High bandwidth
- Low clamping voltage
- Easy layout
- CEA-936-A specification compliant

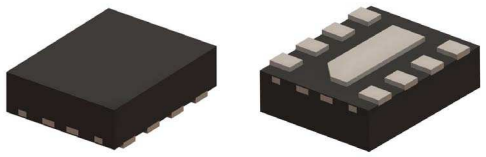
Complies with following standards

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

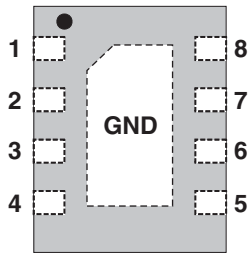
Where transient over-voltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment



Micro QFN-8L package

Figure 1. Pin configuration (top view)



Description

The USBULC1606-4M8 is an application specific discrete device dedicated to ESD protection of an enhanced Mini USB interface.

The device is ideal for applications where both reduced print circuit board space and power absorption capability are required.

1 Characteristics

Table 1. Absolute maximum ratings T_{amb} = 25 °C

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, level 4 Contact discharge HV diode Contact discharge LV diodes Air discharge all pins	 15 15 8	kV
V_{LVMAX}	DC Voltage on low-voltage pins	6.0	V
V_{HVMAX}	DC Voltage on high-voltage pin (V_{cc} pin)	14.5	V
I_{pp}	Peak pulse current (8/20 µs) on high voltage pin (V_{cc} pin)	2.5	A
P_{pp}	Peak pulse power dissipation (8/20 µs) on high voltage pin (V_{cc} pin)(1) $T_{j\ initial} = T_{amb}$	70	W
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-30 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Table 2. Electrical characteristics T_{amb} = 25 °C, otherwise specified

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{F1+}	LV Diode Reverse Voltage – Positive Voltage	I_F = 10 mA	6.8		9.2	V
V_{F1-}	LV Diode Forward Voltage – Negative Voltage	I_F = 10 mA	-1.05		-0.6	V
I_{RM1}	Low Voltage diode leakage current	V_{IN} = 3.3 V, V_N = 0 V T_a = -30 to + 65 °C			0.1	µA
Rd_1	Dynamic Resistance of LV Diode	I_{PP} = 1 A, tp = 8/20 µs		1.5		Ω
C_1	Low Voltage diode input capacitance	V_{IN} = 0 V, V_{osc} = 30 mV F = 1 MHz Any I/O pin to V_N		0.95	1.1	pF
		V_{IN} = 200 mV, V_{osc} = 200 mV F = 240 MHz Any I/O pin to V_N		0.5	0.55	
V_{CL1}	Low Voltage diode clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs Positive Transient Negative transient		10 -2.4		V
V_{CL2}	High Voltage diode clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs I_{PP} = 2.5 A, t_p = 8/20 µs			21 28	V
V_{F2+}	HV Diode Reverse Voltage – Positive Voltage	I_F = 10 mA	14.6		17.7	V

Table 2. Electrical characteristics T_{amb} = 25 °C, otherwise specified (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{F2-}	HV Diode Forward Voltage – Negative Voltage	I_F = 10 mA	-1.5		-0.4	V
I_{RM2}	High Voltage diode leakage current	V_{IN} = 11 V, DAP grounded		0.1	1.0	µA
Rd_2	Dynamic Resistance of HV Diode	I_{PP} = 1 A, t_p = 8/20 µs		2.8		Ω
C_2	High Voltage diode input capacitance	Exposed pad grounded, V_{IN} = 2.5 V, F = 1 MHz		10		pF

Figure 2. S21 attenuation measurement on high speed lines

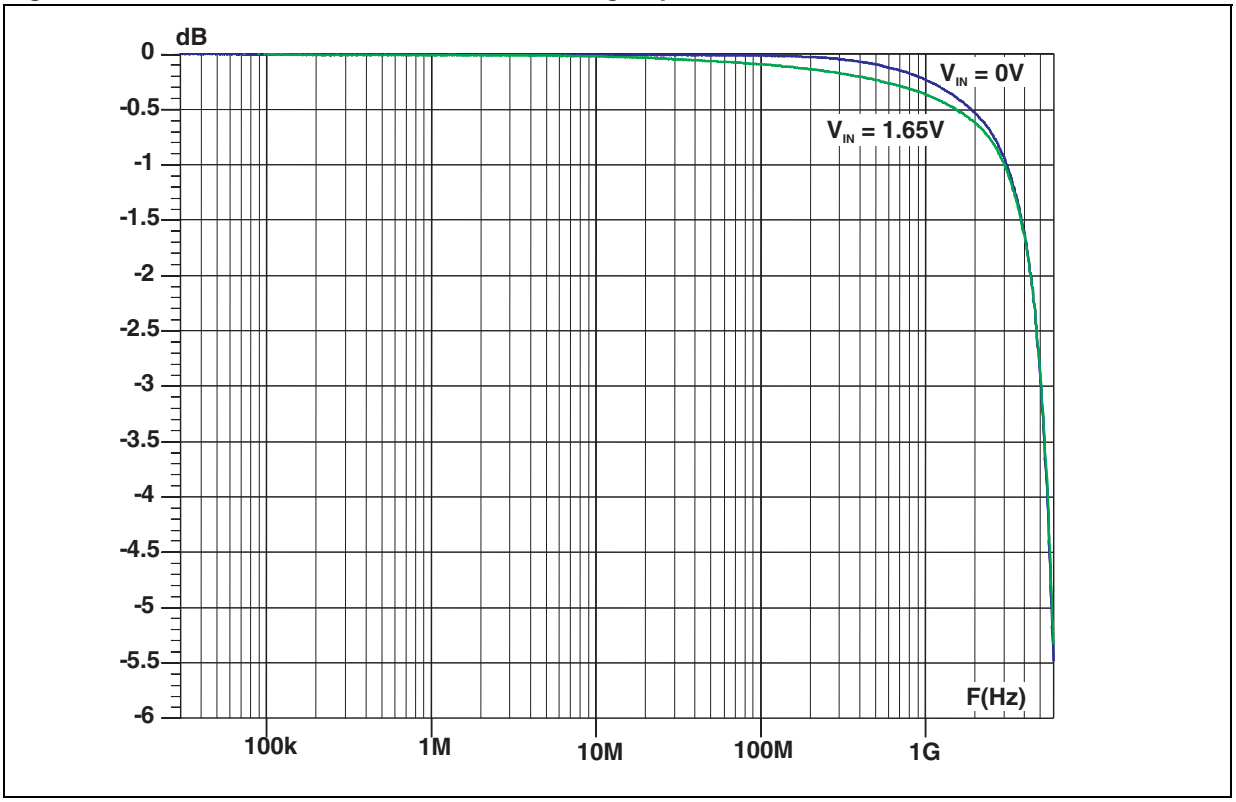


Figure 3. Electrical schematic

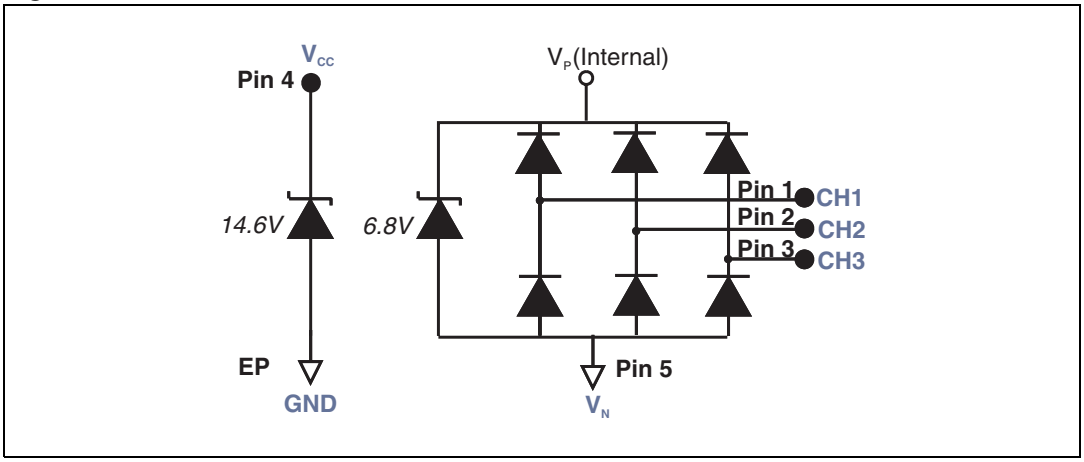


Figure 4. Typical application

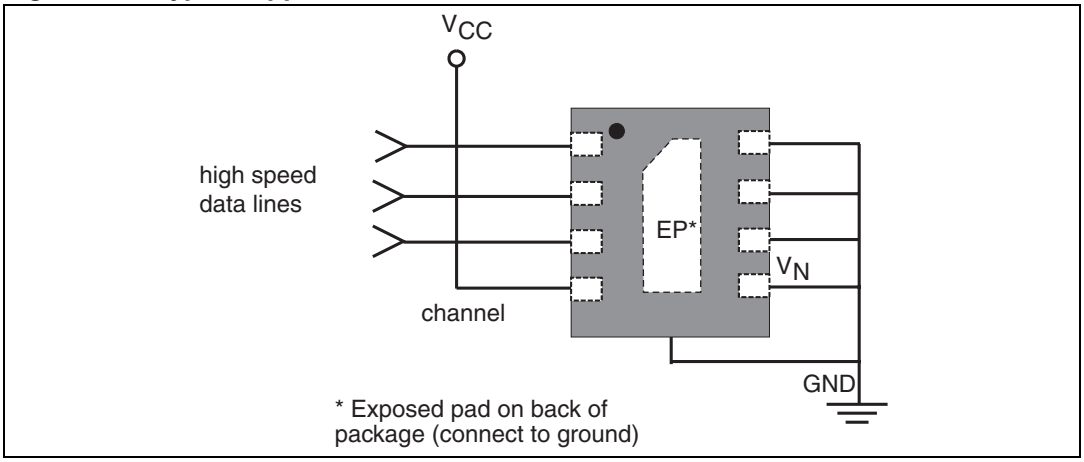


Table 3. Pin configuration typical application

Pin	Name	Type	Description
1	CH1	I/O	LV low-capacitance ESD channel
2	CH2	I/O	LV low-capacitance ESD channel
3	CH3	I/O	LV low-capacitance ESD channel
4	VCC	HV VDD	HV ESD Channel
5	VN		Negative voltage supply rail
6	NC		
7	NC		
8	NC		
EP	GND		Exposed pad

Figure 5. Low voltage diode capacitance vs. reverse voltage (typical value)

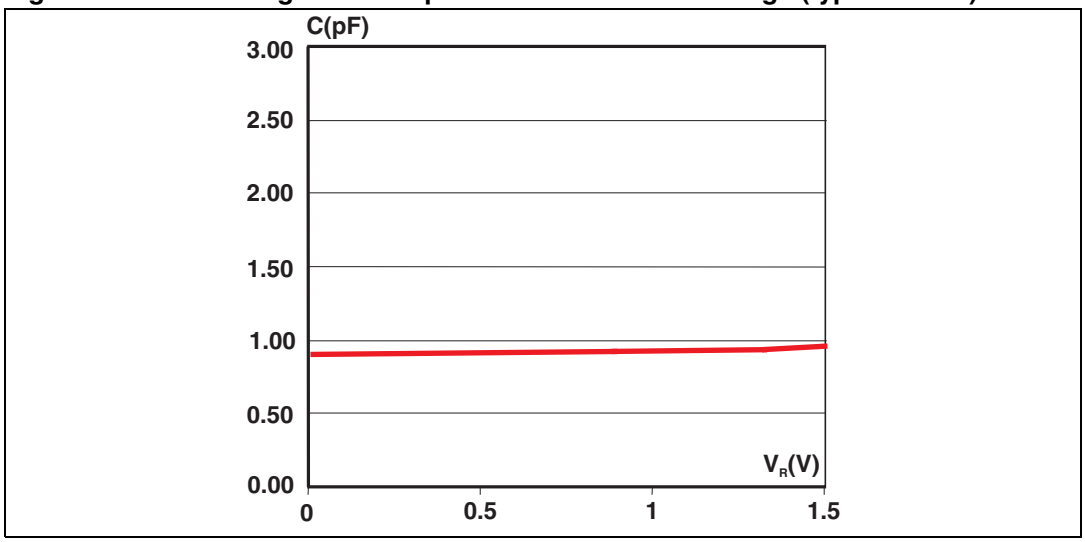


Figure 6. Low voltage diode capacitance versus frequency (typical value)

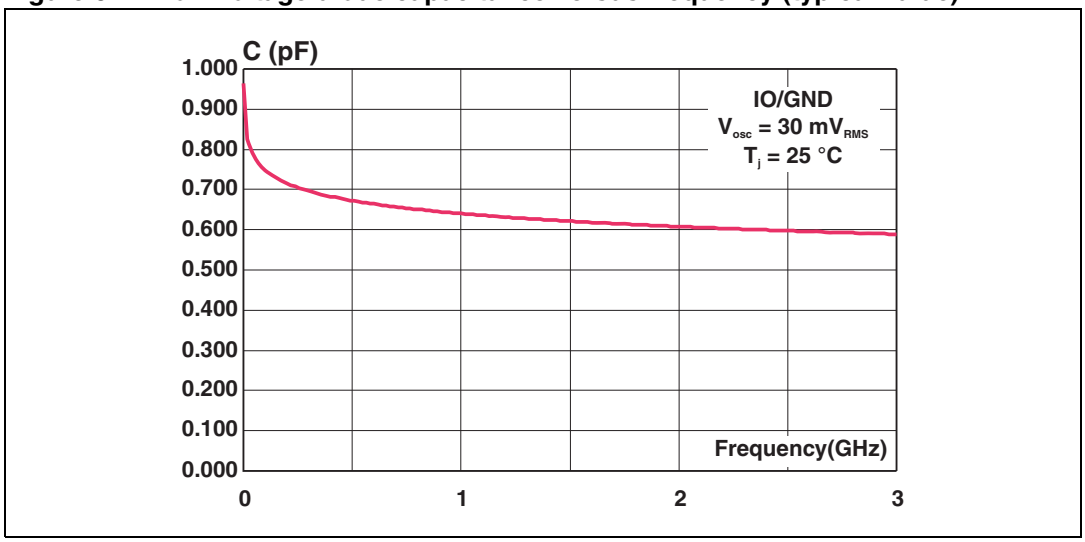


Figure 7. ESD response to IEC 61000-4-2 (+15 kV air discharge) on high speed lines

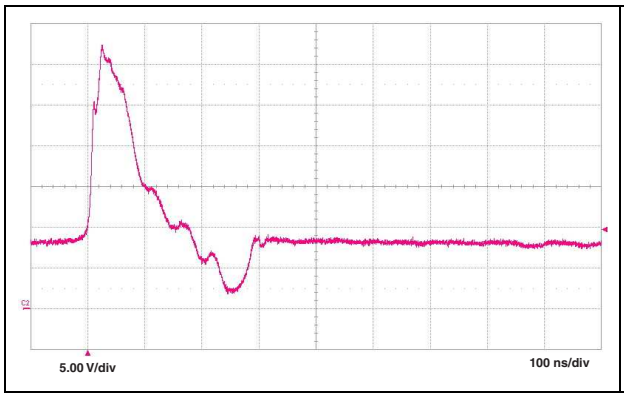


Figure 8. ESD response to IEC 61000-4-2 (-15 kV air discharge) on high speed lines

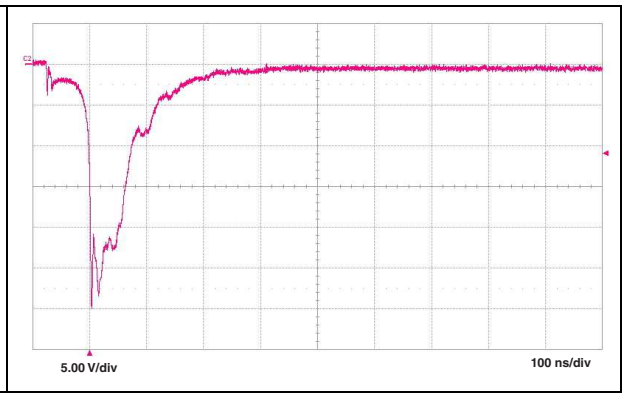


Figure 9. ESD response to IEC 61000-4-2 (+15 kV air discharge) on Vcc

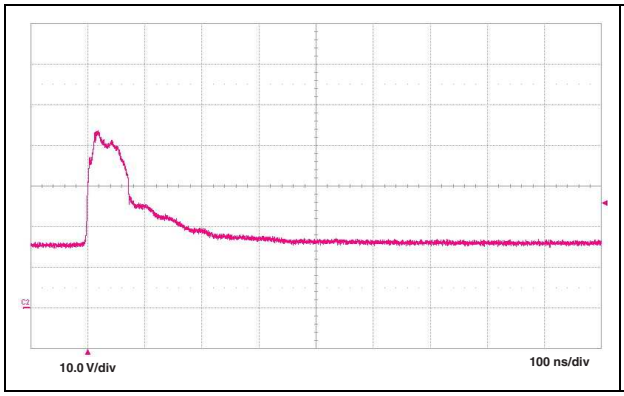


Figure 10. ESD response to IEC 61000-4-2 (-15 kV air discharge) on Vcc

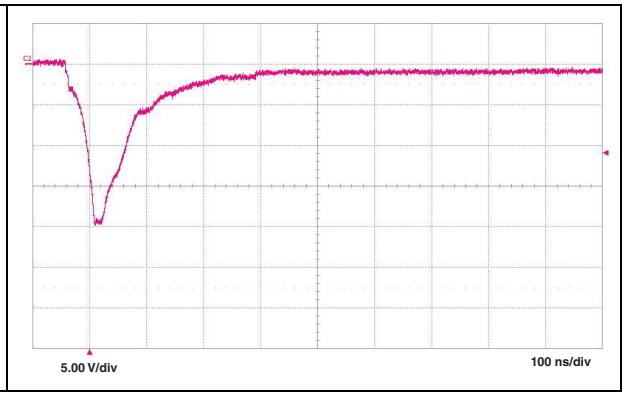


Figure 11. Relative variation of peak pulse power versus initial junction temperature

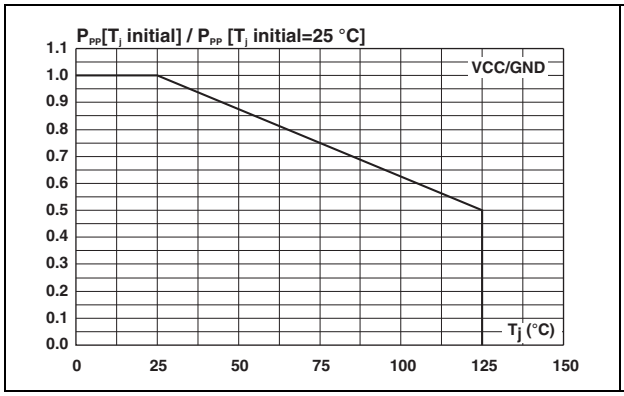


Figure 12. Peak pulse power versus exponential pulse duration (Typical values - V_{CC} pin)

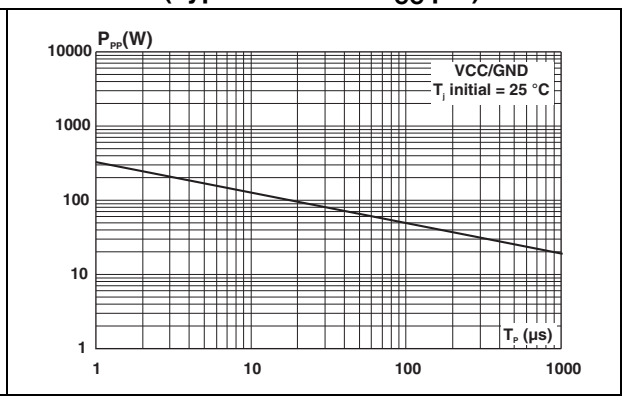


Figure 13. Clamping voltage versus peak pulse current (typical values - V_{CC} pin)

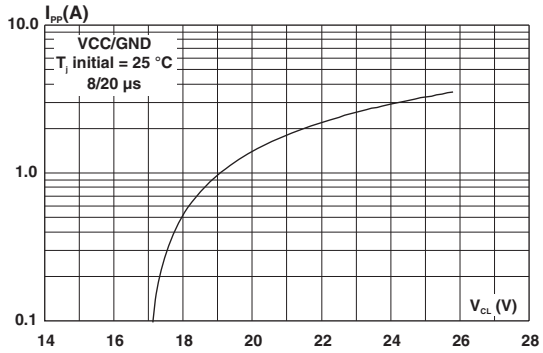


Figure 14. Forward voltage drop versus peak forward current (typical values - V_{CC} pin)

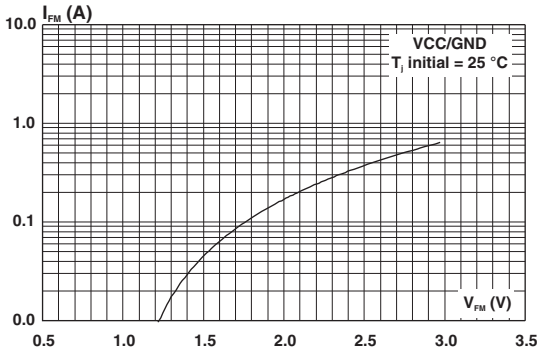


Figure 15. Relative variation of leakage current versus junction temperature (typical values -V_{CC} pin)

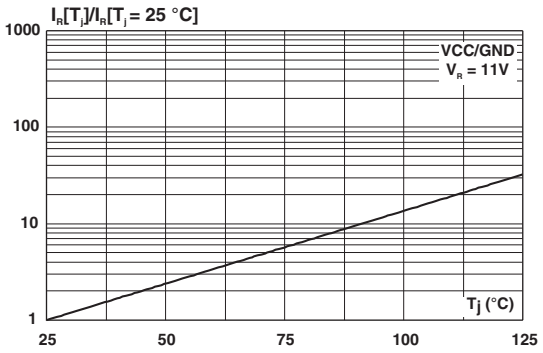


Figure 16. Eye diagram PCB only 400 mV amplitude, F = 480 Mbps

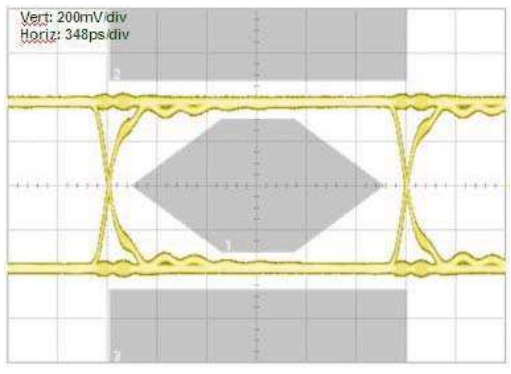
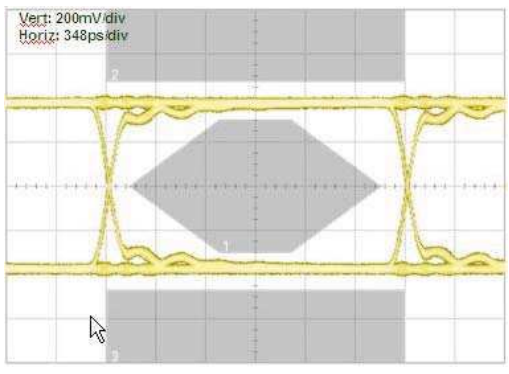
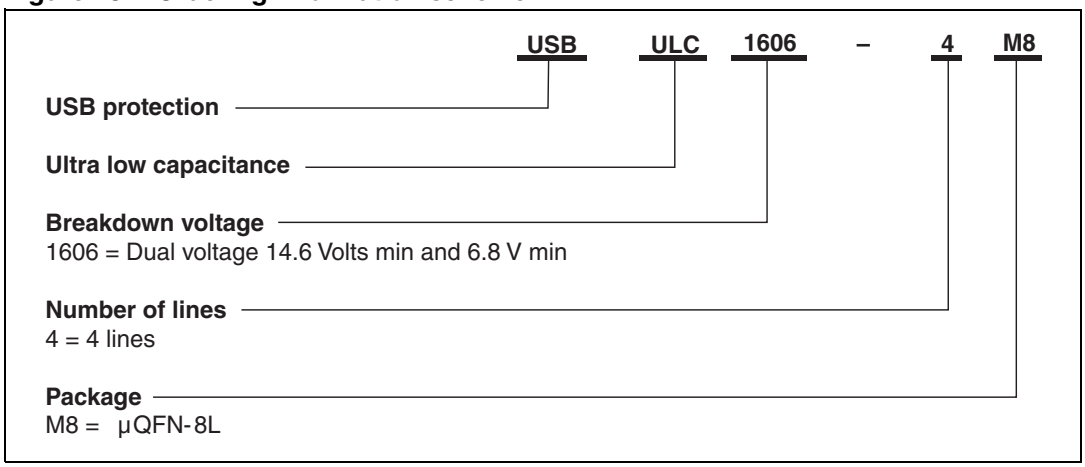


Figure 17. Eye diagram PCB + USBULC106-4M8 400 mV amplitude, F = 480 Mbps



2 Ordering information scheme

Figure 18. Ordering information scheme

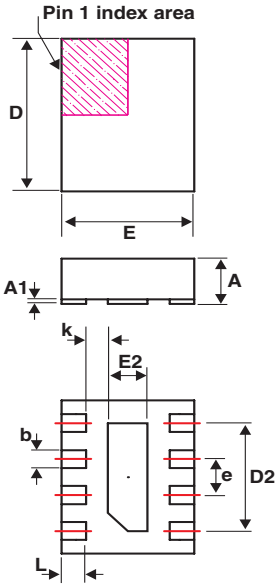


3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 4. Micro QFN 1.7 x 1.35 package dimensions



Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.025	0.05	0.00	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.60	1.7	1.80	0.063	0.067	0.071
D2	1.10	1.2	1.30	0.043	0.047	0.051
E	1.25	1.35	1.45	0.050	0.053	0.057
E2	0.30	0.40	0.50	0.012	0.016	0.020
e		0.40			0.016	
k	0.17			0.007		
L	0.15	0.25	0.35	0.006	0.010	0.014

Figure 19. Foot print recommendations (dimensions in mm)

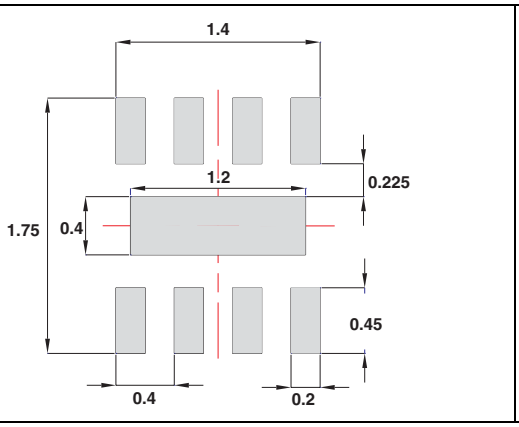


Figure 20. Marking

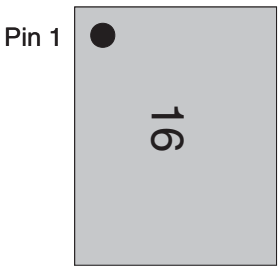
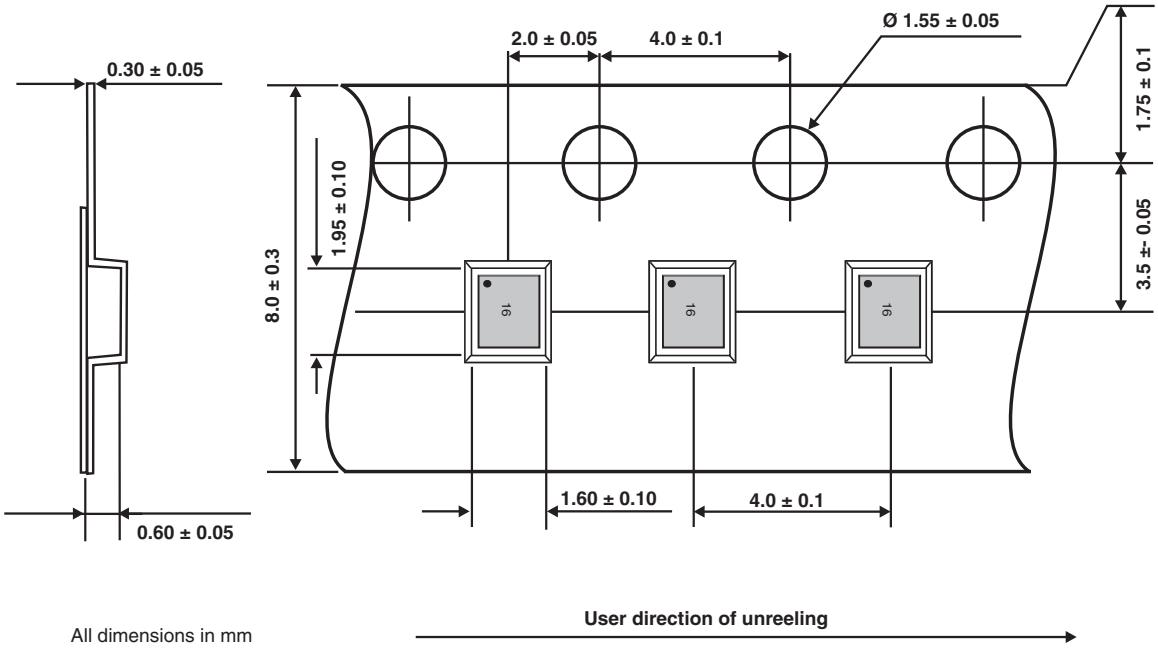


Figure 21. Micro QFN-8L tape and reel specifications



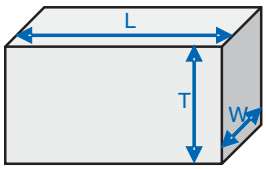
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 22. Stencil opening dimensions



   b) General design rule

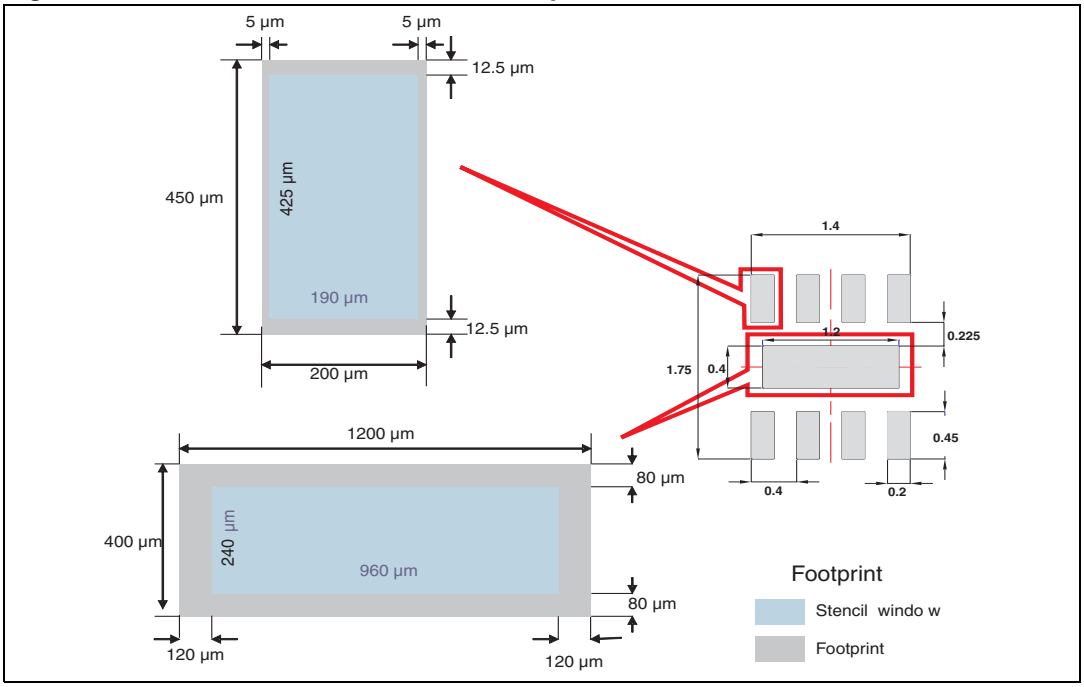
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 23. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

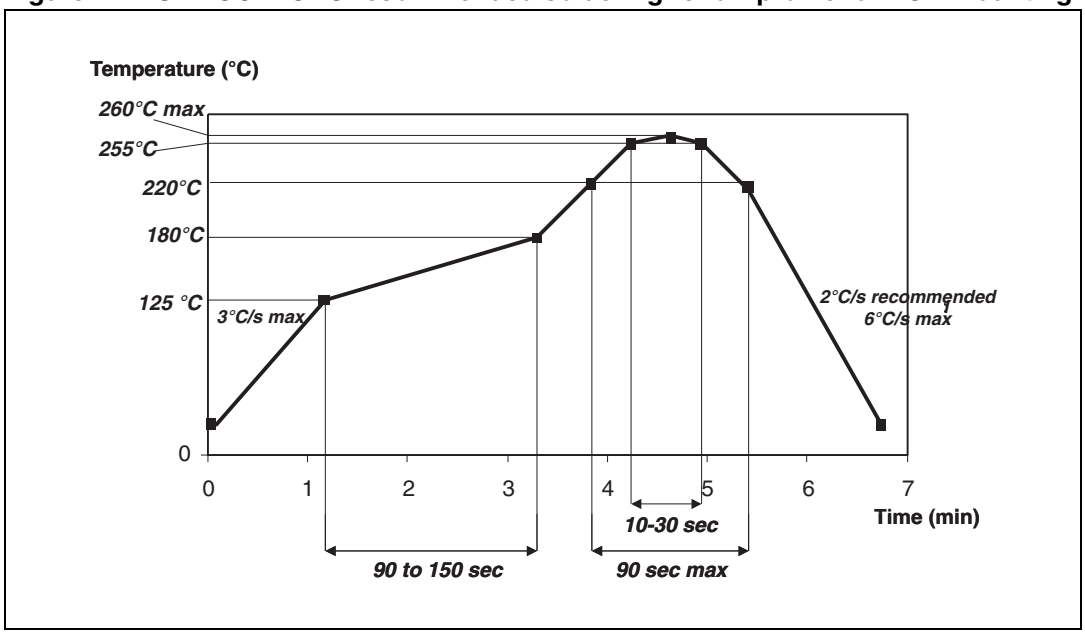
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 24. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBULC1606-4M8	16(1)	µQFN	3.43 mg	3000	Tape and reel (7”)

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
03-Dec-2009	1	Initial release.

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