LFTVS10-1F3

Transil™, transient voltage suppressor

Features

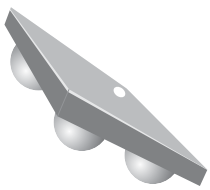
- Transient voltage suppressor
- Electrostatic discharge protection
- Electrical overstress protection
- Unidirectional device
- Low clamping factor V_{CL}/V_{BR}
- Fast response time
- Very thin package: 0.605 mm
- RoHS compliant

Complies with the following standards:

- IEC 61000-4-2 level 4
  - ± 15 kV (air discharge)
  - ± 8 kV (contact discharge)

Description

The LFTVS10-1F3 is a single line diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electronic devices subject to ESD and EOS transient overvoltages.



Flip Chip
(4 bumps)

Figure 1. Pin configuration (bump side)

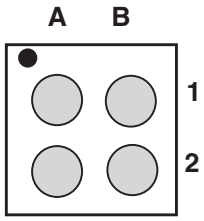
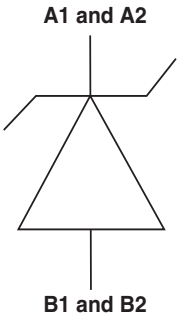


Figure 2. Device configuration



TM: Transil is a trademark of STMicroelectronics

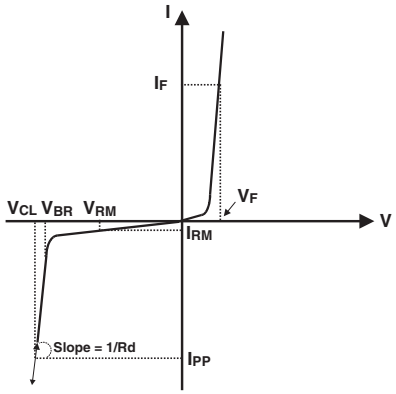
1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Test condition	Value	Unit
P_{PP}	Peak pulse power dissipation (10/1000 µs pulse)	T_j initial = T_{amb}	44	W
	Peak pulse power dissipation (8/20 µs pulse)		350	
I_{FSM}	Non repetitive surge peak forward current	t_p = 10 ms T_j initial = T_{amb}	11	A
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Maximum operating junction temperature		125	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 15 mA	10			V
I_{RM}	V_{RM} = 8 V			0.5	µA
V_{CL}	I_{PP} = 1 A(1)			13	V
V_F	I_F = 850 mA(2)			1.05	V
αT				8	10^{-4}/ °C
C_{line}	V_R = 0 V, V_{OSC} = 30 mV, F = 1 MHz		200		pF

1. 8 / 20 µs pulse waveform
2. DC current not recommended for more than 5 s. Even if diode failure mode is short circuit the bumps could exceed melting temperature and the component disassembled from the board.

Figure 3. Relative variation of peak pulse power versus initial junction temperature

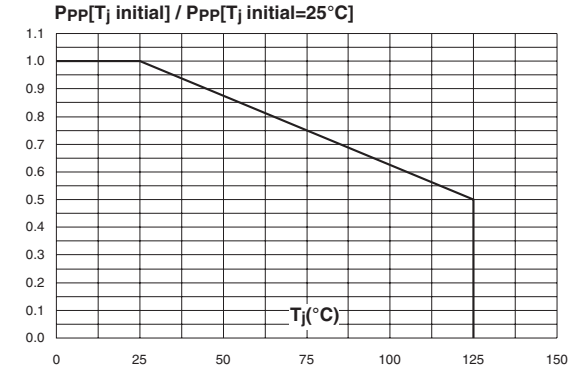


Figure 4. Peak pulse power versus exponential pulse duration (typical value)

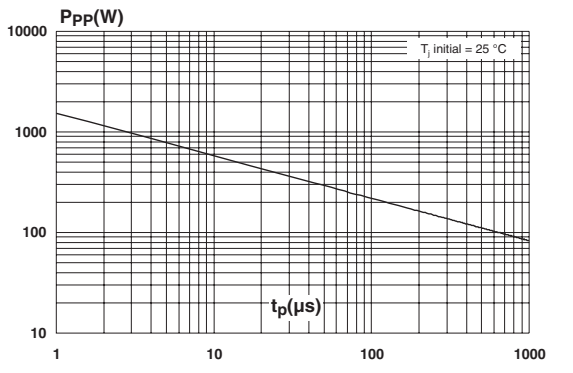


Figure 5. Clamping voltage versus peak pulse current (typical values)

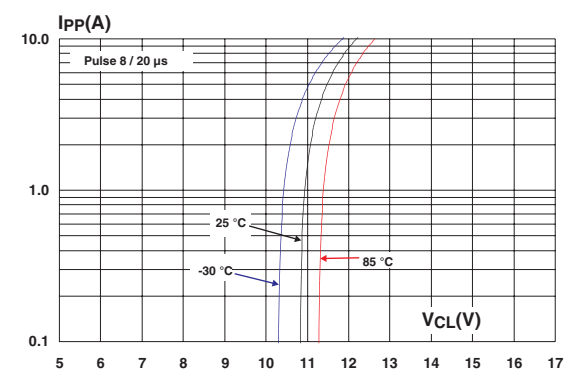


Figure 6. Relative variation of leakage current versus junction temperature (typical values)

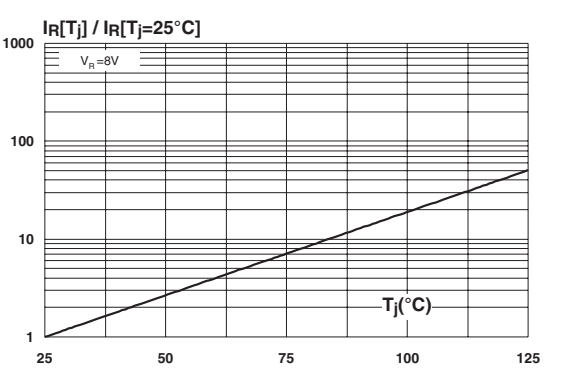


Figure 7. Forward voltage drop versus peak forward current (typical values)

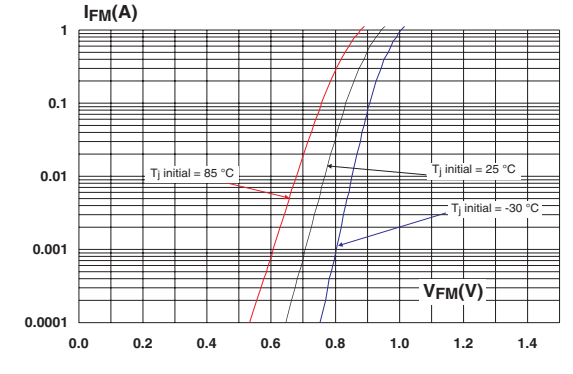


Figure 8. Junction capacitance versus line voltage (typical values)

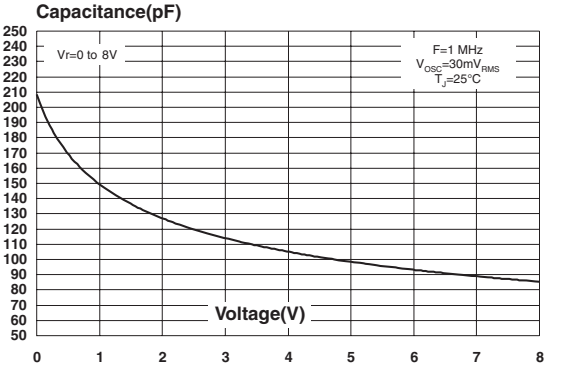
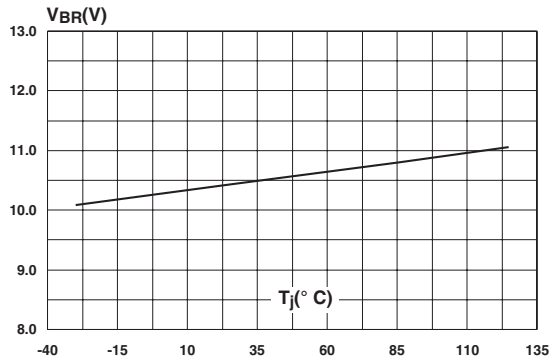
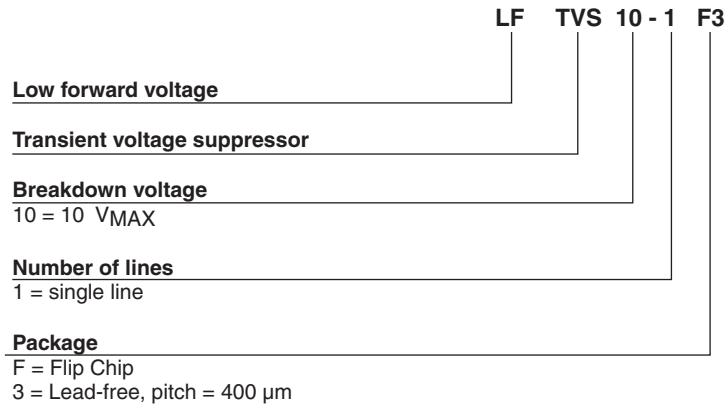


Figure 9. Breakdown voltage versus initial junction temperature (typical value)



2 Ordering information scheme

Figure 10. Ordering information scheme



3 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 11. Flip Chip dimensions

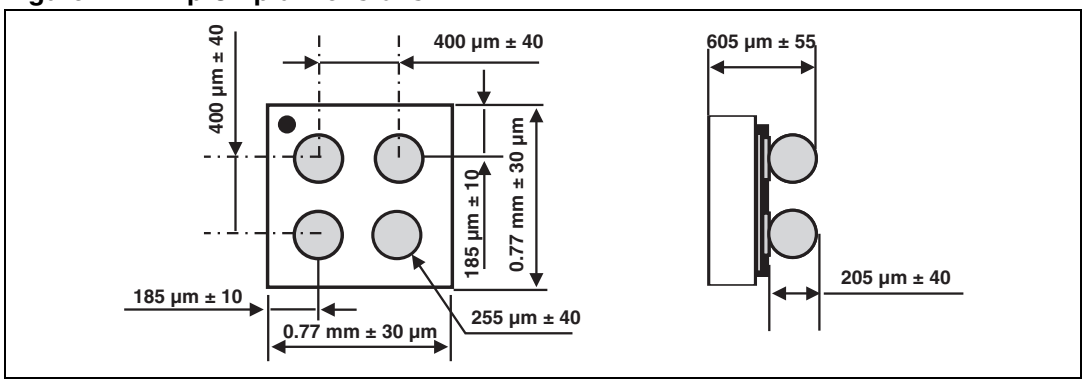


Figure 12. Footprint recommendations

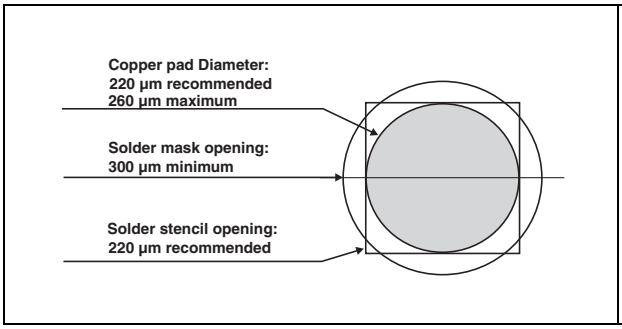


Figure 13. Marking

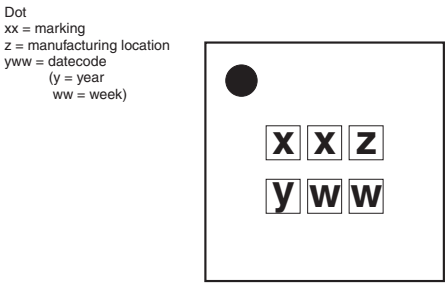
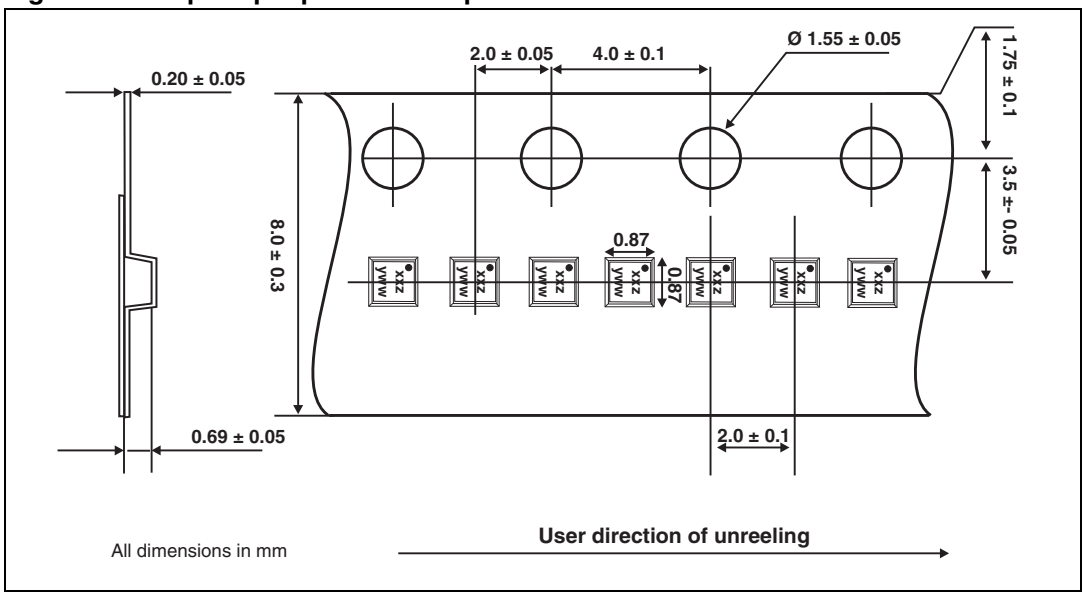


Figure 14. Flip Chip tape and reel specifications



Note: More information is available in the application notes:
AN2348: “400 µm flip chip: Package description and recommendations for use”
AN1751: "EMI Filters: Recommendations and measurements"

4 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
LFTVS10-1F3	EN	Flip Chip	0.86 mg	10 000	Tape and reel (7”)

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
21-Nov-2008	1	Initial release.

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