USBULC6-2F3

2-line IPAD™, ultra low capacitance protection for high speed USB

Features

- Ultra low diode capacitance (1.2 pF max)
- Two data lines (D+ and D-) protected against 15 kV ESD
- Breakdown voltage V_{BR} = 6.0 V min
- Flip Chip 400 µm pitch, lead-free
- Very low leakage current
- Very small PCB area
- RoHS compliant

Benefits

- Minimized impact on rise and fall times for maximum data integrity
- Low PCB space occupation
- Higher reliability offered by monolithic integration

Complies with the following standards

- IEC 61000-4-2 level 4 on external pins:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G - Method 3015.7
  - 25 kV (Human body model)

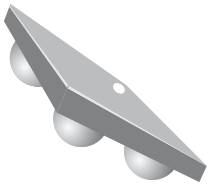
Application

This device is designed to protect high speed USB port in wireless handsets (up to 480 Mb/s according to USB 2.0 high speed specification).

Description

The USBULC6-2F3 is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces.

Its ultra low line capacitance secures a high level of signal integrity without compromizing the protection of downstream sensitive chips against the most stringently characterized ESD strikes.



Flip Chip
(4 bumps)

Figure 1. Pin layout (bump side)

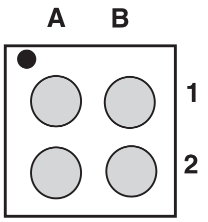
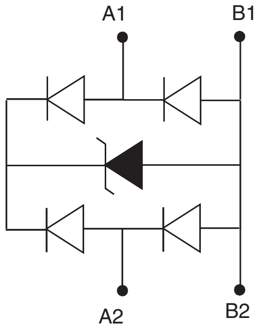


Figure 2. Device configuration



Note: B1 and B2 bumps must be grounded on the PCB together

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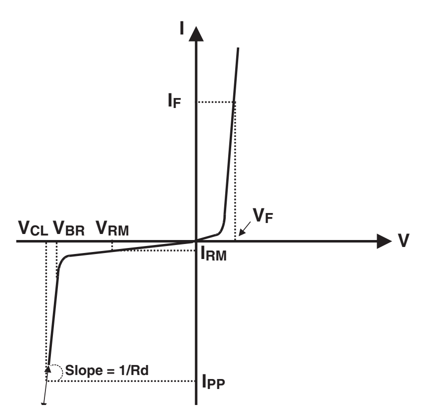
1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge	15 15	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)	60	W
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-30 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	
V_{BR}	Breakdown voltage	
I_{RM}	Leakage current @ V_{RM}	
V_{RM}	Stand-off voltage	
V_{CL}	Clamping voltage	
R_d	Dynamic impedance	
I_{PP}	Peak pulse current	
αT	Voltage temperature coefficient	
V_F	Forward voltage drop	

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	-	9	V
I_{RM}	V_{RM} = 3 V	-	-	100	nA
R_d	Exponential wave form 8/20 µs, I_{pp} = 1 to 5 A	-	1.6	-	Ω
αT	I_R = 1 mA	-	-	5	10^{-4}/ °C
C_{line}	V_{LINE} = 0 V, V_{OSC} = 30 mV, F = 1 MHz	-	-	1.2	pF

Figure 3. Eye diagram, board only (according to USB high speed specification)

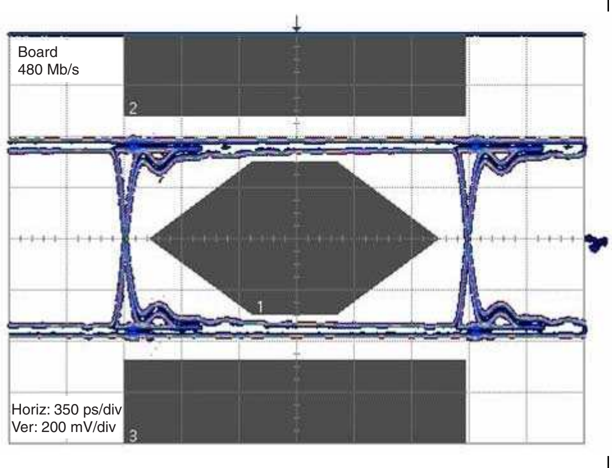


Figure 4. Eye diagram, board with USBULC6-2F3 (according to USB 2.0 high speed specification)

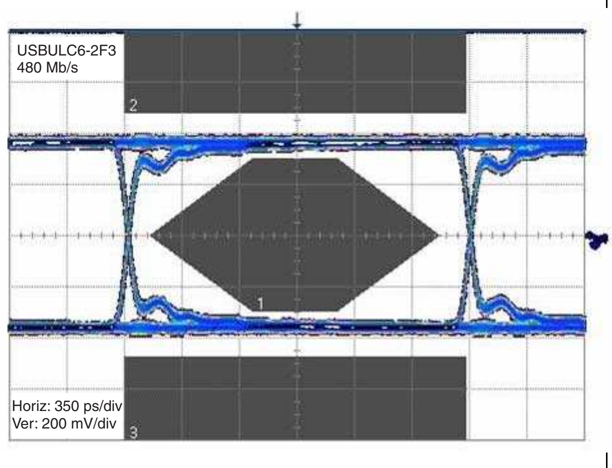


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge)

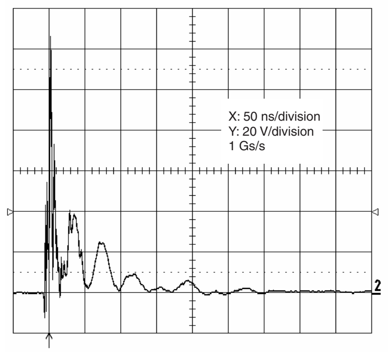


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge)

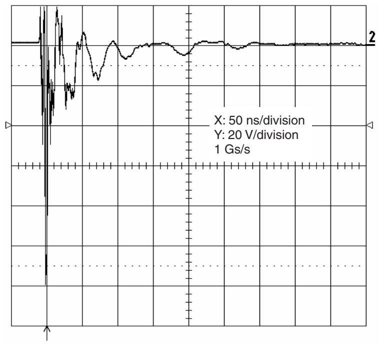


Figure 7. ESD response to IEC 61000-4-2 (+8 kV contact discharge)[1]

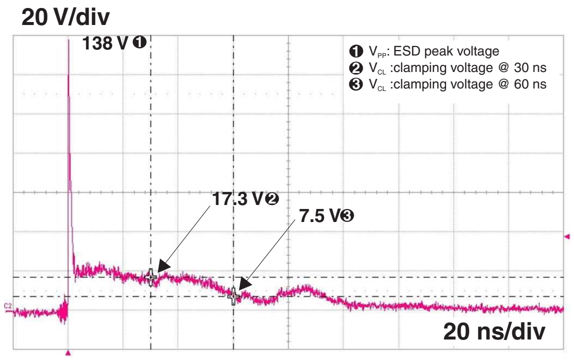
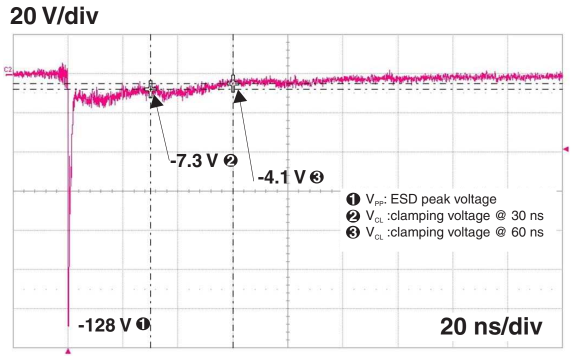


Figure 8. ESD response to IEC 61000-4-2 (-8 kV contact discharge)[1]



1. Test board connected to oscilloscope through 50 Ω cable and 20 dB + 6 dB attenuator. ESD generator return path connected to PCB ground plane.

Figure 9. Junction capacitance versus frequency (typical values)

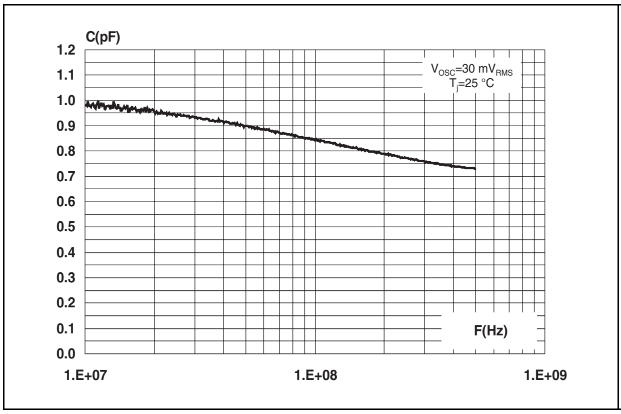


Figure 10. Analog crosstalk measurement

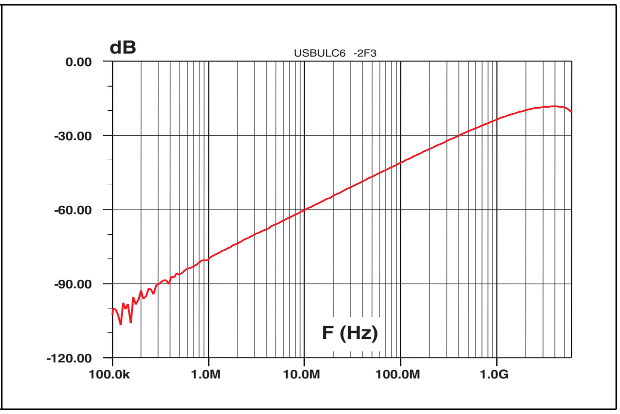


Figure 11. S21 (dB) attenuation measurement

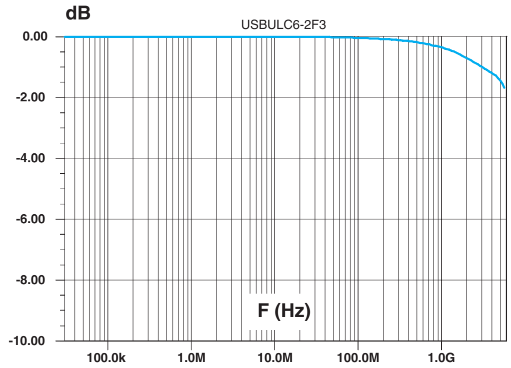


Figure 12. Digital crosstalk

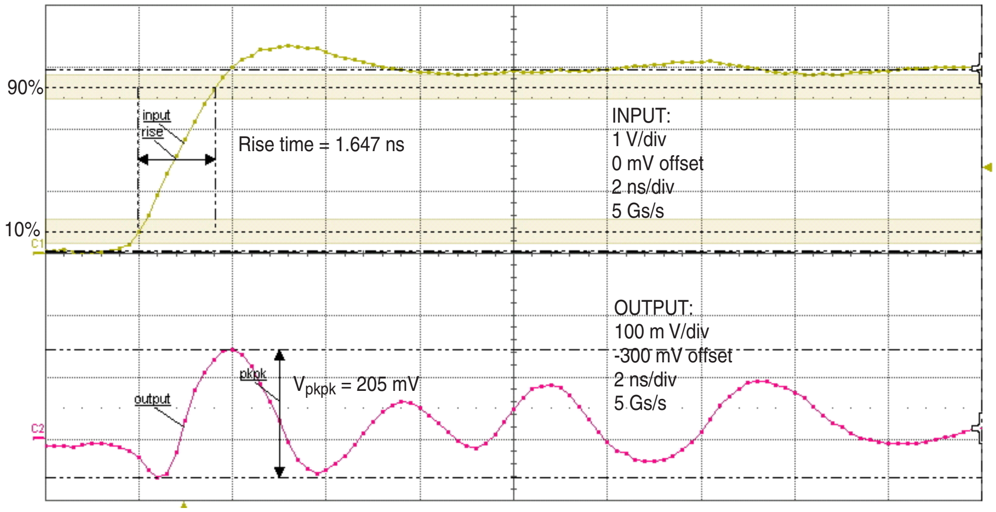


Figure 13. Relative variation of peak pulse power versus initial junction temperature

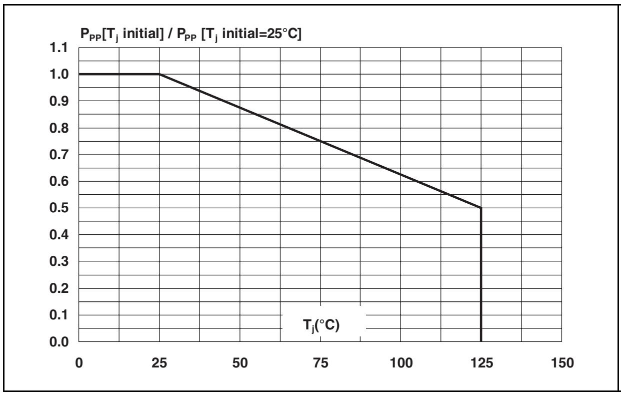


Figure 14. Peak pulse power versus exponential pulse duration

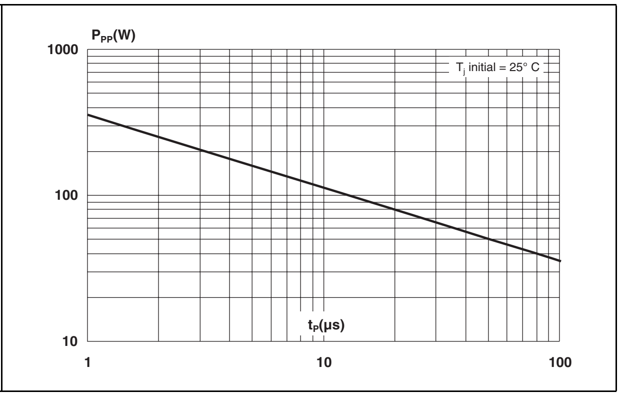


Figure 15. Clamping voltage versus peak pulse current (typical values, exponential waveform)

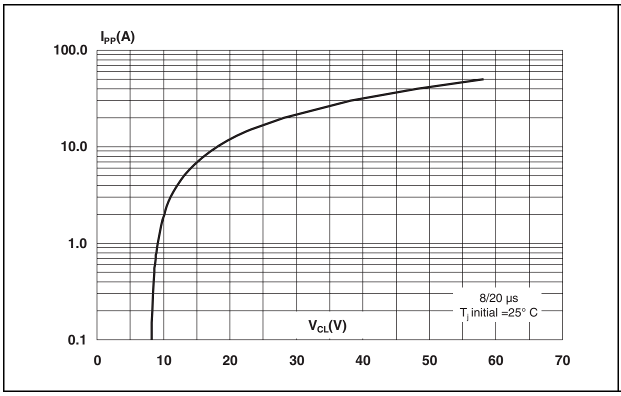
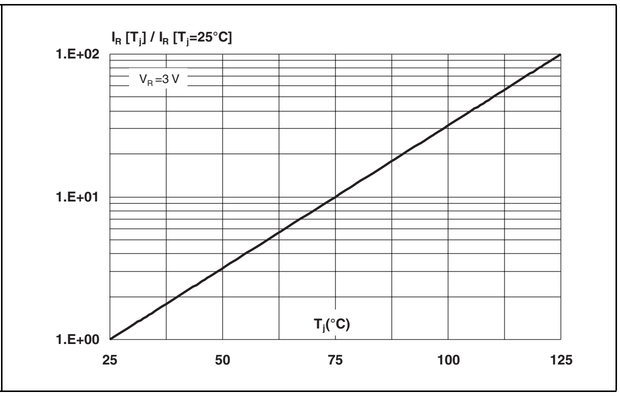
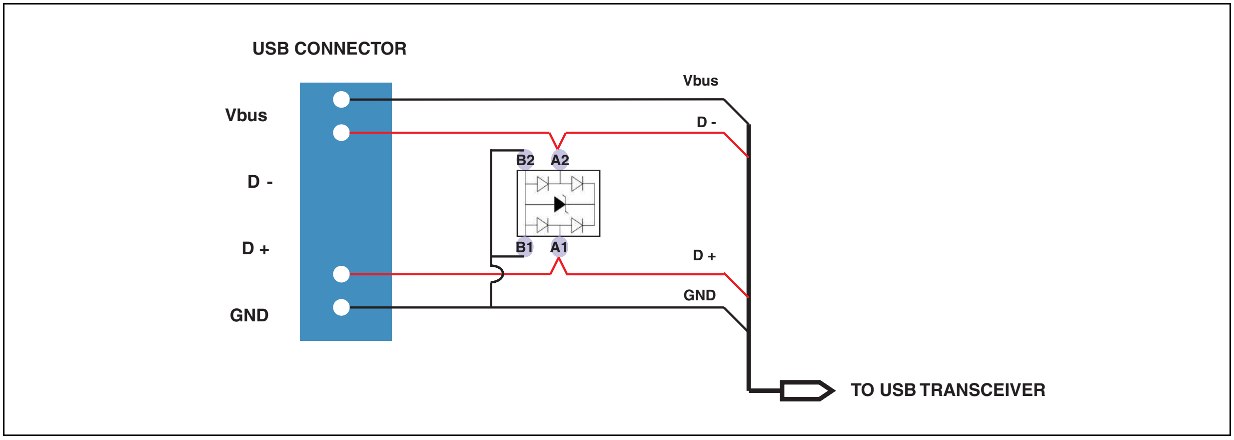


Figure 16. Relative variation of leakage current versus junction temperature (typical values)



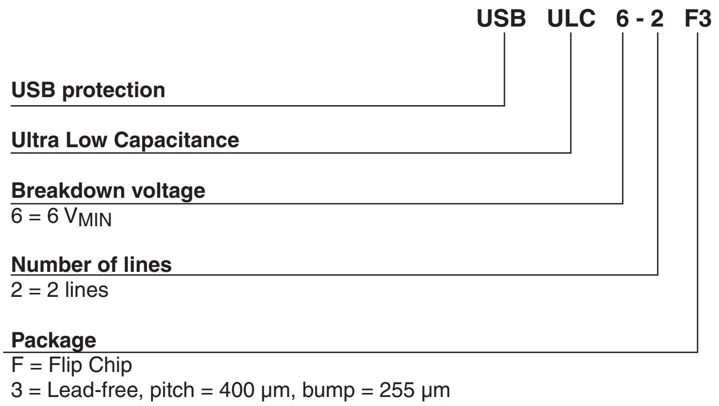
2 Application information

Figure 17. Application diagram



3 Ordering information scheme

Figure 18. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. Package dimensions

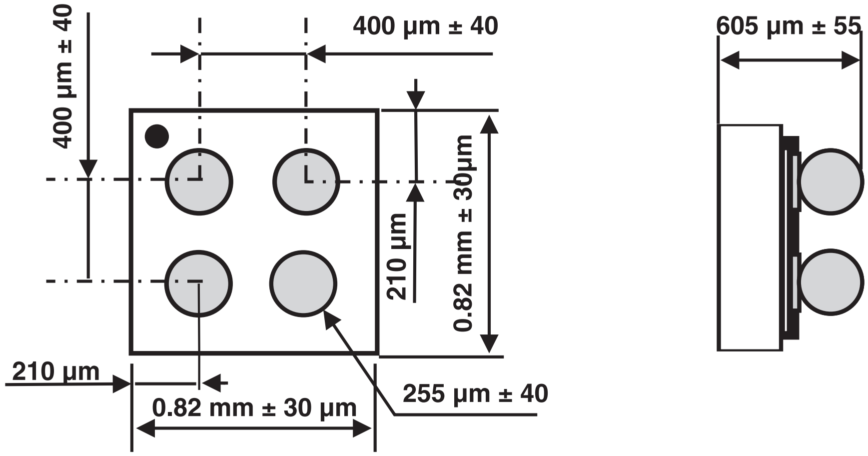


Figure 20. Footprint recommendations

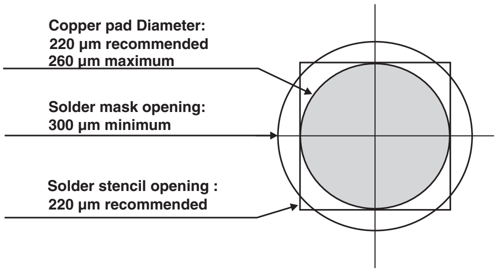


Figure 21. Marking

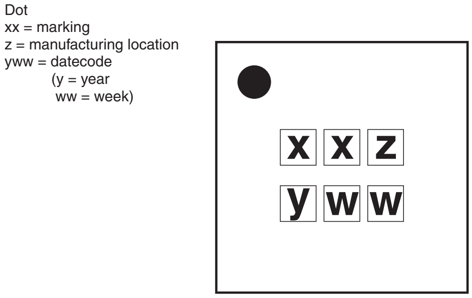
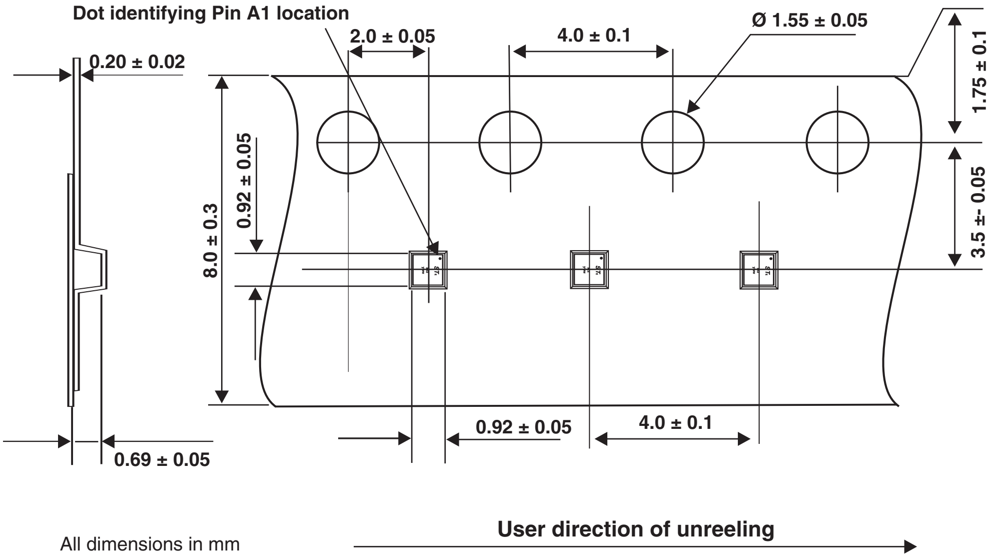


Figure 22. Flip-Chip tape and reel specifications



Note: *More information is available in the application notes:*

AN2348: "400 µm Flip Chip: Package description and recommendations for use"

AN1751: "EMI Filters: Recommendations and measurements"

5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBULC6-2F3	EH	Flip Chip	0.91 mg	5000	Tape and reel (7")

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
15-Dec-2006	1	Initial release.
29-Apr-2008	2	Updated ECOPACK statement. Updated *Figure 19*, *Figure 20* and *Figure 22.* Reformatted to current standards.
27-Jun-2011	3	Added *Figure 7* and *Figure 8*. Updated die dimensions in *Figure 19* and pocket dimensions in *Figure 22*.

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