

TRANSIL™ diode for ESD protection

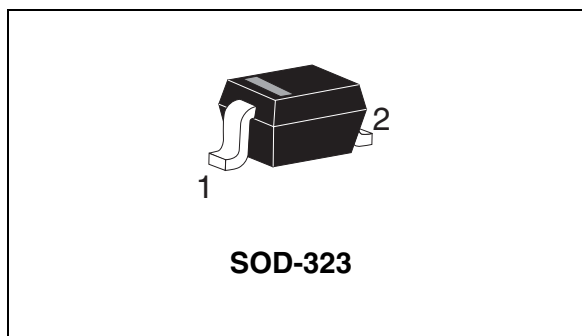
Features

- Max peak pulse power 160 W (8/20 μ s)
- Asymmetrical bidirectional device
- Stand-off voltage: 15 and 24 V
- Low clamping factor V_{CL}/V_{BR}
- Complies with the following standards :
 - IEC 61000-4-2 level 4 (> 15 kV air discharge, > 8 kV contact discharge)
 - IEC 61000-4-5; I_{pp} = 3 A (8/20 μ s)
 - HBM MIL STD 833, class 3 (> 4 kV)
- Low Leakage current

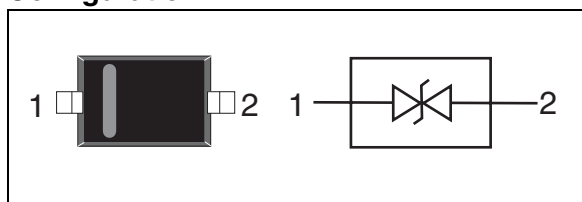
Description

The ESDLIN1524BJ is an asymmetrical TRANSIL diode designed specifically for protecting one automotive LIN bus line against electrostatic discharge (ESD). The SOD-323 is a very small package which allows space saving on high density printed circuit board .

Transil diodes provide high overvoltage protection by clamping action and have instantaneous response to transient overvoltages.



Configuration



| Pin | Description |
|-----|--|
| 1 | Cathode 1 (15 V reverse stand-off voltage) |
| 2 | Cathode 2 (24 V reverse stand-off voltage) |

Table 1. Absolute maximum ratings (limiting values) $T_{amb} = 25^{\circ}C$

| Symbol | Parameter | Value | Unit |
|--------------------|---|---------------------------|-------------|
| P_{PP} | Peak pulse power dissipation 8/20 μ s ⁽¹⁾ | 160 | W |
| T_{stg} T_j | Storage temperature range Operating junction temperature range | -65 to +175 -40 to 150 | $^{\circ}C$ |
| T_L | Maximum lead temperature for soldering during 10 s | 260 | $^{\circ}C$ |

1. For a surge greater than maximum values, the diode will fail in short-circuit

Table 2. ESD Maximum ratings

| Symbol | Parameter | Conditions | Value | Unit |
|--------|------------------------------------|-----------------------------------|-------|------|
| ESD | Electrostatic discharge capability | IEC 61000-4-2 (contact discharge) | 23 | kV |
| | | HBM MIL STD 833 | 10 | |

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1 Characteristics

Table 3. Electrical characteristics ($T_{amb} = 25^{\circ}C$)

| Symbol | Parameter |
|----------|------------------------------|
| V_{RM} | Stand-off voltage |
| V_{BR} | Breakdown voltage |
| V_{CL} | Clamping voltage |
| I_{RM} | Leakage current @ V_{RM} |
| I_R | Breakdown current @ V_{BR} |
| I_{PP} | Peak pulse current |
| C | Junction capacitance |

| Types | $I_{RM} @ V_{RM}$ | | V | $V_{BR} @ I_R^{(1)}$ | | | mA | $V_{CL} \text{ max } @ I_{PP} \text{ 8/20 } \mu\text{s}$ | | | | C ⁽²⁾ | | $\alpha T^{(3)}$ |
|-------------------|-------------------|-----|-----|----------------------|------|------|----|--|---|-----|-----|------------------|----|---------------------|
| | nA | | | V | | | | V | A | V | A | pF | | $10^{-4}/^{\circ}C$ |
| | Typ | Max | Min | Typ | Max | V | A | V | A | Typ | Max | Max | | |
| ESDLIN1524BJ(15V) | 1 | 50 | 15 | 17.1 | 18.9 | 20.3 | 5 | 25 | 1 | 35 | 5 | 16 | 20 | 8.8 |
| ESDLIN1524BJ(24V) | 1 | 50 | 24 | 25.4 | 27.8 | 30.3 | 5 | 40 | 1 | 50 | 3 | | | 9.6 |

1. Pulse test: $t_p < 50 \text{ ms}$
2. $V_R = 0 \text{ V}$, $F = 1 \text{ MHz}$
3. $\Delta V_{BR} = \alpha T \times (T_{amb} - 25) \times V_{BR(25^{\circ}C)}$

Figure 1. Relative variation of peak pulse power versus initial junction temperature

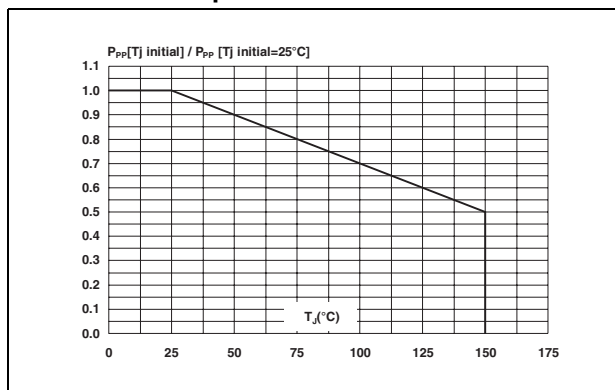


Figure 2. Peak pulse power versus exponential pulse duration

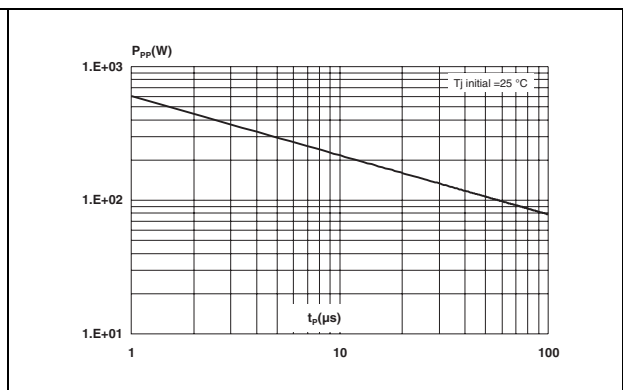


Figure 3. Junction capacitance versus line voltage (typical values), 15 V side

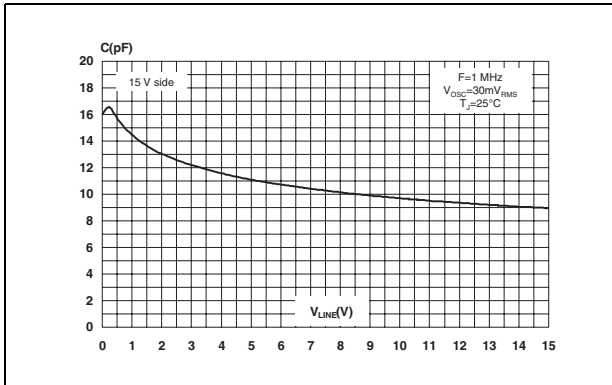


Figure 4. Junction capacitance versus line voltage (typical values), 24 V side

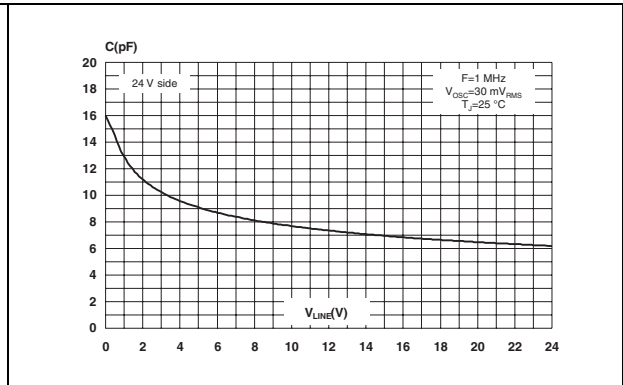
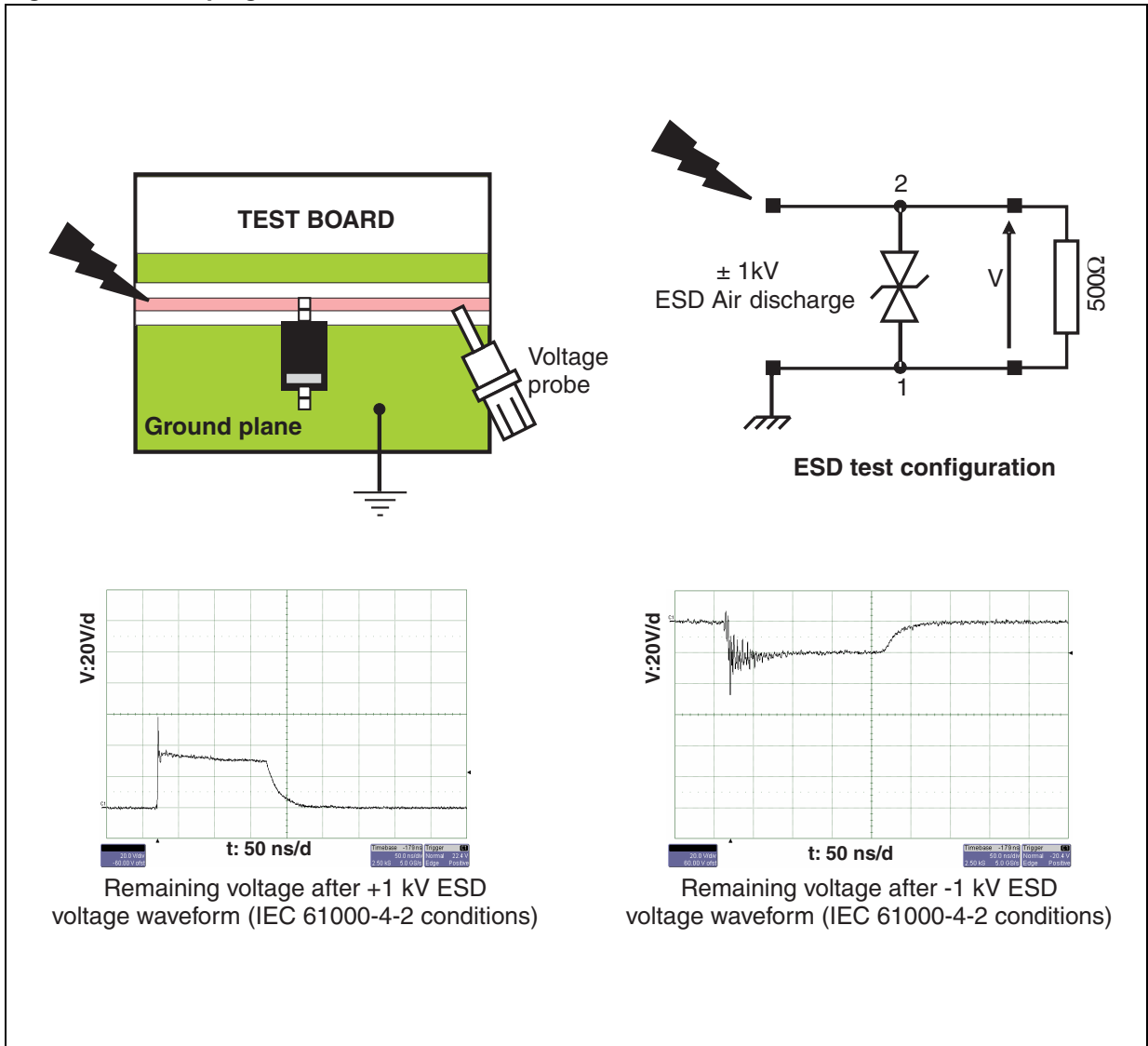


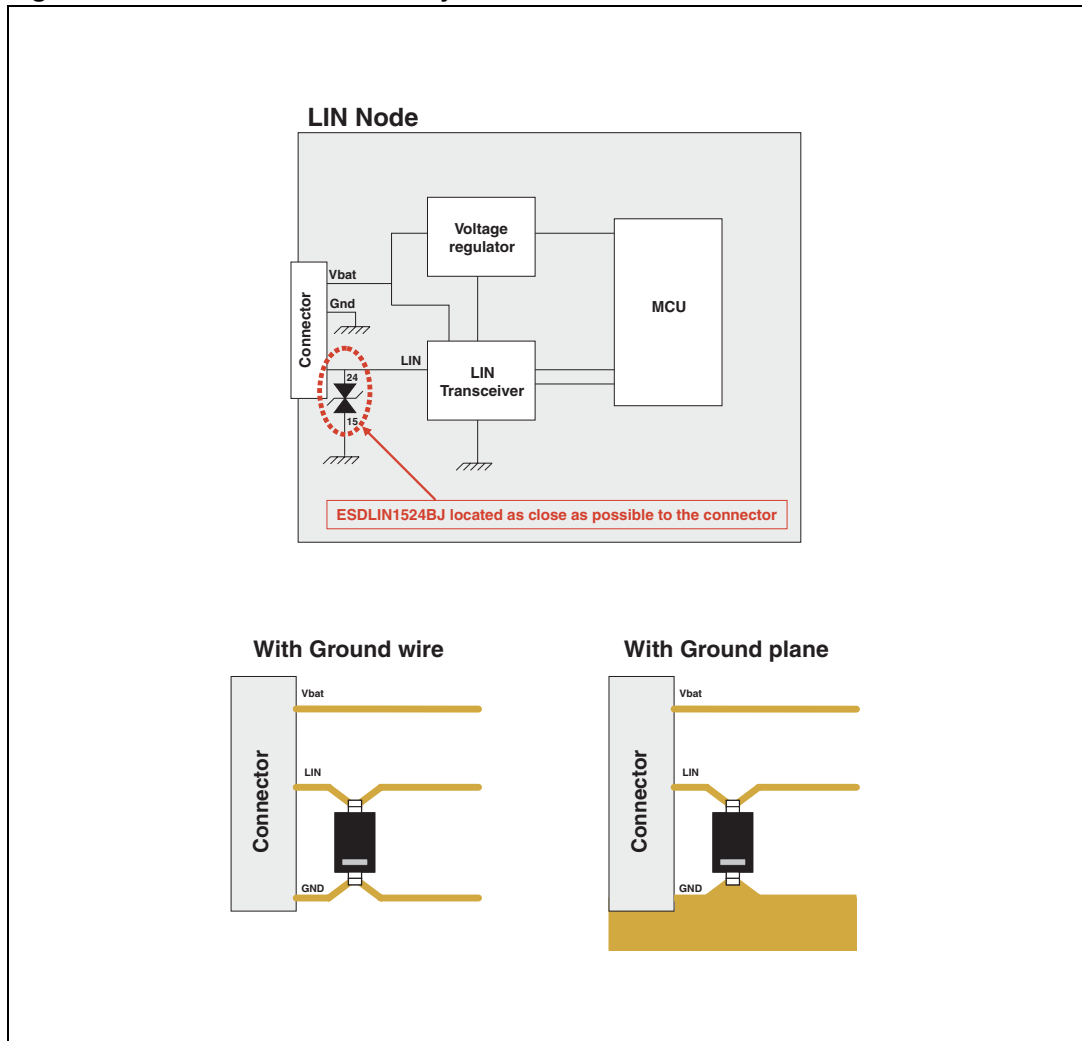
Figure 5. Clamping test conditions and results



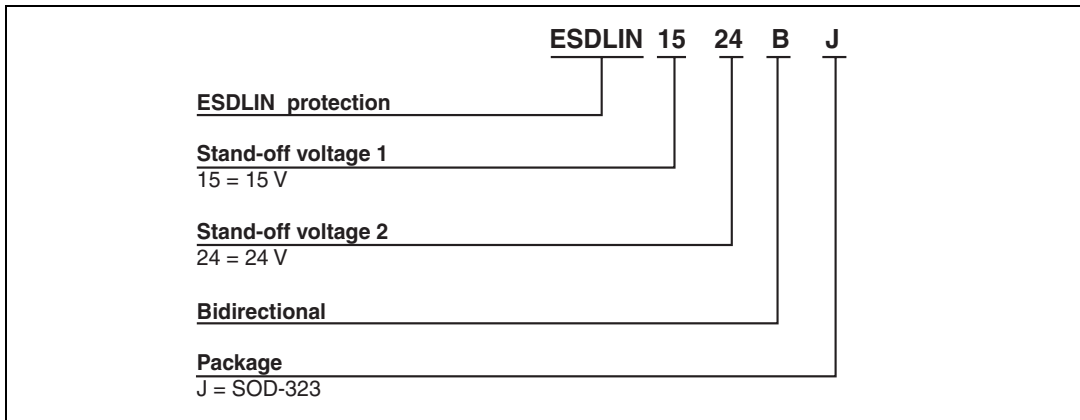
2 Placement and PCB layout recommendations

Figure 6. illustrates recommendations for the placement and layout of the PCB for optimum benefit of the ESDLIN1524BJ.

Figure 6. Placement and PCB layout recommendations



3 Ordering information scheme

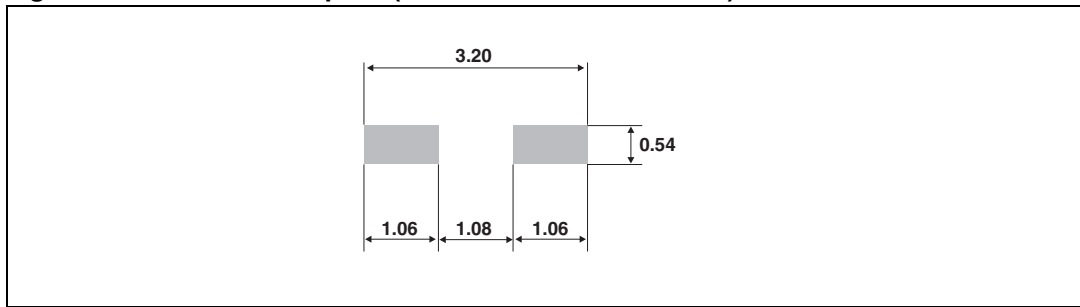


4 Package information

Table 4. SOD-323 dimensions

| Ref. | Dimensions | | | |
|------|-------------|------|--------|-------|
| | Millimeters | | Inches | |
| | Min. | Max. | Min. | Max. |
| A | | 1.17 | | 0.046 |
| A1 | 0 | 0.1 | 0 | 0.004 |
| b | 0.25 | 0.44 | 0.01 | 0.017 |
| c | 0.1 | 0.25 | 0.004 | 0.01 |
| D | 1.52 | 1.8 | 0.06 | 0.071 |
| E | 1.11 | 1.45 | 0.044 | 0.057 |
| H | 2.3 | 2.7 | 0.09 | 0.106 |
| L | 0.1 | 0.46 | 0.004 | 0.02 |
| Q1 | 0.1 | 0.41 | 0.004 | 0.016 |

Figure 7. SOD-323 footprint (dimensions in millimeters)



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5 Ordering information

| Part number | Marking | Package | Weight | Base qty | Delivery mode |
|--------------|---------|---------|--------|----------|---------------|
| ESDLIN1524BJ | 24 | SOD-323 | 5 mg | 3000 | Tape and reel |

6 Revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 28-Aug-2006 | 1 | Initial release. |
| 22-Sep-2006 | 2 | Added Figure 6 Placement and layout recommendations. |

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