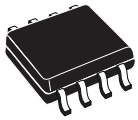
ST1S14

Up to 3 A step down switching regulator

Features

- 3 A DC output current
- Operating input voltage from 5.5 V to 48 V
- 850 kHz internally fixed switching frequency
- Internal soft start
- Power good open collector output
- Current mode architecture
- Embedded compensation network
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- 2 mA maximum quiescent current over temperature range
- 250 mΩ typical $R_{DS(on)}$
- Thermal shutdown



HSOP8 - exposed pad

Application

Factory automation

Printers

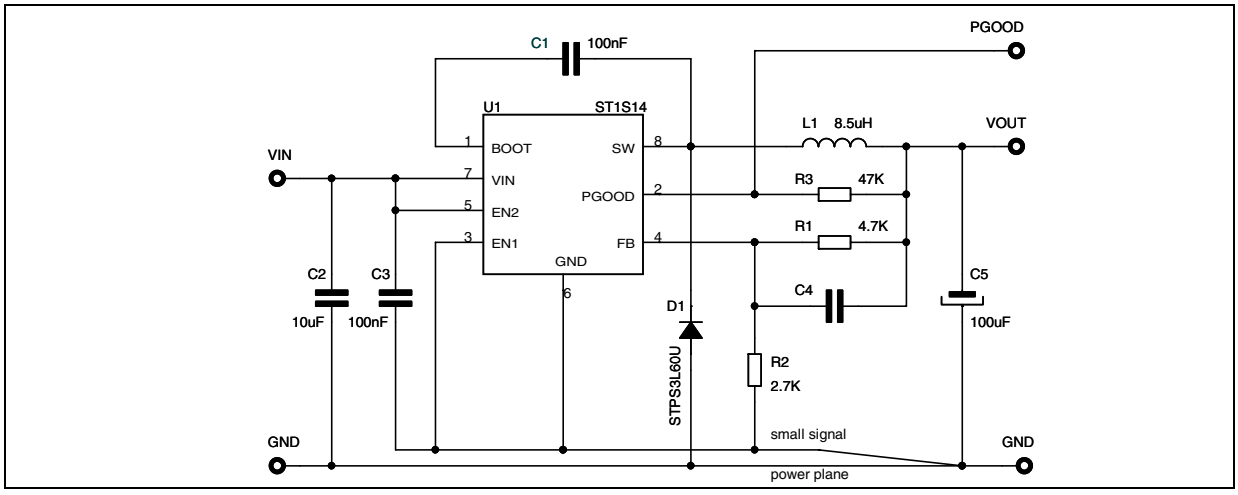
DC-DC modules

High current LED drivers

Description

The ST1S14 is a step down monolithic power switching regulator able to delivers up to 3 A DC current to the load depending on the application conditions. The high current level is also achieved thanks to an HSOP8 package with exposed frame, that allows to reduce the $R_{th(JA)}$ down to approximately 40 °C/W. The output voltage can be set from 1.22 V. The device uses an internal N-channel DMOS transistor (with a typical $R_{DS(on)}$ of 200 mΩ) as switching element to minimize the size of the external components. The internal oscillator fixes the switching frequency at 850 kHz. Power good open collector output validates the regulated output voltage as soon as it reaches the regulation. Pulse by pulse current limit offers an effective constant current short circuit protection. Current foldback decreases overstress in persistent short circuit condition.

Figure 1. Application schematic

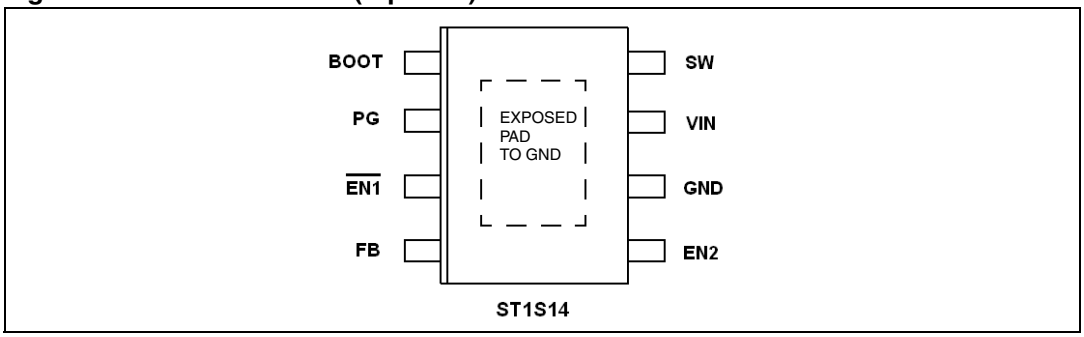


Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N	Pin	Description
1	BOOT	Bootstrap capacitor for N-channel gate driver. Connect 100nF low ESR capacitor from BOOT pin to SW
2	PG	Power good
3	$\overline{EN1}$	Enable pin active low
4	FB	Feedback voltage
5	FB	Enable pin active high
6	GND	Ground pin
7	V_{IN}	Input supply pin
8	SW	Switching node
	E.p.	Exposed pad must be connected to GND

1.3 Enable inputs

Table 2. Truth table

$\overline{EN1}$	EN2	Device status
H	L	INH
H	H	INH
L	L	INH
L	H	ON

2 Electrical data

2.1 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Power supply input voltage	-0.3 to 52	V
$V_{\overline{EN1}}$	Enable 1 voltage	-0.3 to 7	V
V_{EN2}	Enable 2 voltage	-0.3 to (V_{IN}+0.3)	V
PG	Power good	-0.3 to (V_{IN}+0.3)	V
BOOT	Bootstrap pin	-0.3 to 55	V
SW	Switching node	-1 to (V_{IN}+0.3)	V
V_{FB}	Feedback voltage	-0.3 to 3	V
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)	260	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$	Thermal resistance junction-ambient	40	°C/W

2.3 ESD protection

Table 5. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	4	kV
	MM	500	V

3 Electrical characteristics

All the population tested at T_J = 25 °C, V_{CC} =12 V, V_{EN1} = 5 V, V_{EN2} =0 V unless otherwise specified.

The specification is guaranteed from (-40 to +125) T_J temperature range by design, characterization and statistical correlation.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
V_{IN}	Operating input voltage range			5.5		48	V
$R_{DS(on)}$	MOSFET on resistance	I_{SW}=1A			0.2	0.4	Ω
I_{SW}	Maximum limiting current			3.7	4.5	5.2	A
t_{HICCUP}	Hiccup time				16		ms
f_{SW}	Switching frequency			600	850	1000	kHz
	Duty cycle		(1)		90		%
$T_{ON\ MIN}$	Minimum conduction time of the power element		(1)		90		ns
$T_{OFF\ MIN}$	Minimum conduction time of the external diode		(1)	75	90	120	ns
DC characteristics							
V_{FB}	Voltage feedback	I_{LOAD}=0 A		1.202	1.22	1.239	V
		I_{LOAD}=10 mA to 3A		1.196	1.22	1.245	V
I_{FB}	FB biasing current				50		nA
I_q	Quiescent current	V_{FB}=2V			1.3	2	mA
		V_{FB}=2V, V_{IN}=48V			1.7	2.4	mA
$I_{qst\text{-}by}$	Stand-by quiescent current	DEVICE OFF (see *Table 2*					µ
					0.92* V_{OUT}		V
		V_{FB} falling edge			0.8* V_{OUT}		V
	PG output voltage (open collector active)	I_{SINK} = 6mA				0.4	V

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Inhibit							
$V_{\overline{EN1}}$	Enable 1 levels	Device ON V_{IN}=5.5V to 48V				0.5	V
		Device OFF V_{IN}=5.5V to 48V		1.5			V
$I_{\overline{EN1}}$	Enable 1 biasing current	$V_{\overline{EN1}}$=5V			1.6	2.5	µA
V_{EN2}	Enable 2 levels	Device ON V_{IN}=5.5V to 48V		1.5			V
		Device OFF V_{IN}=5.5V to 48V				0.5	V
I_{EN2}	Enable 2 biasing current	V_{EN1}=0V; V_{EN2}=0V		-1.0	-2.4	-3.7	µA
		V_{EN1}=0V; V_{EN2}=12V		2.7	5.8	8.5	µA
		V_{EN1}=0V; V_{CC}=V_{EN2}=48V		3.0	6.0	9.0	µA
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature		(1)	140	150	160	°C
T_{HYS}	Thermal shutdown hysteresis		(1)		15		°C

1. Parameter guaranteed by design

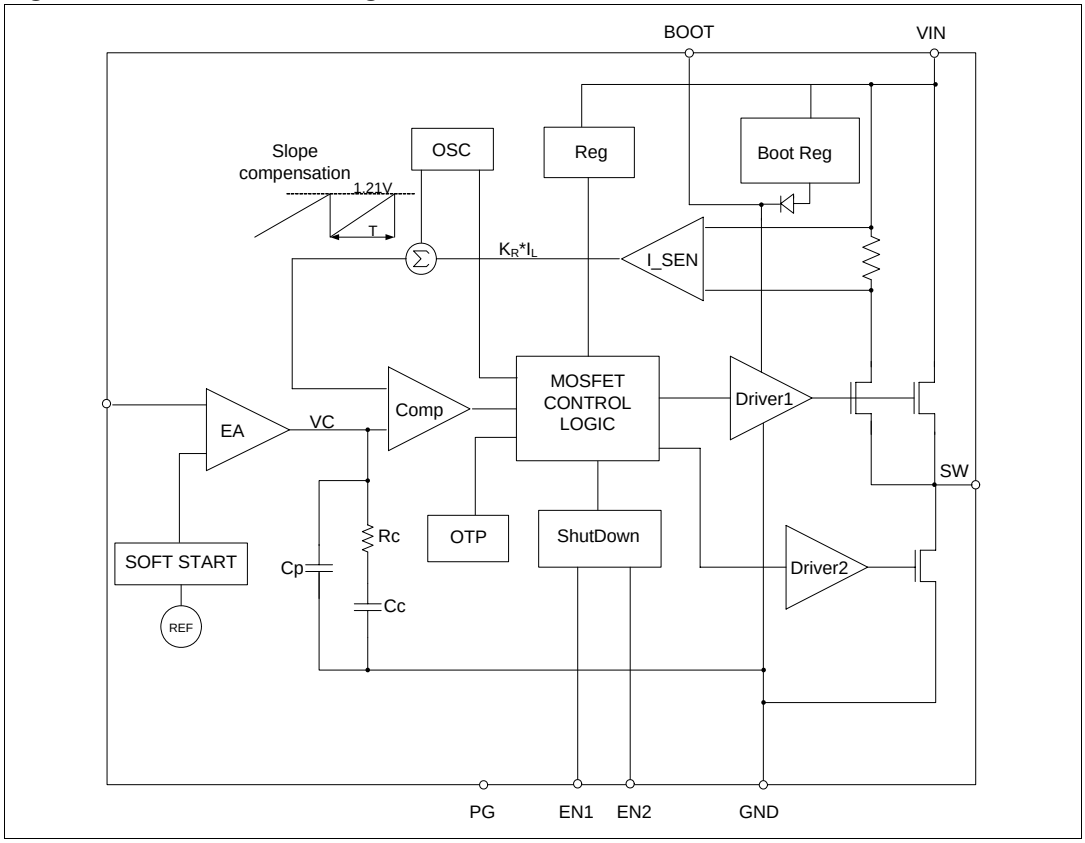
4 Functional description

The ST1S14 is based on a “peak current mode”, constant frequency control. As a consequence the intersection between the error amplifier output and the sensed inductor current generates the control signal to drive the power switch.

The main internal blocks shown in the block diagram in *Figure 3* are:

- A fully integrated sawtooth oscillator with a typical frequency of 850 kHz
- A transconductance error amplifier
- An high side current sense amplifier to track the inductor current
- A pulse width modulator (PWM) comparator and the circuitry necessary to drive the internal power element
- The soft start circuitry to decrease the inrush current at power-up
- The current limitation circuit based on the pulse by pulse current protection with frequency divider based on FB voltage and the HICCUP protection
- The bootstrap circuitry to drive the embedded N-MOS switch.
- A multi input inhibit block for stand-by operation.
- A circuit to implement the thermal protection function.

Figure 3. Device block diagram



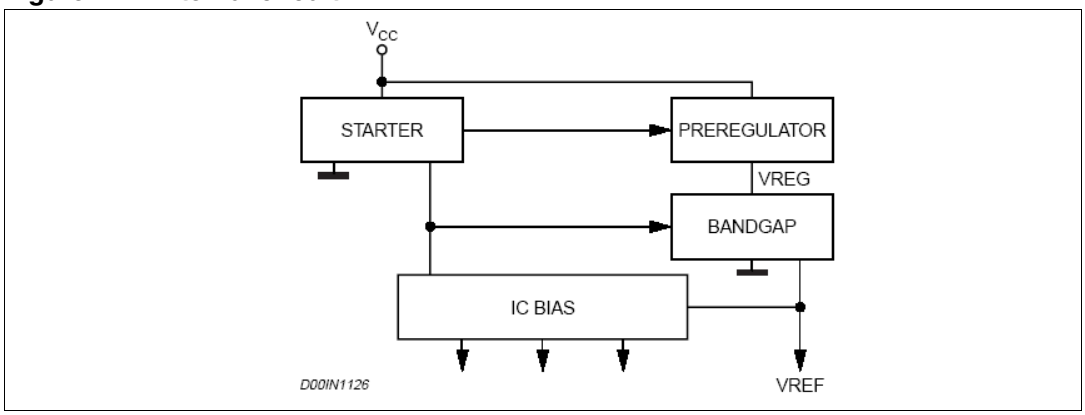
4.1 Power supply and voltage reference

The internal regulator circuit consists of a start-up circuit, an internal voltage pre-regulator, the bandgap voltage reference and the bias block that provides current to all the blocks. The starter supplies the start-up current to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The pre-regulator block supplies the bandgap cell with a pre-regulated voltage that has a very low supply voltage noise sensitivity.

4.2 Voltages monitor

An internal block continuously senses the V_{cc}, V_{ref} and V_{bg}. If the monitored voltages are good, the regulator begins operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



4.3 Soft Start

The startup phase minimizes the inrush current and decreases the stress of the power components at the power up. The startup takes place when V_{IN} crosses the selected UVLO threshold.

As shown in *Figure 5*, the soft start event is composed of three main phases:

Phase 1: [V_{FB}<300 mV]

The output capacitor is charged with a typical peak inductor current equal to 1.45 A and the nominal f_{SW} is divided by 5

Phase 2: [VFB>300 mV & n_{COUNT}<2816 clks]

A internal counter determines phase 2 time (see *Figure 5*).

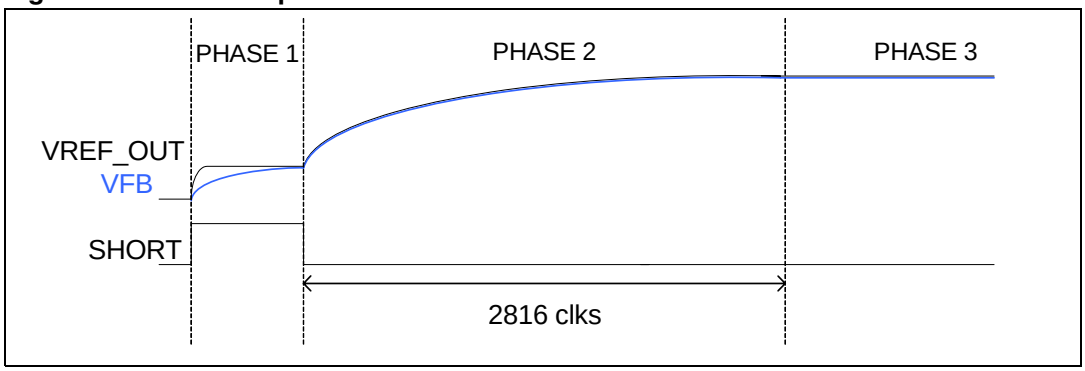
The reference of the error amplifier is ramped in 44 steps (one step every 64 clks).

A low pass filter smooths each step to minimize output discontinuity. Considering the typical 850 kHz switching frequency, the phase two duration is 3.3 msec

Phase 3: [VFB>300 mV & n_{COUNT}=2816 clks]

The reference of the embedded error amplifier is connected to the nominal reference voltage (1.222 typical) derived from the internal bandgap generator. The soft start phase ends at this time.

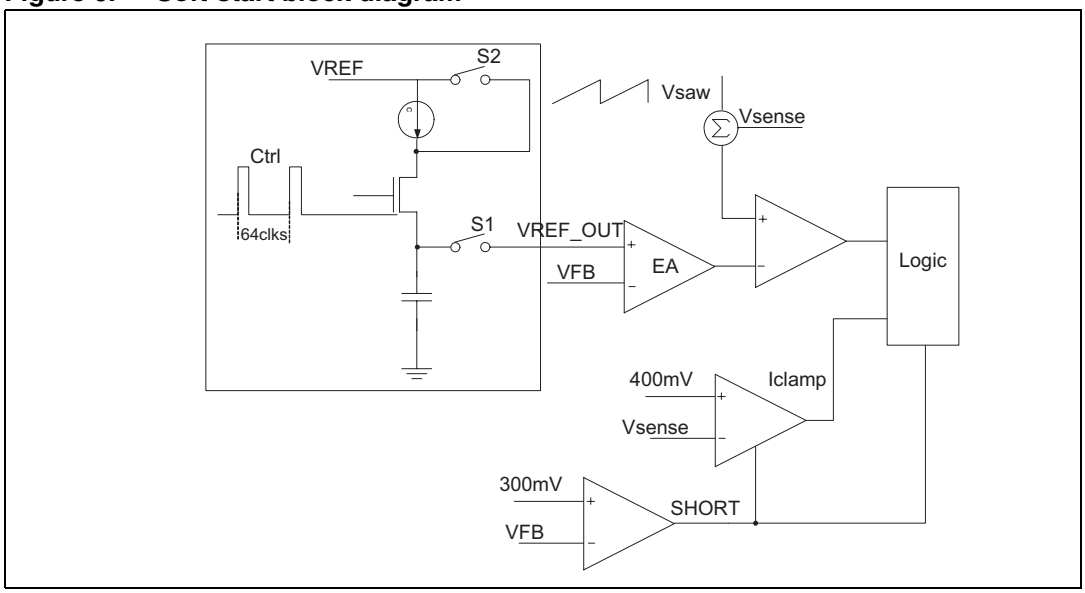
Figure 5. soft start phases



During normal operation a new soft start cycle takes place in case of:

- HICCUP mode current protection
- thermal shutdown event
- UVLO event
- the device is driven in INH mode

Figure 6. Soft-start block diagram



4.4 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.222 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage.

The error amplifier is internally compensated to minimize the size of the final application.

Table 7. Uncompensated error amplifier characteristics

Description	Values
Transconductance	218 µS
Low frequency gain	93 dB
C_P	24 pF
C_C	211 pF
R_C	200 kΩ

The error amplifier output is compared with the inductor current sense information to perform PWM control

4.5 Inhibit function

The inhibit feature is used to set the device in standby mode according to *Table 2: Truth table*. When the device is disabled, the power consumption is reduced to less than 40 µA. The pin EN2 is also V_{IN} compatible.

4.6 Thermal shutdown

The shutdown block generates a signal that turns OFF the power stage if the temperature of the chip goes higher than a fixed internal threshold (150±10 °C). The sensing element of the chip is very close to the PDMOS area, ensuring fast and accurate temperature detection. A hysteresis of approximately 15 °C keeps the device from turning ON and OFF continuously.

5 Additional features and limitations

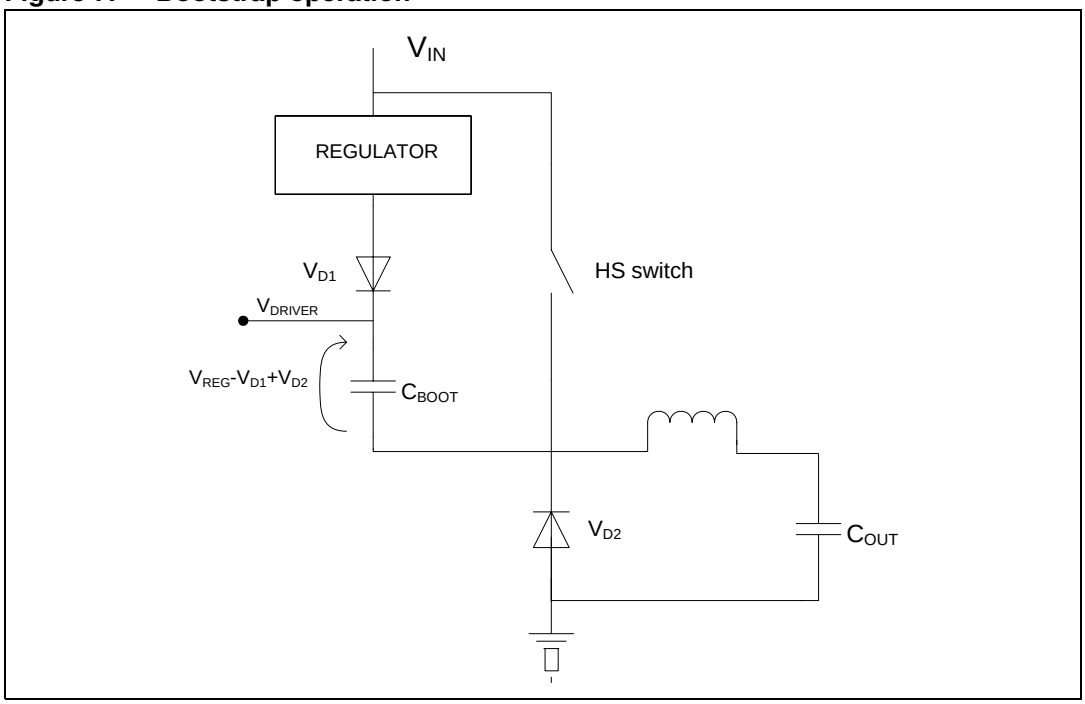
5.1 Maximum duty cycle

The bootstrap circuitry charges cycle by cycle the external bootstrap capacitor to generate a voltage higher than V_{IN} necessary to drive the internal N-channel power element.

An internal linear regulator charges the C_{BOOT} during the conduction time of the external free wheeling diode during the switching activity. The internal logic implements a minimum OFF time of the high side switch (90 nsec typical) to prevent the bootstrap discharge at high duty cycle. As a consequence the ST1S14 can operate at a maximum duty cycle around 90% typical.

The ST1S14 embeds the diode V_{D1} required for the bootstrap operation.

Figure 7. Bootstrap operation



5.2 Minimum output voltage over V_{IN} range

The minimum regulated output voltage at a given input voltage is limited by the minimum conduction time of the power element, that is 90nsec typical for the ST1S14:

Equation 1

$$V_{O\_MIN}(V_{IN}) = V_{IN} \cdot D_{MIN} = V_{IN} \cdot \frac{T_{ON\_MIN}}{T_{SW}} = V_{IN} \cdot \frac{90ns}{1.18\mu s}$$

which is plotted in *Figure 14*. The reference of the embedded error amplifier (1.22V) sets the minimum V_{O_SET} at low V_{IN}.

Figure 8. V_{O_MIN} over input voltage range

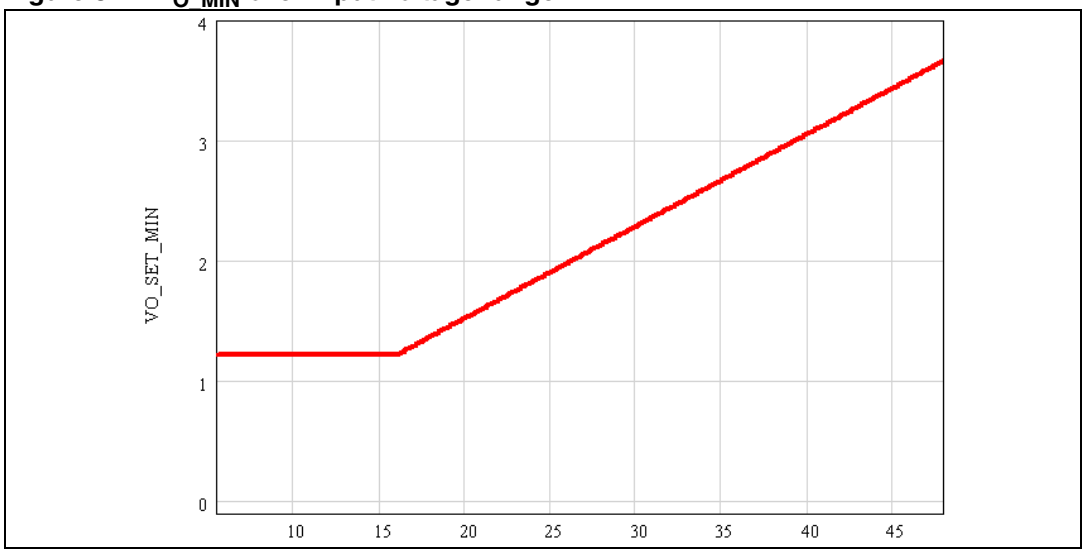


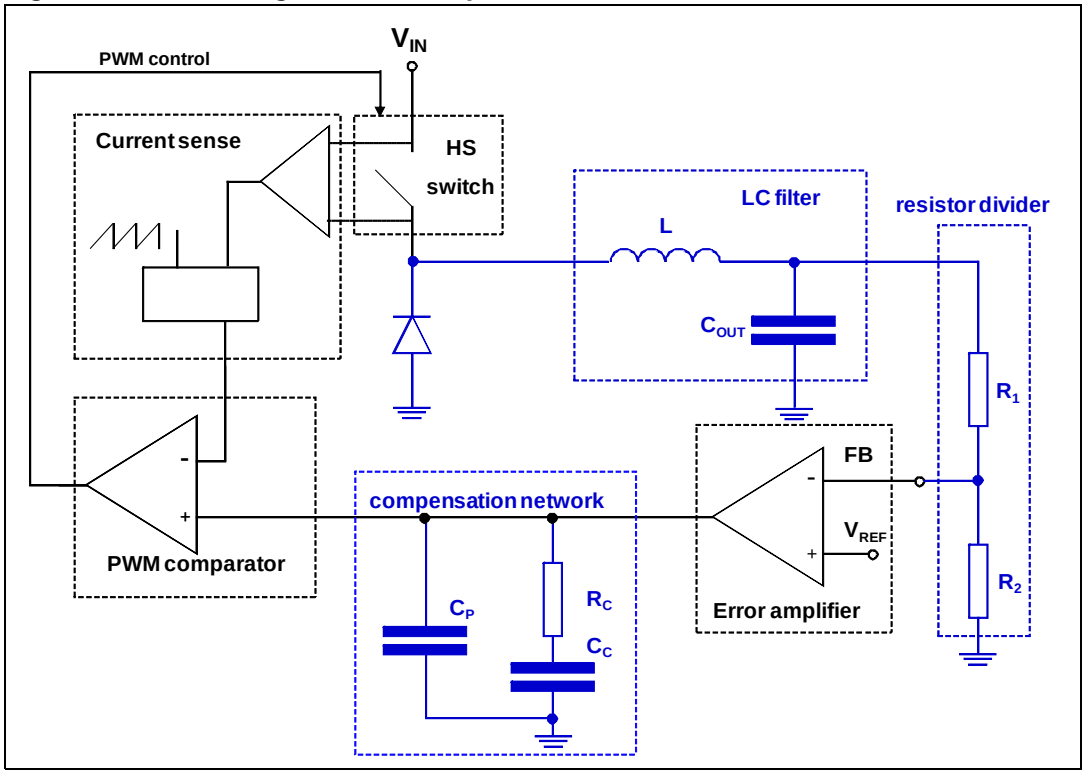
Figure 8 shows the minimum output voltage over input voltage range to have constant switching activity and a predictable output voltage ripple.

The regulator can anyway regulate the minimum input voltage over the entire input voltage range but, given the 90ns minimum conduction time of the power element, it will skip some pulses to keep the output voltage in regulation when *Equation 1* is not satisfied.

This operation is not recommended at the nominal input voltage of the application mainly because it affects the output voltage ripple, but it is generally accepted during a line transient event.

6 Closing the loop

Figure 9. Block diagram of the loop



6.1 $G_{CO}(s)$ Control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

Equation 2

$$G_{CO}(s) = \frac{R_0}{R_i} \cdot \frac{1}{1 + \frac{R_0 \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

where R_0 represents the load resistance, R_i the equivalent sensing resistor of the current sense circuitry, ω_p the single pole introduced by the LC filter and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 3

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

Equation 4

$$\omega_n = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

Equation 5

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{pp} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \cdot R_i \end{cases}$$

S_n represents the on time slope of the sensed inductor current, S_e the on time slope of the external ramp (V_{PP} peak to peak amplitude) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%

The sampling effect contribution $F_H(s)$ is:

Equation 6

where:

Equation 7

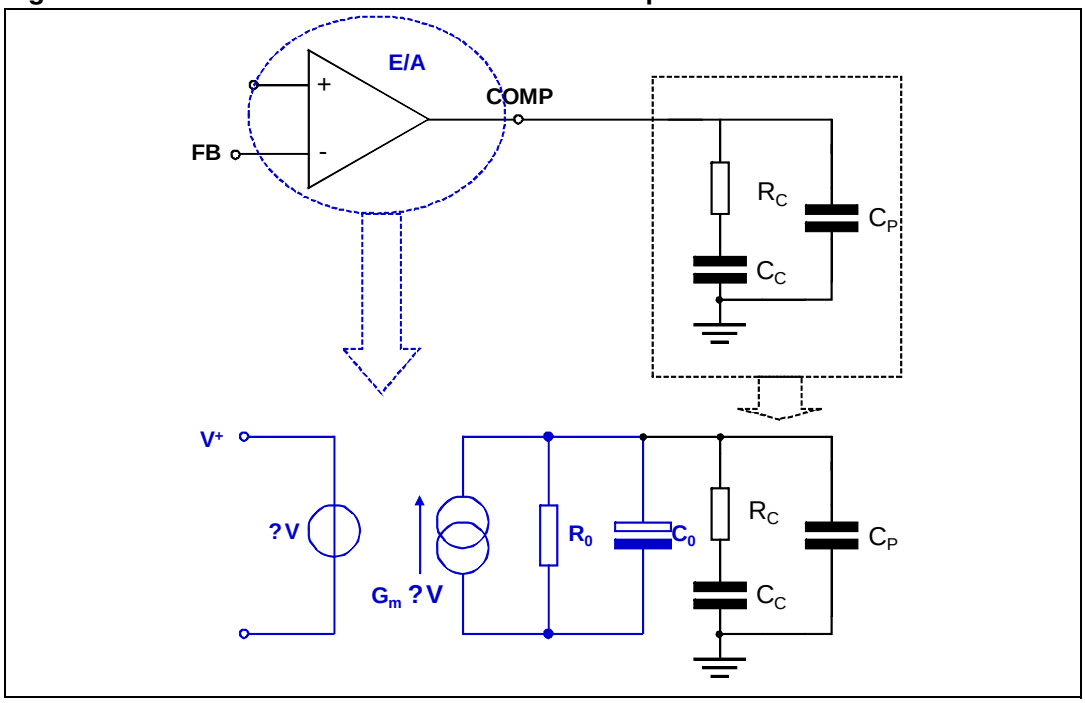
$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]}$$

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

6.2 Error amplifier compensation network

The ST1S14 embeds (see *Figure 10*) the error amplifier and a pre-defined compensation network which is effective to stabilize the system in most of the application conditions

Figure 10. Transconductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it is useful to reduce the noise at the output of the error amplifier.

The transfer function of the error amplifier and its compensation network is:

Equation 8

$$A_0(s) = \frac{A_{V0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

Where $A_{vo} = G_m \cdot R_o$

The poles of this transfer function are (if $C_c >> C_0+C_P$):

Equation 9

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 10

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 11

$$F_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

The embedded compensation network is R_C=200K, C_P=24pF, C_C=211pF and C_O can be considered negligible, so the singularities are:

Equation 12

$$f_Z = 3,77\ kHz \qquad f_{P\,LF} = 3,01\ Hz \qquad f_{P\,HF} = 33,16\ kHz$$

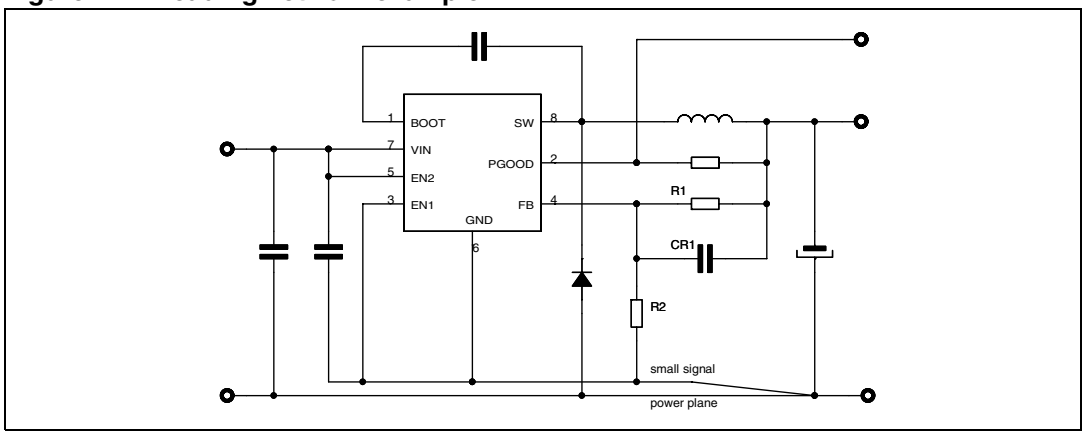
6.3 Voltage divider

The contribution of a simple voltage divider is:

Equation 13

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2}$$

Figure 11. Leading network example



A small signal capacitor in parallel to the upper resistor (see *Figure 11.*) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$), sometimes necessary to improve the system phase margin:

Equation 14

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{(1 + s \cdot R_1 \cdot C_{R1})}{\left(1 + s \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}\right)}$$

where:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{R1}}$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}}$$

$$f_Z < f_P$$

6.4 Total loop gain

In summary, the open loop gain can be expressed as:

Equation 15

$$G(s) = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_0(s)$$

Example: V_{IN} = 12V, V_{OUT} = 3.3V, R_{OUT} = 2Ω

The resistor divider is R_1=5.6K, R_2=3.3K.

C_{R1}=150nF implements a leading network (f_Z=190 kHz, f_P=510 kHz).

Selecting L = 8.2 µH, C_{OUT} = 100 µF and ESR = 75 mΩ, the gain and phase bode diagrams are plotted respectively in *Figure 12* and *Figure 13* over input voltage range (V_{IN}=6V to 48V, I_{OUT}=3A)

Figure 12. Module plot

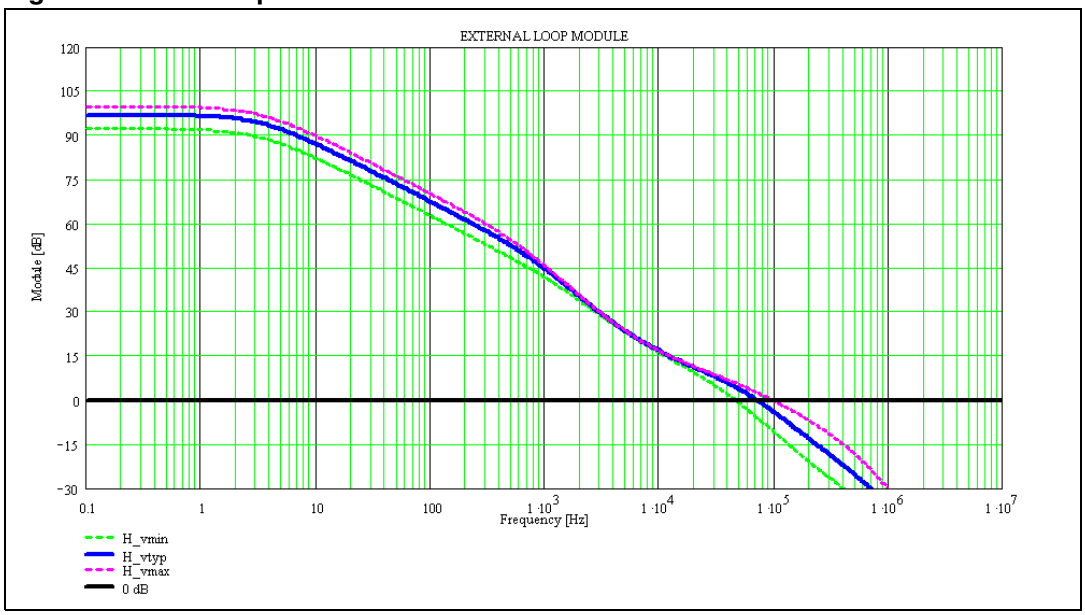
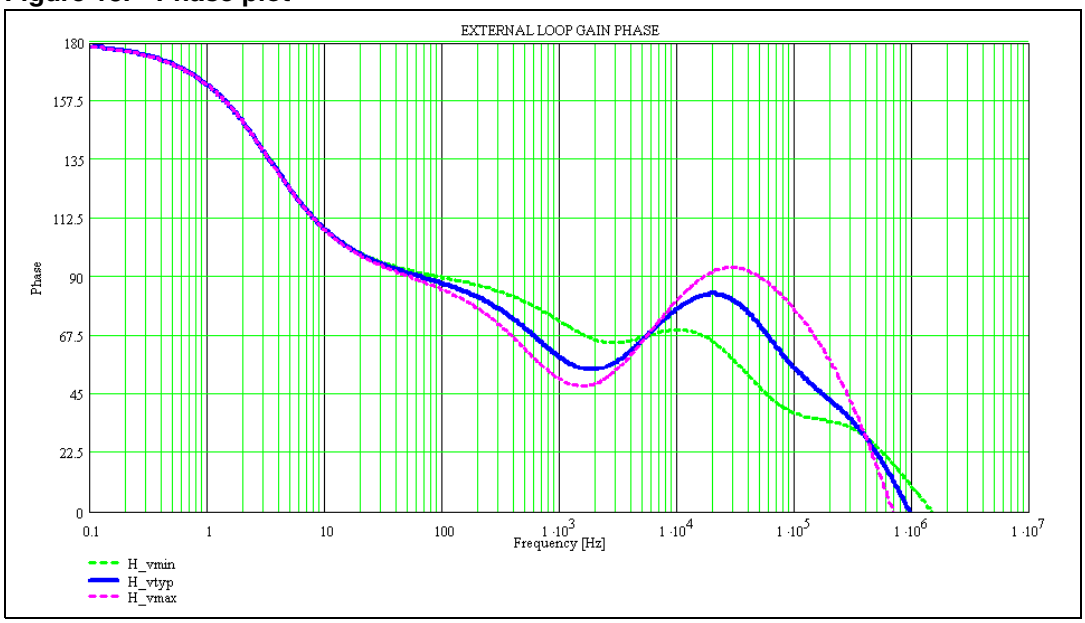


Figure 13. Phase plot



The cut-off frequency and the phase margin are:

Equation 16

$$V_{IN} = 6V \quad f_C = 46\ kHz \quad pm = 49°$$
$$V_{IN} = 12V \quad f_C = 71\ kHz \quad pm = 62°$$
$$V_{IN} = 48V \quad f_C = 97\ kHz \quad pm = 78°$$

7 Application information

7.1 Component selection

7.1.1 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, whose RMS value can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors has to be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS current flowing through the capacitor. The maximum RMS input current (flowing through the input capacitor) is:

Equation 17

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where η is the expected system efficiency, D is the duty cycle and I_O is the output DC current. Considering $\eta = 1$ this function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2. The maximum and minimum duty cycles are:

Equation 18

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 19

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where V_F is the free wheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX}, it is possible to determine the max IRMS going through the input capacitor. Capacitors that can be considered are:

Electrolytic capacitors:

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

Tantalum capacitors:

Small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is suggested to avoid this type of capacitor for the input filter of the device as they could be stressed by an high surge current when connected to the power supply.

Table 8. List of ceramic capacitors for the ST1S14

Manufacturer	Series	Capacitor value (µ)	Rated voltage (V)
TAIYO YUDEN	UMK325BJ106MM-T	10	50
MURATA	GRM42-2 X7R 475K 50	4.7	50

In case the selected capacitor is ceramic (so neglecting the ESR contribution), the input voltage ripple can be calculated as:

Equation 20

$$V_{IN\,PP} = \frac{I_O}{C_{IN} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

7.1.2 Output capacitor

The output capacitor is very important to meet the output voltage ripple requirement.

Using a small inductor value is useful to reduce the size of the choke but it increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to a very high frequency, its effect is negligible.

Ceramic capacitors

Ceramic capacitors and very low ESR capacitors that introduce a zero outside the designed bandwidth (f_Z=1/(2*pi*ESR*C_{OUT}, see *Chapter 6: Closing the loop*) in general should be avoided. A leading network across the upper resistor of the voltage divider is useful to increase the phase margin and compensate the system (see *Chapter 6.3: Voltage divider*). The effectiveness of the leading network increases at high output voltage because the singularities becomes more split.

High ESR capacitors

The “high ESR capacitor” definition stands for a capacitor having an ESR value able to introduce a zero into the designed system bandwidth, which can be, as a general rule, up to f_{SW}/5 at maximum. Tantalum or electrolytic capacitors belongs to this group.

Equation 21

$$f_Z = \frac{1}{2 \cdot \pi \cdot ESR \cdot COUT} < BW < \frac{f_{SW}}{5}$$

A list of some tantalum capacitor manufacturers is provided in *Table 9.: Output capacitor selection*.

Table 9. Output capacitor selection

Manufacturer	Series	Rated voltage (V)	Cap value (µF)(1)	ESR (mΩ)(1)
Nippon Chemicon	KZE	6.3 to 50	$f_Z = \frac{1}{2 \cdot \pi \cdot ESR \cdot COUT} < BW$	
Sanyo POSCAP(2)	TAE	4 to 16		
	THB/C/E	4 to 16		
AVX	TPS	4 to 35		

1. see *Chapter 6: Closing the loop* for the selection of the output capacitor
2. POSCAP capacitors have some characteristics which are very similar to tantalum.

7.1.3 Inductor

The inductor value is very important as it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20 - 40% of I_{omax}, which is 0.6 - 1.2 A with $I_O$max = 3 A. The approximate inductor value is obtained using the following formula:

Equation 22

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \cdot T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D · T. For example, with V_{OUT} = 3.3 V, V_{IN} = 24 V and ΔI_O = 0.8 A, the inductor value is about 4.7 µH. The peak current through the inductor is given by:

Equation 23

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, when the peak current is fixed, a higher inductor value allows a higher value for the output current. In the *Table 10.: Inductor selection*, some inductor manufacturers are listed.

Table 10. Inductor selection

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Wurth Elektronik	WE-HCI 7040	1 to 4.7	20 to 7
	WE-HCI 7050	4.9 to 10	20 to 4.0
Coilcraft	XPL 7030	2.2 to 10	29 to 7.2

7.2 Layout considerations

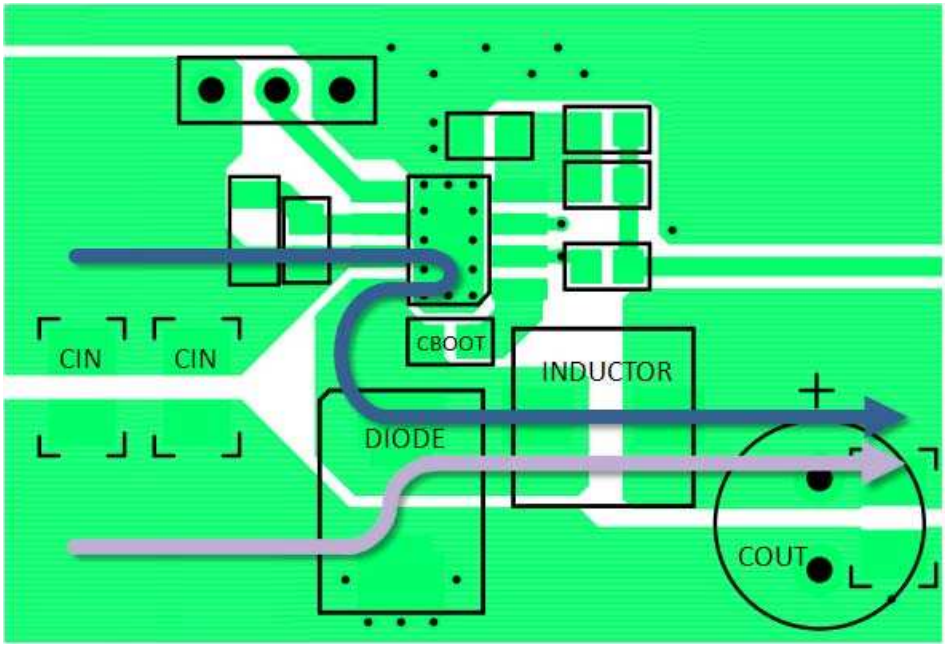
The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. A layout example is provided in *Figure 14* below.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pick-up noise. Another important issue is the ground plane of the board. Since the package has an exposed pad, it is very important to connect it to an extended ground plane in order to reduce the thermal resistance junction-to-ambient.

To increase the design noise immunity, different signal and power ground should be implemented in the layout (see *Chapter 7.5: Application circuit*). The signal ground serves the small signal components, the device ground pin, the exposed pad and a small filtering capacitor connected to the VCC pin. The power ground serves external diode and the input filter. The different grounds are connected underneath the output capacitor. Neglecting the current ripple contribution, the current flowing through this component is constant during the switching activity and so this is the cleanest ground point of the buck application circuit.

Figure 14. Layout example



7.3 Thermal considerations

The dissipated power of the device is tied to three different sources:

- Conduction losses due to the not insignificant R_{DSON}, which are equal to:

Equation 24

$$P_{ON} = R_{DSON} \cdot (I_{OUT})^2 \cdot D$$

Where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but in practice it is substantially higher than this value to compensate for the losses in the overall application. For this reason, the conduction losses related to the R_{DSON} increase compared to an ideal case.

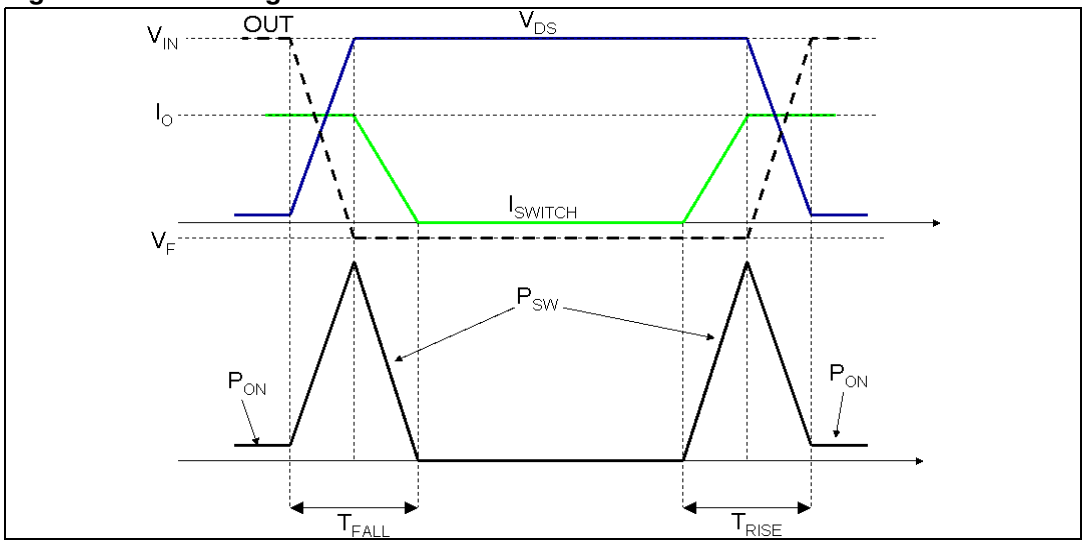
- Switching losses due to turning ON and OFF. These are derived using the following equation:

Equation 25

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW\_EQ} \cdot F_{SW}$$

Where T_{RISE} and T_{FALL} represent the switching times of the power element that cause the switching losses when driving an inductive load (see *Figure 15*). T_{SW} is the equivalent switching time.

Figure 15. Switching losses



- Quiescent current losses.

Equation 26

$$P_Q = V_{IN} \cdot I_Q$$

Example:

- V_{IN} = 24 V
- V_{OUT} =5 V
- I_{OUT} = 3 A

$R_{DS(on)}$ has a typical value of 0.2Ω @ 25 °C and increases to a maximum value of 0.4Ω @ 125 °C. We can consider a value of 0.3 Ω.

T_{SW_EQ} is approximately 12 ns.

I_Q has a typical value of 2 mA @ V_{IN} = 24 V.

The overall losses are:

Equation 27

$$P_{TOT} = R_{DSON} \cdot (I_{OUT})^2 \cdot D + V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} + V_{IN} \cdot I_Q = ""$$
$$= 0.3 \cdot (3)^2 \cdot 0.137 + 24 \cdot 3 \cdot 12 \cdot 10^{-9} \cdot 850 \cdot 10^{-3} + 24 \cdot 2 \cdot 10^{-3} \cong 1.15W$$

The junction temperature of device will be:

Equation 28

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

Where T_A is the ambient temperature and Rth_{J-A} is the thermal resistance junction-to-ambient. Considering that the device is mounted on board with a good ground plane, that it has a thermal resistance junction-to-ambient (Rth_{J-A}) of about 40 °C/W, and an ambient temperature of about 40 °C:

$$T_J = 40 + 1.15 \cdot 40 \cong 86°C$$

7.4 Short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit, the device disables the power element and it is able to reduce the conduction time down to the minimum value (approximately 90 nsec typical) to keep the inductor current limited. This is the pulse by pulse current limitation to implement constant current protection feature.

For the ST1S14, the operation of the pulse by pulse current limitation depends on the FB voltage:

- **300 mV <V_{FB} <1.22V:** the device operates at nominal switching frequency and the current limitation value
- **V_{FB} < 300mV:** the switching frequency is decreased five times the nominal value (170 kHz = 850 kHz/5) and the peak current value is foldback to 1.45A typical. The frequency foldback helps to prevent the current diverging at low V_{OUT} / high input voltage. The current foldback reduces the stress of the embedded power element and the external power components in case of persistent short circuit at the output.

In overcurrent condition, the duty cycle is strongly reduced and, in most applications, this is enough to limit the switch current to the active current threshold, nominal or foldback depending on the FB voltage.

The inductor current ripple during ON and OFF phases can be written as:

- ON phase

Equation 29

$$\Delta I_{L\,TON} = \frac{V_{IN} - V_{OUT} - (DCR_L + R_{DSON}) \cdot I}{L}(T_{ON})$$

- OFF phase

Equation 30

$$\Delta I_{L\,TON} = \frac{-(V_D + V_{OUT} + DCR_L \cdot I)}{L}(T_{OFF})$$

where V_D is the voltage drop across the diode, DCR_L is the series resistance of the inductor.

The pulse by pulse current limitation is effective to implement constant current protection when:

Equation 31

$$|\Delta I_{L\,TON}| = |\Delta I_{L\,TOFF}|$$

The overcurrent protection is operating over the entire output voltage, which goes from the regulated output voltage (V_{O_SET}) down to GND during heavy short circuit applied at the output.

From *Equation 29* and *Equation 30* we can gather that the implementation of the constant current protection becomes more critical the lower is the V_{OUT} and the higher is V_{IN}.

In fact, the voltage applied to the inductor during the OFF time becomes equal to the voltage drop across parasitic components (typically the DCR of the inductor and the V_{FW} of the free wheeling diode) when VOUT is negligible, while during T_{ON} the voltage applied the inductor is maximized and it is approximately equal to V_{IN}. In general the worst case scenario is heavy short-circuit at the output with maximum input voltage.

7.4.1 300 mV < V_{FB} < 1.22 V

The nominal output voltage can be written as:

Equation 32

$$V_{O\_SET} = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) = 1.22 \cdot \left(1 + \frac{R_1}{R_2}\right)$$

From *Equation 32* the voltage can be expressed as:

Equation 33

$$\left(1 + \frac{R_1}{R_2}\right) = \frac{V_{O\_SET}}{1.22}$$

so the output voltage is:

Equation 34

$$V_O = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) = V_{FB} \cdot \frac{V_{O\_SET}}{1.22}$$

The *Equation 29* and *Equation 30* in overcurrent conditions can be simplified to:

Equation 35

$$\Delta I_{L\,TON} = \frac{V_{IN} - (DCR_L + R_{DSON}) \cdot I}{L}(T_{ON\,MIN}) \cong \frac{V_{IN}}{L}(90ns)$$

considering T_{ON} that has been already reduced to its minimum.

Equation 36

$$\Delta I_{L\,TOFF} = \frac{-(V_D + V_{O\_MIN} + DCR_L \cdot I)}{L}(T_{SW} - 90ns) \cong \frac{-\left(V_D + V_{FB} \cdot \frac{V_{O\_SET}}{1.22} + DCR_L \cdot I\right)}{L}(1.18\mu s)$$

where $T_{SW}=1/f_{SW}$ and considering the nominal f_{SW}.

The voltage divider introduces a gain factor K between the V_{O_SET} and V_{FB} that affect the effectiveness of the current protection. The worst case scenario is the minimum K, that is the minimum output voltage, over the input voltage (*Chapter 5.2: Minimum output voltage over V_{IN} range*).

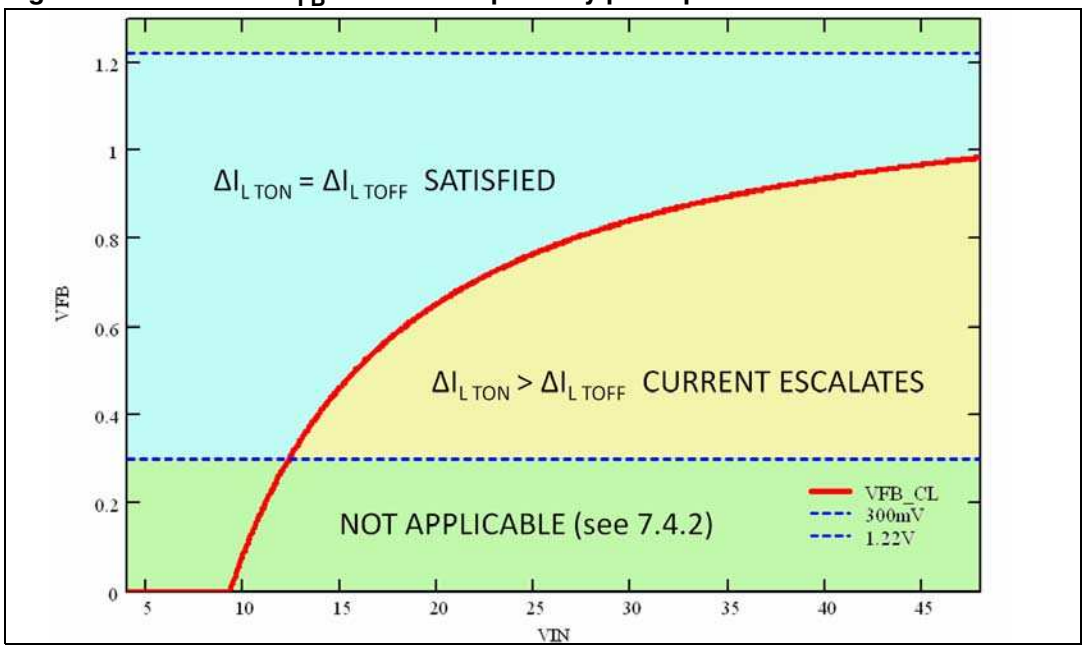
As a consequence the minimum feedback voltage to keep the inductor current limited over the input voltage range can be expressed making *Equation 35* equal to *Equation 36* and expressing V_{O_SET} as given in *Equation 1*:

Equation 37

$$V_{FB}(V_{IN}) = 1.22 - \left(\frac{1.22 \cdot T_{SW}}{V_{IN} \cdot T_{ON\_MIN}} \cdot (V_D + (I_L \cdot DCR))\right)$$

Equation 37 expresses the worst case scenario as it considers the minimum K gain of the voltage divider over the entire input voltage range. The *Figure 16* plots the *Equation 37* considering the minimum value of the peak current limit given in *Table 6: Electrical characteristics on page 6*.

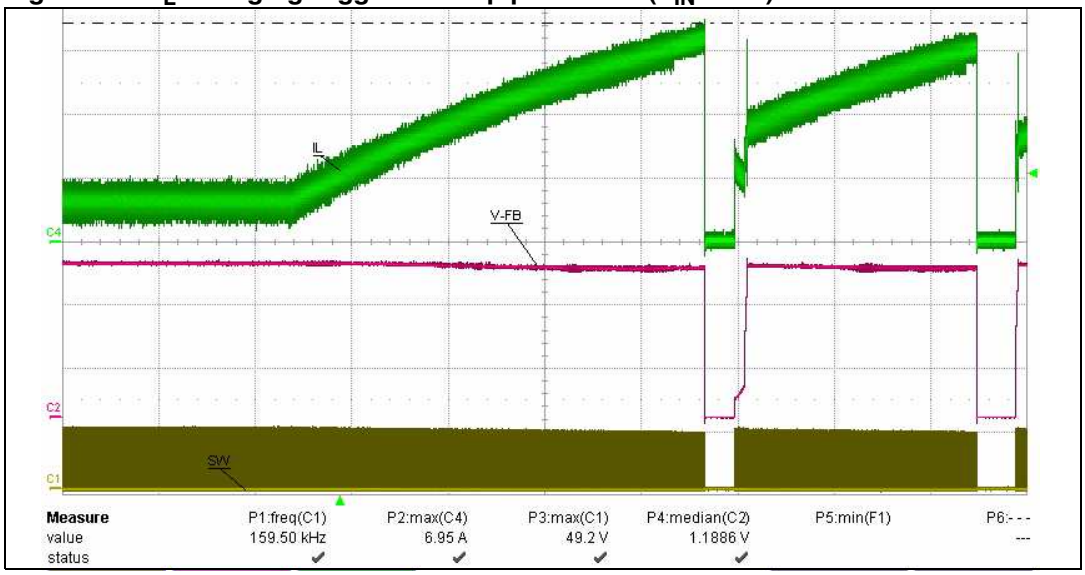
Figure 16. Minimum V_{FB} for effective pulse by pulse protection over VIN



As a consequence for VIN > 12V the pulse by pulse current protection (in the worst case scenario which is minimum V_{OSET}) could not be effective to limit the inductor current to the peak current limitation over entire FB range 300mV < V_{FB} < 1.22V.

In fact at higher input voltage $\Delta I_{L\ TON}$ could be higher than $\Delta I_{L\ TOFF}$ and so the inductor current could escalate. The system typically meets the *Equation 31* at a current level higher than the nominal value thanks to the voltage drop across stray components.

Figure 17. I_L diverging triggers hiccup protection (V_{IN}= 48V)



In most of the application condition the pulse by pulse current limitation is effective to limit the inductor current.

Whenever the current escalates, a second level current protection called “hiccup mode” is enabled. In case the hiccup current level (6.2A typical) is triggered the switching activity is prevented for 16ms and then a new soft start phase takes place (see *Figure 17*).

7.4.2 V_{FB} < 300 mV

The device reduces the switching frequency five time than the nominal value when V_{FB}<300mV. The frequency foldback makes the pulse by pulse current protection effective to keep the current limited when the output voltage is shorted and V_{OUT} negligible.

The *Equation 29* and *Equation 30* in overcurrent conditions can be simplified to:

Equation 38

$$\Delta I_{L\,TON} = \frac{V_{IN} - (DCR_L + R_{DSON}) \cdot I}{L}(T_{ON\,MIN}) \cong \frac{V_{IN}}{L}(90ns)$$

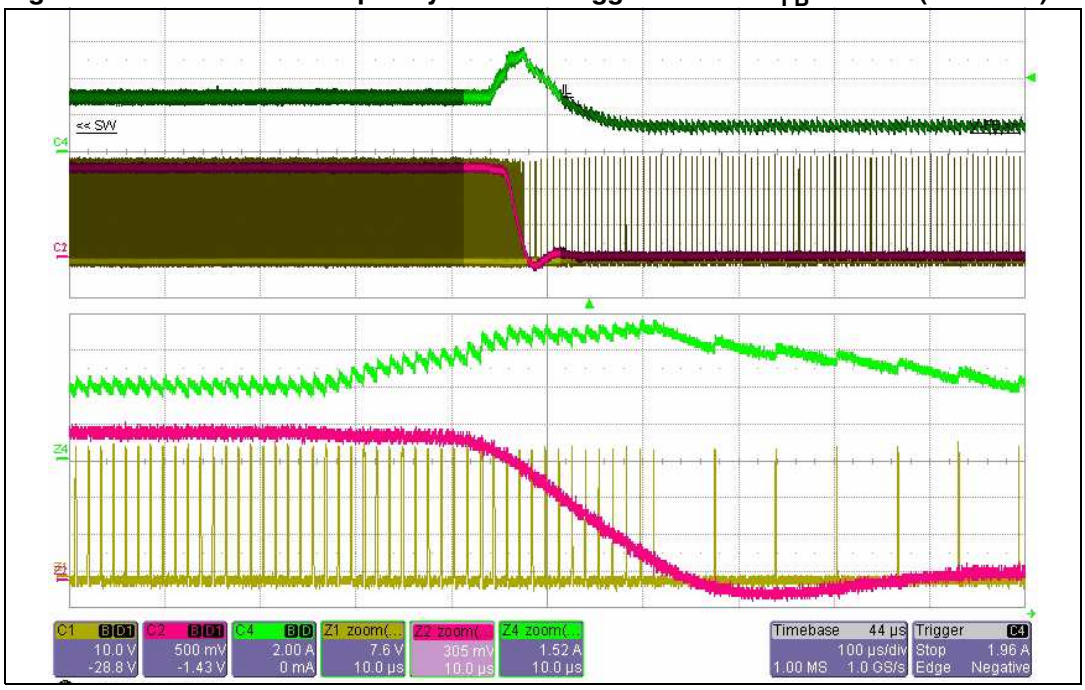
considering T_{ON} that has been already reduced to its minimum.

Equation 39

$$\Delta I_{L\,TOFF} = \frac{-(V_D + V_{O\_MIN} + DCR_L \cdot I)}{L}\left(\frac{T_{SW}}{5} - 90ns\right) \cong \frac{-\left(V_D + V_{FB} \cdot \frac{V_{O\_SET}}{1.22} + DCR_L \cdot I\right)}{L}(5.9\mu s)$$

taking in consideration the frequency foldback feature.

Figure 18. Current and frequency foldback triggered when V_{FB}<300mV (red trace)



The content given in *Chapter 7.4.1* is valid and the equivalent expression of *Equation 37* is:

Equation 40

$$V_{FB}(V_{IN}) = \frac{1.22}{5} - \left(\frac{1.22 \cdot T_{SW}}{V_{IN} \cdot T_{ON\_MIN}} \cdot (V_D + (I_L \cdot DCR))\right)$$

The *Figure 19* plots the *Equation 40* considering the foldback current limitation threshold (1.45A) given in *Table 6: Electrical characteristics on page 6*.

Equation 40 expresses the worst case scenario as it considers the minimum K gain of the voltage divider over the entire input voltage range (see *Figure 14*).

In most of the application conditions the pulse by pulse current limitation with frequency foldback is effective to limit the inductor current in short circuit condition. The current foldback helps to decrease the power component stress in persistent short circuit condition.

The hiccup protection offers an additional protection against heavy short circuit condition at very high input voltage even considering the spread of the minimum conduction time of the power element. In case the hiccup current level (6.2A typical) is triggered the switching activity is prevented for 15ms and then a new soft start phase takes place.

Figure 19. Minimum V_{FB} for effective pulse by pulse protection over VIN

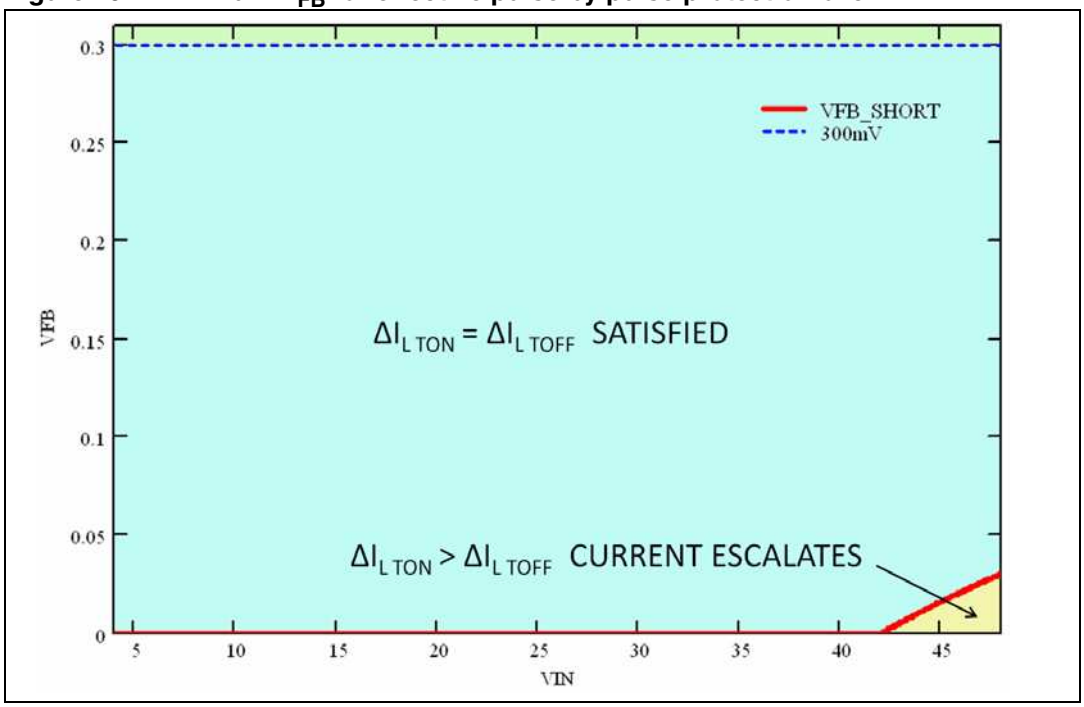


Figure 20 shows the effectiveness of the constant current protection limiting the inductor current to the peak current of 1.45A typical during a short circuit event.

Figure 20. Short-circuit current V_{IN} = 24V ($I_{L\_PK} = I_{FOLD}$)

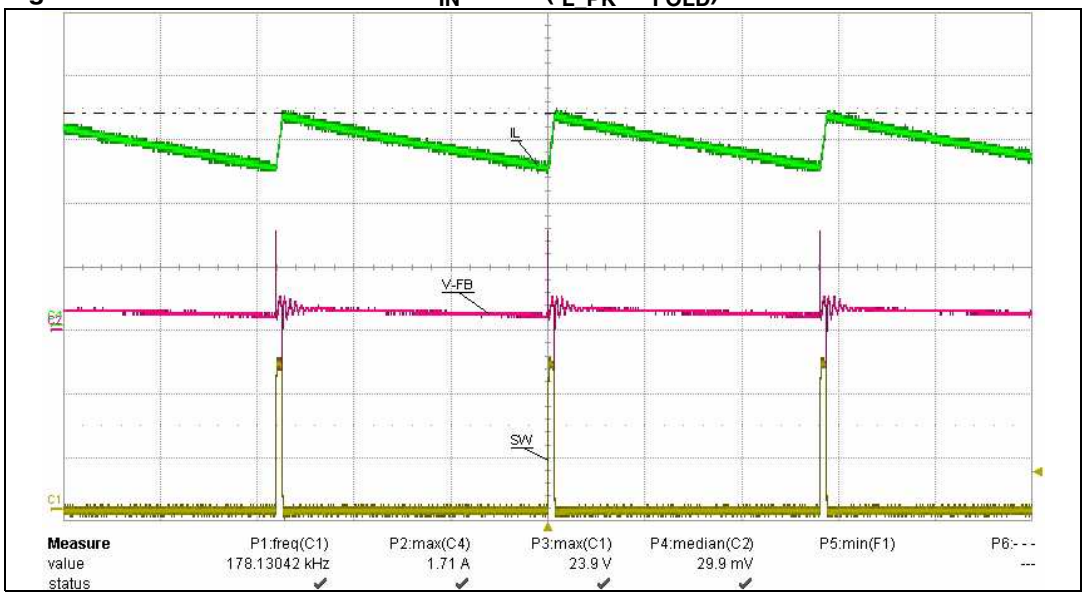
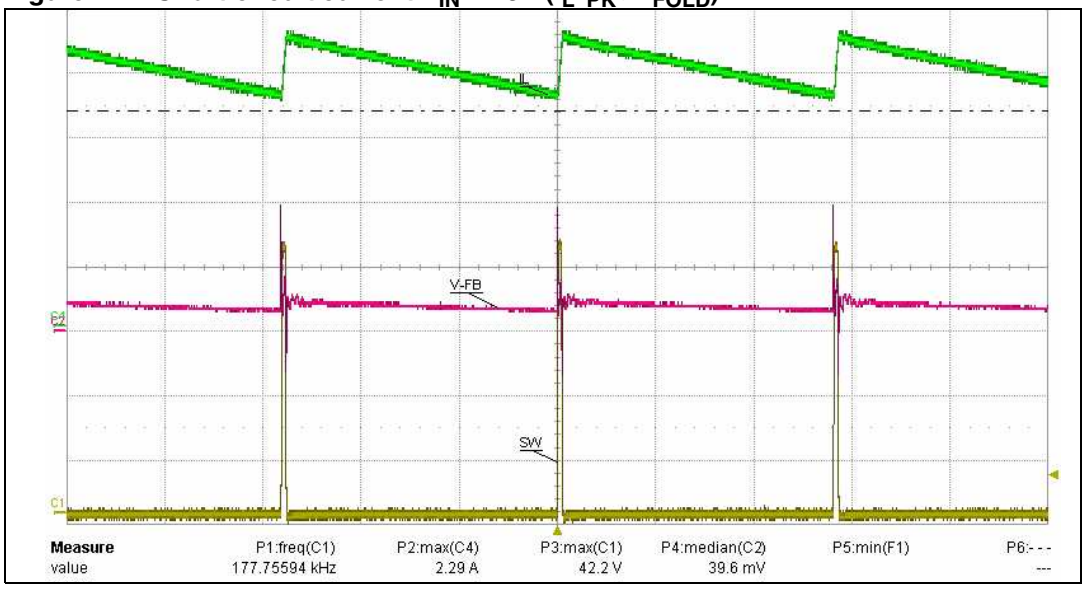


Figure 21 shows the operation of the constant current protection when a short circuit is applied at the output at the maximum input voltage. Accordingly to *Figure 20* the maximum inductor current escalates over the foldback current limitation.

Figure 21. Short-circuit current V_{IN} = 43V ($I_{L\_PK} > I_{FOLD}$)



7.5 Application circuit

Figure 22. Evaluation board application circuit

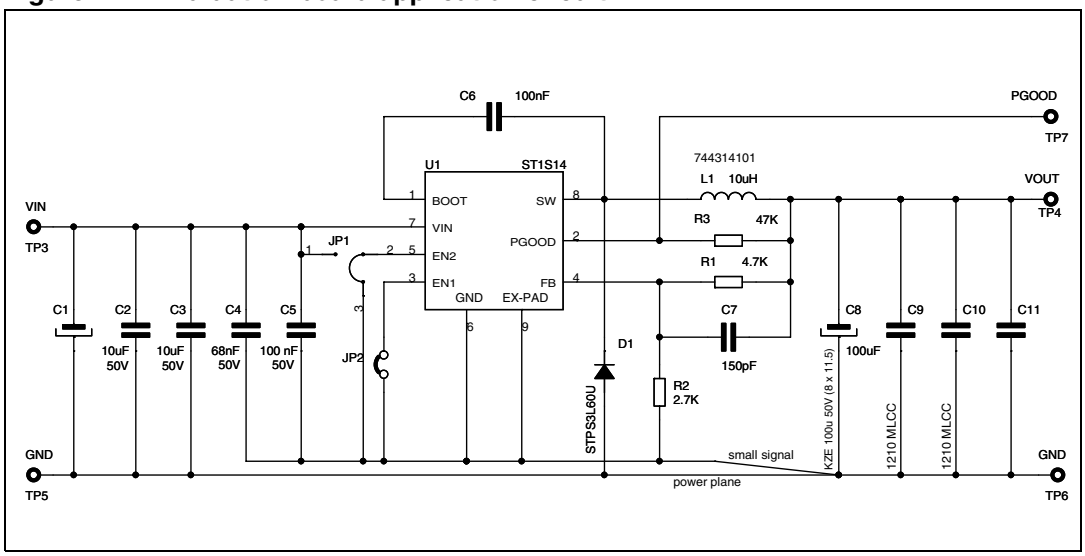


Table 11. Component list

Reference	Part number	Description	Manufacturer
C2, C3	UMK325BJ106MM-T	10 µF 50V (size 1210)	Taiyo Yuden
C6,C6		100nF 50V (size 0603)	
C7		150pF 50V (size 0603)	
C8	EKZE500ESS101MHB5D	100 µF 50V (size 8 x 11.5 mm)	Nippon Chemicon
C1,C9,C10,C11		NOT MOUNTED	
R1		4.7 KΩ (size 0603)	
R2		2.7 KΩ (size 0603)	
R3		47 KΩ (size 0603)	
D1	STPS3L60U	3A 60V (size SMB)	STMicroelectronics
L1	744314850	8.5µH I_{SAT}=4.5A, I_{RMS}=4A (size 7 x 6.9 x 4.8 mm)	Wurth

Figure 23. PCB layout (component side)

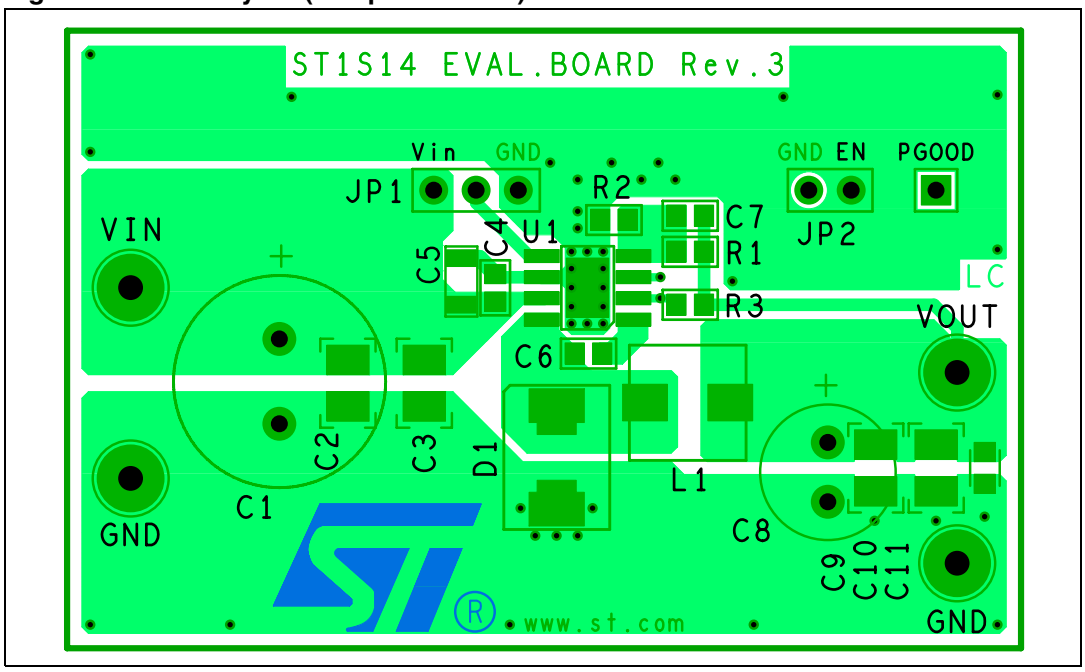
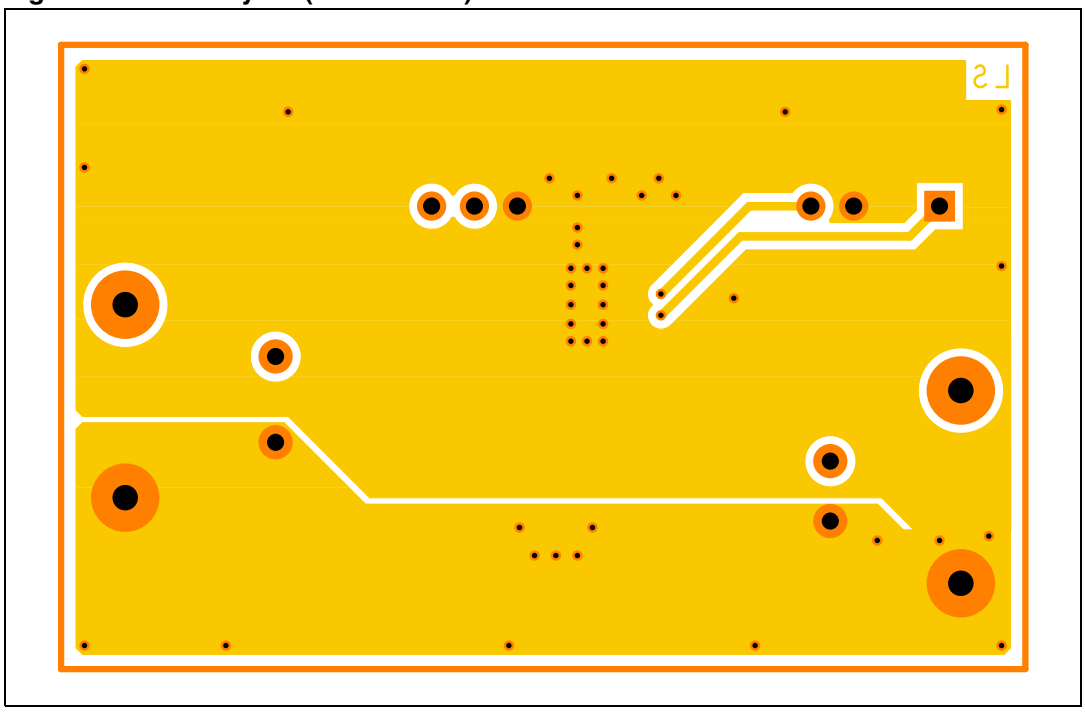


Figure 24. PCB layout (bottom side)



8 Typical characteristics

Figure 25. Line regulation

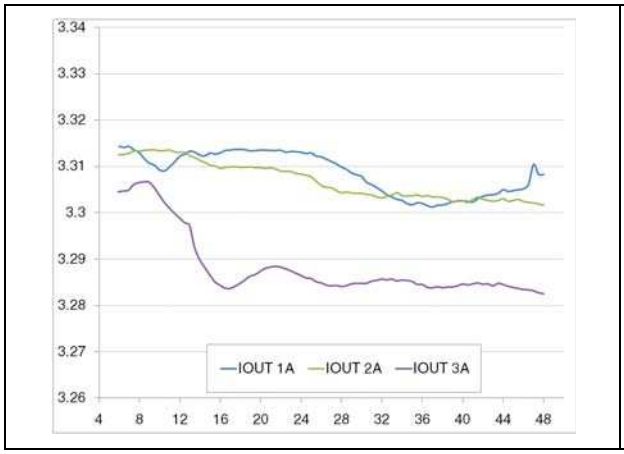


Figure 26. Load regulation

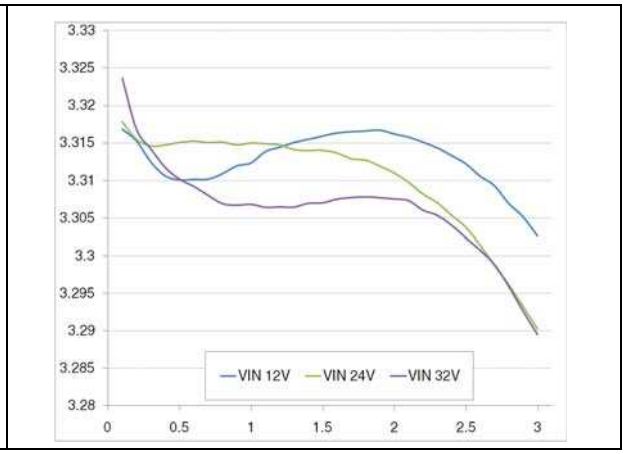


Figure 27. R_{DSon} vs temperature (V_{IN} = 12 V)

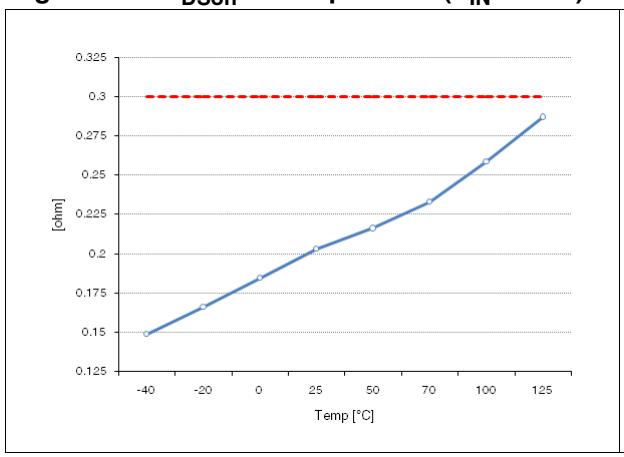


Figure 28. V_{FB} vs temperature (V_{IN} = 12 V)

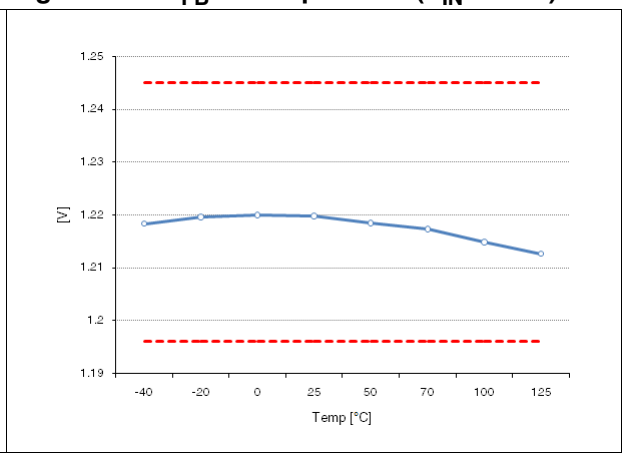


Figure 29. f_{SW} vs temperature

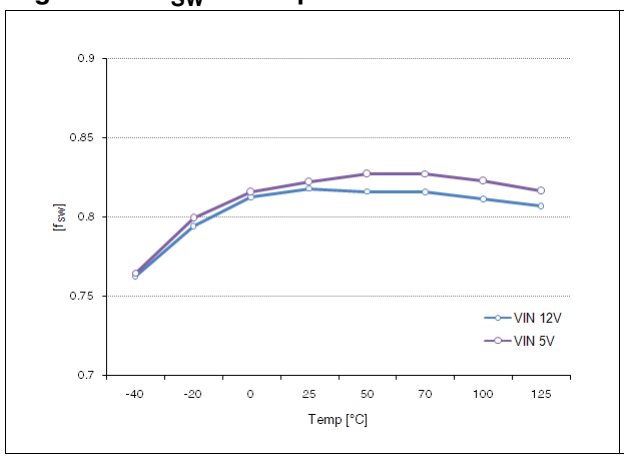


Figure 30. Quiescent current vs temperature

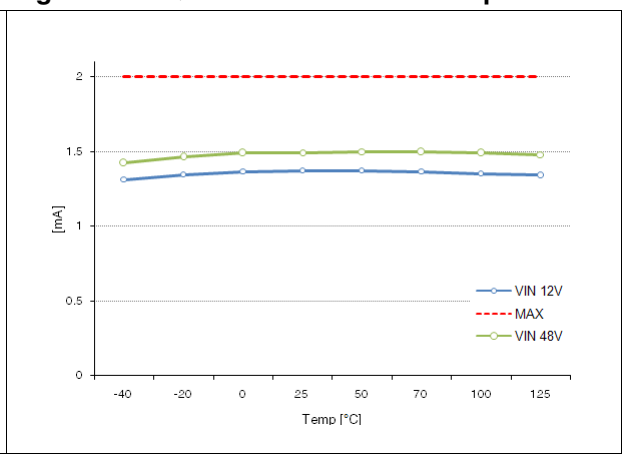


Figure 31. Shutdown current vs temperature

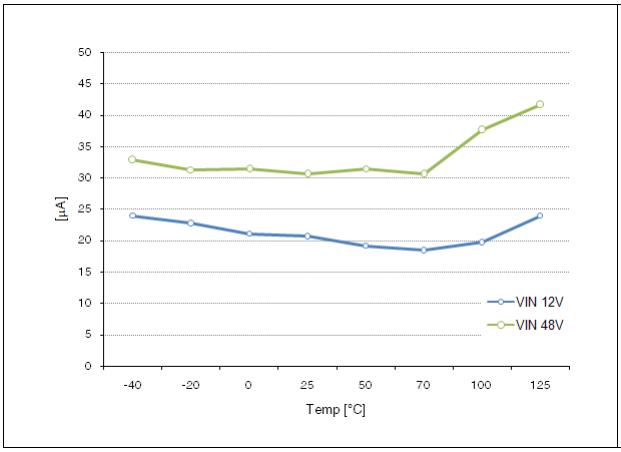


Figure 32. Duty cycle max vs temperature

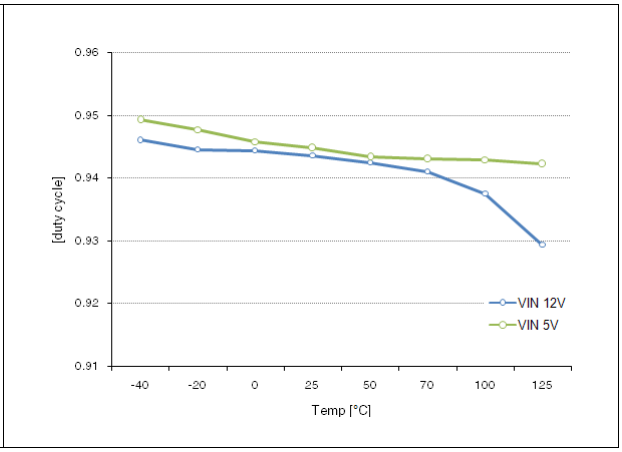


Figure 33. Efficiency vs I_{OUT} (V_{IN} 12 V)

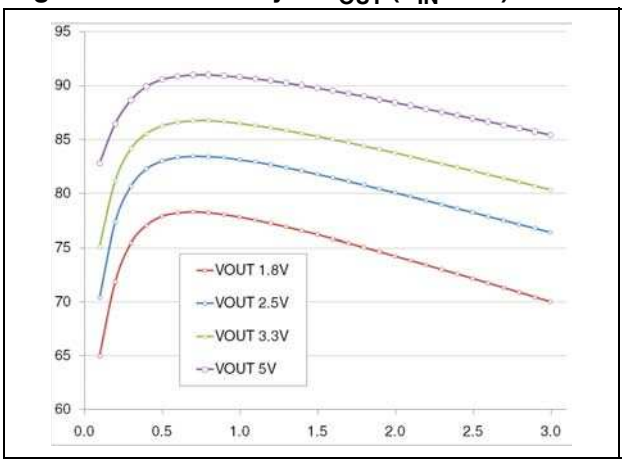


Figure 34. T_J vs I_{OUT} (V_{IN} 12 V)

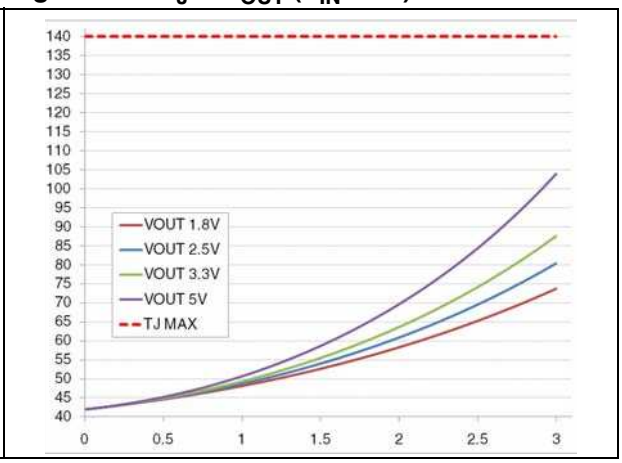


Figure 35. Efficiency vs I_{OUT} (V_{IN} 24 V)

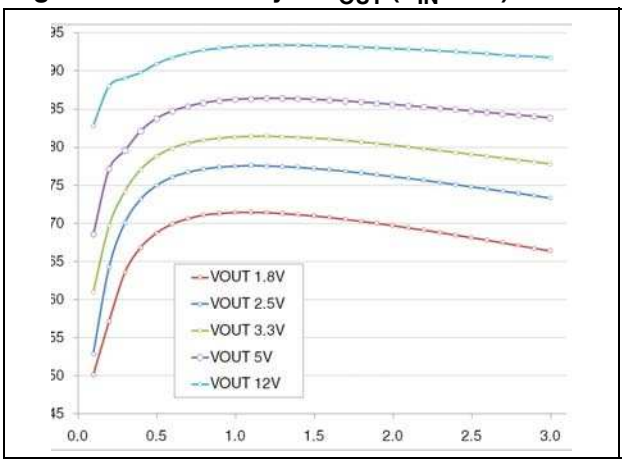


Figure 36. T_J vs I_{OUT} (V_{IN} 24 V)

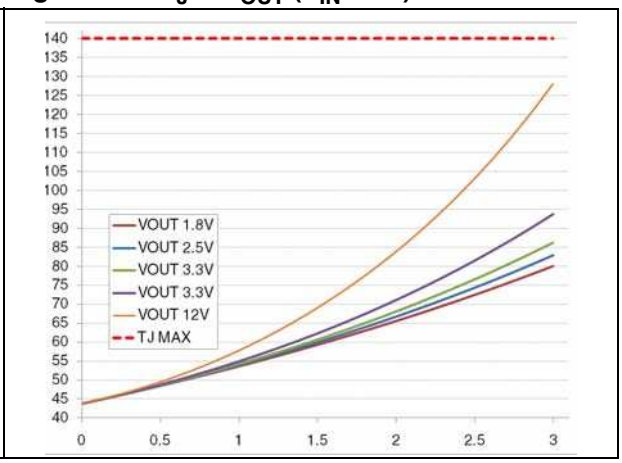


Figure 37. Efficiency vs I_{OUT} (V_{IN} 32 V)

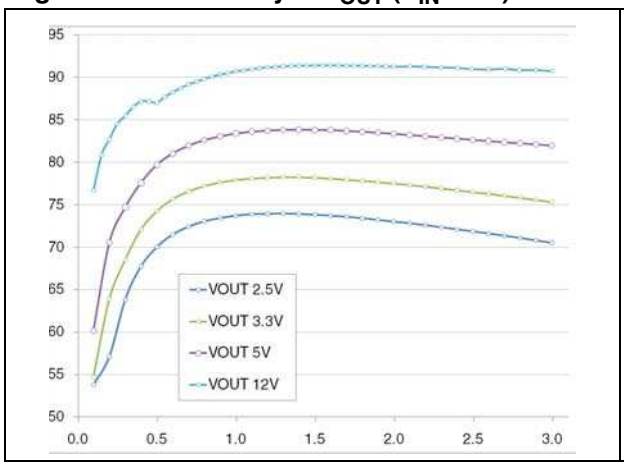


Figure 38. T_J vs I_{OUT} (V_{IN} 32 V)

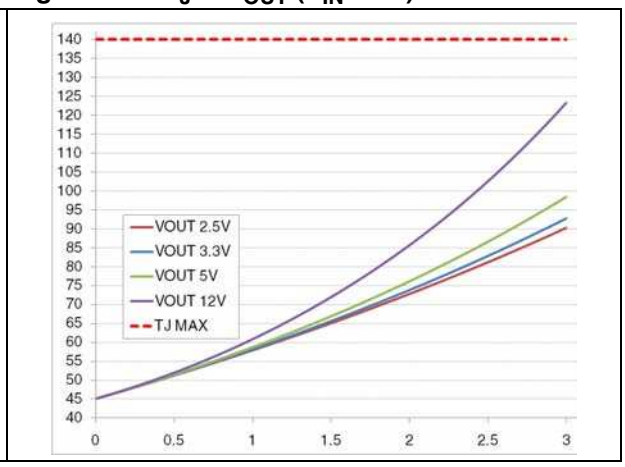


Figure 39. 1 A to 3 A load transient (V_{IN} 12 V)

Figure 40. Zoom - 1 A to 3 A load transient (V_{IN} 12 V)

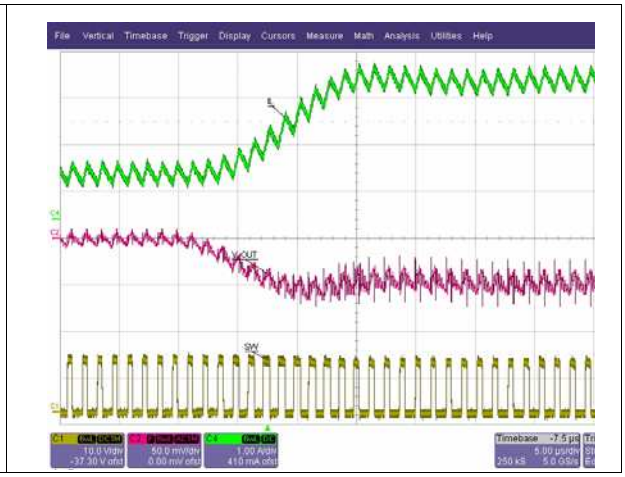


Figure 41. Zoom - 1 A to 3 A rising edge load transient (V_{IN} 12 V)

Figure 42. 1 A to 3 A falling edge load transient (V_{IN} 24 V)

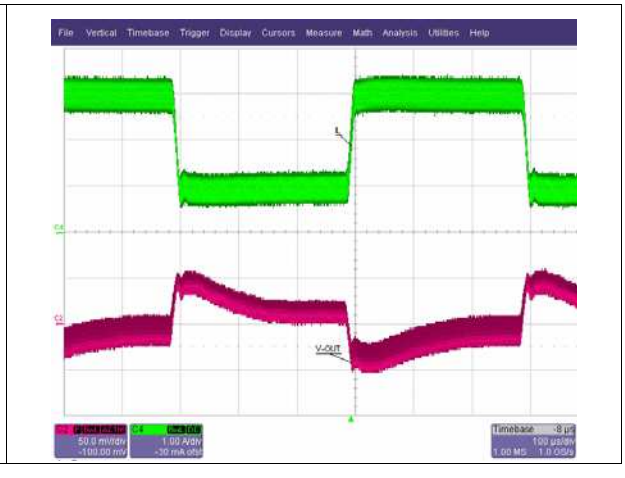


Figure 43. Zoom - 1 A to 3 A rising edge load transient (V_{IN} 24 V)

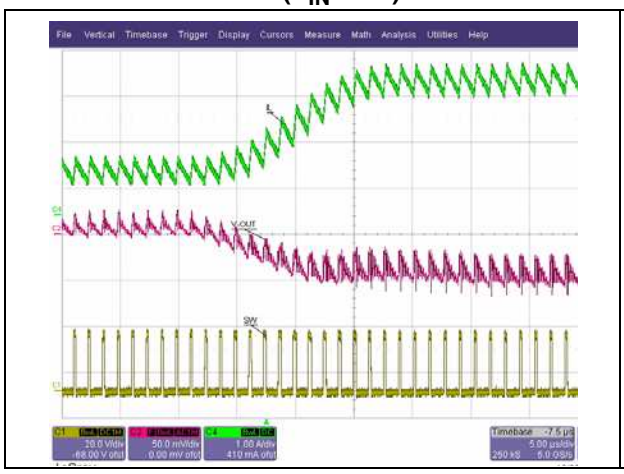


Figure 44. Zoom - 1 A to 3 A falling edge load transient (V_{IN} 24 V)

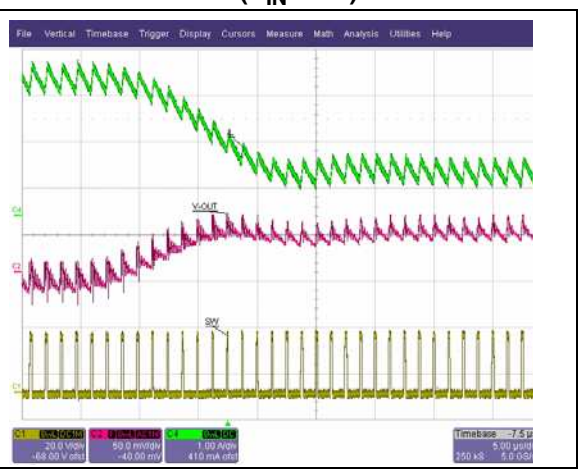


Figure 45. 1 A to 3 A load transient (V_{IN} 32 V)

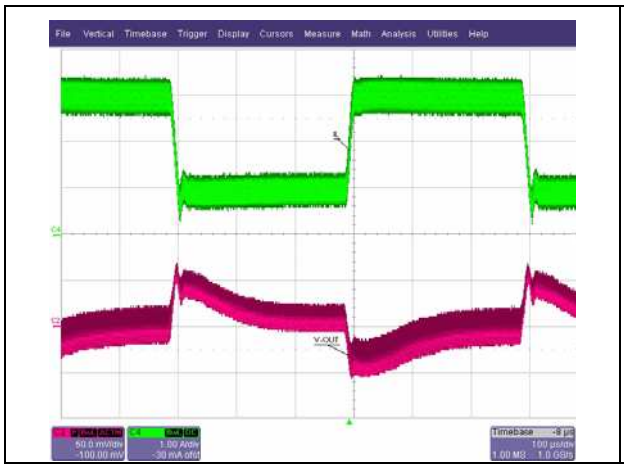


Figure 46. Zoom - 1 A to 3 A rising edge load transient (V_{IN} 32 V)

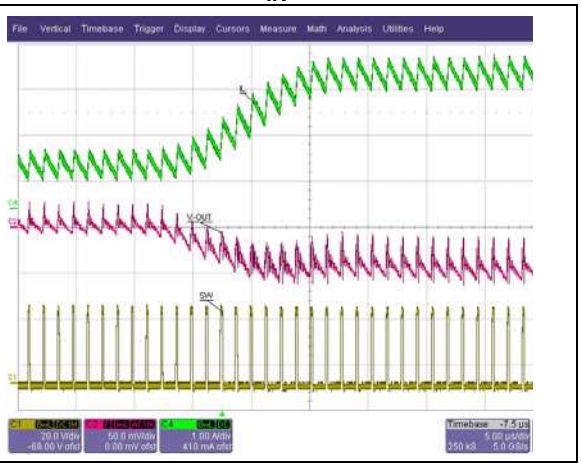
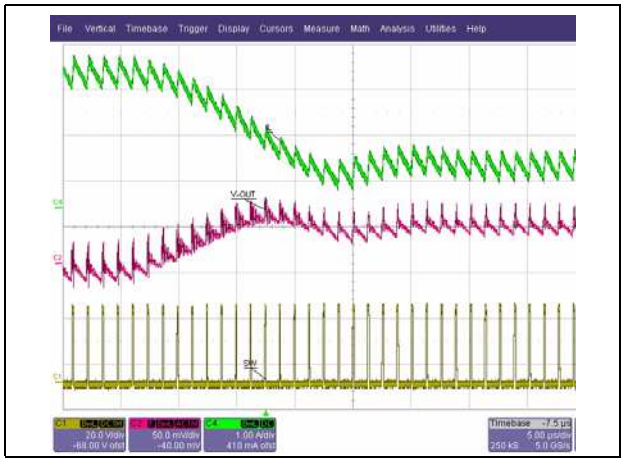


Figure 47. Zoom - 1 A to 3 A falling edge load transient (V_{IN} 32 V)



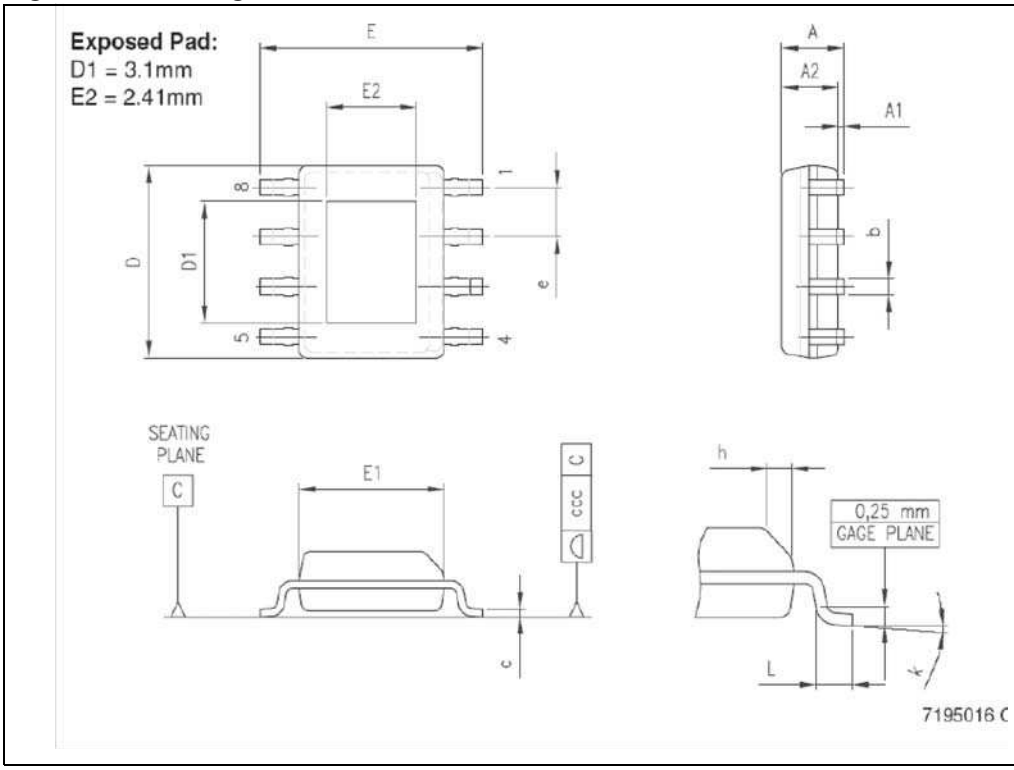
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 12. HSOP8 mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.70			0.0669
A1	0.00		0.10		0.00	0.0039
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
D1	3	3.1	3.2	0.118	0.122	0.126
E	5.80	6.00	6.20	0.2283		0.2441
E1	3.80	3.90	4.00	0.1496		0.1575
E2	2.31	2.41	2.51	0.091	0.095	0.099
e		1.27				
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0° (min), 8° (max)					
ccc			0.10			0.0039

Figure 48. Package dimensions



10 Order code

Table 13. Ordering information

Order code	Package
ST1S14PHR	HSOP8 - exposed pad

11 Revision history

Table 14. Document revision history

Date	Revision	Changes
27-Oct-2010	1	Initial release

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