

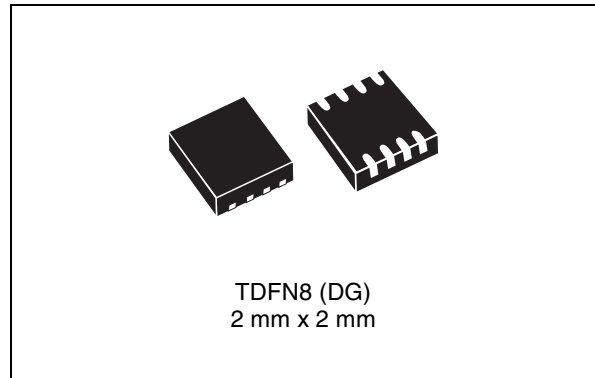


## STM6522

### Dual push-button Smart Reset™ with capacitor-adjustable setup delay

#### Features

- Dual Smart Reset™ push-button inputs with capacitor-adjustable extended reset setup delay ( $t_{SRC}$ )
- No power-on reset
- Dual  $\overline{RST}$  output, active-low, open-drain
- Fixed Smart Reset™ input logic voltage levels
- Broad operating voltage range 1.65 V to 5.5 V, inactive reset output levels valid down to 1.0 V
- Low supply current (1.5  $\mu$ A)
- Operating temperature:  
industrial grade  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- TDFN8 package: 2 mm x 2 mm x 0.75 mm
- RoHS compliant



#### Applications

- Mobile phones, smartphones
- e-books
- MP3 players
- Games
- Portable navigation devices
- Any application that requires delayed reset push-button(s) response for improved system stability

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# 1 Description

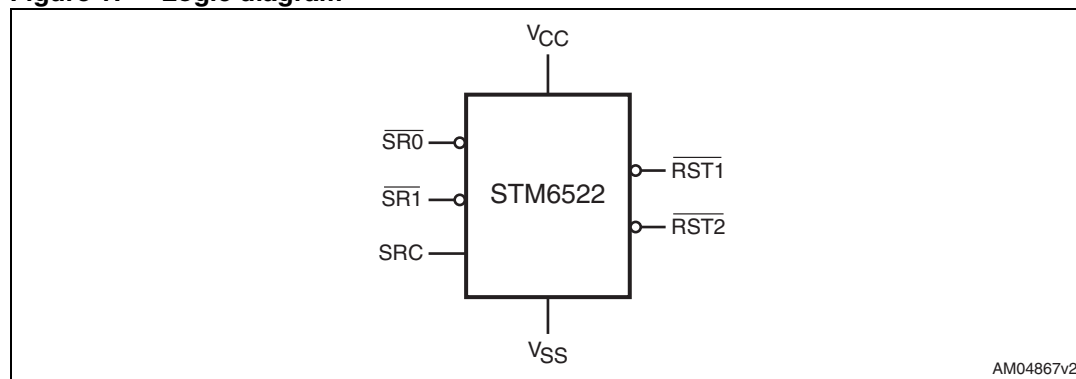
The Smart Reset™ devices provide a useful feature that ensures that inadvertent short reset push-button closures do not cause system resets as the extended Smart Reset™ delay setup periods are implemented. Once the valid Smart Reset™ input levels and setup delay are met, the device generates an output reset pulse for a fixed timeout period ( $t_{REC}$ ).

The typical application hookup shows that either a single Smart Reset™ input, or both reset inputs can be connected to the applications interrupt and control both the interrupt pin and the hard reset functions. If the push-button is closed for a short time, the processor is only interrupted. If the system still does not respond properly, holding the push-button(s) for the extended setup time ( $t_{SRC}$ ) causes a hard reset of the processor. The Smart Reset™ feature helps significantly increase system stability and eliminates the need for a dedicated reset button.

The STM65xx family of Smart Reset™ devices consists of low-current microprocessor reset circuits targeted at applications such as MP3 players, portable navigation or mobile phones, generally any application that requires delayed reset push-button(s) response for improved system stability. The devices in the STM65xx Smart Reset™ family include various combinations of useful features for the targeted applications.

The STM6522 has two combined Smart Reset™ inputs ( $\overline{SR0}$  and  $\overline{SR1}$ ) with delayed reset setup time ( $t_{SRC}$ ) programmed by an external capacitor on the SRC pin.

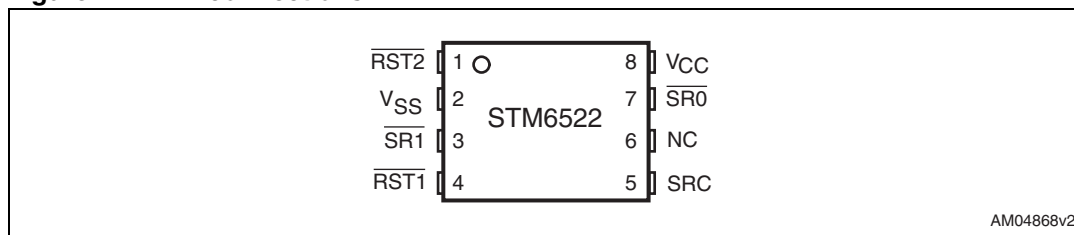
Figure 1. Logic diagram



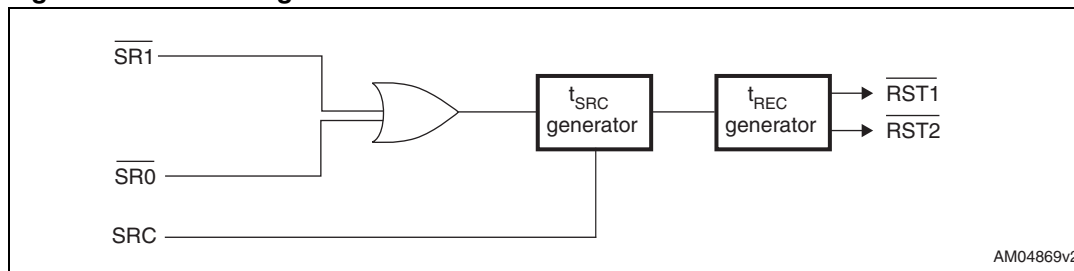
**Table 1. Signal names**

Symbol	Input/output	Description
$\overline{RST1}$	Output	Open-drain reset output, active-low, no internal pull-up resistor.
$\overline{RST2}$	Output	Open-drain reset output, active-low, no internal pull-up resistor.
$\overline{SR0}$	Input	Primary push-button Smart Reset™ input, active-low, fixed voltage input logic levels, no internal pull-up.
$\overline{SR1}$	Input	Secondary push-button Smart Reset™ input - combines with the primary push-button reset to provide setup delay time, active-low, fixed voltage input logic levels, no internal pull-up.
SRC	Input	Smart Reset™ input delay setup control: connect to an external capacitor to adjust the delay setup time ( $t_{SRC}$ ).
$V_{CC}$	Supply	Supply voltage input. Power supply for the device. A 0.1 $\mu F$ decoupling ceramic capacitor is recommended to be connected between $V_{CC}$ and $V_{SS}$ pins.
$V_{SS}$	Supply	Supply ground.
NC		No connect (not bonded); should be connected to $V_{SS}$ .

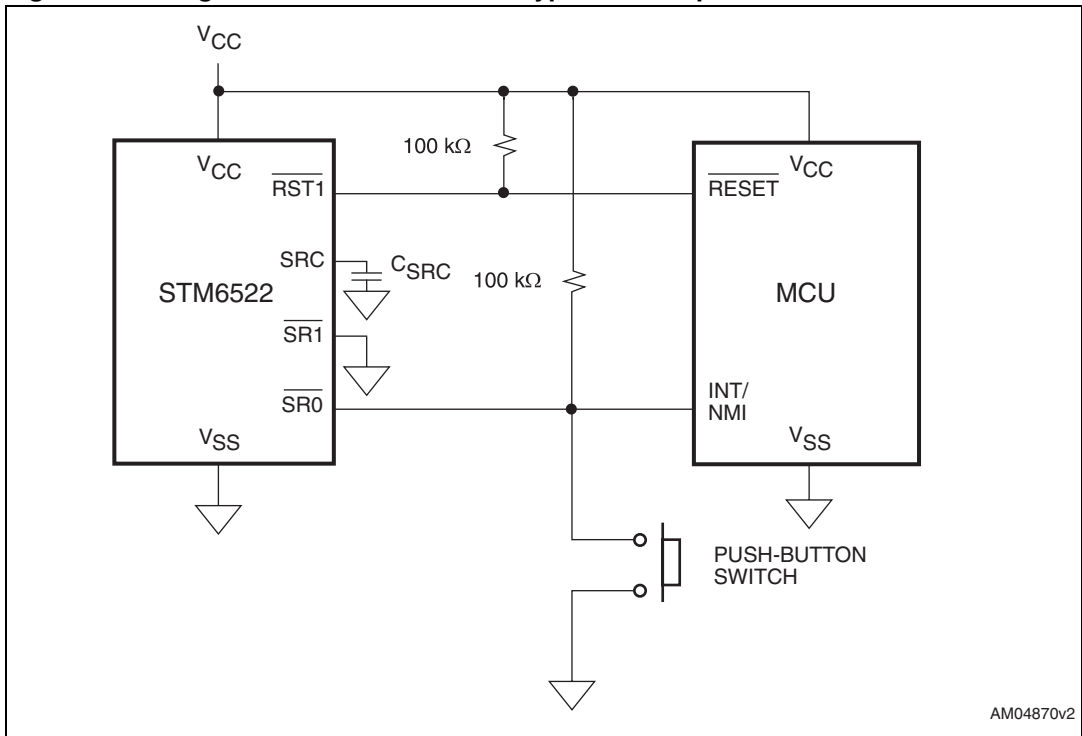
**Figure 2. Pin connections**



**Figure 3. Block diagram**



**Figure 4. Single-button Smart Reset™ typical hookup**



**Figure 5. Dual-button Smart Reset™ typical hookup**

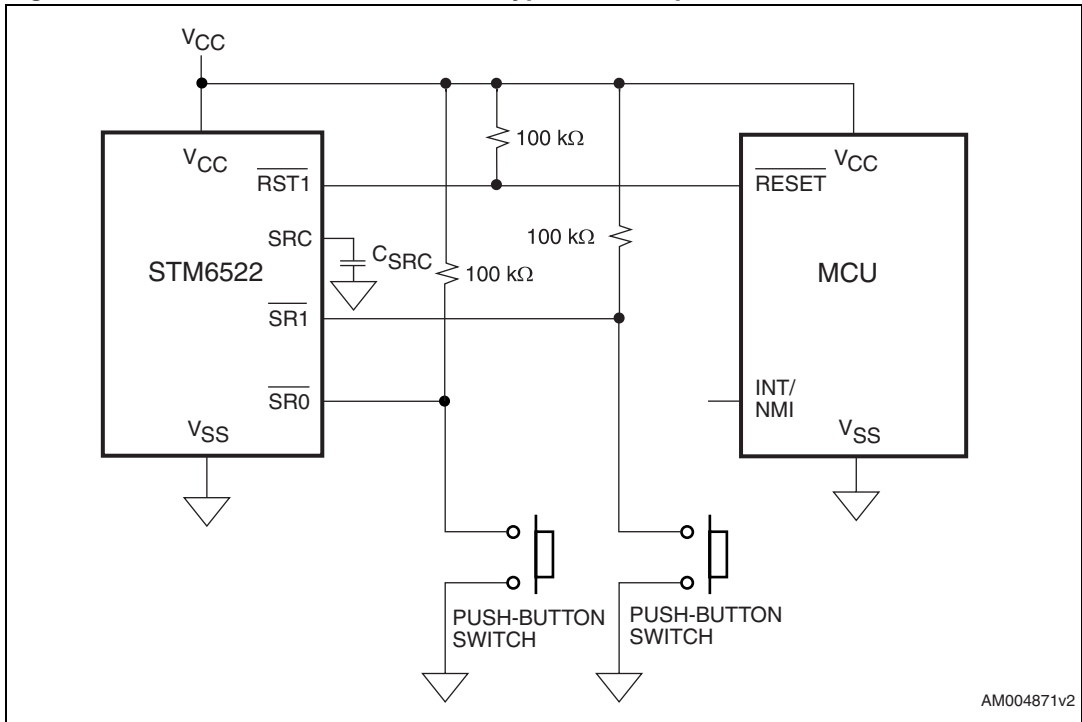
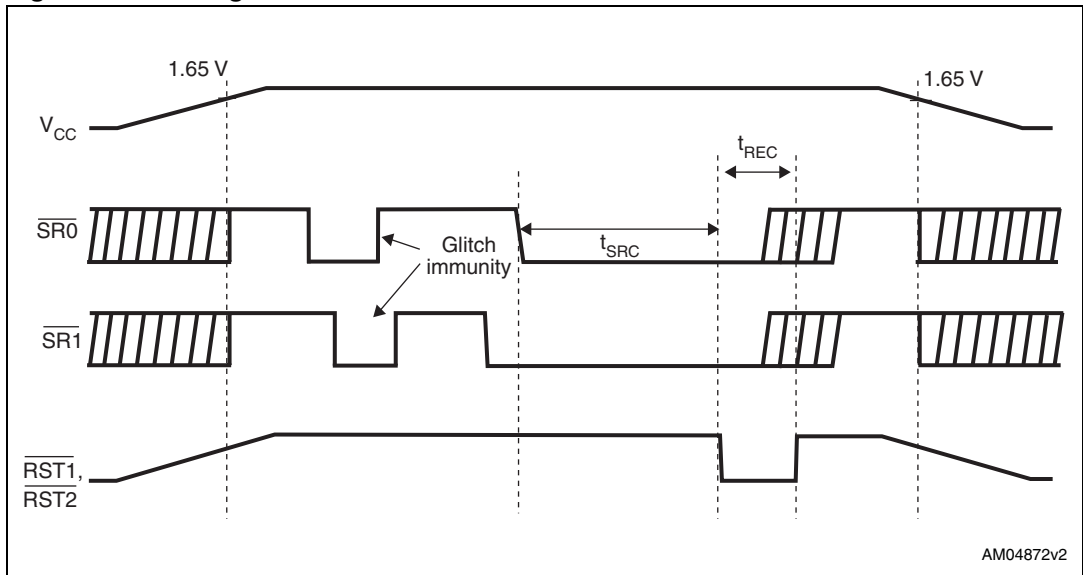


Figure 6. Timing waveforms



## 2 Pin descriptions

### 2.1 Power supply ( $V_{CC}$ )

This pin is used to provide the power to the device. A 0.1  $\mu\text{F}$  decoupling ceramic capacitor is recommended to be connected between  $V_{CC}$  and  $V_{SS}$  pins.

### 2.2 Ground ( $V_{SS}$ )

This is the supply ground for the device.

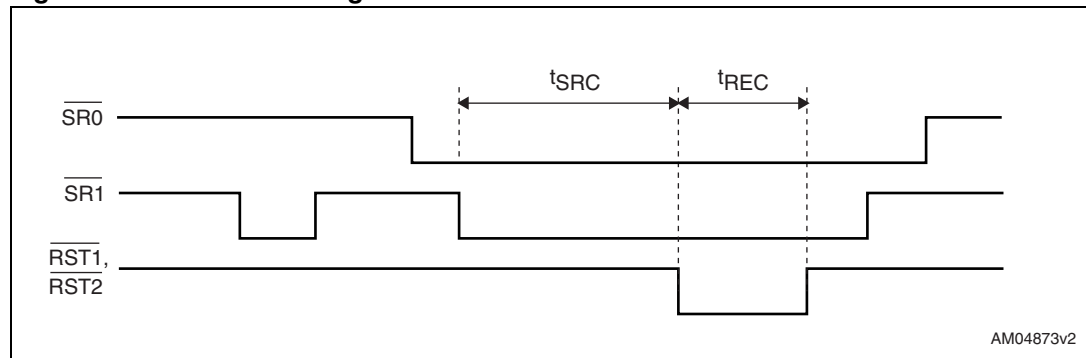
### 2.3 Primary Smart Reset™ input ( $\overline{\text{SR0}}$ )

The primary push-button Smart Reset™ input, active-low pin is connected to the push-button switch. The input logic voltage levels are set to a fixed voltage level and have no internal pull-up resistor.

### 2.4 Secondary Smart Reset™ input ( $\overline{\text{SR1}}$ )

The secondary push-button Smart Reset™ input, active-low pin is connected to the second push-button switch. The input logic voltage levels are set to a fixed voltage level and have no internal pull-up resistor. Keeping both Smart Reset™ inputs  $\overline{\text{SR0}}$  and  $\overline{\text{SR1}}$  active for longer than  $t_{\text{SRC}}$  activates the reset output pulse.

**Figure 7. STM6522 timing**



Reset is asserted “low” right after the Smart Reset™ setup delay ( $t_{\text{SRC}}$ ) has been met and returns to high after the  $t_{\text{REC}}$  period.

## 2.5 Adjustable delay of Smart Reset™ (SRC pin)

This pin controls the setup time before the push-button action is validated by the reset output. It is connected to an external capacitor ( $C_{SRC}$ ), which is tied to ground to provide the desired value of setup time ( $t_{SRC}$ ).

Selected calculated  $t_{SRC}$  and  $C_{SRC}$  examples are given in [Table 2](#). Refer also to [Table 5](#).

**Table 2.  $t_{SRC}$  programmed by an ideal external capacitor**

Calculated $C_{SRC}$ value [ $\mu$ F]	Setup delay $t_{SRC}$ [s] <sup>(1)(2)</sup>			Closest common $C_{SRC}$ value [ $\mu$ F]
	Min.	Typ.	Max.	
0.2	2	2.5	3.0	0.22
0.3	3	3.75	4.5	0.33
0.6	6	7.5	9	0.56
1	10	12.5	15	1

1. At 25 ° C. Example calculations based on an ideal capacitor. During application design and component selection it should be considered that the current flowing into the external  $t_{SRC}$  programming capacitor ( $C_{SRC}$ ) is on the order of 100 nA, therefore a low-leakage capacitor (ceramic or film capacitor) should be used and placed as close as possible to the SRC pin. Also an adequate low-leakage PCB environment should be ensured to prevent  $t_{SRC}$  accuracy from being affected. A recommended minimum value of  $C_{SRC}$  is 0.1  $\mu$ F.
2. In case of quickly repeated activations of  $t_{SRC}$  counter, an interval of 10 ms min. is needed between the activations to fully discharge  $C_{SRC}$ , so that the next  $t_{SRC}$  is as specified.

## 2.6 Reset output ( $\overline{RST1}$ )

This output is active-low, open-drain with no internal pull-up resistor.

## 2.7 Reset output ( $\overline{RST2}$ )

This output is active-low, open-drain with no internal pull-up resistor.

### 3 Typical operating characteristics

Figure 8. Supply current ( $I_{CC}$ ) vs. temperature

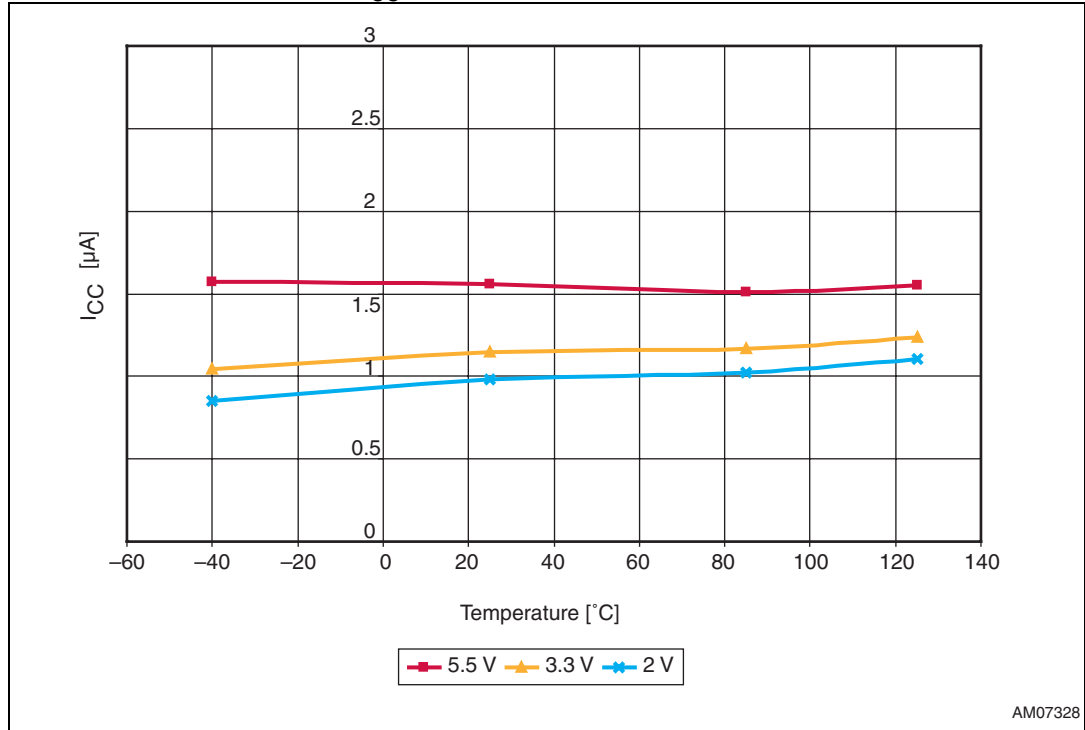


Figure 9. Smart Reset™ delay ( $t_{SRC}$ ) vs. temperature,  $C_{SRC} = 0.6 \mu$ F

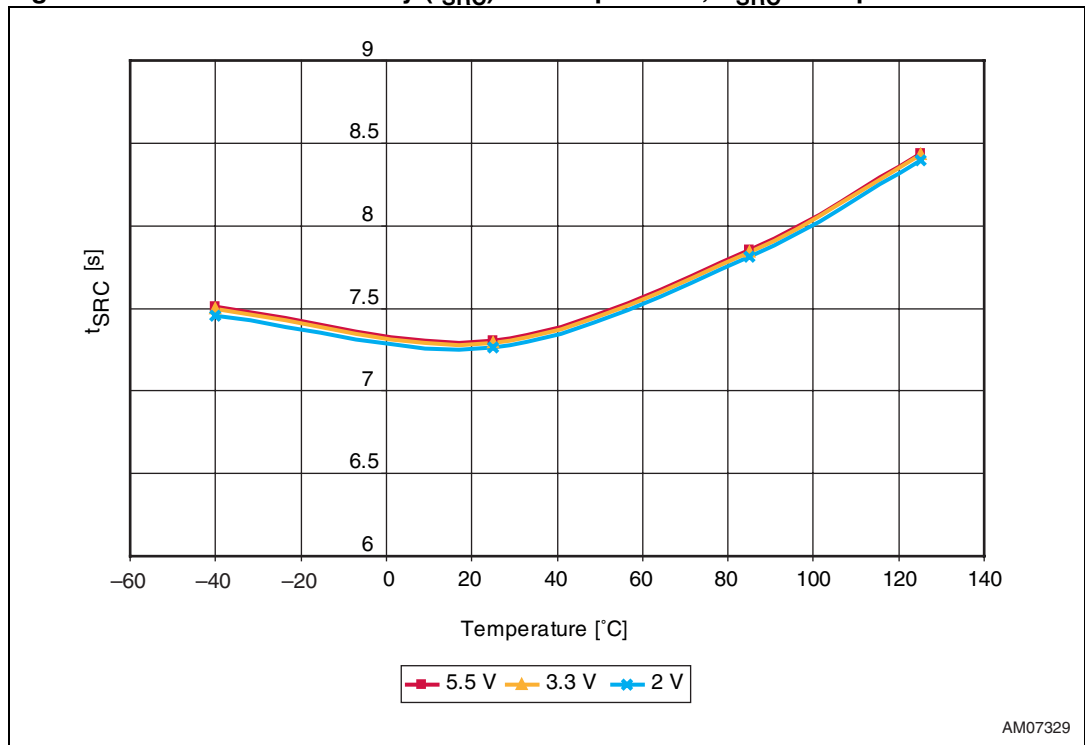


Figure 10. Reset timeout period ( $t_{REC}$ ) vs. temperature

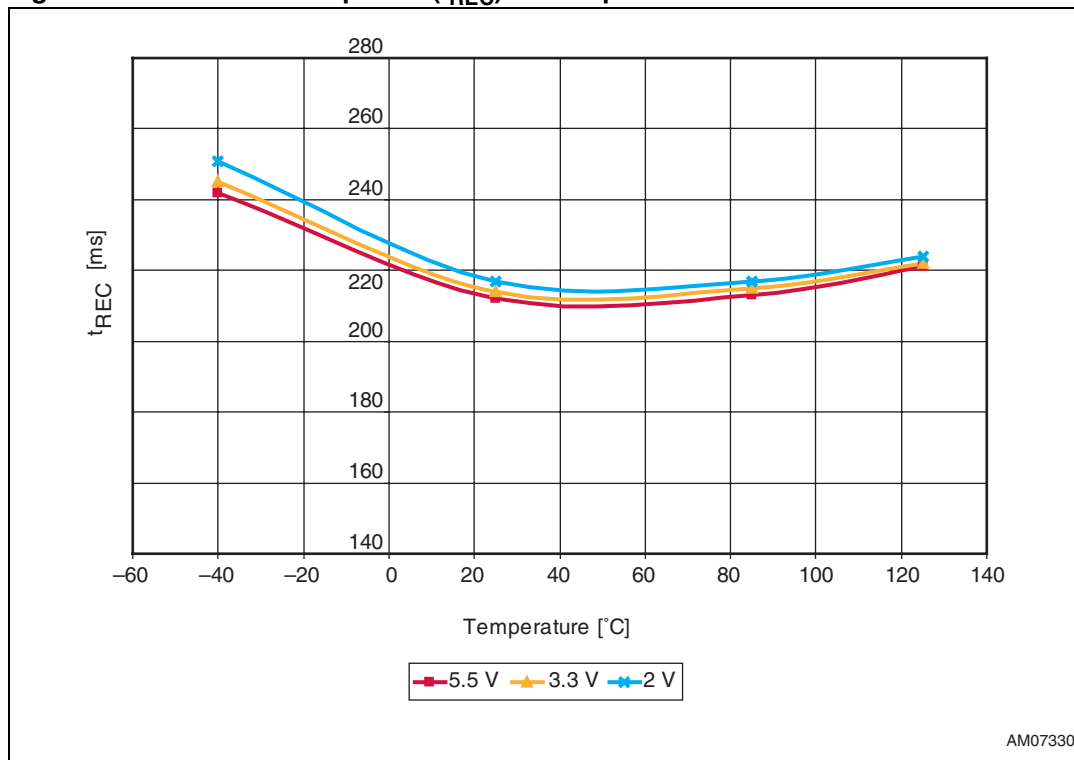
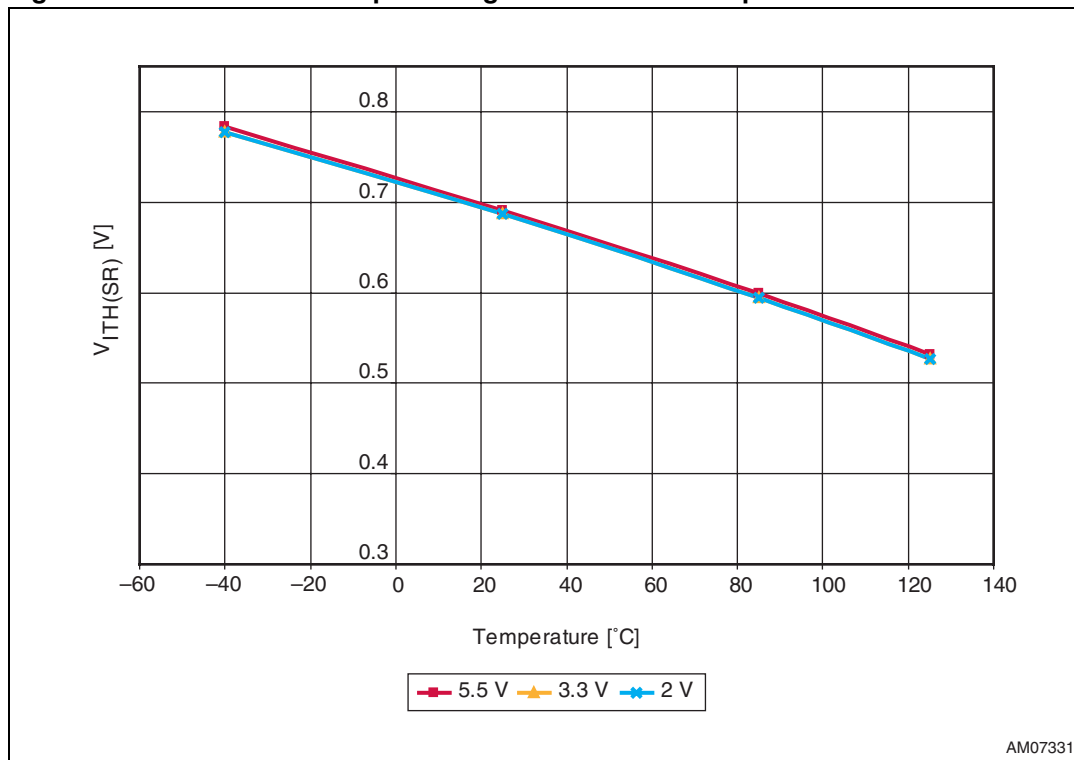


Figure 11. Smart Reset™ input voltage threshold vs. temperature



## 4 Maximum ratings

Stressing the device above the ratings listed in [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Table 4: Operating and measurement conditions](#) of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter		Value	Unit
$T_{STG}$	Storage temperature ( $V_{CC}$ off)		-55 to +150	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds		260	°C
$\theta_{JA}$	Thermal resistance (junction to ambient)	TDFN8	149.0	°C/W
$V_{IO}$	Input or output voltage		-0.3 to 5.5	V
$V_{CC}$	Supply voltage		-0.3 to 7	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

## 5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in [Table 5: DC and AC characteristics](#) that follows, are derived from tests performed under the measurement conditions summarized in [Table 4: Operating and measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 4. Operating and measurement conditions**

Parameter	Value	Unit
V <sub>CC</sub> supply voltage	1.65 to 5.5	V
Ambient operating temperature (T <sub>A</sub> )	-40 to +85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V <sub>CC</sub>	V
Input and output timing ref. voltages	0.3 to 0.7 V <sub>CC</sub>	V

**Figure 12. AC testing input/output waveforms**

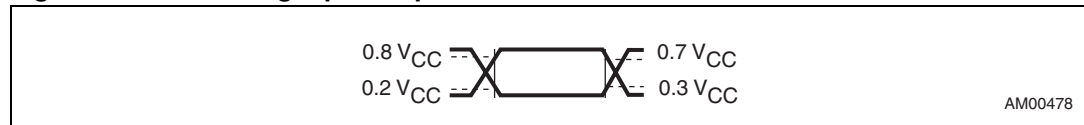


Table 5. DC and AC characteristics

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{CC}$	Supply voltage range		1.65		5.5	V
$I_{CC}$	Supply current (inputs in their inactive state, neither $t_{REC}$ nor $t_{SRC}$ in progress)	$V_{CC} = 5.0$ V		2	3	$\mu$ A
		$V_{CC} = 3.0$ V		1.5		$\mu$ A
$V_{OL}$	Reset output voltage low (active-low reset asserted)	$V_{CC} \geq 4.5$ V, sinking 3.2 mA			0.3	V
		$V_{CC} \geq 3.3$ V, sinking 2.5 mA			0.3	V
		$V_{CC} \geq 1.65$ V, sinking 1 mA			0.3	V
$t_{REC}$	Reset timeout delay, factory programmed		140	210	280	ms
<b>Smart Reset™ inputs</b>						
$V_{IL}$	$\overline{SR0}$ , $\overline{SR1}$ input voltage low		$V_{SS} - 0.3$		0.3	V
$V_{IH}$	$\overline{SR0}$ , $\overline{SR1}$ input voltage high		0.85		5.5	V
$I_{LI(SR)}$	Input leakage current, $\overline{SRx}$ input		-1		+1	$\mu$ A
<b>Smart Reset™ delay</b>						
$t_{SRC}^{(3)}$	Delayed Smart Reset™ setup time. Refer to <a href="#">Table 2</a> .	$T_A = 25$ °C	$10 \times C_{SRC}$ ( $\mu$ F)	$12.5 \times C_{SRC}$ ( $\mu$ F)	$15 \times C_{SRC}$ ( $\mu$ F)	s

1. Valid for ambient operating temperature:  $T_A = -40$  to  $+85$  °C;  $V_{CC} = 1.65$  to  $5.5$  V (except where noted).

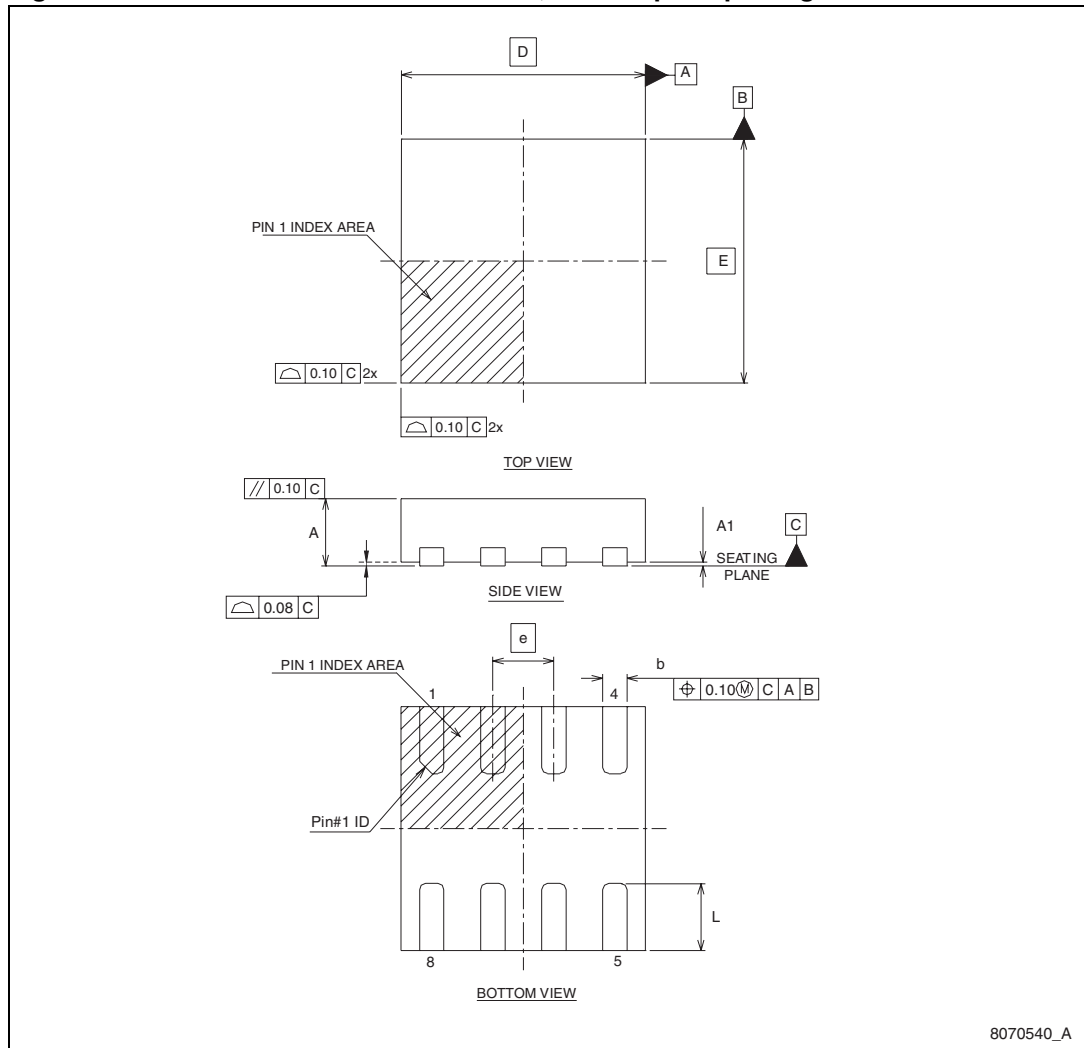
2. Typical value is at  $25$  °C and  $V_{CC} = 3.3$  V unless otherwise noted.

3. Input glitch immunity is equal to  $t_{SRC}$  (when both  $\overline{SR}$  inputs are low, otherwise infinite).

## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 13. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package outline



8070540\_A

Table 6. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package mechanical data

Symbol	Dimension (mm)			Dimension (inches)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D BSC	1.9	2.00	2.1	0.075	0.079	0.083
E BSC	1.9	2.00	2.1	0.075	0.079	0.083
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

## 7 Package footprint

Figure 14. Landing pattern - TDFN – 8-lead 2 x 2 mm without thermal pad

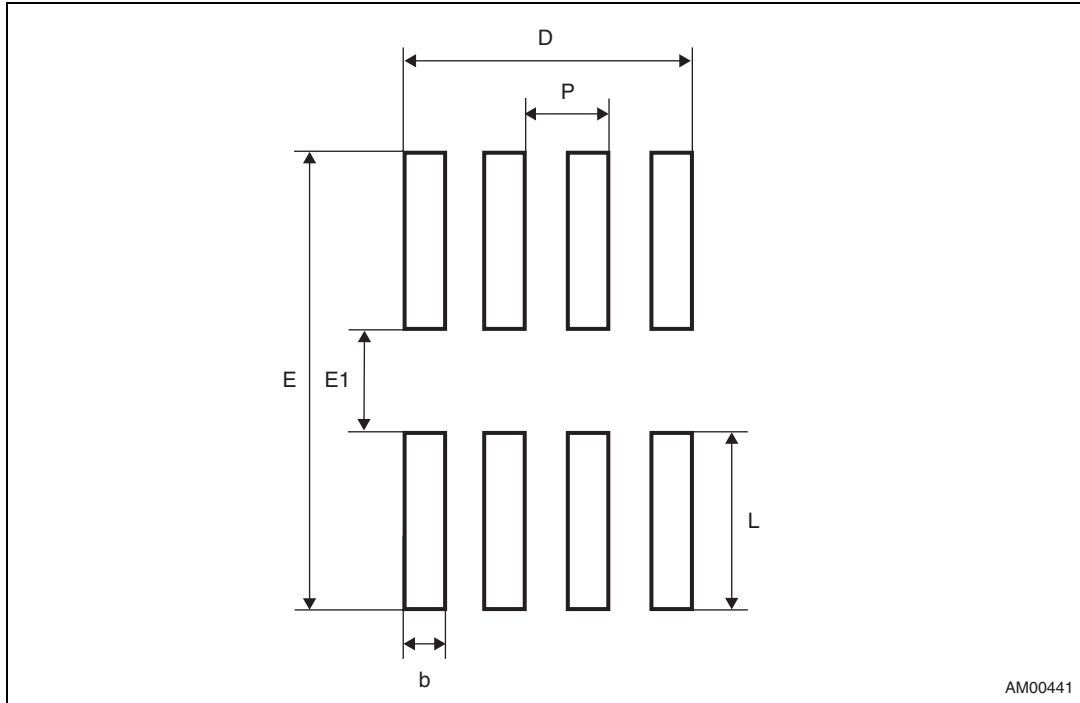


Table 7. Parameters for landing pattern - TDFN – 8-lead 2 x 2 mm package

Parameter	Description	Dimension (mm)		
		Min.	Nom.	Max.
L	Contact length	1.05	—	1.15
b	Contact width	0.25	—	0.30
E	Max. land pattern Y-direction	—	2.85	—
E1	Contact gap spacing	—	0.65	—
D	Max. land pattern X-direction	—	1.75	—
P	Contact pitch	—	0.5	—

## 8 Tape and reel information

Figure 15. Carrier tape

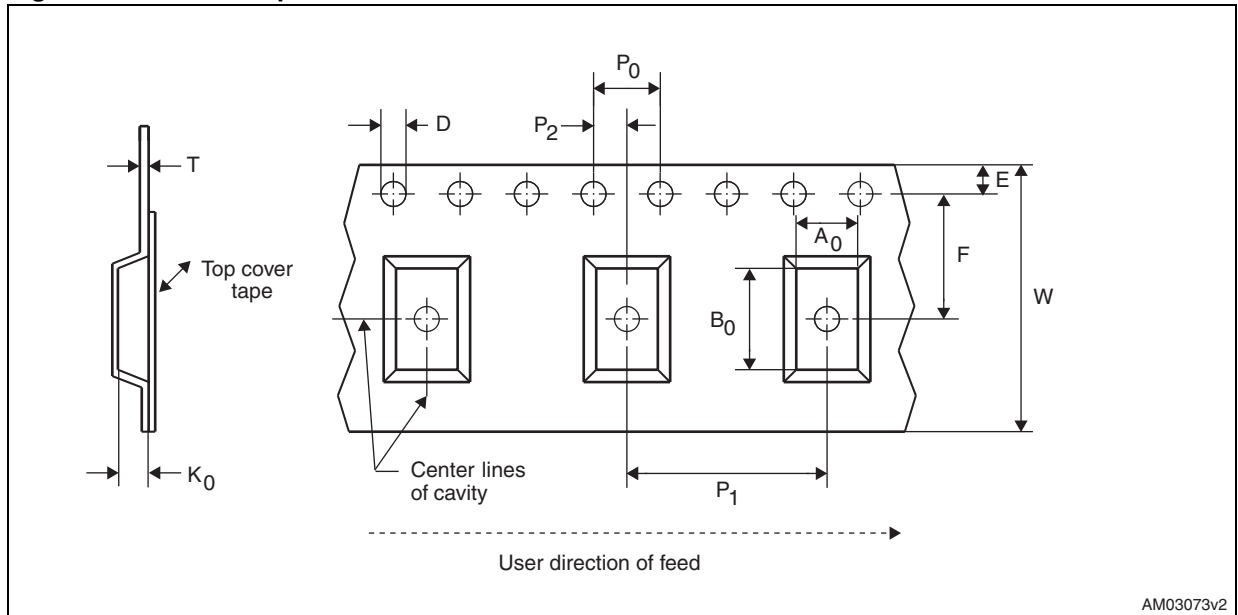


Table 8. Carrier tape dimensions

Package	W	D	E	P <sub>0</sub>	P <sub>2</sub>	F	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	P <sub>1</sub>	T	Unit	Bulk qty.
TDFN8	8.00 +0.30 -0.10	1.50 +0.10/ -0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	3.50 ±0.05	2.30 ±0.05	2.30 ±0.05	1.00 ±0.05	4.00 ±0.10	0.250 ±0.05	mm	3000

Figure 16. Reel dimensions

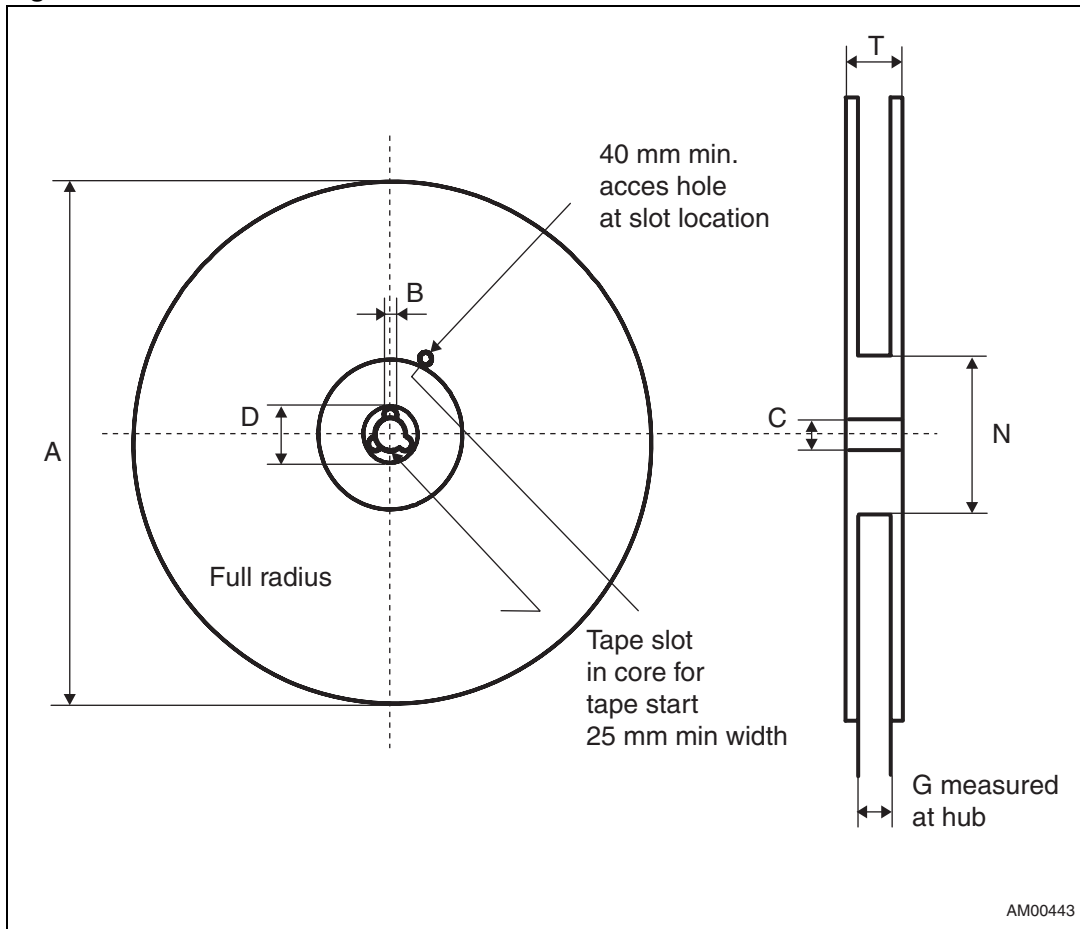
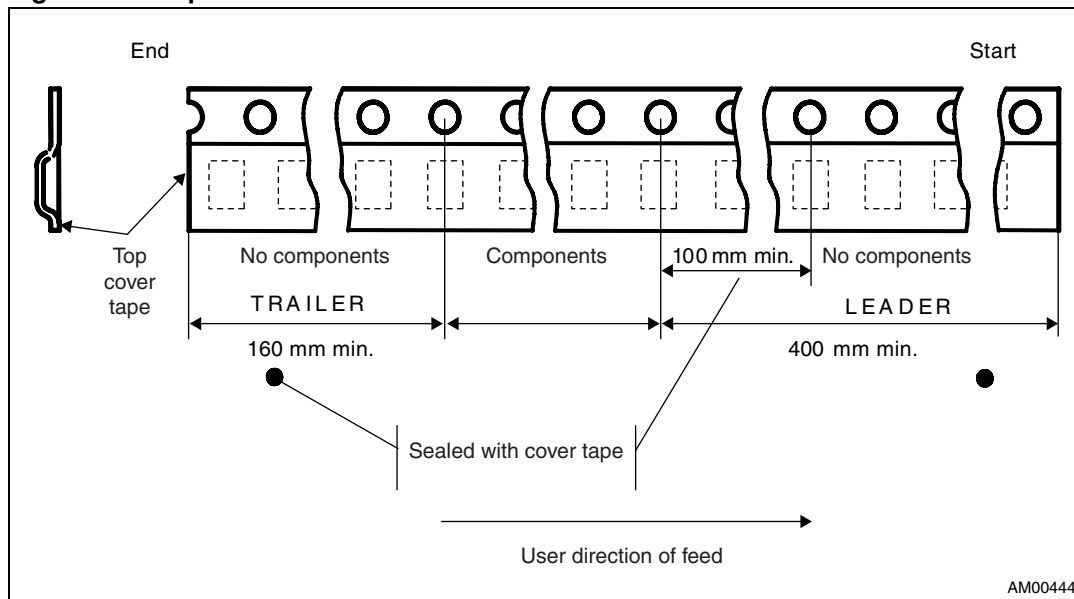


Table 9. Reel dimensions

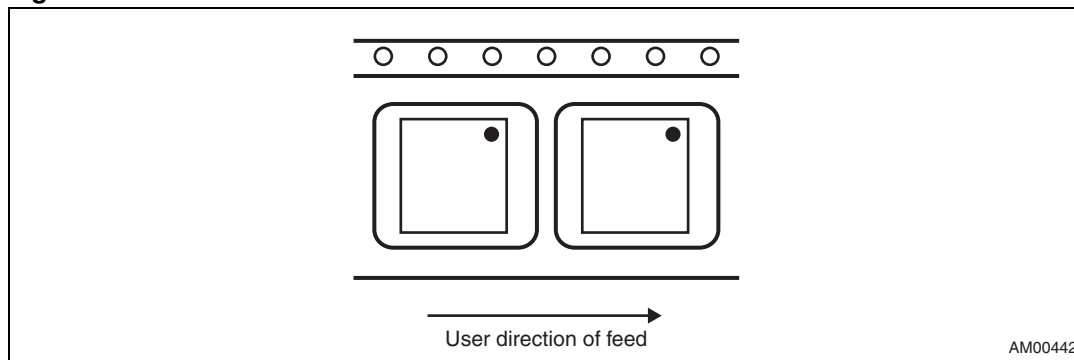
Tape sizes	A max.	B min.	C	D min.	N min.	G	T max.
8 mm	180 (7 inches)	1.50	13.0 +/- 0.20	20.20	60	8.4 +2/-0	14.40

Figure 17. Tape trailer/leader



AM00444

Figure 18. Pin 1 orientation



AM00442

- Note: 1 Drawings are not to scale.  
 2 All dimensions are in mm, unless otherwise noted.

## 9 Part numbering

**Table 10. Ordering information scheme**

Example:	STM6522	A	A	A	A	DG	6	F
<b>Device type</b>								
STM6522								
<b>V<sub>CC</sub> monitoring, power-on reset</b>								
A = no V <sub>CC</sub> monitoring, no power-on reset								
<b>Smart Reset™ setup delay (t<sub>SRC</sub>); presence of internal input pull-up on all Smart Reset™ inputs (<math>\overline{SRx}</math>)</b>								
A = user-programmed (external capacitor); no input pull-up								
<b>Output type</b>								
A = both $\overline{RST1}$ and $\overline{RST2}$ open-drain, no pull-up, active-low								
<b>Reset timeout period (t<sub>REC</sub>)</b>								
A = 140 ms min.								
<b>Package</b>								
DG = TDFN8 2 x 2 x 0.75 mm, 0.5 mm pitch								
<b>Temperature range</b>								
6 = -40 °C to +85 °C								
<b>Shipping method</b>								
F = ECOPACK® package, tape and reel								

For device options currently available refer to [Table 11](#). For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

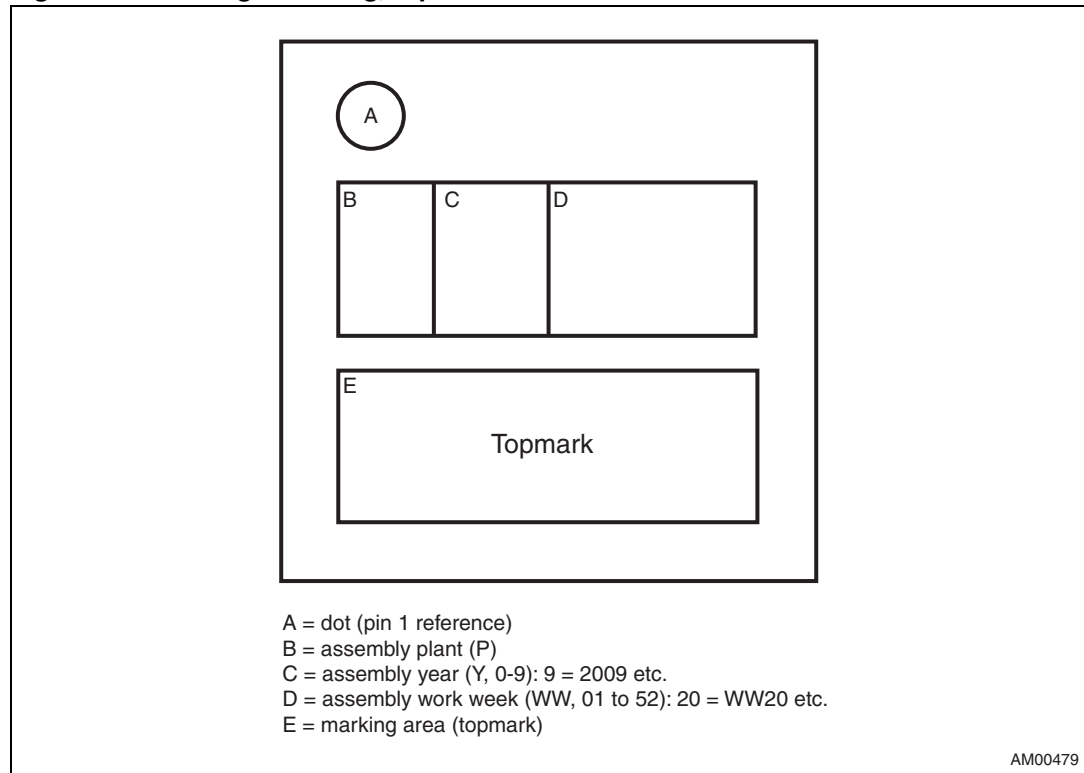
# 10 Package marking

**Table 11. Package marking**

Part number	t <sub>SRC</sub> delay control	Smart Reset™ inputs <sup>(1)</sup>	Power-on reset, V <sub>CC</sub> monitoring	$\overline{\text{RST1}}$ output <sup>(1)</sup>	$\overline{\text{RST2}}$ output <sup>(1)</sup>	t <sub>REC</sub> option	Topmark
STM6522AAAADG6F	C <sub>SRC</sub>	AL	—	AL, OD	AL, OD	A	CAL, AAL

1. AL = active-low, AH = active-high, PU = with internal pull-up resistor, OD = open-drain.

**Figure 19. Package marking, top view**



# 11 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
03-Feb-2010	1	Initial release.
10-May-2010	2	Updated title, <i>Features, Applications, Section 1, Figure 1, Table 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Section 2.4, Figure 7</i> , note 1 below <i>Table 2, Section 2.6</i> , added <i>Section 2.7, Section 3, Table 5, Table 6, Table 7, Table 10, Section 8, Table 11</i> .
09-Jan-2012	3	Updated <i>Table 3, Table 5, Table 11</i> and Disclaimer, minor text corrections throughout document.

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