



STB50NF25 STP50NF25

N-channel 250V - 0.055Ω - 45A - D²PAK - TO-220
low gate charge STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} Max	I _D	P _W
STP50NF25	250 V	<0.069 Ω	45 A	160 W
STB50NF25	250 V	<0.069 Ω	45 A	160 W

- 100% avalanche tested
- Gate charge minimized
- Low intrinsic capacitances

Application

Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize on-resistance and gate charge. It is therefore suitable as primary side switch allowing high efficiencies.

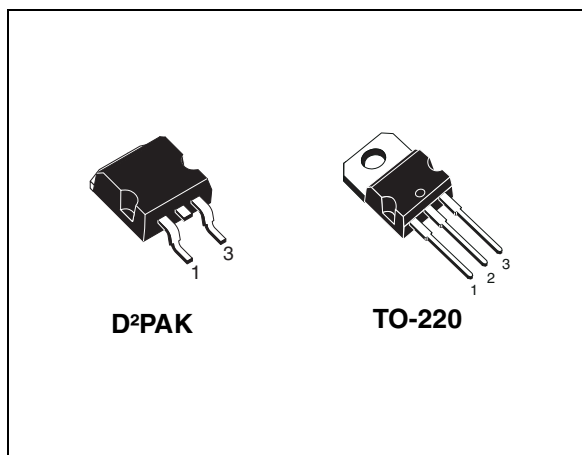


Figure 1. Internal schematic diagram

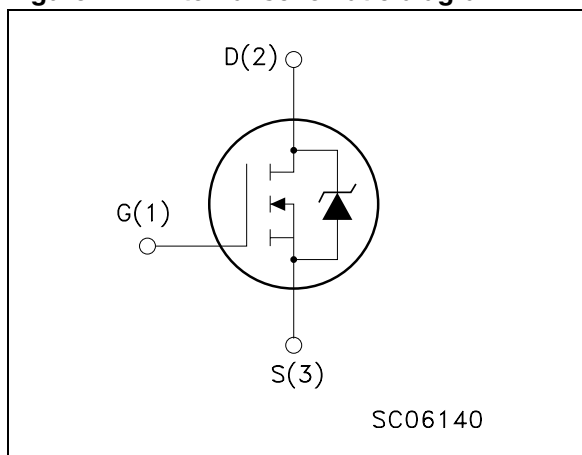


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP50NF25	50NF25	TO-220	Tube
STB50NF25	50NF25	D ² PAK	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	250	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	45	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	28	A
$I_{DM}^{(2)}$	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	160	W
	Derating factor	1.28	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	10	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Value limited by wire bonding
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 45\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.78	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not-repetitive	32	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	160	mJ

1. Pulse width limited by T_{jmax}
2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	250			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating} @ 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$, $I_D = 22 \text{ A}$		0.055	0.069	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10 \text{ V}$, $I_D = 22 \text{ A}$		20		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		2670 465 70.5		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 200 \text{ V}$, $I_D = 45 \text{ A}$ $V_{GS} = 10 \text{ V}$ (see Figure 14)		68.2 12.2 33.4		nC nC nC
R_G	Gate input resistance	$f = 1 \text{ MHz}$ Gate Bias, Bias=0 Test signal level=20 mV open drain		1.1		Ω

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 125\text{ V}$, $I_D = 22\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13)		45 26		ns ns
$t_{d(off)}$ t_f	Off-voltage rise time Fall time	$V_{DD} = 125\text{ V}$, $I_D = 22\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13)		63 20		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD}	Source-drain current				45	A
I_{SDM}	Source-drain current (pulsed)				180	A
V_{SD}	Forward on voltage	$I_{SD} = 45\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 45\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 18)		198		ns
Q_{rr}	Reverse recovery charge			1.5		μC
I_{RRM}	Reverse recovery current			15		A
t_{rr}	Reverse recovery time	$I_{SD} = 45\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18)		256		ns
Q_{rr}	Reverse recovery charge			2.2		μC
I_{RRM}	Reverse recovery current			17		A

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

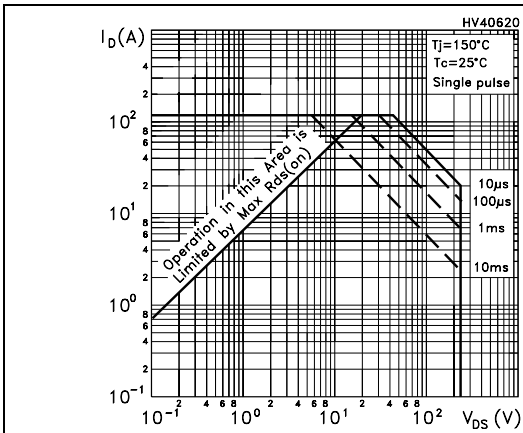


Figure 3. Thermal impedance

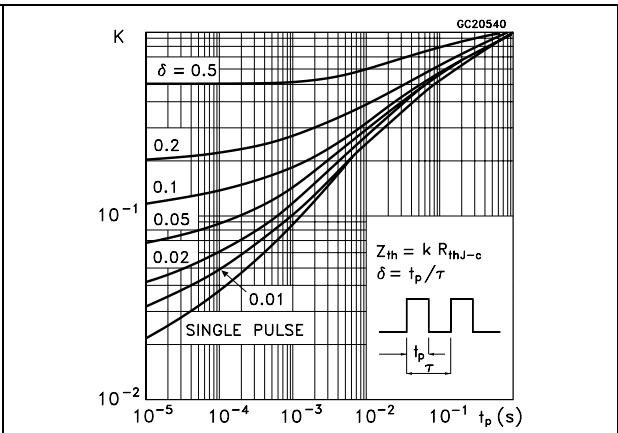


Figure 4. Output characteristics

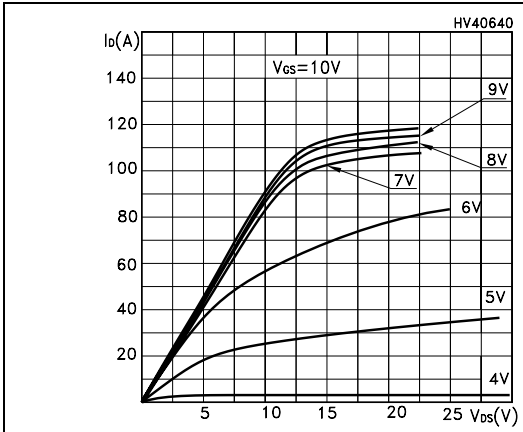


Figure 5. Transfer characteristics

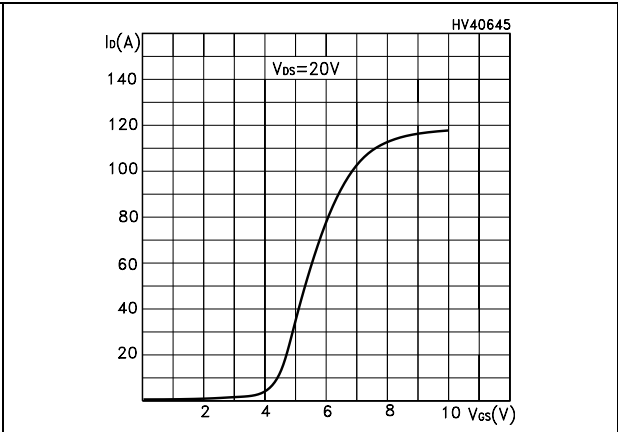


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

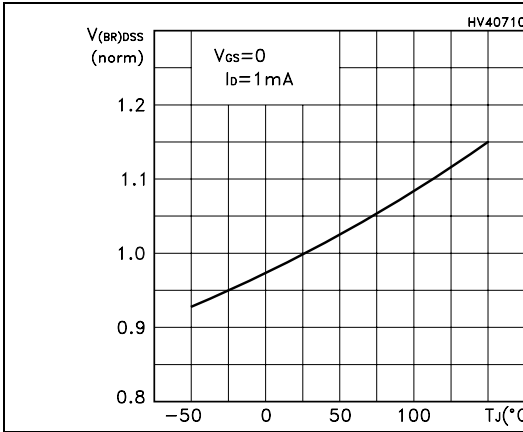


Figure 7. Static drain-source on resistance

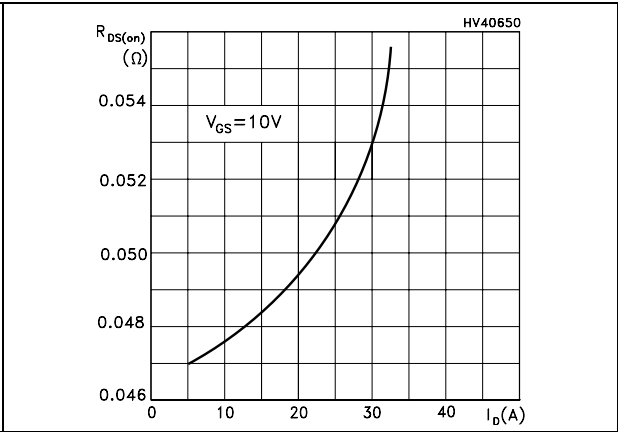


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

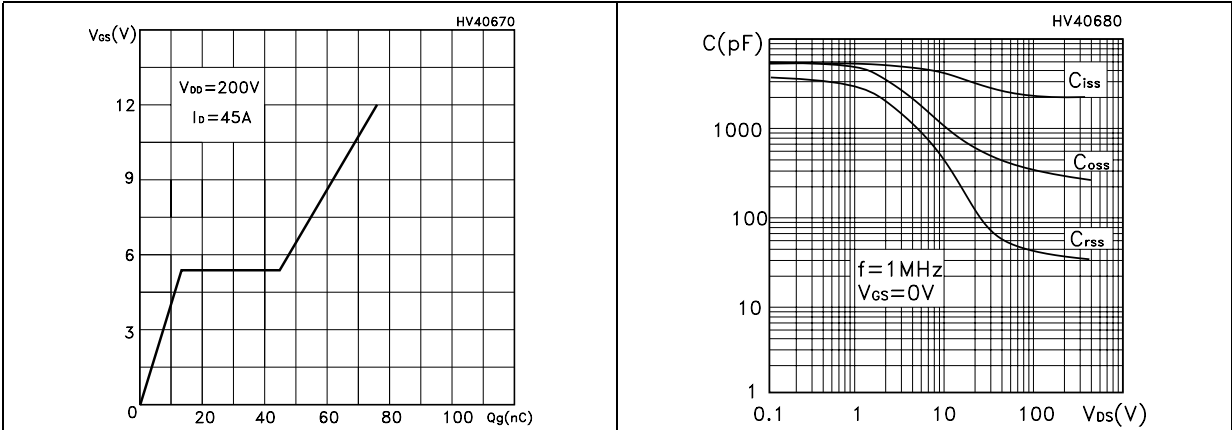


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

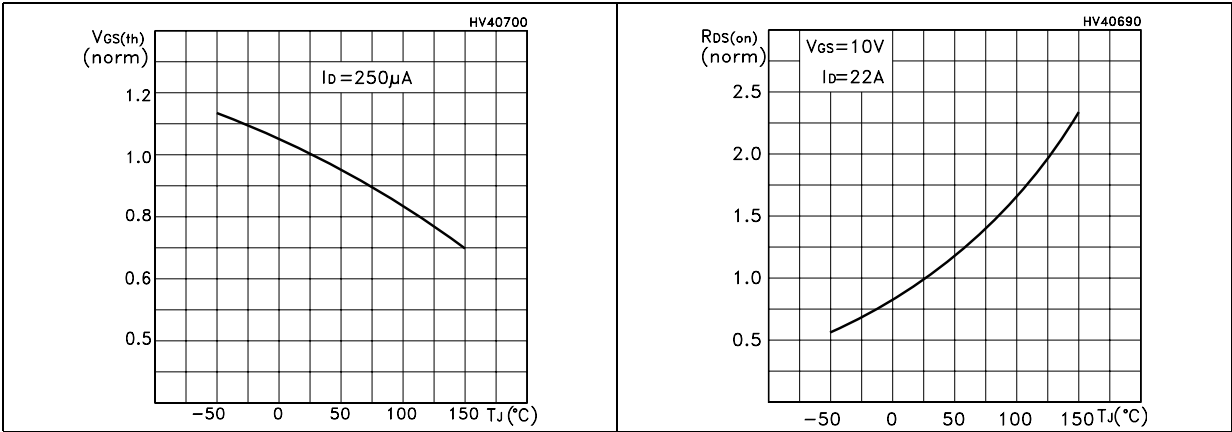
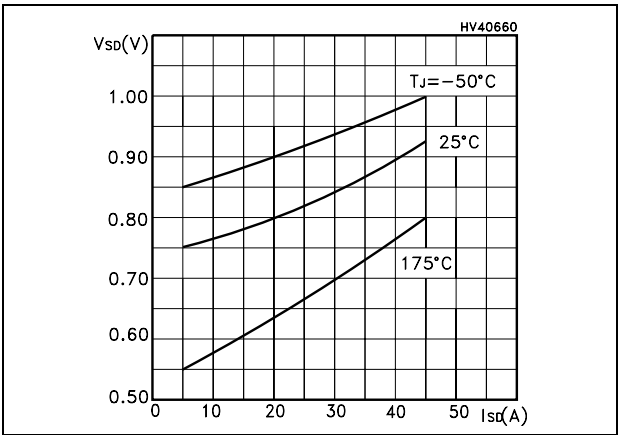


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

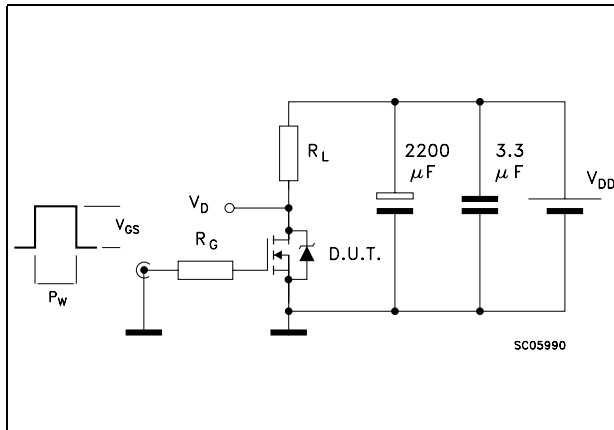


Figure 14. Gate charge test circuit

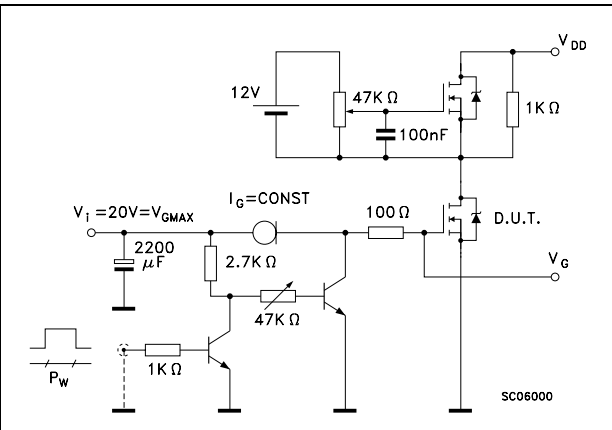


Figure 15. Test circuit for inductive load switching and diode recovery times

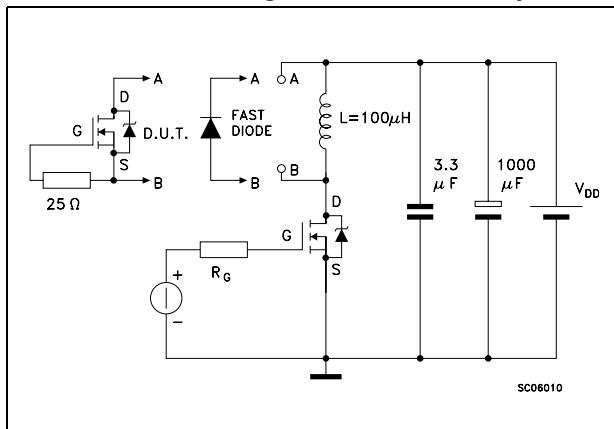


Figure 16. Unclamped Inductive load test circuit

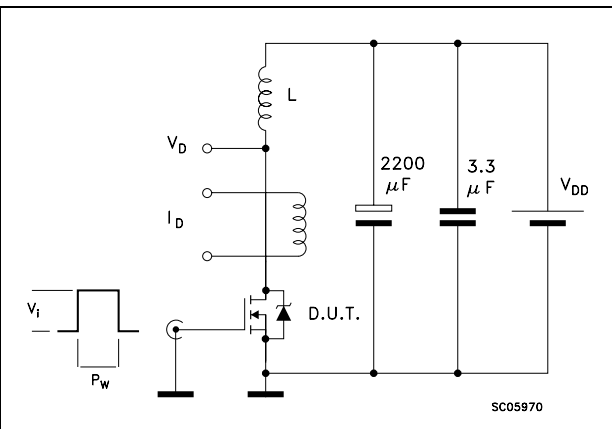


Figure 17. Unclamped inductive waveform

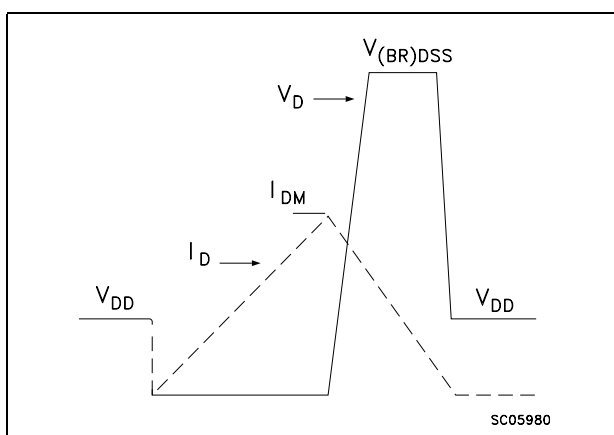
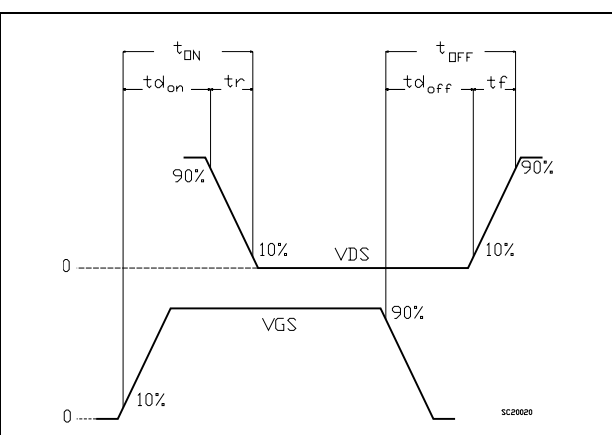


Figure 18. Switching time waveform

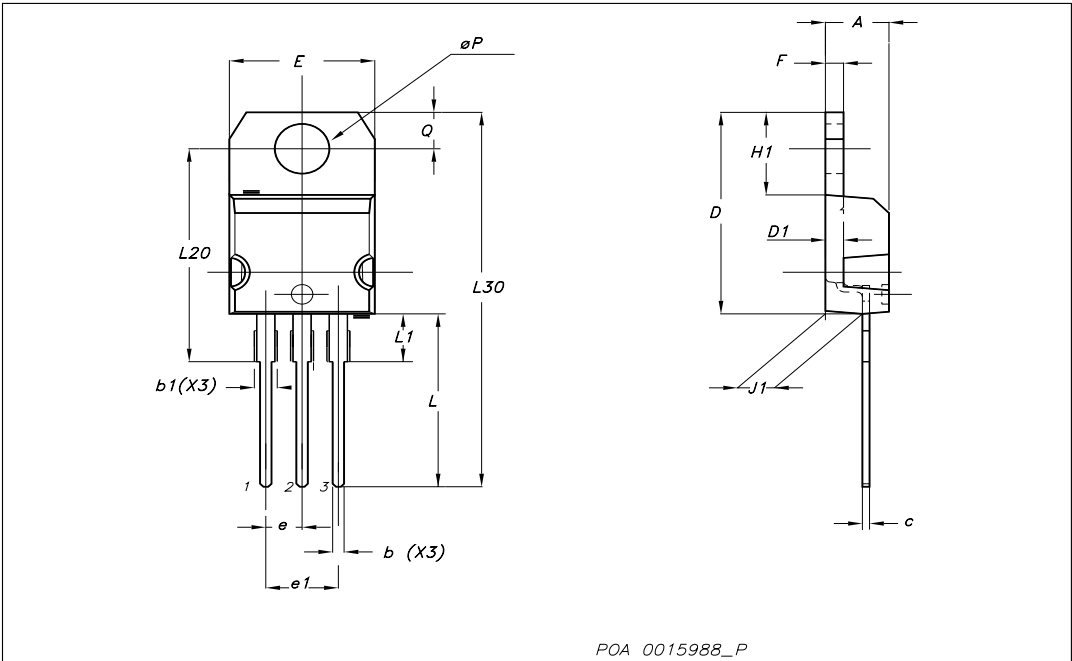


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 mechanical data

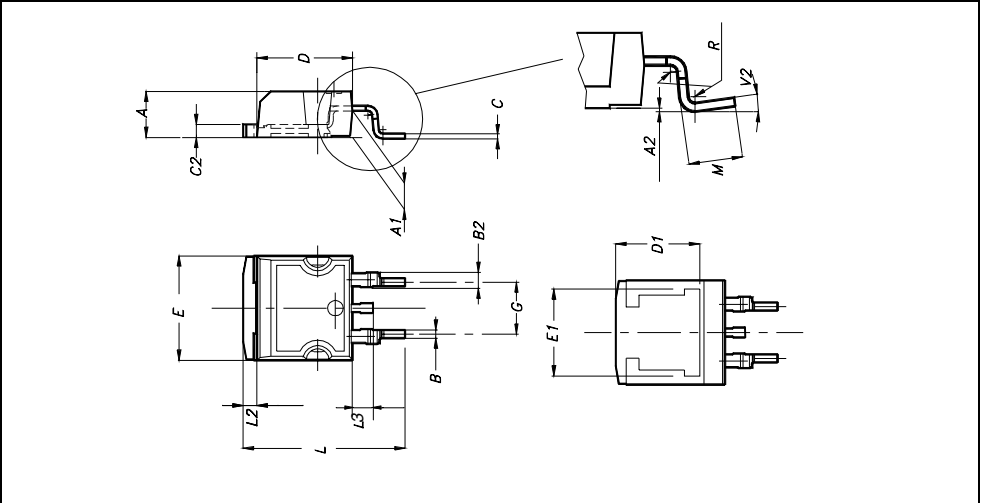
Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



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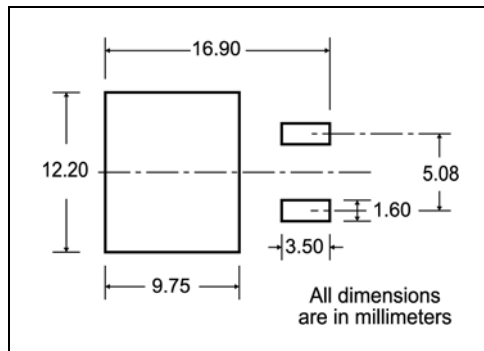
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

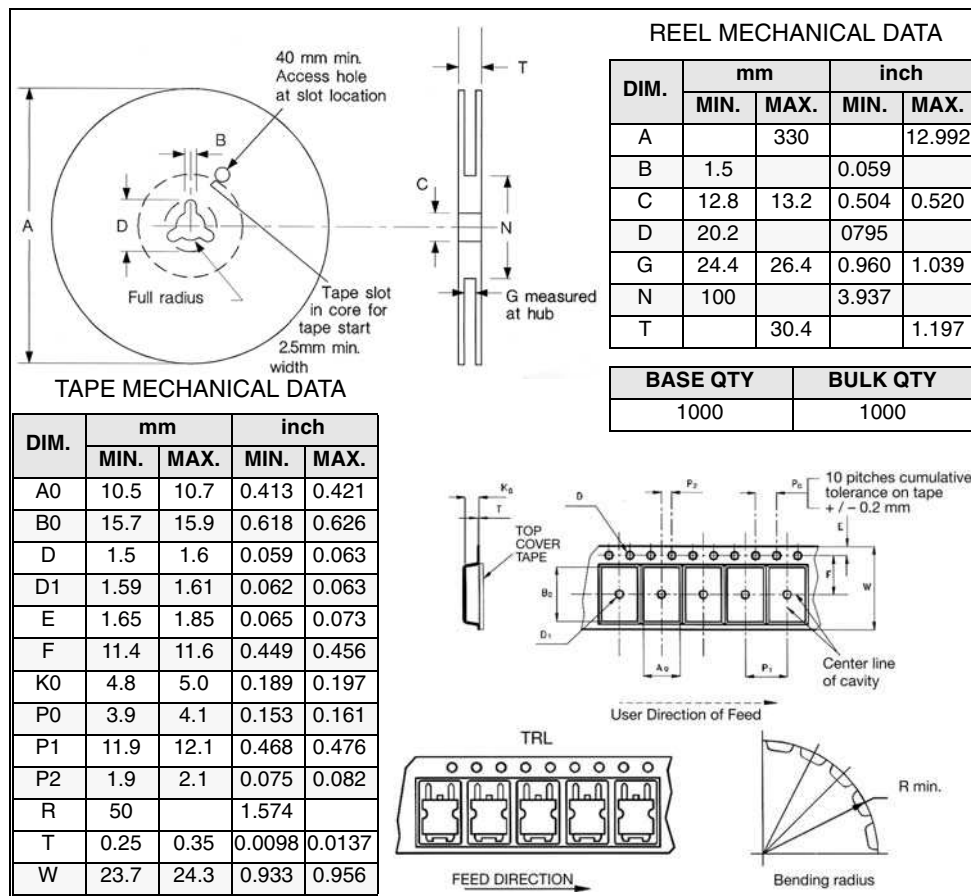


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Mar-2007	1	First release
10-Mar-2007	2	Typo mistake on page 1 (marking)
13-Apr-2007	3	Corrected value on Table 6 .
14-Nov-2007	4	Added new section: Electrical characteristics (curves)

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