ATWILC1000-MR110PB DATASHEET

IEEE 802.11 b/g/n Link Controller SoC

Datasheet

Description

The Atmel® ATWILC1000-MR110PB is a low-power consumption 802.11 b/g/n IoT (Internet of Things) module, which is specifically optimized for low power IoT applications. The highly integrated module features small form factor (21.5mm x 14.5mm x 2.1mm) while fully integrating Power Amplifier, LNA, Switch, Power Management, and PCB antenna. With advanced security, it could be interoperable with various vendors' 802.11b/g/n Access Points in wireless LAN. The module provides SPI and SDIO to interface to host controller. The content provided in this datasheet is for both the ATWILC1000-MR110PB and ATWILC1000-MR110UB modules unless otherwise noted.

Features

- IEEE® 802.11 b/g/n 20MHz (1x1) solution
- Single spatial stream in 2.4GHz ISM band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce host load
- SPI and SDIO host interfaces
- 2/3 wire Bluetooth® coexistence interface
- Operating temperature range of -40°C to +85°C
- Power save modes:
  - <1µA Power Down mode typical @3.3V I/O
  - 380µA Doze mode with chip settings preserved (used for beacon monitoring)
  - On-chip low power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or host I/O transaction

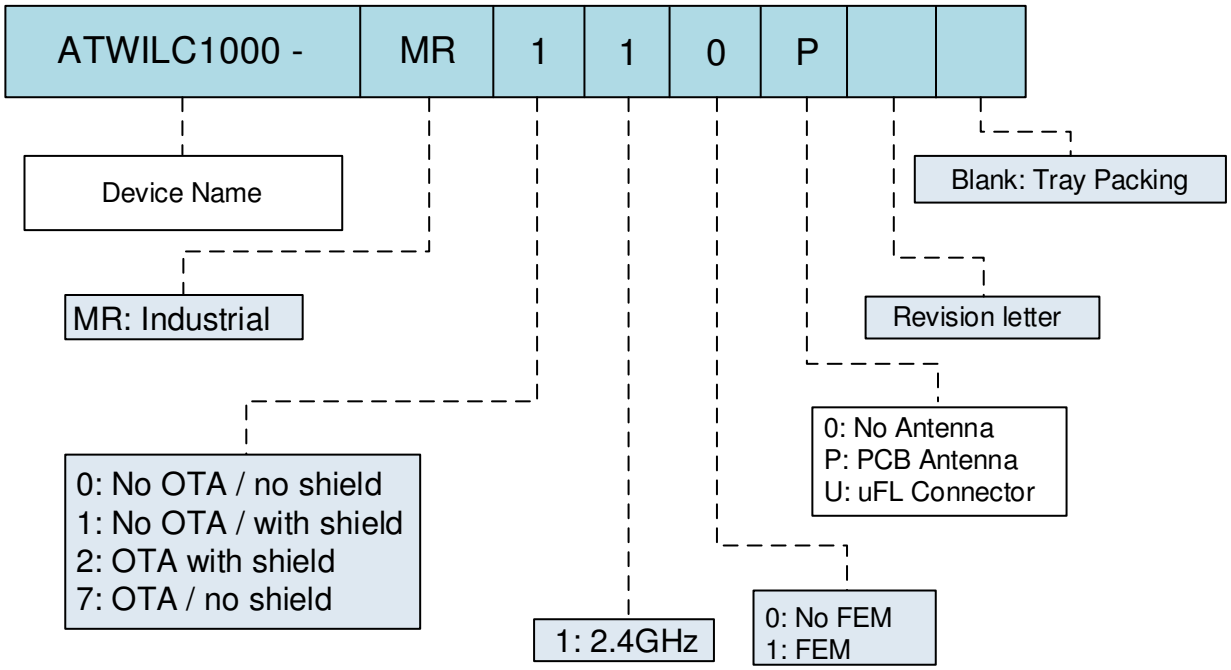
Table of Contents

1 Ordering Information and Module Marking

Table 1-1. Ordering Details

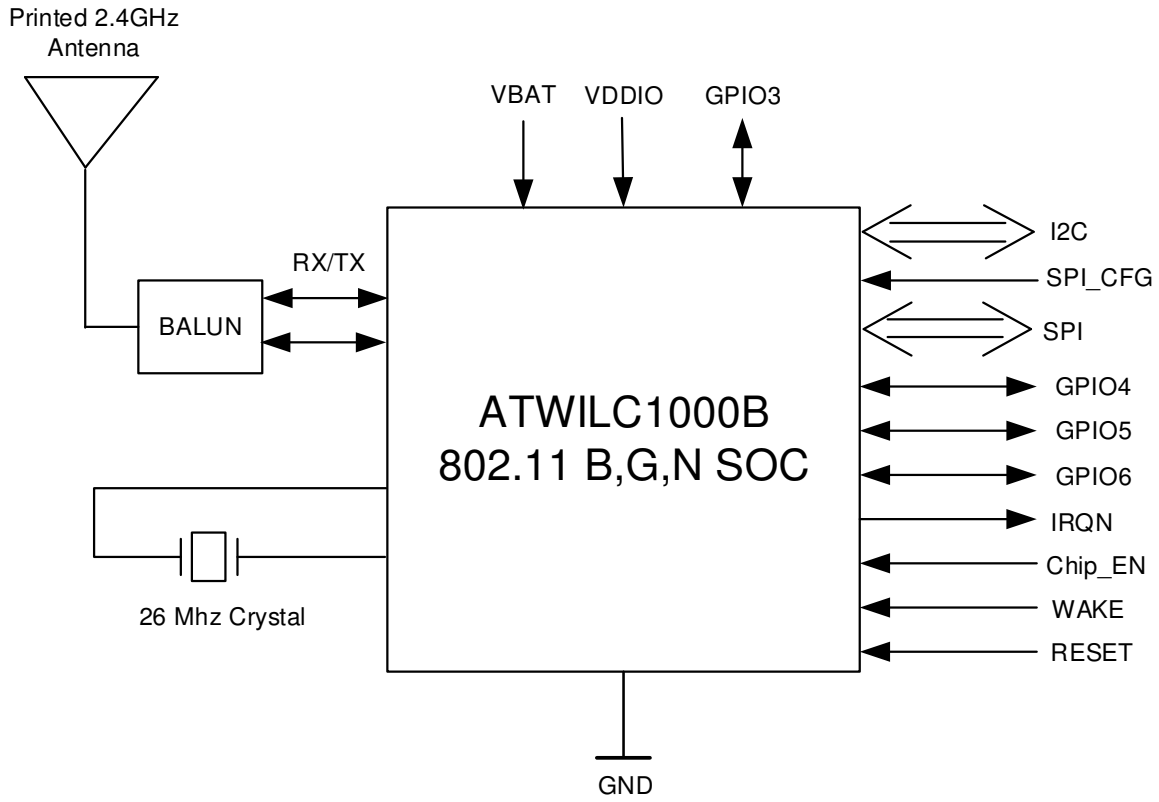
Ordering Code	Package	Description	Pins	Regulatory Certification
ATWILC1000-MR110PB	22x15mm	Certified module with AT-WILC1000B-Mu chip and PCB antenna	28	FCC, IC
ATWILC1000-MR110UB	22x15mm	Certified module with AT-WILC1000B-Mu chip and uFL connector	28	FCC

Figure 1-2. Marking Information



2 Block Diagram

Figure 2-1. Block Diagram



3 Pin-out and Package Information

3.1 Pin Description

Figure 3-1. Pin Assignment

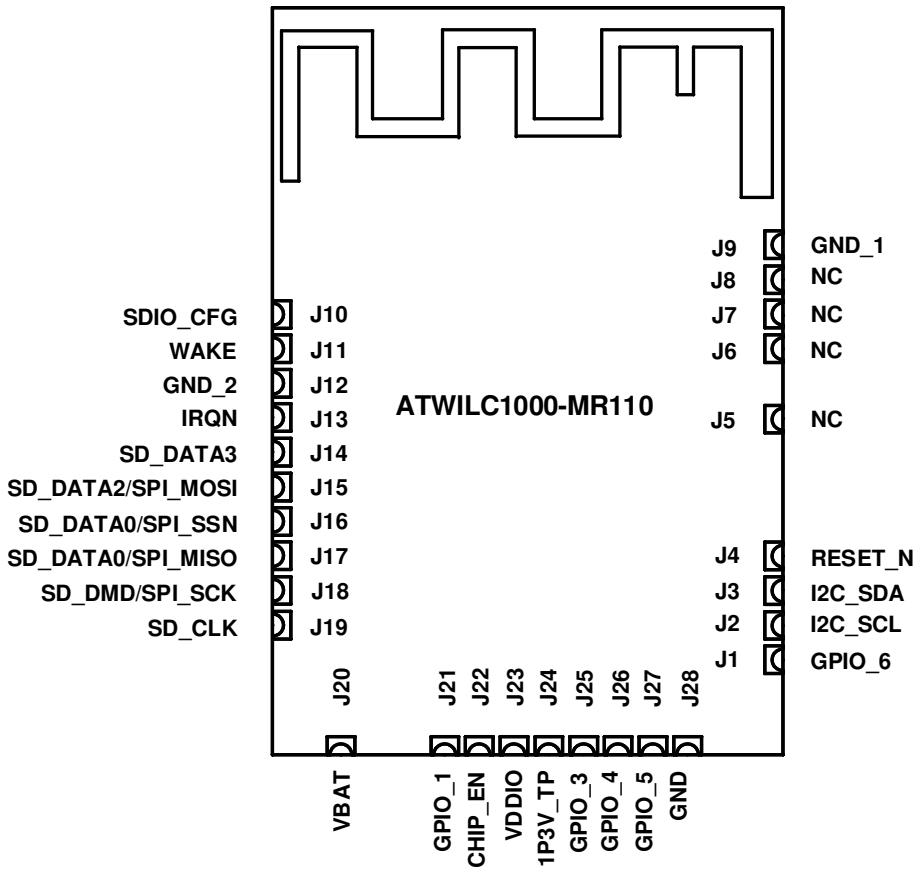


Table 3-1. Pin Description

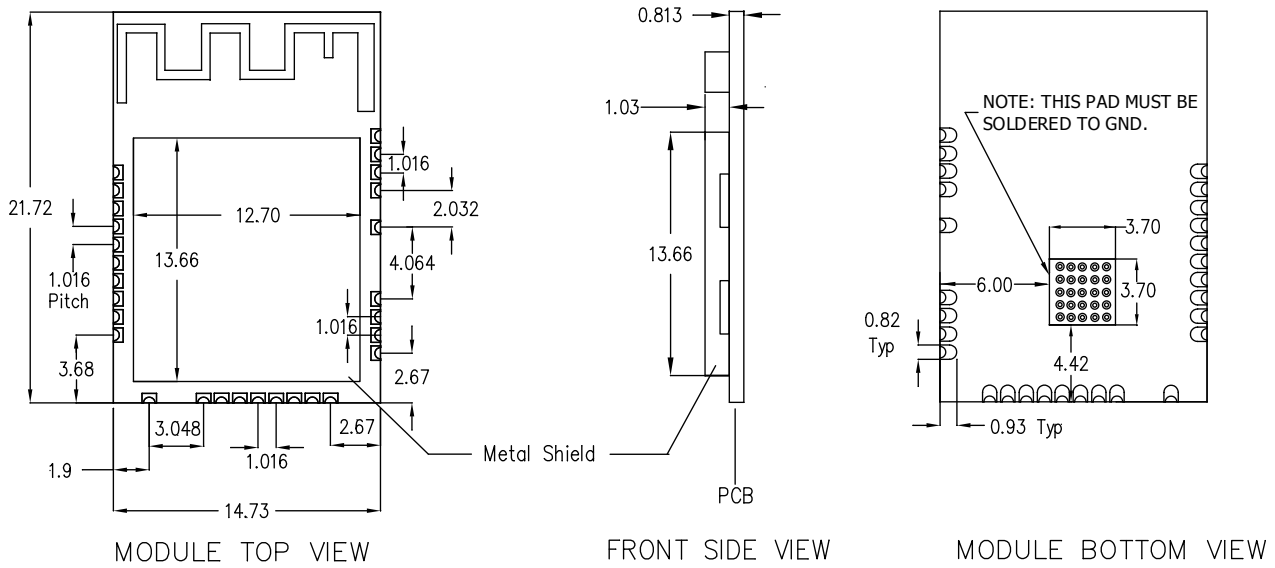
NO	Name	Type	Description	Programmable pull-up resistor
1	GPIO_6	I/O	General purpose I/O	
2	I2C_SCL	I/O	I²C Slave Clock. Can be configured as either master or slave. I²C interface is only used for test purposes. This pin should be brought to a test point only. Do not add a pull-up resistor.	
3	I2C_SDA	I/O	I²C Slave Data. Can be configured as either master or slave. I²C interface is only used for test purposes. This pin should be brought to a test point only. Do not add a pull-up resistor.	Yes

NO	Name	Type	Description	Programmable pull-up resistor
4	RESET_N	I	Active-Low Hard Reset. When asserted to a low level, the module will be placed in a reset state. When asserted to a high level, the module will run normally. Connect to a host output that defaults low at power up. If the output floats, add a 1M ohm pull-down resistor if necessary to ensure a low level at power up.	Yes
5	NC	-	No connect	Yes
6	NC	-	No connect	No
7	NC	-	No connect	
8	NC	-	No connect	
9	GND_1	-	GND	
10	SDIO~_SPI_CFG	I	Tie to VDDIO through a 1M ohm resistor to enable the SPI interface. Connect to ground to enable SDIO interface.	No
11	WAKE	I	Host Wake control. Can be used to wake up the module from Doze mode. Connect to a host GPIO.	No
12	GND_2	-	GND	
13	IRQN	O	ATWINC1500 Device Interrupt	No
14	SD_DAT3	SDIO=I/O	SDIO Data Line 3 from ATWILC1000-MR110PB when module is configured for SDIO.	Yes
15	SD_DAT2/SPI_RXD	SDIO=I/O SPI=I	SDIO Data Line 2 signal from ATWILC1000-MR110PB when module is configured for SDIO. SPI MOSI (Master Out Slave In) pin when module is configured for SPI.	Yes
16	SD_DAT1/SPI_SSN	SDIO=I/O SPI=I	SDIO Data Line 1 from ATWILC1000-MR110PB when module is configured for SDIO. Active Low SPI Slave Select from ATWILC1000 when module is configured for SPI.	Yes
17	SD_DAT0/SPI_TXD	SDIO=I/O SPI=O	SDIO Data Line 0 from ATWILC1000-MR110PB when module is configured for SDIO. SPI MISO (Master In Slave Out) pin from ATWILC1000 when module is configured for SPI.	Yes
18	SD_CMD/SPI_CLK	SDIO=I/O SPI=I	SDIO CMD Line from ATWILC1000-MR110PB when module is configured for SDIO. SPI Clock from ATWILC1000 when module is configured for SPI.	Yes
19	SD_CLK	SDIO=I	SDIO Clock Line from ATWILC1000-MR110PB when module is configured for SDIO.	Yes
20	VBATT	-	Battery power supply	Yes
21	GPIO_1	I	General Purpose I/O	Yes

NO	Name	Type	Description	Programmable pull-up resistor
22	CHIP_EN	I	Module enable. High level enables module, low-level places module in Power Down mode. Connect to a host Output that defaults low at power up. If the output floats, add a 1MΩ pull-down resistor if necessary to ensure a low level at power up.	No
23	VDDIO	-	I/O Power Supply. Must match host I/O voltage.	
24	1P3V_TP	-	1.3V VDD Core Test Point	
25	GPIO_3	-	General purpose I/O	Yes
26	GPIO_4	I/O	General purpose I/O	Yes
27	GPIO_5	I/O	General purpose I/O	Yes
28	GND_3	-	GND	

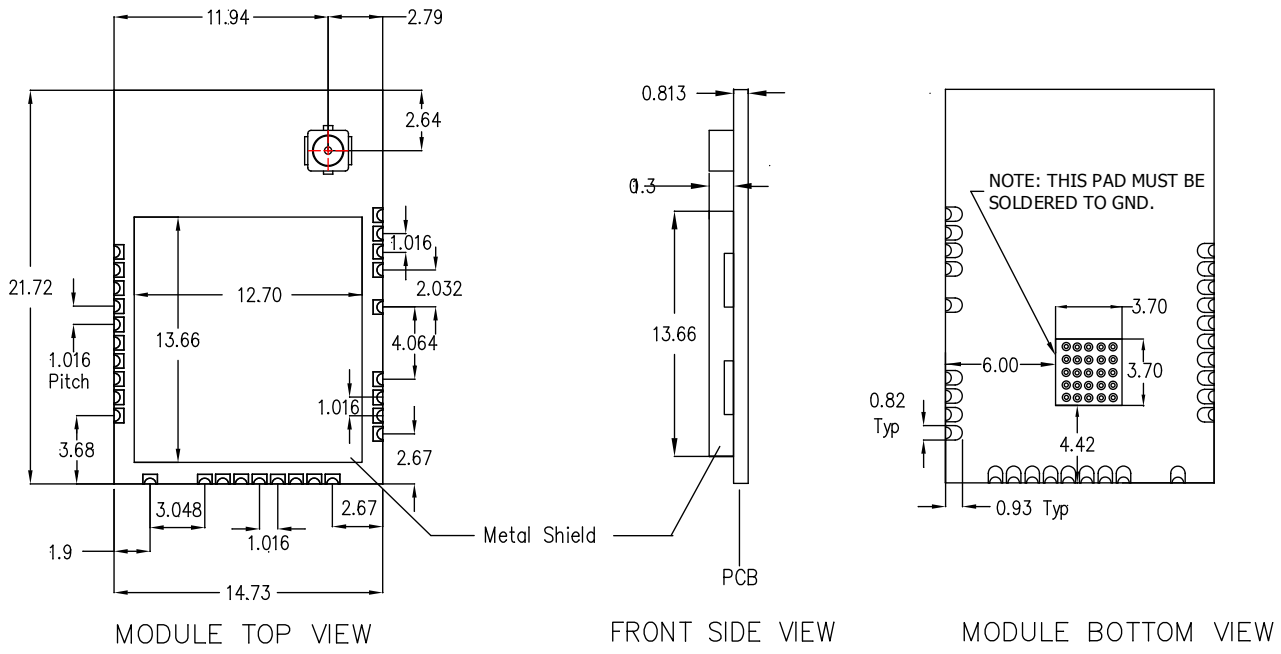
3.2 Module Outline Drawings

Figure 3-2. Module Drawings – ATWILC1000-MR110PB - Top and Bottom Views (Unit = mm)



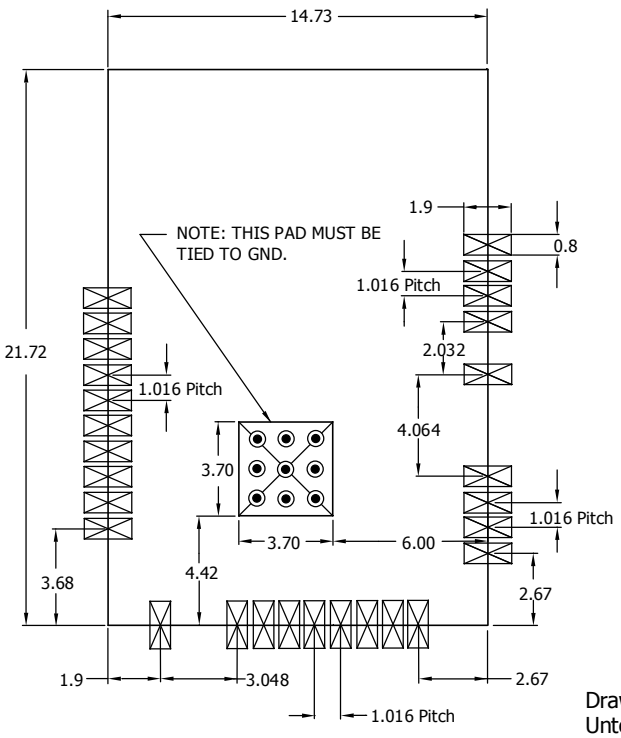
Drawing not to scale.
Untoleranced dimension.
Units = mm.

Figure 3-3. Module Drawings – ATWILC1000-MR110UB - Top and Bottom Views (Unit = mm)



Drawing not to scale.
Untoleranced dimension.
Units = mm.

Figure 3-4. ATWILC1000-MR110XB Recommended Solder Pad Footprint.



Drawing not to scale.
Untoleranced dimensions.
Units=mm.

4 Electrical Specifications

4.1 Absolute Ratings

Table 4-1. Voltages

Symbol	Description	Min.	Max.	Unit
VBATT	Input supply Voltage	-0.3	5.5	V
VDDIO	SPI, SDIO, and GPIO Voltage	-0.3	3.6	V

4.2 Recommended Operating Ratings

Table 4-2. Pin Recommended Operating Ratings

Test conditions: -40ºC - +85ºC				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VBATT [1]	3.0	3.6	4.2	V
VDDIO [2]	1.8	3.3	3.6	V

Notes: 1. VBATT should be equal to or greater than VDDIO.
2. The voltage of VDDIO is dependent on system I/O voltage.

5 CPU and Memory Subsystems

5.1 Processor

ATWILC1000B has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

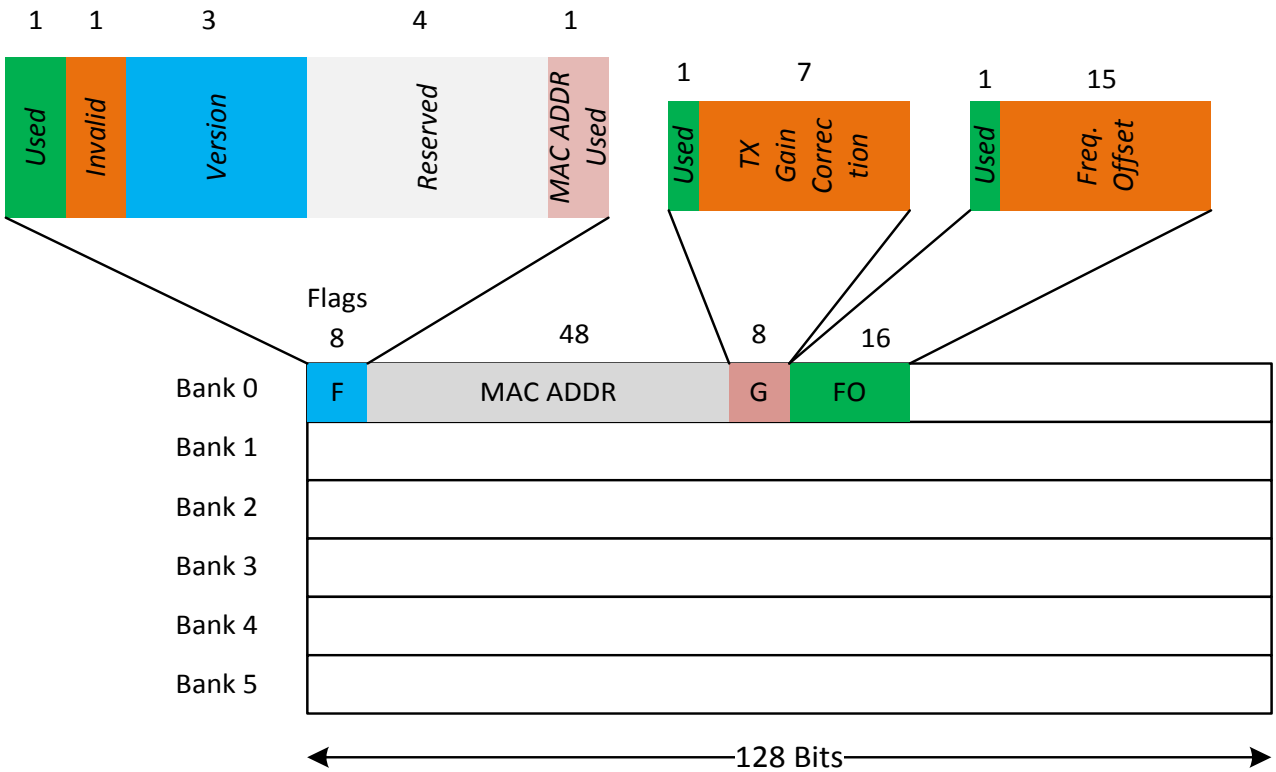
5.2 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 160KB instruction RAM and a 64KB data RAM. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

5.3 Non-volatile Memory (eFuse)

ATWILC1000B has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bit map, which is shown in Figure 5-1. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating MAC address. Refer to Wi-Fi eFuse Programming Guide for the eFuse programming instructions.

Figure 5-1. eFuse Bit Map



6 WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

6.1 MAC

6.1.1 Features

The ATWILC1000B IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA security with key management:
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Advanced power management
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

6.1.2 Description

The ATWILC1000B MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association
- Functions that need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling

6.2 PHY

6.2.1 Features

The ATWILC1000B IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800, and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

6.2.2 Description

The ATWILC1000B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

6.3 Radio

Table 6-1. Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; Temp.: 25ºC

Feature	Description
Module Part Number	ATWILC1000-MR110PB
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Host Interface	SPI, SDIO
Dimension	L x W x H: 21.5 x 14.5 x 1.5 (typical) mm
Frequency Range	2.412GHz ~ 2.4835GHz (2.4GHz ISM Band)
Number of Channels	11 for North America, 13 for Europe, and 13 for Japan
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM/64-QAM,16-QAM, QPSK, BPSK

Feature	Description
Data Rate	802.11b: 1, 2, 5.5, 11Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz, short GI, 400ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2Mbps
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

6.3.2 Receiver Performance

Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; temp.: 25°C

Table 6-2. Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,412		2,484	MHz
Sensitivity 802.11b	1Mbps DSS		-98		dBm
	2Mbps DSS		-94		
	5.5Mbps DSS		-92		
	11Mbps DSS		-88		
Sensitivity 802.11g	6Mbps OFDM		-90		dBm
	9Mbps OFDM		-89		
	12Mbps OFDM		-88		
	18Mbps OFDM		-85		
	24Mbps OFDM		-83		
	36Mbps OFDM		-80		
	48Mbps OFDM		-76		
	54Mbps OFDM		-74		
Sensitivity 802.11n (BW=20MHz)	MCS 0		-89		dBm
	MCS 1		-87		
	MCS 2		-85		
	MCS 3		-82		
	MCS 4		-77		
	MCS 5		-74		
	MCS 6		-72		
	MCS 7		-70.5		
Maximum Receive Signal	1-11Mbps DSS	-10	0		dBM

Parameter	Description	Min.	Typ.	Max.	Unit
Level	6-54Mbps OFDM	-10	0		
	MCS 0 – 7	-10	0		
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)		50		dB
	11Mbps DSS (25MHz offset)		43		
	6Mbps OFDM (25MHz offset)		40		
	54Mbps OFDM (25MHz offset)		25		
	MCS 0 – 20MHz BW (25MHz offset)		40		
	MCS 7 – 20MHz BW (25MHz offset)		20		
Cellular Blocker Immunity	776-794MHz CDMA		-14		dBm
	824-849MHz GSM		-10		
	880-915MHz GSM		-10		
	1710-1785MHz GSM		-15		
	1850-1910MHz GSM		-15		
	1850-1910MHz WCDMA		-24		
	1920-1980MHz WCDMA		-24		

6.3.3 Transmitter Performance

Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; temp.: 25°C.

Table 6-3. Transmitter Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,412		2,484	MHz
Output Power, (1-3) ON_Transmit_High_Power Mode	802.11b 1Mbps		17.5		dBm
	802.11b 11Mbps		18.5		
	802.11g 6Mbps		17.5		
	802.11g 54Mbps		16		
	802.11n MCS 0		17.0		
	802.11n MCS 7		14.5		
Output Power, (1-3) ON_Transmit_Low_Power Mode	802.11b 1Mbps		17.0		dBm
	802.11b 11Mbps		17.5		
	802.11g 6-18Mbps		16.0		
	802.11g >18Mbps		N/A		
	802.11n MCS 0-3		14.5		
	802.11n >MCS 3		N/A		
TX Power Accuracy			±1.5		dB
Carrier Suppression			30.0		dBc
Out of Band Transmit Power	76-108		-125		dBm/Hz

Parameter	Description	Min.	Typ.	Max.	Unit
	776-794		-125		
	869-960		-125		
	925-960		-125		
	1570-1580		-125		
	1805-1880		-125		
	1930-1990		-125		
	2110-2170		-125		
Harmonic Output Power	2nd		-33		dBm/MHz
	3rd		-38		dBm/MHz

Notes:
1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured after RF matching network. See reference design.
3. Typical value measured mid-band. Additional back off of band edges is typically needed to meet agency requirements.

7 External Interfaces

7.1 SPI Interface

7.1.1 Overview

When the module is configured for SPI mode by connecting the SDIO~_SPI_CFG pin to VDDIO, the ATWILC1000-MR110PB has a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in Table 7-1. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

Table 7-1. SPI Interface Pin Mapping

Pin #	SPI function
10	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
15	MOSI: Serial Data Receive
18	SCK: Serial Clock
17	MISO: Serial Data Transmit

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO and SCK pins of the ATWILC1000-MR110PB have internal programmable pull-up resistors (see Section 8.1). These resistors should be programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while the ATWILC1000-MR110PB is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

7.1.2 SPI Timing

The SPI timing is provided in Figure 7-1 and Table 7-2.

Figure 7-1. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)

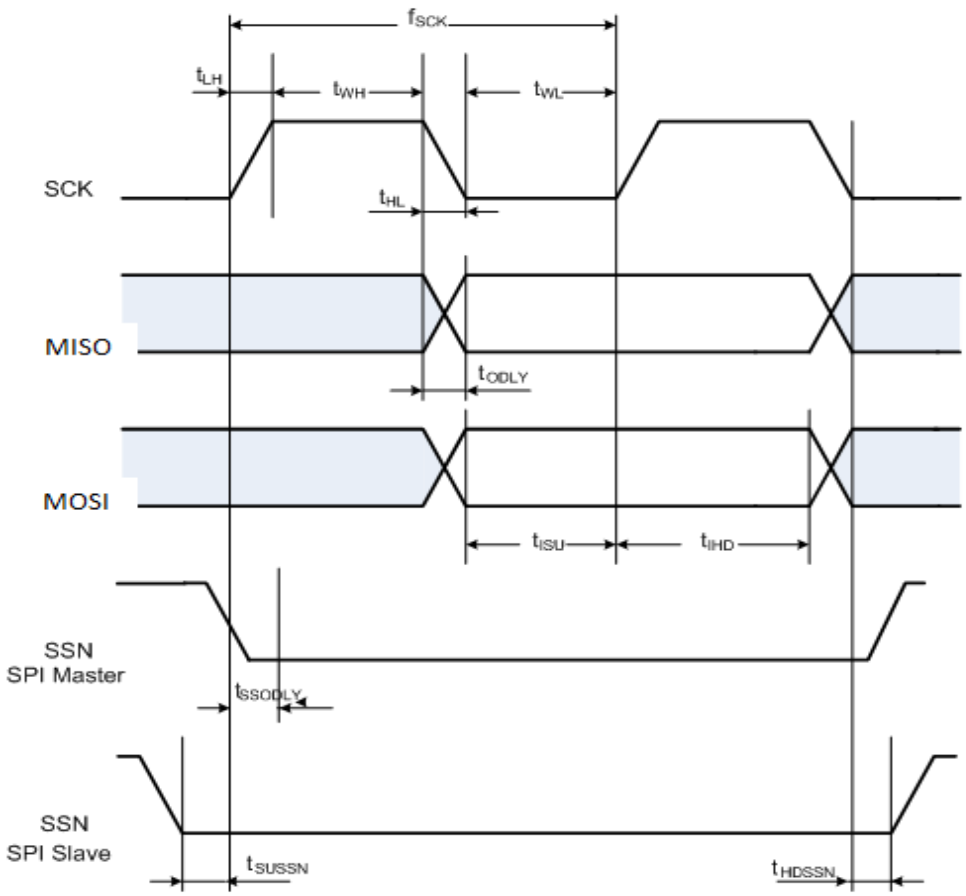


Table 7-2. SPI Slave Timing Parameters (1)

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency (2)	f_{SCK}		48	MHz
Clock Low Pulse Width	t_{WL}	4		ns
Clock High Pulse Width	t_{WH}	5		
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay (3)	t_{ODLY}	4	9 from SCK fall 12.5 from SCK rise	
RXD Input Setup Time	t_{ISU}	1		
RXD Input Hold Time	t_{IHD}	5		
SSN Input Setup Time	t_{SUSSN}	3		
SSN Input Hold Time	t_{HDSSN}	5.5		

Notes:
1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15pF output loading.

7.2 SDIO Interface

7.2.1 Overview

When the module is configured for SDIO mode by connecting the SDIO~_SPI_CFG pin to Ground, the ATWILC1000-MR110PB has a SDIO interface. The SDIO interface can be used for control and for serial I/O of 802.11 data. The SDIO pins are mapped as shown in Table 7-3. The SDIO interface is available immediately following reset when pin 10 (SPI_CFG) is tied to ground.

The ATWILC1000-MR110PB SDIO is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50MHz. The Host can use this interface to read and write from any register within the chip as well as configure the ATWILC1000-MR110PB for data DMA.

Table 7-3. ATWILC1000 SDIO Interface Pin Mapping

Pin #	SDIO Function
10	CFG: Must be tied to ground
14	DAT3: Data 3
15	DAT2: Data 2
16	DAT1: Data 1
17	DAT0: Data 0
18	CMD: Command
19	CLK: Clock

When the SDIO card is inserted into an SDIO aware host, the detection of the card will be via the means described in SDIO specification. During the normal initialization and interrogation of the card by the host, the card will identify itself as an SDIO device. The host software will obtain the card information in a tuple (linked list) format and determine if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it will be allowed to power up fully and start the I/O function(s) built into it.

The SD memory card communication is based on an advanced 9-pin interface (Clock, Command, 4 Data and 3 Power lines) designed to operate at maximum operating frequency of 50MHz.

7.2.2 Features

- Meets SDIO card specification version 2.0
- Host clock rate variable between 0 and 50MHz
- 1 bit/4-bit SD bus modes supported
- Allows card to interrupt host
- Responds to Direct read/write (IO52) and Extended read/write (IO53) transactions
- Supports Suspend/Resume operation

7.2.3 SDIO Timing

Figure 7-2. SDIO Timing Diagram

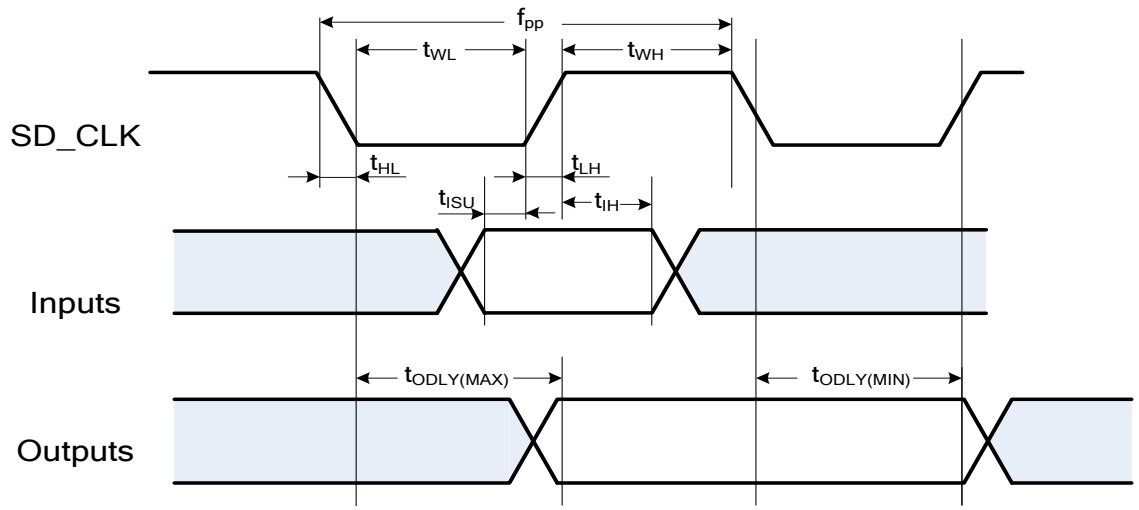


Table 7-4. SDIO Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency (1)	f_{PP}		50	MHz
Clock Low Pulse Width	t_{WL}	9		ns
Clock High Pulse Width	t_{WH}	4.5		ns
Clock Rise Time	t_{LH}	0	5	ns
Clock Fall Time	t_{HL}	0	5	ns
Input Setup Time	t_{ISU}	6		ns
Input Hold Time	t_{IH}	4		ns
Output Delay (2)	t_{ODLY}	3	11	ns

Notes: 1. Maximum clock frequency specified is limited by the SDIO Slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
2. Timing based on 15pF output loading.

7.3 I²C Interface

7.3.1 Overview

The ATWILC1000-MR110PB provides an I²C bus slave that allows for easy debugging of the ATWILC1000-MR110PB devices. The ATWILC1000-MR110PB supports I²C bus Version 2.1 – 2000.

The I²C interface, used primarily for debug, is a two-wire serial interface consisting of a serial data line (SDA, Pin 17) and a serial clock (SCL, Pin 18). It responds to the seven bit address value 0x60. The ATWILC1000-MR110PB I²C interface can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I²C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to

perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1.”

7.3.2 I²C Timing

The I²C timing is provided in Figure 7-3 and Table 7-5.

Figure 7-3. I²C Timing Diagram

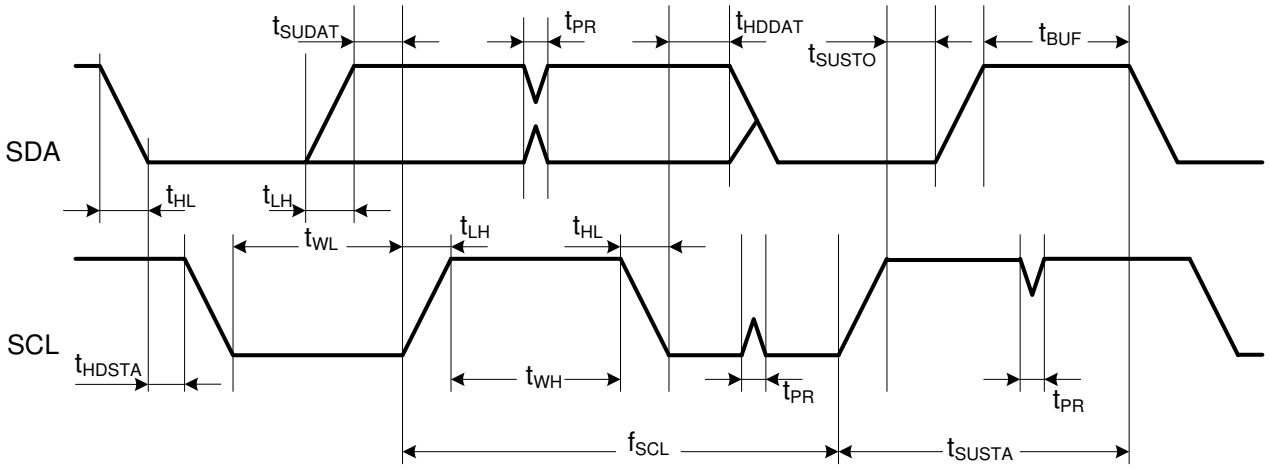


Table 7-5. I²C Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6		µs	
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300	ns	This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6		µs	
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40		ns ns	Slave and Master Default Master Programming Option
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3		µs	
Glitch Pulse Reject	t_{PR}	0	50	ns	

7.4 Wi-Fi/Bluetooth Coexistence

ATWILC1000B-MR110PB supports 2-wire and 3-wire Wi-Fi/Bluetooth Coexistence signaling conforming to the IEEE 802.15.2-2003 standard, Part 15.2. The type of coexistence interface used (2- or 3-wire) is chosen to be

compatible with the specific Bluetooth device used in a given application. Coexistence interface can be enabled on the following pins: GPIO_1, GPIO_3, GPIO_4, GPIO_5, GPIO_6, I2C_SCL, I2C_SDA – each of these pins can be configured for any function of the coexistence interface. Table 7-6 shows a usage example of the 2-wire interface using the GPIO_3 and GPIO_4 pins; 3-wire interface using the GPIO_3, GPIO_4, and GPIO_5 pins; for more specific instructions on configuring Coexistence refer to Atmel Wi-Fi eFuse Programming Guide.

Table 7-6. Coexistence Pin Assignment Example

Pin name	Pin #	Function	Target	2-wire	3-wire
GPIO_3	25	BT_Req	BT is requesting to access the medium to transmit or receive. Goes high on TX or RX slot.	Used	Used
GPIO_4	26	WL_Act	Device response to the BT request. High - BT_req is denied and BT slot blocked.	Used	Used
GPIO_5	27	BT_Pri	Priority of the BT packets in the requested slot. High to indicate high priority and low for normal.	Not Used	Used
GPIO_6	1	Ant_SW	Direct control on Antenna (coex bypass)	Optional	Optional

8 Power Consumption

8.1 Description of Device States

ATWILC1000B has several Devices States:

- ON_Transmit_High_Power – Device is actively transmitting an 802.11 signal. Highest output power and nominal current consumption.
- ON_Transmit_Low_Power – Device is actively transmitting an 802.11 signal. Reduced output power and reduced current consumption.
- ON_Receive_High_Power – Device is actively receiving an 802.11 signal. Lowest sensitivity and nominal current consumption.
- ON_Receive_Low_Power – Device is actively receiving an 802.11 signal. Degraded sensitivity and reduced current consumption.
- ON_Doze– Device is on but is neither transmitting nor receiving
- Power_Down – Device core supply off (Leakage)

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – Device pin (pin #22) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state CHIP_EN has to change between high and low (GND) voltage. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (see Section 8.3).

8.2 Current Consumption in Various Device States

Table 8-1. Current Consumption

Device state	Code rate	Output power [dBm]	Current consumption (1)	
			I_{VBATT}	I_{VDDIO}
ON_Transmit_High_Power	802.11b 1Mbps	19.5	294mA	22mA
	802.11b 11Mbps	20.5	290mA	22mA
	802.11g 6Mbps	19.5	292mA	22mA
	802.11g 54Mbps	17.5	250mA	22mA
	802.11n MCS 0	18.0	289mA	22mA
	802.11n MCS 7	15.5	244mA	22mA
ON_Transmit_Low_Power	802.11b 1Mbps	18.0	233mA	2mA
	802.11b 11Mbps	18.5	231mA	2mA
	802.11g 6-18Mbps	17.0	146mA	2mA
	802.11g >18Mbps	N/A	N/A	N/A
	802.11n MCS 0-3	15.5	132mA	2mA
	802.11n >MCS 3	N/A	N/A	N/A
ON_Receive_High_Power	802.11b 1Mbps	N/A	52.5mA	22mA
	802.11b 11Mbps	N/A	52.5mA	22mA

Device state	Code rate	Output power [dBm]	Current consumption (1)	
			I_{VBATT}	I_{VDDIO}
	802.11g 6Mbps	N/A	55.0mA	22mA
	802.11g 54Mbps	N/A	57.5mA	22mA
	802.11n MCS 0	N/A	54.0mA	22mA
	802.11n MCS 7	N/A	58.5mA	22mA
ON_Receive_Low_Power	802.11b 1Mbps	N/A	63.5mA	2.4mA
	802.11b 11Mbps	N/A	64.2mA	2.4mA
	802.11g 6Mbps	N/A	65.4mA	2.4mA
	802.11g 54Mbps	N/A	65.4mA	2.4mA
	802.11n MCS 0	N/A	65.6mA	2.4mA
	802.11n MCS 7	N/A	70.1mA	2.4mA
ON_Doze	N/A	N/A	380µA	<10µA
Power_Down	N/A	N/A	<0.5µA	<0.2µA

Note: 1. Conditions: VBATT @ 3.6v, VDDIO@ 3.3V, temp. 25℃.

8.3 Restrictions for Power States

When no power supplied to the device, i.e., the DC/DC Converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

8.4 Power-up/down Sequence

The power-up/down sequence for ATWILC1000B is shown in Figure 8-1. The timing parameters are provided in Table 8-2.

Figure 8-1. Power-up/down Sequence

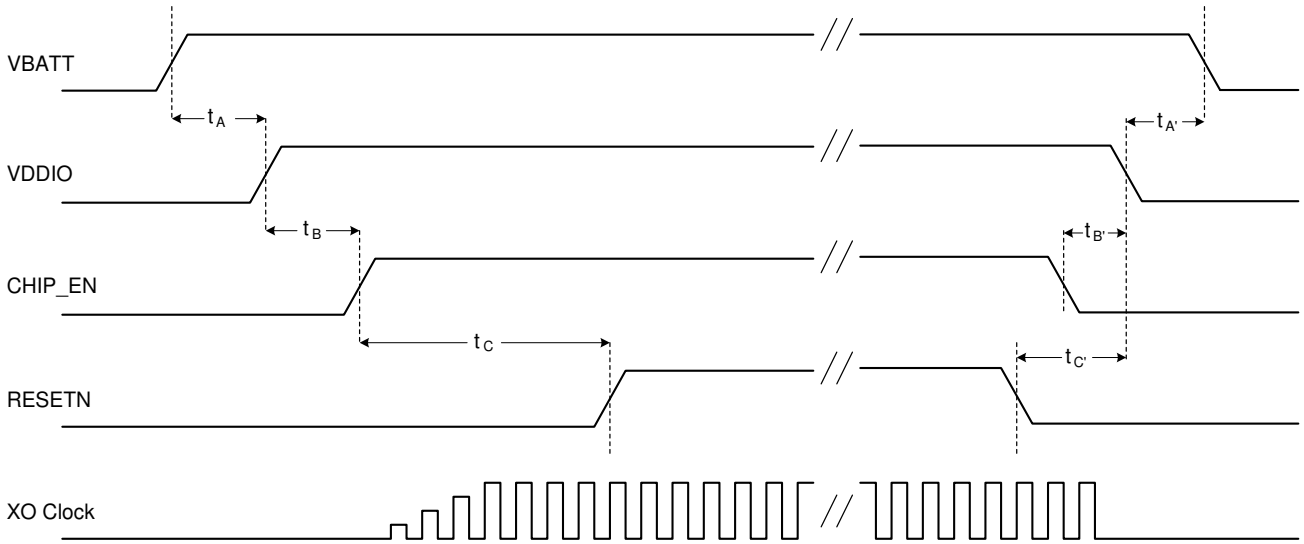


Table 8-2. Power-up/down Sequence Timing

Parameter	Min.	Max.	Unit	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5		ms	CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0		ms	VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0		ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0		ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

8.5 Digital I/O Pin Behavior during Power-up Sequences

Table 8-3 represents digital I/O pin states corresponding to device power modes.

Table 8-3. Digital I/O Pin Behavior in Different Device States

Device state	VDDIO	CHIP_EN	RESETN	Output driver	Input driver	Pull-up/down resistor (96Ω)
Power_Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Disabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

9 Notes on Interfacing to the ATWILC1000-MR110PB

9.1 Programmable Pull-up Resistors

The ATWILC1000-MR110PB provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused module pin on the ATWILC1000-MR110PB should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATWILC1000-MR110PB is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. Since the value of the pull-up resistor is approximately 100KΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current through each pull-up resistor that is driven low would be approximately 3.3V/100K = 33µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

See the Atmel Wi-Fi eFuse Programming Guide for information on enabling/disabling the programmable pull-up resistors.

10 RF Performance Placement Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

Module must be placed on main board - printed antenna area must overlap with the carrier board. The portion of the module containing the antenna should not stick out over the edge of the main board. The antenna is designed to work properly when it is sitting directly on top of a 1.5mm thick printed circuit board.

If the module is placed at the edge of the main board, a minimum 22mm by 5mm area directly under the antenna must be clear of all metal on all layers of the board. “In-land” placement is acceptable; however, deepness of keep-out area must grove to: module edge to main board edge plus 5mm. DO NOT PLACE MODULE IN THE MIDDLE OF THE MAIN BOARD OR FAR AWAY FROM THE MAIN BOARD EDGE.

Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking.

Do not enclose the antenna within a metal shield.

Keep any components which may radiate noise or signals within the 2.4GHz – 2.5GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.

Contact Atmel for assistance if any other placement is required.

10.1 External Antenna Types

The ATWILC1000-MR110UB module has an ultra-miniature coaxial connector (u.FL) for the external antenna.

The choice of antenna is limited to the antenna types in which the module was tested and approved. For a list of tested and approved antennas that may be used with the module, refer to the respective country in section 15 “Regulatory Approval”.

Table 10-1 below lists the approved antenna types.

Table 10-1. Tested External Antenna Types

Antenna Type	Gain
PCB Antenna	2dBi

11 Reflow Profile Information

This chapter provides guidelines for reflow processes in getting the Atmel module soldered to the customer's design.

11.1 Storage Condition

11.1.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH.

The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

11.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, <30%.

11.2 Stencil Design

The recommended stencil is laser-cut, stainless-steel type with thickness of 100µm to 130µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25µm larger than the top can be utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

11.3 Baking Conditions

This module is rated at MSL level 3. After sealed bag is opened, no baking is required within 168 hours so long as the devices are held at <= 30°C/60% RH or stored at <10% RH.

The module will require baking before mounting if:

1. The sealed bag has been open for > 168 hours.
2. Humidity Indicator Card reads >10%.
3. SIPs need to be baked for 8 hours at 125°C.

11.4 Soldering and Reflow Condition

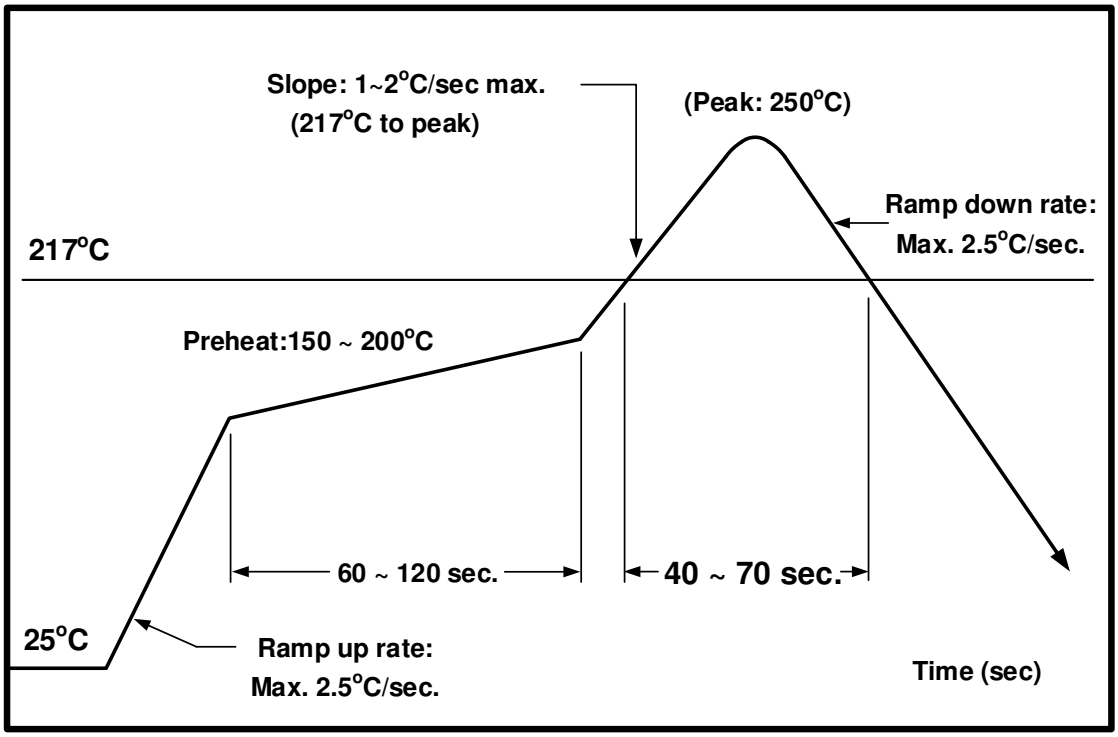
11.4.1 Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. Nitrogen atmosphere has shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items should also be observed in the reflow process:

1. Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V Type 3, no clean paste.
2. Allowable reflow soldering iterations: Three times based on the following reflow soldering profile (as shown in Figure 11-1).
3. Temperature profile: Reflow soldering shall be done according to the following temperature profile (as shown in Figure 11-1).
4. Peak temperature: 250°C.

Figure 11-1. Solder Reflow Profile



11.5 Module Assembly Considerations

The ATWILC1000-MR110PB modules are assembled with an EMI Shield to ensure compliance with EMI emission and immunity rules. The EMI shield is made of a tin-plated steel (SPTE) and is not hermetically sealed. Solutions like IPA and similar solvents can be used to clean the ATWILC1000-MR110PB module. However, cleaning solutions, which contain acid, should never be used on the module.

The Atmel/Microchip ATWILC1000-MR110PB modules are manufactured without any conformal coating applied. It is the customer's responsibility if a conformal coating is specified and applied to the ATWILC1000-MR110PB module.

12 Application Reference Design

The ATWILC1000-MR110PB reference design schematic is shown in Figure 12-1.

Figure 12-1. ATWILC1000-MR110PB SDIO

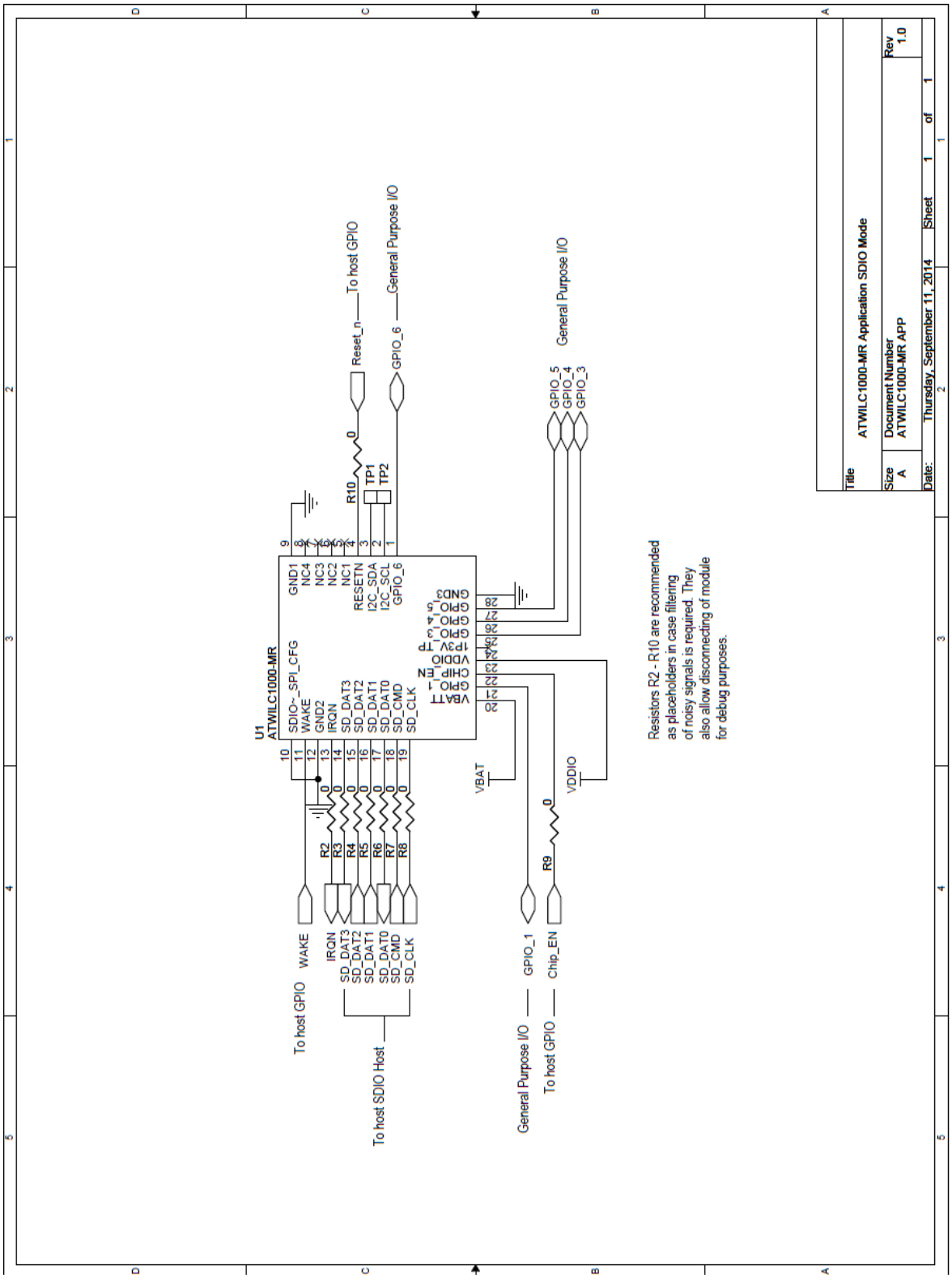
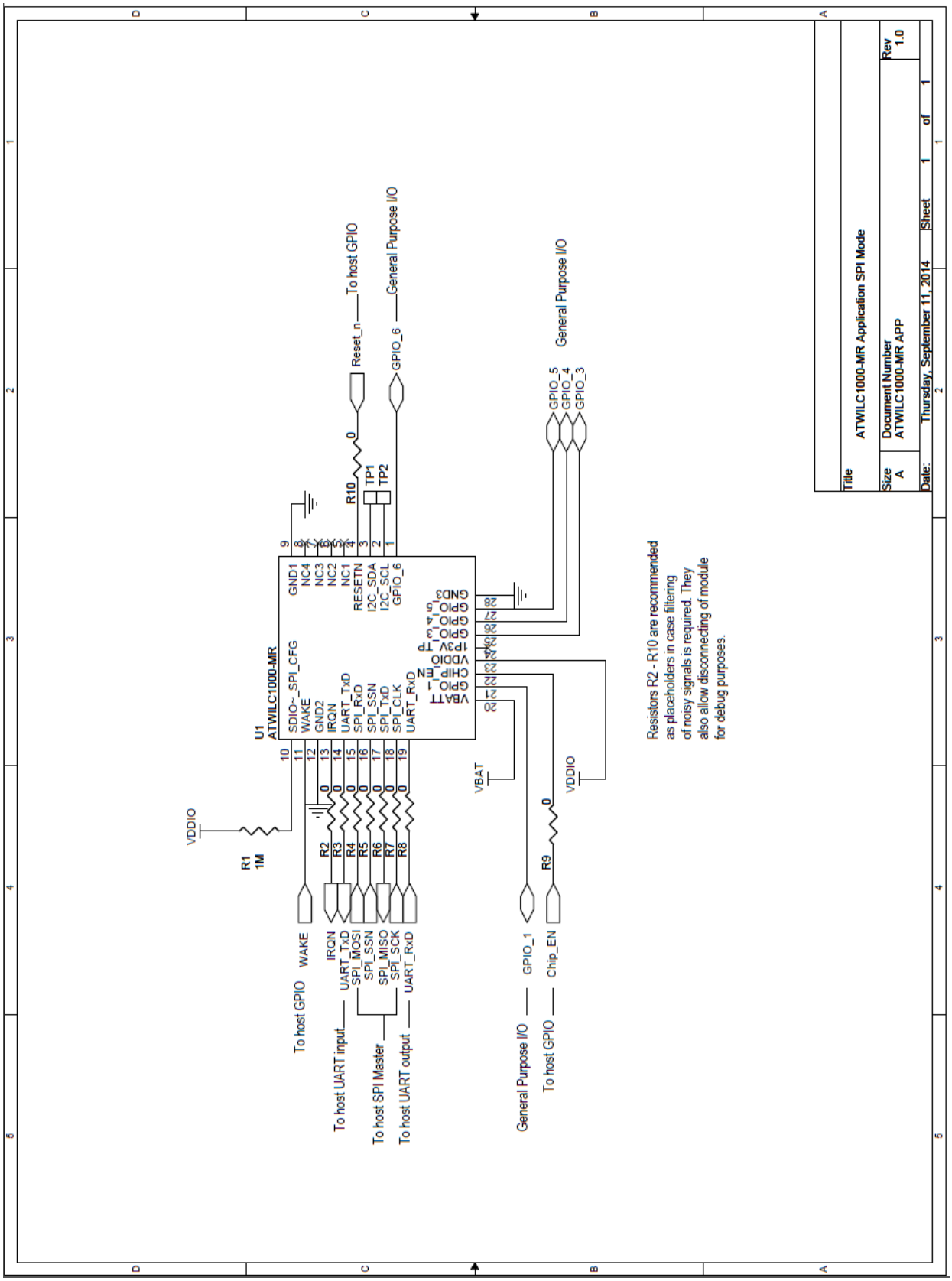


Figure 12-2. ATWILC1000-MR110PB SPI



13 Reference Documentation and Support

13.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp.

The following list of documents available on Atmel web or integrated into development tools.

To enable fast development contact your local FAE or visit the http://www.atmel.com/.

Title	Content
Datasheet	This Document
Design Files Package	User Guide, Schematic, PCB layout, Gerber, BOM, and System notes on: RF/Radio Full Test Report, radiation pattern, design guidelines, temperature performance, ESD.
Platform Getting Started Guide	How to use package: Out of the Box starting guide, HW limitations, and notes, SW Quick start guidelines.
HW Design Guide	Best practices and recommendations to design a board with the product, including: Antenna Design for Wi-Fi (layout recommendations, types of antennas, impedance matching, using a power amplifier, etc.), SPI protocol between Wi-Fi SoC and the Host MCU.
SW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters, and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
SW Programmer Guide	Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample App note

For a complete listing of development-support tools and documentation, visit http://www.atmel.com/, or contact the nearest Atmel field representative.

14 Certification Notices

Regulatory Approvals received:

ATWILC1000-MR110PB

- United States/FCC ID:2ADHKATWILC1000
- Canada
  - IC ID: 20266-ATWILC1000
  - HVIN: ATWILC1000-MR110PB

ATWILC1000-MR110UB

- United States/FCC ID:2ADHKATWILC1000U

15 Regulatory Approval

This section outlines the regulatory information for the ATWILC1000-MR110PB and ATWILC1000-MR110UB modules for the following countries:

- • United States
- • Canada

Note that not all device models are certified by all agencies.

15.1 United States

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” modular approval in accordance with Part 15.212 Modular Transmitter approval. Modular approval allows the end user to integrate the ATWILC1000-MR110PB or ATWILC1000-MR110UB module into a finished product without obtaining subsequent and separate FCC approvals for intentional radiation, provided no changes or modifications are made to the module circuitry. Changes or modifications could void the user’s authority to operate the equipment.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

The finished product is required to comply with all applicable FCC equipment authorizations regulations, requirements and equipment functions not associated with the transmitter module portion. For example, compliance must be demonstrated to regulations for other transmitter components within the host product; to requirements for unintentional radiators (Part 15 Subpart B “Unintentional Radiators”), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Verification, or Declaration of Conformity) (e.g., transmitter modules may also contain digital logic functions) as appropriate.

15.1.1 Labeling And User Information Requirements

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have been labeled with its own FCC ID number, and if the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label can use wording as follows:

For the ATWILC1000-MR110PB:

Contains Transmitter Module FCC ID: 2ADHKATWILC1000 **or**

Contains FCC ID: 2ADHKATWILC1000

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

For the ATWILC1000-MR110UB:

Contains Transmitter Module FCC ID: 2ADHKATWILC1000U or

Contains FCC ID: 2ADHKATWILC1000U

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

A user's manual for the finished product should include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) https://apps.fcc.gov/oetcf/kdb/index.cfm.

15.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification.

In the end product, the antenna(s) used with this transmitter must be installed to provide a separation distance of at least 6.5 cm from all persons and must not be co-located or operation in conjunction with any other antenna or transmitter. User and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying the RF exposure compliance.

15.1.3 Approved Antenna Types

To maintain modular approval in the United States, only the antenna types that have been tested shall be used. It is permissible to use different antenna provided the same antenna type and antenna gain (equal to or less than) is used. An antenna type comprises antennas having similar in-band and out-of-band radiation patterns.

Testing the ATWILC1000-MR110UB module was performed with the antenna types listed in Table 10-1.

15.1.4 Helpful Web Sites

Federal Communications Commission (FCC): http://www.fcc.gov

FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB)

https://apps.fcc.gov/oetcf/kdb/index.cfm.

15.2 Canada

The ATWILC1000-MR110PB module has been certified for use in Canada under Innovation, Science, and Economic Development (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

15.2.1 Labeling and User Information Requirements

Labeling Requirements (from RSP-100 - Issue 10, Section 3): The host device shall be properly labeled to identify the module within the host device.

Modular Devices (from RSP-100 - Issue 10, Section 7): The Industry Canada certification label of a module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labeled to display the Industry Canada certification number of the module, preceded by the words “Contains transmitter module”, or the word “Contains”, or similar wording expressing the same meaning, as follows:

For the ATWILC1000-MR110PB module:

Contains transmitter module IC: 20266-ATWILC1000

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 4, November 2014): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device complies with Industry Canada license exempt RSS standard(s). Operation is subject to the following two conditions:

(1) This device may not cause interference, and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Transmitter Antenna (From Section 8.3 RSS-GEN, Issue 4, November 2014): User manuals, for transmitters shall display the following notice in a conspicuous location:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établisse-ment d'une communication satisfaisante.

The above notice may be affixed to the device instead of displayed in the user manual.

15.2.2 RF Exposure

All transmitters regulated by IC must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radio communication Apparatus (All Frequency Bands).

15.2.3 Helpful Web Sites

Industry Canada: http://www.ic.gc.ca/

16 Revision History

Doc Rev.	Date	Comments
42503C	11/2016	1. Updated the device pinout drawing Figure 3-1 to make it easier to read. 2. Added section 11.5 regarding PCBA coatings. 3. Updated Marking diagram in Figure 1-2. 4. Revised values for Transmit Power and added notes in Table 6-3. 5. Added Pins and Agencies to Ordering Information in Table 1-1. 6. Added section 10.1 for External Antenna Types for ATWILC1000-MR110UB 7. Added section 14 for Certification Notices. 8. Added section 15 Regulatory Approval. 9. Updated Description to indicate both the MR110PB and MR110UB are covered. 10. Removed "With seamless roaming capabilities" from description. 11. Revised description to remove Seamless Roaming. 12. Revised features to only support SPI and SDIO hosts. 13. Removed references to WAPI. 14. Removed UART. 15. Moved Solder Pad drawing to be with POD drawings as Figure 3-4. 16. Minor edits.
42503B	5/2016	1. Revised POD drawings in Section 3.2. 2. Revised Footprint drawing in Section **Error! Reference source not found.**. 3. Removed Module schematics and BOM's. 4. Added Reflow profile Chapter 11. 5. Updated SDIO timing content in Table 7-4. 6. Added footnotes to recommended operating ratings in Table 4-2. 7. Updated SPI timing content in Table 7-2.
42503A	08/2015	Updated due to changes from ATWILC100A(42380D) to ATWILC1000B: 1. Updated power numbers and description, added high-power and low-power modes. 2. Updated radio performance numbers. 3. Fixed typos in SPI interface timing. 4. Added hardware accelerators in feature list (security and checksum). 5. Increased instruction RAM size from 128KB to 160KB. 6. Improved and corrected description of Coexistence interface. 7. Miscellaneous minor updates and corrections.

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