STMUX1800E

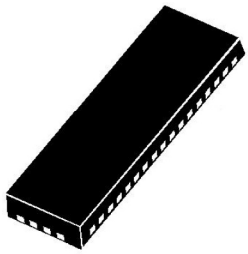
16-bit to 8-bit MUX/DEMUX for gigabit Ethernet LAN switch with LED switch and enhanced ESD protection

Features

- Low R_{ON}: 4.0 Ω typical
- V_{CC} operating range: 3.0 to 3.6 V
- Enhanced ESD protection: > 8 kV (contact) and 15 kV (HBM)
- Low power mode for minimum power consumption
- Channel on capacitance: 9.5 pF typical
- Switching time speed: 9 ns
- Near to zero propagation delay: 250 ps
- Very low crosstalk: -45 dB at 250 MHz
- Bit-to-bit skew: 200 ps
- > 600 MHz -3 dB typical bandwidth (or data frequency)
- Three SPDT switches for LED support
- Rail-to-rail switching on data I/O ports (0 V to 5 V)
- Package: QFN42
- Lead-free

Applications

- 10/100/1000 Mbit Ethernet switching
- Audio/video switching



QFN42

Description

The STMUX1800E is a 16 to 8-bit multiplexer/ demultiplexer low R_{ON} bidirectional LAN switch designed for various standards, such as 10/100/1000 Ethernet. It is designed for very low crosstalk, low bit-to-bit skew and low I/O capacitance.

The differential signal from the Gigabit Ethernet transceiver is multiplexed into one of two selected outputs while the unselected switch goes to Hi-Z status.

The device integrates three SPDT (single pole dual throw) switches, for LED support.

The device can be put into low power mode consuming minimum power.

Table 1. Device summary

Order code	Package	Packing
STMUX1800EQTR	QFN42	Tape and reel

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1 Pin description

Figure 1. Pin connection (top through view)

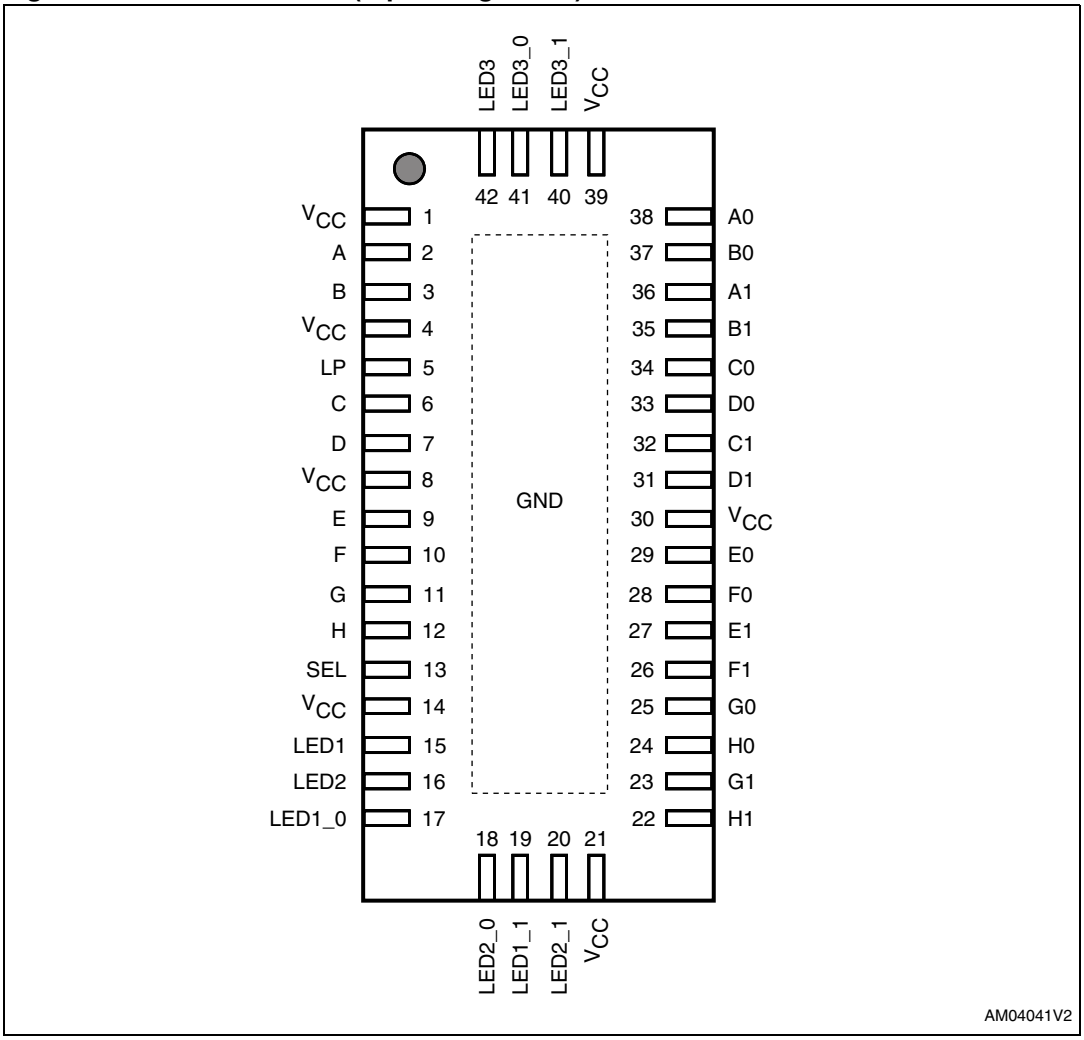


Table 2. Pin description

Pin	Symbol	Name and function
2, 3, 6, 7, 9, 10, 11, 12	A, B, C, D, E, F, G, H	8-bit bus
38, 37, 34, 33, 29, 28, 25, 24	A0, B0, C0, D0, E0, F0, G0, H0	8-bit multiplexed to bus 0
36, 35, 32, 31, 27, 26, 23, 22	A1, B1, C1, D1, E1, F1, G1, H1	8-bit multiplexed to bus 1
5	LP	Low power mode enable
13	SEL	Bus and LED switch selection
15, 16, 42	LED1, LED2, LED3	LED switch input
17, 18, 41, 19, 20, 40	LED1_0, LED2_0, LED3_0, LED1_1, LED2_1, LED3_1	LED switch output
1, 4, 8, 14, 21, 30, 39	V_{CC}	Supply voltage

Figure 2. Input equivalent circuit

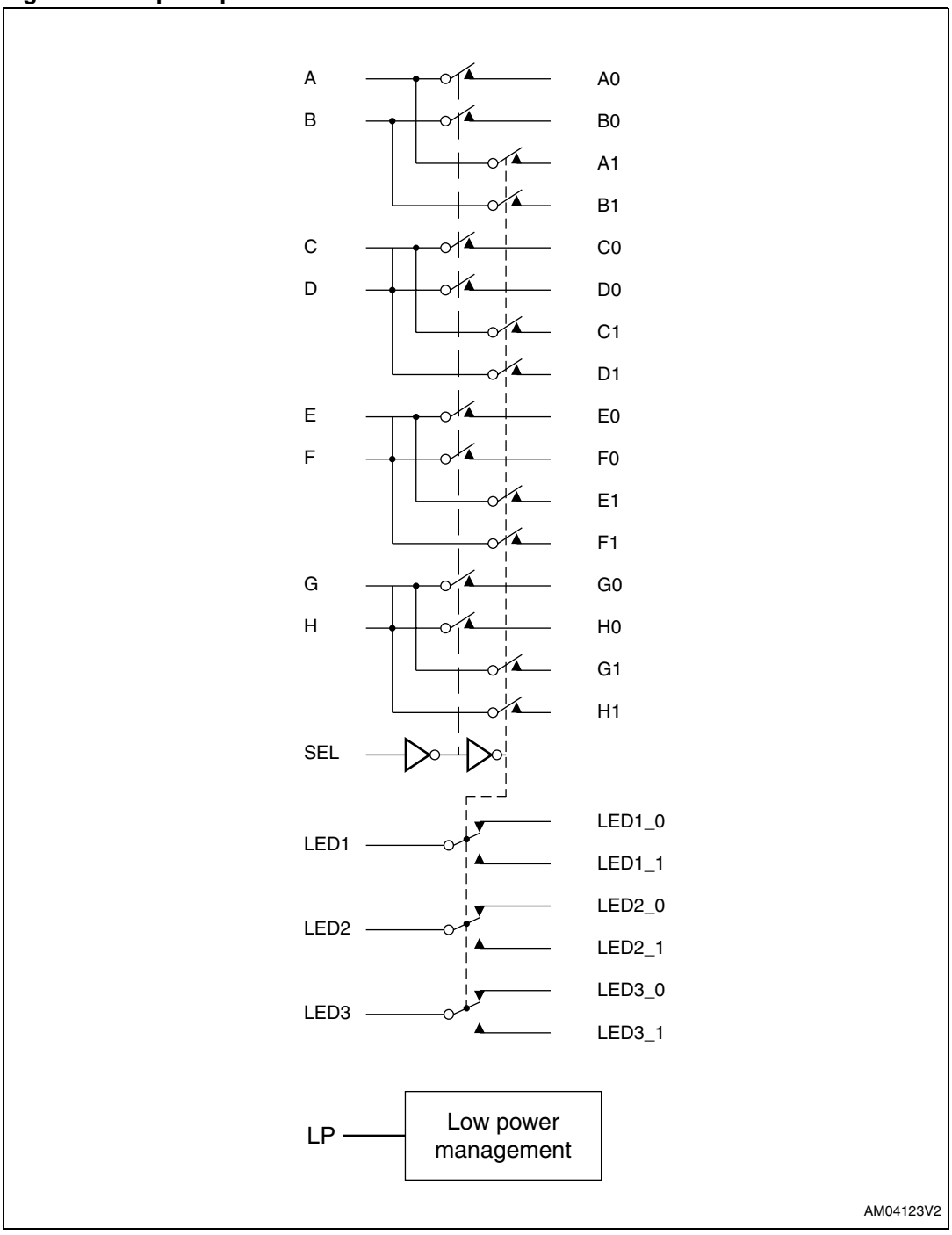


Table 3. LAN switch function table

LP	SEL	Function
L	L	8-bit bus to 8-bit multiplexed bus 0
L	H	8-bit bus to 8-bit multiplexed bus 1
H	X	Bus 0 and 1 in Hi-Z

Table 4. LED switch function table

LP	SEL	Function
L	L	LED switch input connected to LED switch output X_0
L	H	LED switch input connected to LED switch output X_1
H	X	Output X_0 and X_1 in Hi-Z

2 Maximum rating

Stressing the device above the rating listed in *Table 5: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 6: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage to ground	-0.5 to 4.6	V
V_{IO}	DC input output voltage	-0.5 to 4.6	V
V_{IC}	DC control input voltage	-0.5 to 4.6	V
I_O	DC output current(1)	120	mA
P_D	Power dissipation	0.5	W
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 seconds)	300	°C

1. If V_{IO} x I_O does not exceed the maximum limit of P_D.

Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage to ground	3	—	3.6	V
V_{IC}	DC control input voltage (SEL, LP)	0	—	V_{CC}	V
V_{IO}	DC input/output voltage	0	—	V_{CC}	V
T_A	Operating temperature	-40	—	85	°C

3 Electrical characteristics

Table 7. DC electrical characteristics for Gigabit Ethernet LAN8/16MUX/DEMUX (V_{CC} = 3.3 V ±10%)

Symbol	Parameter	Test condition	Value			Unit
			-40 to 85 °C			
			Min.	Typ.	Max.	
V_{IH}	Voltage input high (SEL, LP)	High level guaranteed	2.4	—	—	V
V_{IL}	Voltage input low (SEL, LP)	Low level guaranteed	-0.5	—	0.8	V
V_{IK}	Clamp diode voltage (SEL, LP)	V_{CC} = 3.6 V I_{IN} = -18 mA	—	-0.8	-1.2	V
I_{IH}	Input high current (SEL, LP)	V_{CC} = 3.6 V V_{IN} = V_{CC}	—	—	±5	µA
I_{IL}	Input low current (SEL, LP)	V_{CC} = 3.6 V V_{IN} = GND	—	—	±5	µA
$IOFF_{(SW)}$[1]	Leakage current through the switch common terminals (A to H) (LED1 to LED3)	V_{CC} = 3.6 V A to H = V_{CC} LED1 to LED3 = V_{CC} A0 to H0 = 0 V A1 to H1 = floating LEDx_0 = 0 V LEDx1 = floating SEL = V_{CC} LP = GND	—	—	±1	µA
Ioff(sw_LP)	Leakage current through the switch in LP mode	V_{CC} = 3.6 V; A to H = V_{CC}; LED1 to LED3 = V_{CC}; A0 to H0, A1 to H1 = 0V; LEDx_0, LEDx_1 = 0V LP = V_{CC}			±10	µA
$IOFF_{(SEL)}$	SEL pin leakage current	V_{CC} = 0 V SEL = 0 to 3.6 V	—	—	±1	µA
R_{ON}	Switch ON resistance[2]	V_{CC} = 3.0 V V_{IN} = 1.5 to V_{CC} I_{IN} = -40 mA	—	4.0	6.5	Ω

Table 7. DC electrical characteristics for Gigabit Ethernet LAN8/16MUX/DEMUX (V_{CC} = 3.3 V ±10%) (continued)

Symbol	Parameter	Test condition	Value			Unit
			-40 to 85 °C			
			Min.	Typ.	Max.	
R_{FLAT}	ON resistance flatness(2), (3)	V_{CC} = 3.0 V V_{IN} at 1.5 and V_{CC} I_{IN} = -40 mA	—	0.5	—	Ω
ΔR_{ON}	ON resistance match between channel $\Delta R_{ON} = R_{ONMAX}-R_{ONMIN}$(2), (4)	V_{CC} = 3.0 V V_{IN} = 1.5 to V_{CC} I_{IN} = -40 mA	—	0.4	1	Ω

1. Refer to *Figure 4: Test circuit for leakage current (I_{OFF}) on page 15*.
2. Measured by voltage drop between channels at indicated current through the switch. ON resistance is determined by the lower of the voltages.
3. Flatness is defined as the difference between the R_{ONMAX} and R_{ONMIN} of ON resistance over the specified range.
4. ΔR_{ON} measured at the same V_{CC}, temperature and voltage level.

Table 8. DC electrical characteristics for 10/100 Ethernet LAN8/16MUX/DEMUX (V_{CC} = 3.3 V ±10)

Symbol	Parameter	Test condition	Value			Unit
			-40 to 85 °C			
			Min.	Typ.	Max.	
V_{IH}	Voltage input high (SEL, LP)	High level guaranteed	2.4	—	—	V
V_{IL}	Voltage input low (SEL, LP)	Low level guaranteed	-0.5	—	0.8	V
V_{IK}	Clamp diode voltage (SEL, LP)	V_{CC} = 3.6 V I_{IN} = -18 mA	—	-0.7	-1.2	V
I_{IH}	Input high current (SEL, LP)	V_{CC} = 3.6 V V_{IN} = V_{CC}	—	—	±5	µA
I_{IL}	Input low current (SEL, LP)	V_{CC} = 3.6 V V_{IN} = GND	—	—	±5	µA
$IOFF_{(SW)}$ (1)	Leakage current through the switch common terminals (A to H) (LED1 to LED3)	V_{CC} = 3.6 V A to H = V_{CC} LED1 to LED3 = V_{CC} A0 to H0 = 0 V A1 to H1 = floating LEDx_0 = 0 V LEDx1 = floating SEL = V_{CC} LP = GND	—	—	±1	µA
Ioff(sw_LP)	Leakage current through the switch in LP mode	V_{CC} = 3.6 V; A to H = V_{CC}; LED1 to LED3 = V_{CC}; A0 to H0, A1 to H1 = 0 V; LEDx_0, LEDx_1 = 0 V LP = V_{CC}			±10	µA
$IOFF_{(SEL)}$	SEL pin leakage current	V_{CC} = 0 V SEL = 0 to 3.6 V	—	—	±1	µA
R_{ON}	Switch ON resistance (2)	V_{CC} = 3.0 V V_{IN} = 1.5 to V_{CC} I_{IN} = -10 to -30 mA	—	4.0	6.5	Ω
R_{FLAT}	ON resistance flatness (2) (3)	V_{CC} = 3.0 V V_{IN} at 1.5 and V_{CC} I_{IN} = -10 to -30 mA	—	0.5	—	Ω
ΔR_{ON}	ON resistance match between channel $\Delta R_{ON} = R_{ONMAX}-R_{ONMIN}$ (2)(4)	V_{CC} = 3.0 V V_{IN} = 1.5 to V_{CC} I_{IN} = -10 to -30 mA	—	0.4	1	Ω

1. Refer to *Figure 4: Test circuit for leakage current (I_{OFF}) on page 15*.
2. Measured by voltage drop between channels at indicated current through the switch. ON resistance is determinate by the lower of the two voltages.
3. Flatness is defined as the difference between the R_{ONMAX} and R_{ONMIN} of ON resistance over the specified range.
4. ΔR_{ON} measured at the same V_{CC}, temperature and voltage level.

Table 9. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
C_{IN}	SEL pin input capacitance(1)	DC = 0.25 V AC = 0.5 V_{PP} f = 1 MHz	—	2	3	pF
C_{OFF}	Switch off capacitance(2)	DC = 0.25 V AC = 0.5 V_{PP} f = 1 MHz	—	4	5	pF
C_{ON}	Switch on capacitance(3)	DC = 0.25 V AC = 0.5 V_{PP} f = 1 MHz	—	9.5	11	pF

1. Refer to *Figure 5: Test circuit for SEL pin input capacitance (C_{IN}) on page 15*.
2. Refer to *Figure 6: Test circuit for switch off capacitance (C_{OFF}) on page 16*.
3. Refer to *Figure 7: Test circuit for switch on capacitance (C_{ON}) on page 16*.

Table 10. Power supply characteristics

Symbol	Parameter	Test condition	Value			Unit
			-40 to 85 °C			
			Min.	Typ.	Max.	
I_{CC}	Active mode power supply current	V_{CC} = 3.6 V, V_{IN} = V_{CC} or GND, LP = GND	—	150	500	µA
	Low power mode power supply current	V_{CC} = 3.6 V, V_{IN} = V_{CC} or GND, LP = V_{CC}	—	10	50	µA

Table 11. Dynamic electrical characteristics (V_{CC} = 3.3 V ±10%)

Symbol	Parameter	Test condition	Value			Unit
			-40 to 85 °C			
			Min.	Typ.	Max.	
X_{talk}	Crosstalk(1)	R_L= 100 Ω f = 250 MHz	—	-45	—	dB
O_{IRR}	Off isolation(2)	R_L= 100 Ω f = 250 MHz	—	-37	—	dB
BW	-3 dB bandwidth(3)	R_L= 100 Ω 0 < V_{IN} ≤3.6 V	—	600	—	MHz

1. Refer to *Figure 9: Test circuit for crosstalk measurement (x_{talk}) on page 18*.
2. Refer to *Figure 10: Test circuit for off isolation measurement (O_{IRR}) on page 19*.
3. Refer to *Figure 8: Test circuit for bandwidth measurement (BW) on page 17*.

Table 12. Switching characteristics (T_A = 25 °C, V_{CC} = 3.3 V ±10%)

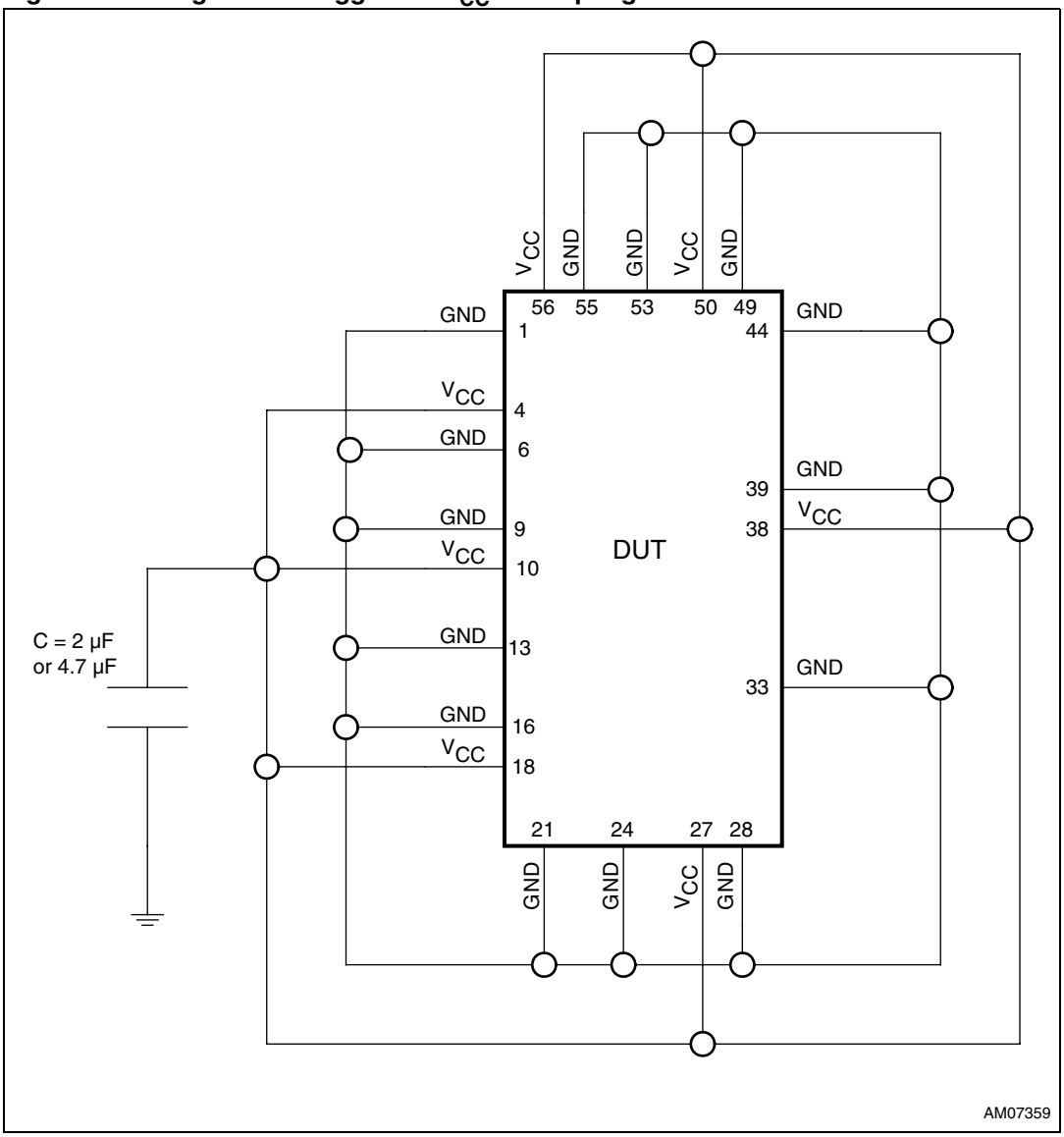
Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
t_{PD}	Propagation delay	V_{CC} = 3 to 3.6 V	—	0.25	—	ns
t_{PZH}, t_{PZL}	Line enable time, SE to x to x0 or x to x1	V_{CC} = 3 to 3.6 V	0.5	6.5	15	ns
t_{PHZ}, t_{PLZ}	Line disable time, SE to x to x0 or x to x1	V_{CC} = 3 to 3.6 V	0.5	6.5	8.5	ns
$t_{SK(O)}$	Output skew between center port to any other port	V_{CC} = 3 to 3.6 V	—	0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transition of the same output (t_{PHL}, t_{PLH})	V_{CC} = 3 to 3.6 V	—	0.1	0.2	ns

Table 13. ESD performance

Symbol	Test condition	Value			Unit
		Min.	Typ.	Max.	
ESD	Contact discharge(1) IEC61000-4-2	—	±8	—	kV
	Human body model (MIL-STD-883)	—	±15	—	kV

1. Refer to *Figure 3: Diagram for suggested V_{CC} decoupling on page 14*.

Figure 3. Diagram for suggested V_{CC} decoupling



1. Applicable for system level ESD test.
2. 100 nF capacitors must be used as local bypass capacitors between the adjacent V_{CC} and GND pairs (total 7).

Figure 4. Test circuit for leakage current (I_{OFF})

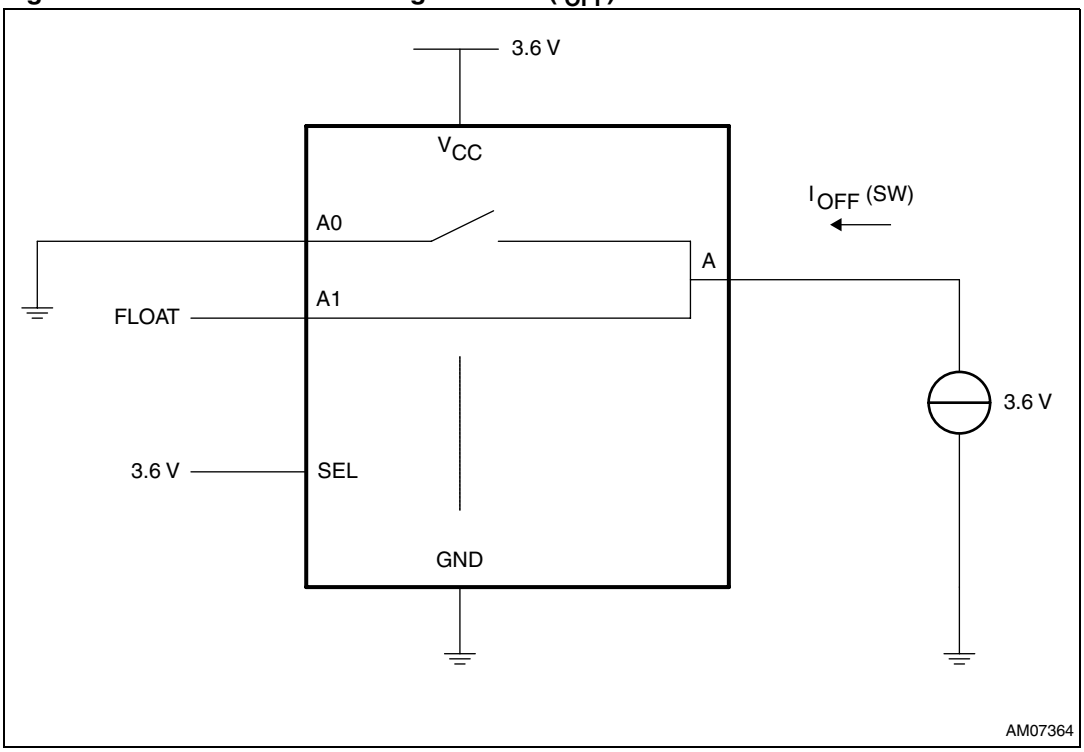


Figure 5. Test circuit for SEL pin input capacitance (C_{IN})

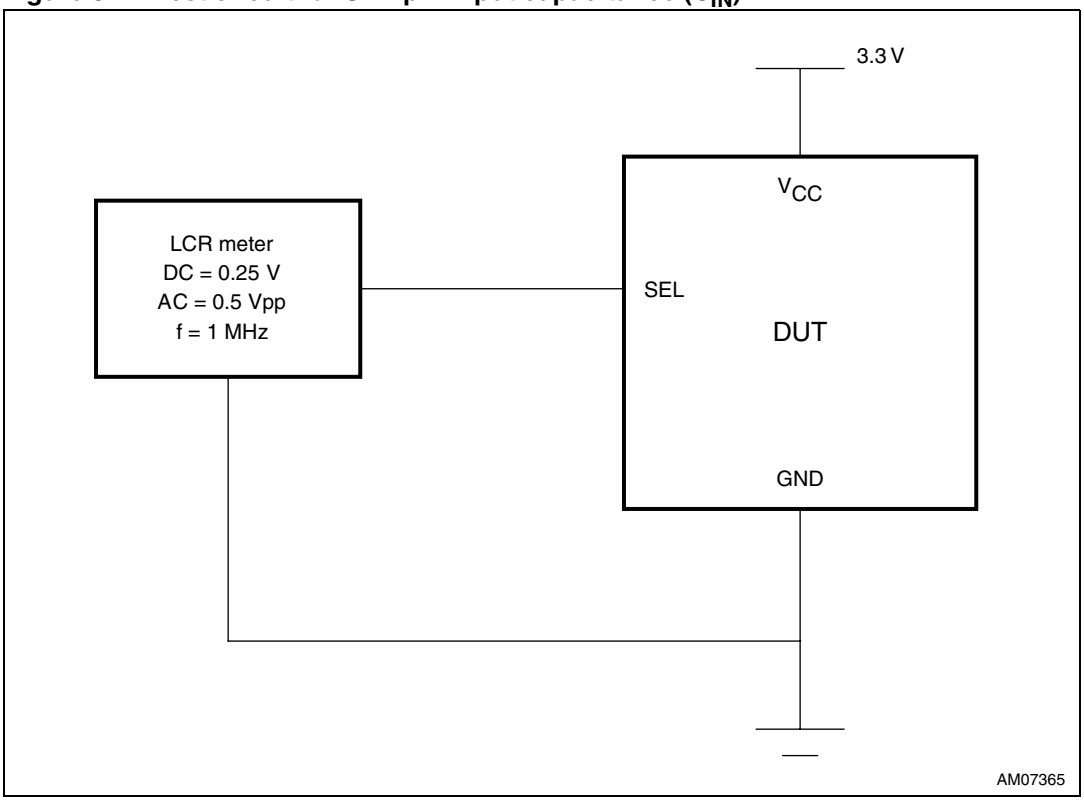


Figure 6. Test circuit for switch off capacitance (C_{OFF})

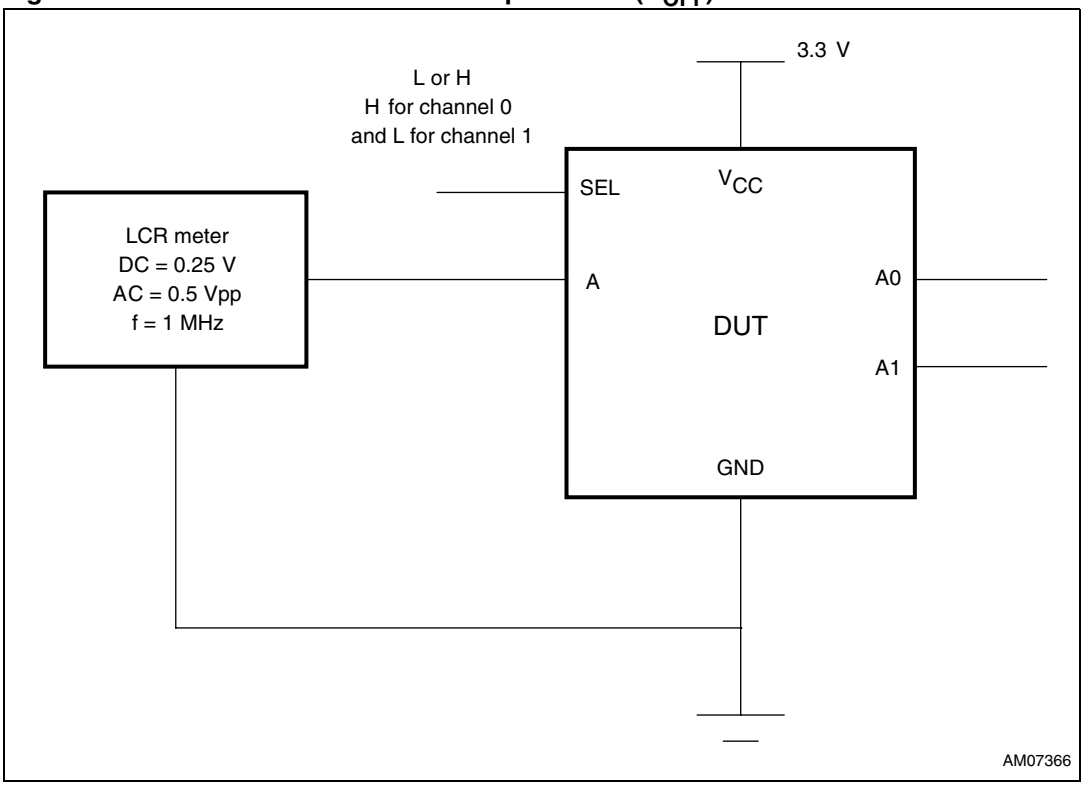


Figure 7. Test circuit for switch on capacitance (C_{ON})

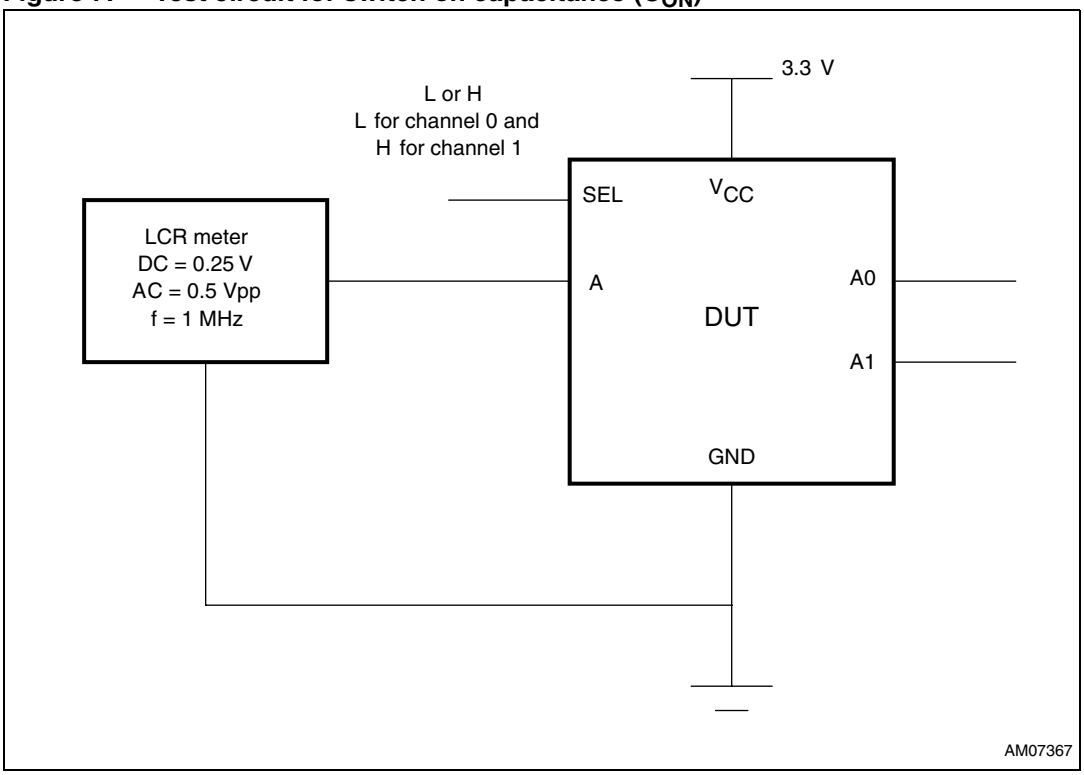
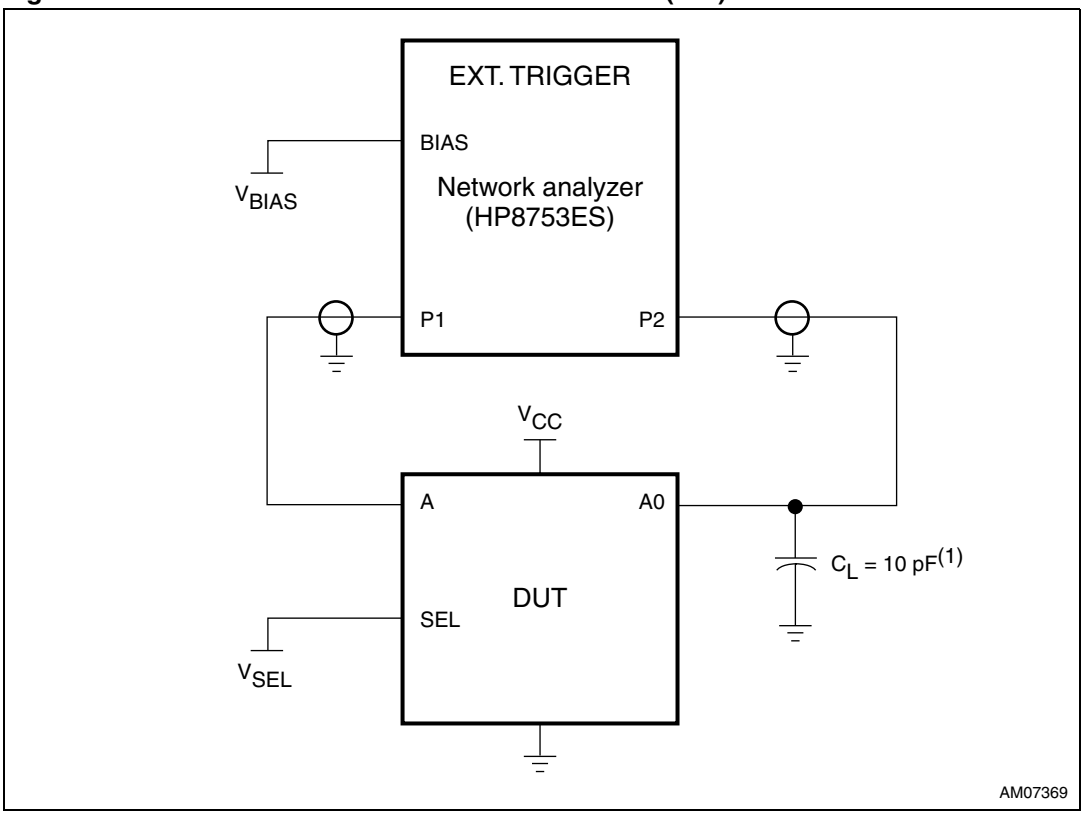


Figure 8. Test circuit for bandwidth measurement (BW)



1. C_L includes probe and jig capacitance.

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A is the input, the output is measured at A0. All unused analog I/O ports are left open.

HP8753ES setup:

Average = 4

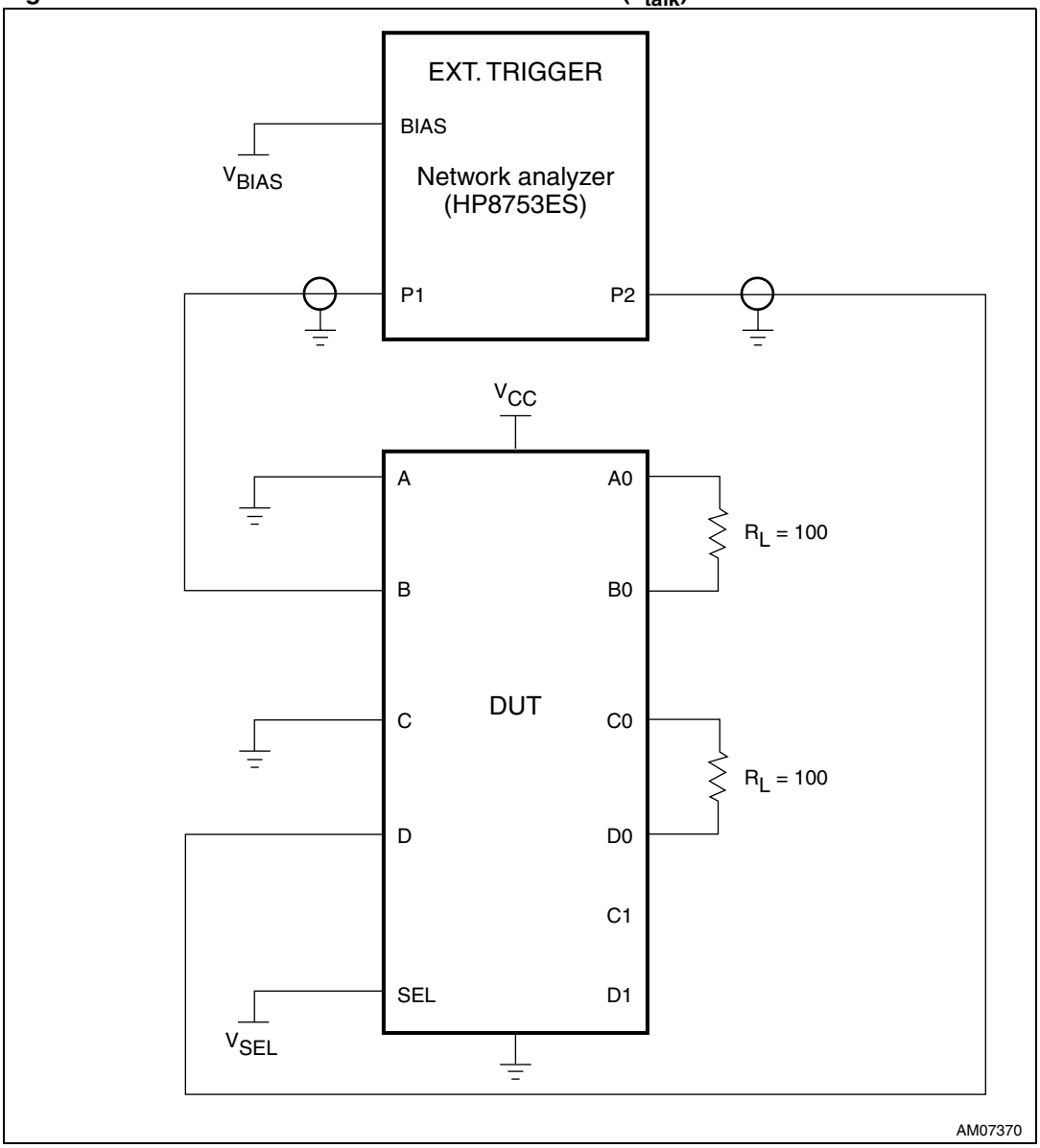
R_{BW} = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBm

Figure 9. Test circuit for crosstalk measurement (x_{talk})



1. C_L includes probe and jig capacitance.
2. A 50 Ω termination resistor is needed to match the loading of the network analyzer.

Crosstalk is measured at the output of the non-adjacent ON channel. For example, when V_{SEL} = 0, and B is the input, the output is measured at D. All unused analog input ports are connected to GND and output ports are left open.

HP8753ES setup:

Average = 4

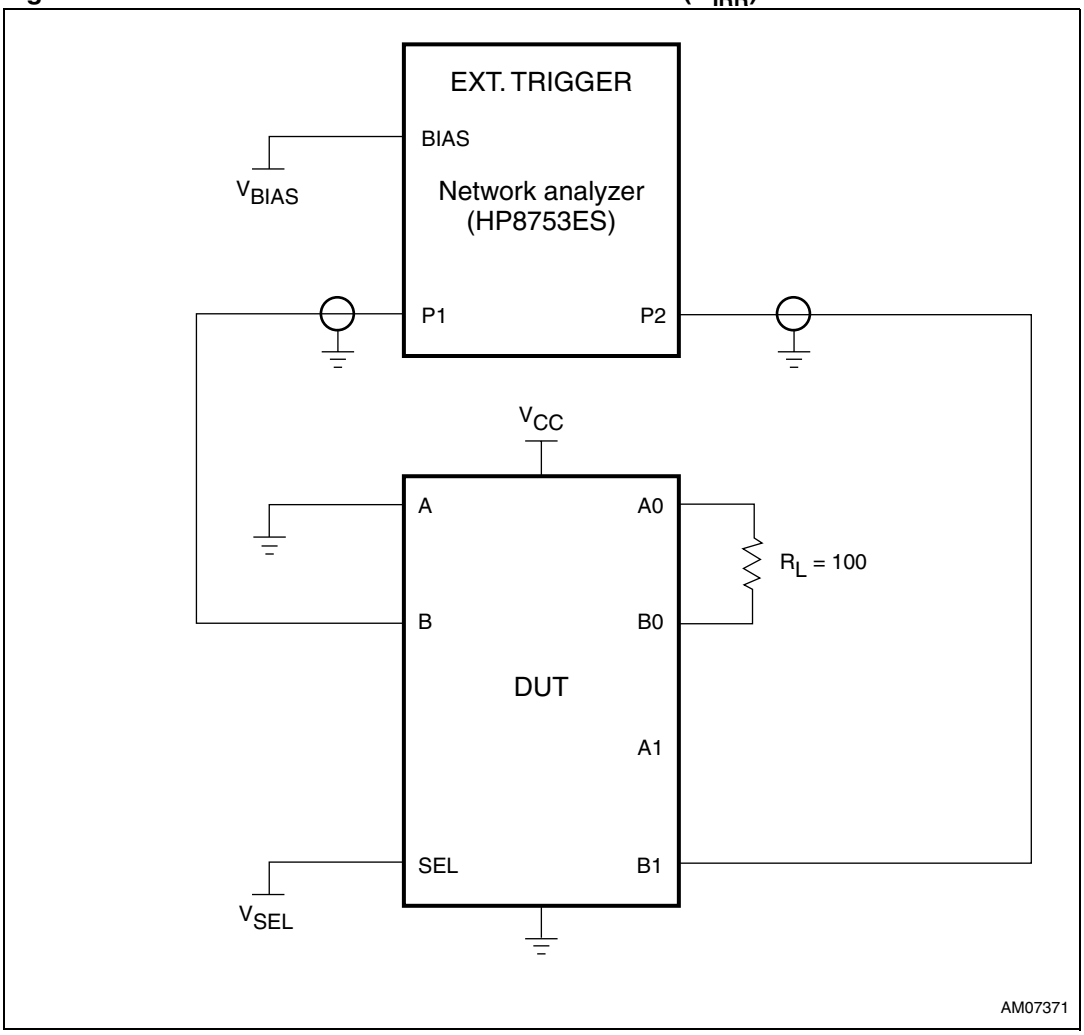
R_{BW} = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBm

Figure 10. Test circuit for off isolation measurement (O_{IRR})



1. C_L includes probe and jig capacitance.
2. A 50 Ω termination resistor is needed to match the loading of the network analyzer.

Off isolation is measured at the output of the OFF channel. For example, when V_{SEL}= 0, and B is the input, the output is measured at B1. All unused analog input ports are connected to GND and output ports are left open.

HP8753ES setup:

Average = 4

R_{BW} = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBm

4 Package mechanical data

ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 11. Package outline for QFN42 (3.5 x 9 x 0.75) - pitch 0.5 mm

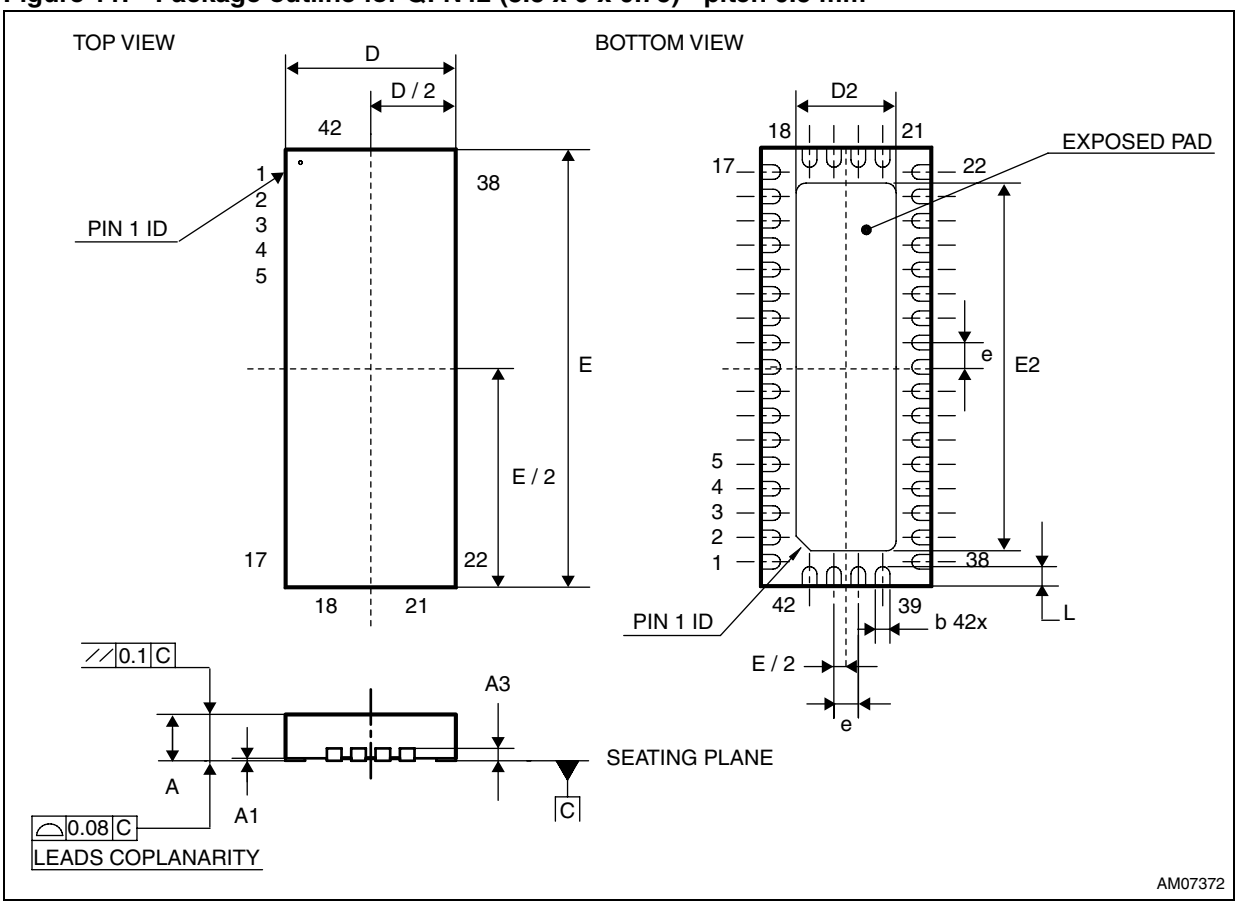


Table 14. Mechanical data for QFN42 (3.5 x 9 x 0.75) - pitch 0.5 mm

Symbol	millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	—	0.20	—
b	0.20	0.25	0.30
D	3.40	3.50	3.60
D2	2	2.05	2.10
E	8.90	9	9.10
E2	7.50	7.55	7.60
e	—	0.50	—
L	0.30	0.40	0.50

Figure 12. Footprint recommendation for QFN42 (3.5 x 9 x 0.75) - pitch 0.5 mm

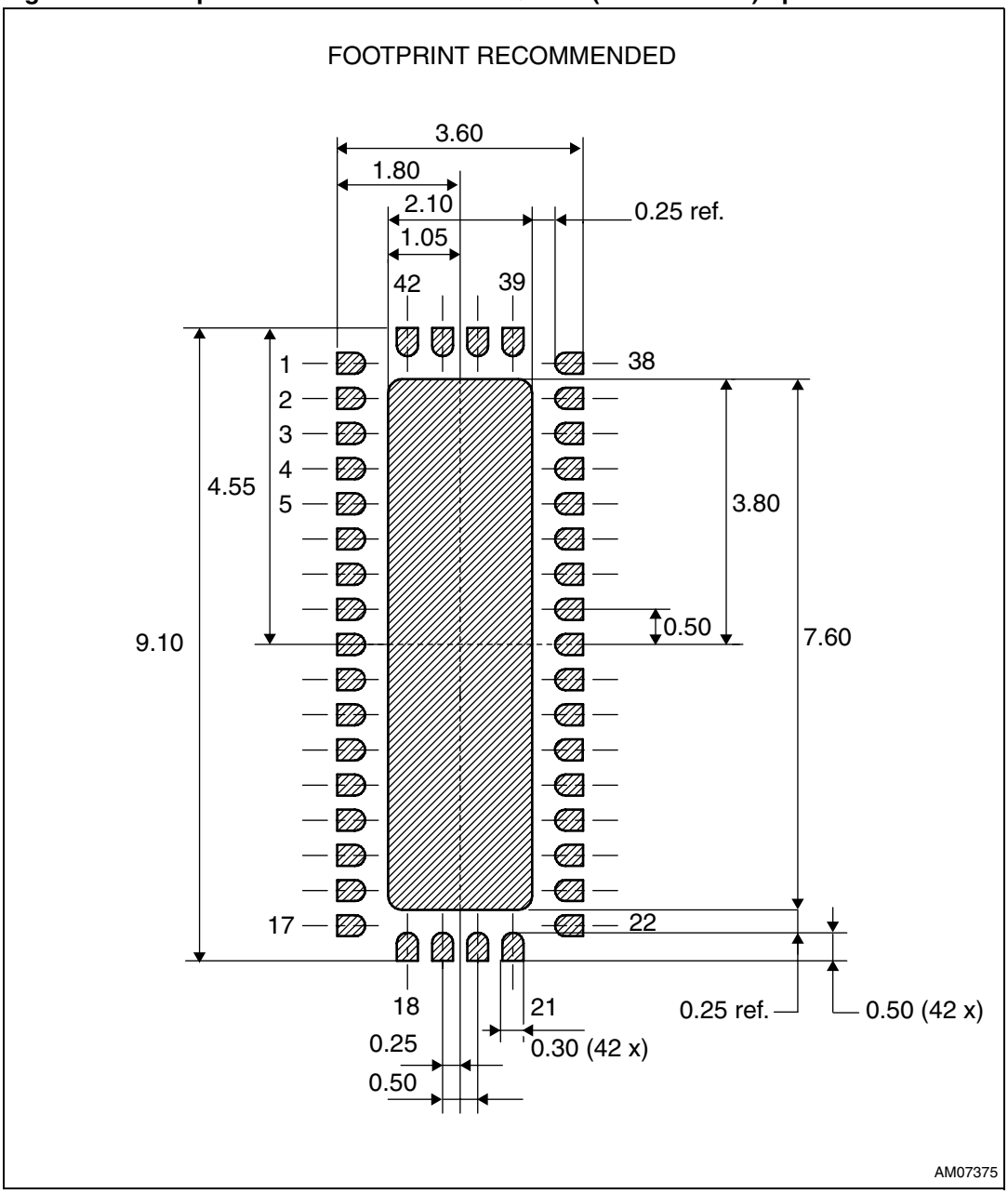
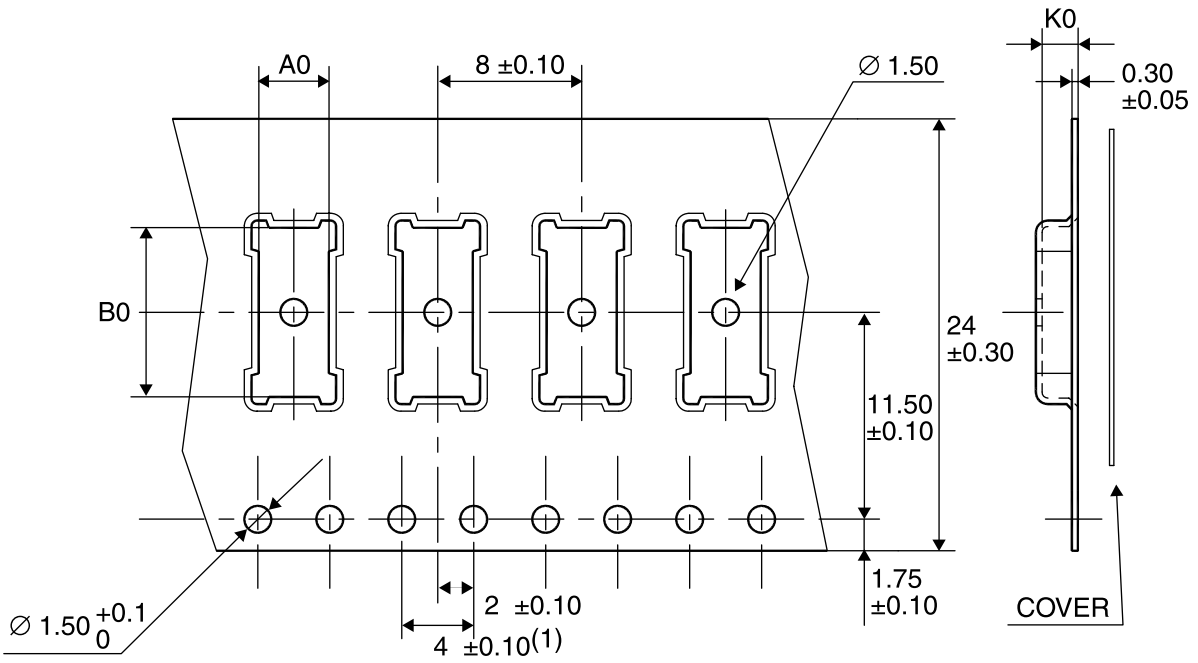


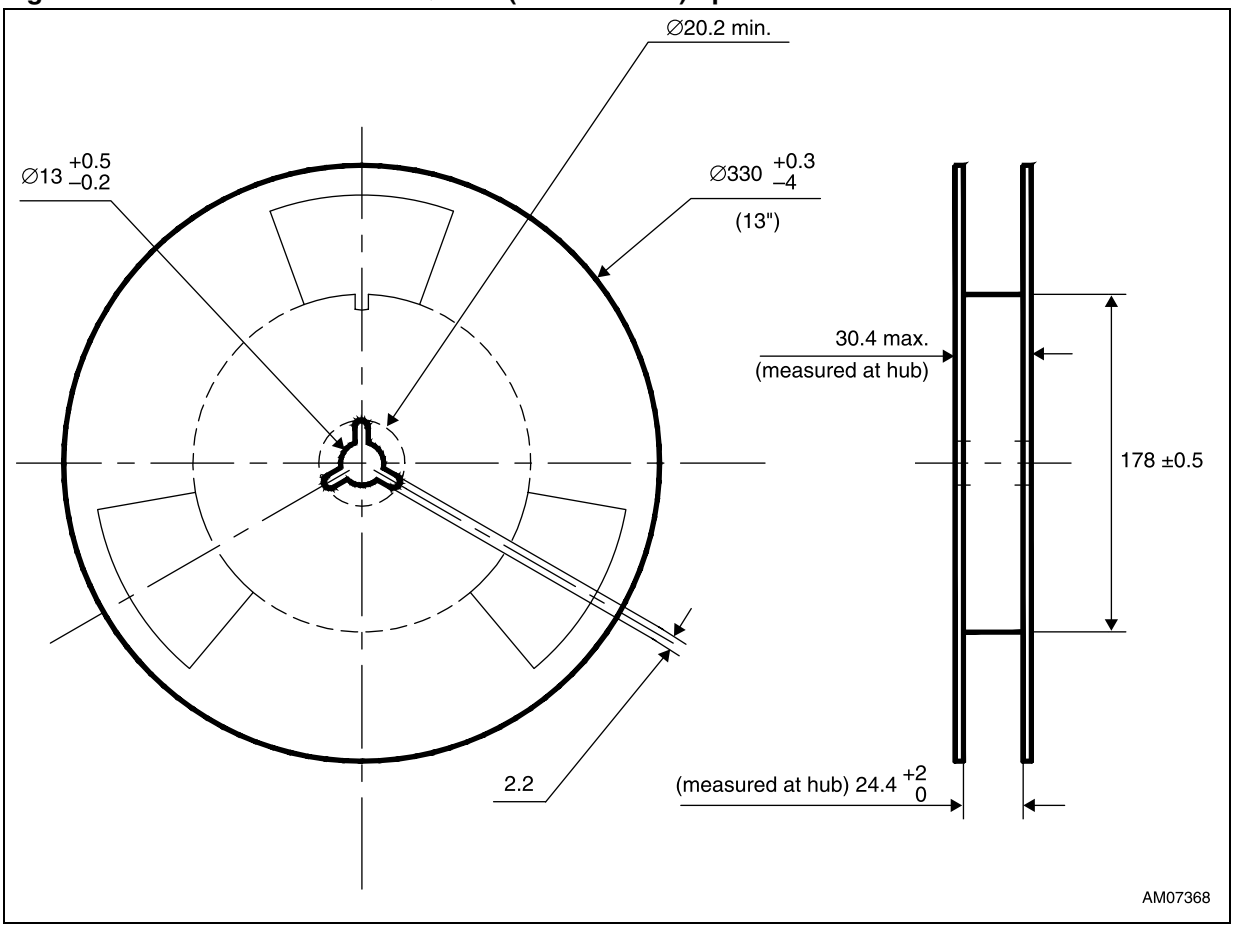
Figure 13. Carrier tape information for QFN42 (3.5 x 9 x 0.75) - pitch 0.5 mm



A0	3.90 ±0.10
B0	9.40 ±0.10
K0	1 ±0.10

1. 10 sprocket hole pitch cumulative tolerance ±0.20.

Figure 14. Reel information for QFN42 (3.5 x 9 x 0.75) - pitch 0.5 mm



5 Revision history

Table 15. Document revision history

Date	Revision	Changes
09-Dec-2009	1	Initial release.
11-Oct-2010	2	Document reformatted, updated *Features* and “max. low power mode” in *Table 10.*, replaced V_{DD} by V_{CC}, corrected typo in *Figure 1*, *Figure 3* to *Figure 7*.
09-Nov-2011	3	Corrected order code in *Table 1*, updated *Section 2* and Disclaimer, minor text corrections throughout document.

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