

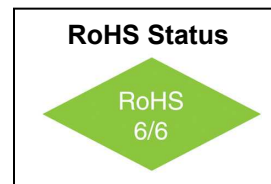
VF230V

VCXO Low Jitter 3.3V

5x7mm SMD, LVPECL / LVDS

Features

- Tristate
- 750KHz to 800MHz frequency range
- <5.0 ps RMS Jitter over 12kHz to 20MHz
- APR to ± 150 ppm



Applications

- Optical Networking, SONET / SDH
- 10 Gigabit Ethernet
- Broadband Access

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Frequency Range	F		0.75		800	MHz	
Frequency Stability	$\Delta F/F$	Vs. Operating Temperature			± 50 ± 25	ppm	
		Vs. Supply Voltage		± 1.5	± 3	ppm/V	First Year After first year
		Vs. Aging / Year		± 3 ± 1		ppm ppm/y	
Operating Temperature	T		0° -40°		+70° +85°	°C	Order Code A Order Code B
Supply Voltage	V _{CC}		3.15	3.3	3.45	V	
Voltage Control	V _C		0.3 0		3 3.3	V	Order codes A,B Order codes C,D
APR				100	150	ppm	
Input Impedance				50		kOhm	
Period Jitter RMS		19.44MHz 77.76MHz 155.52MHz 622.08MHz		5 8 9 10		ps	
Integrated Jitter RMS 12kHz to 20MHz		155.52MHz		3	5	ps	

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Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Symmetry		$(V_{DD}-1.3) V_{DC}$ $1.25V_{DC}$	40 40	50 50	60 60	%	PECL LVDS
Phase Noise		10Hz		-60		dBc/Hz	@19.44MHz
		100Hz		-90			
		1kHz		-112			
		10kHz		-140			
		100kHz		-140			
		10Hz		-60		dBc/Hz	@106.25MHz
		100Hz		-90			
		1kHz		-112			
		10kHz		-127			
		100kHz		-125			
		10Hz		-60		dBc/Hz	@155.52MHz
		100Hz		-90			
		1kHz		-112			
		10kHz		-125			
		100kHz		-123			
		10Hz		-60		dBc/Hz	@622.08MHz
		100Hz		-90			
		1kHz		-109			
		10kHz		-110			
		100kHz		-109			
Supply Current	I_{CC}	0.75 – 24MHz			25	mA	PECL
		24 – 160MHz			65		
		160 – 800MHz			100		
		0.75 – 24MHz			25	mA	LVDS
		24 – 96MHz			45		
		96 – 800MHz			80		
Load	50 Ohms to $V_{DD}-2V$ (PECL) 100 Ohms (LVDS)						
Output High Voltage	V_{OH}			$V_{DD}-1.025$ 1.4	1.6	V	PECL LVDS
Output Low Voltage	V_{OL}		0.9	1.1	$V_{DD}-1.620$	V	PECL LVDS
Output Differential Voltage	V_{OD}		247	355	454	mV	LVDS
Offset Voltage	V_{OS}		1.125	1.2	1.375	V	LVDS
Rise / Fall Time	T_r/T_f	20% to 80%		0.6 0.7	1.5 1.0	ns	PECL LVDS
Tristate	"1": Output Enable – Pin 2 may float or 2.8V min (3.3V V_{DD}) "0": Tristate – Pin 2 requires 0.4V max (3.3V V_{DD})						

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Lead Temperature		Soldering, 10s max			260	°C	
Storage Temperature	T _s		-55		+125°	°C	
Junction Temperature	T _J				+125°	°C	
Supply Voltage	V _c		-1		4.6	V	
ESD Protection		Human Body Model			2	kV	

Environmental and Mechanical Conditions

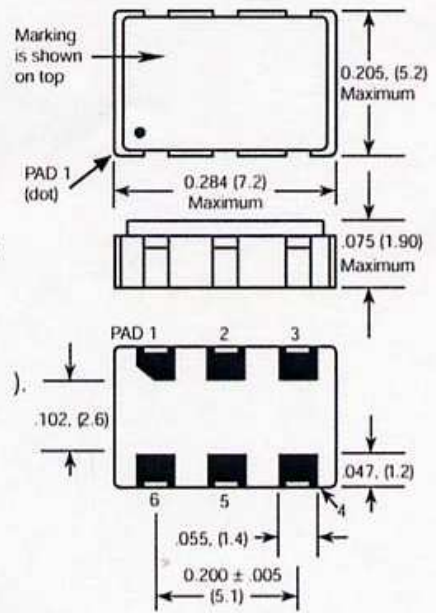
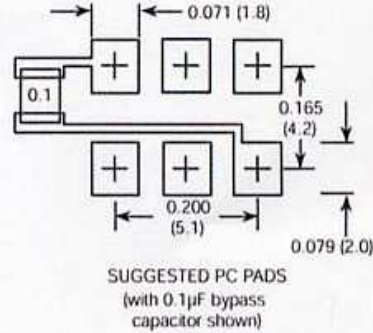
Parameter	Specification
Shock	1000 Gs, 0.35ms, ½ sine wave, 3 shocks in each plane
Humidity	Resistant to 85 °R.H. at 85 °C
Vibration	10-2000 Hz of 0.06" d.a. or 20 Gs, whichever is less
Leak	MIL STD 883, Method 1014, Condition A1 and C1
Case	Ceramic with hermetic resistance-welded metal lid
Pads	Solderable gold over nickel
Marking	Epoxy ink or laser engraved
Resistance to Solvents	MIL STD 202, Method 215

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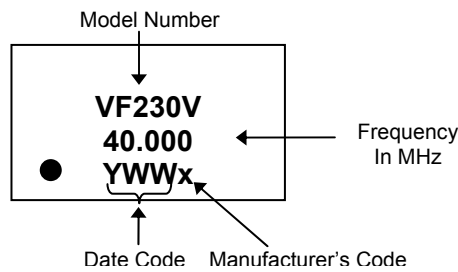
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Pin #	Connection
1	V _C
2	Tristate
3	Case, GND
4	Output
5	Output
6	Supply Voltage



Marking Specification



How to Order



Stability		
Code	Specification	
A	± 50 ppm	} 0.3-1.65-3V
B	± 25 ppm	
C	± 50 ppm	} 0-1.65-3.3V
D	± 25 ppm	

Temperature Range	
Code	Specification
A	0°C to +70°C
B	-40°C to +85°C

Tristate	
Code	Specification
T	Tristate
N	Non-Tristate

Output Logic	
Code	Specification
A	45/55% LVDS
B	40/60% LVDS
C	45/55% PECL
D	40/60% PECL

APR	
Code	Specification
A	100 ppm
B	150 ppm