TFF1024HN

Integrated mixer oscillator PLL for satellite LNB

Rev. 1 — 13 January 2015 | Product data sheet

1. General description

The TFF1024HN is an integrated downconverter for use in Low Noise Block (LNB) convertors in a 10.70 GHz to 12.85 GHz K_u band satellite receiver system.

2. Features and benefits

- Low current consumption integrated pre-amplifier, mixer, buffer amplifier and PLL synthesizer
- Flat gain over frequency
- Single 5 V supply pin
- Low cost 25 MHz crystal
- Crystal controlled LO frequency generation
- Switched LO frequency (selectable to 9.75 GHz, 10.00 GHz, 10.25 GHz, 10.55 GHz, 10.60 GHz, 10.75 GHz, 11.25 GHz or 11.30 GHz) with a 25 MHz crystal as reference
- Other LO frequencies within the 9.75 GHz to 11.30 GHz range can be realized by using an alternative reference frequency
- Low phase noise
- Low spurious
- Low external component count
- Alignment-free concept
- ESD protection on all pins

3. Applications

- K_u band LNB converters for VSAT and digital satellite reception (DVB-S / DVB-S2)

4. Quick reference data

Table 1. Quick reference data

9.75 GHz $\leq f_{LO} \leq$ 11.30 GHz; operating conditions of Table 6 apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	RF input and IF output AC coupled [1]	4.5	5	5.5	V
I_{CC}	supply current	RF input and IF output AC coupled [1]	-	56	70	mA
NF_{SSB}	single sideband noise figure	f_{IF} = 1450 MHz; T_{amb} = 25 °C; 10.55 GHz $\leq f_{LO} \leq$ 10.60 GHz	-	9.0	11.0	dB
f_{RF}	RF frequency	[2]	10.70	-	12.85	GHz

Table 1. Quick reference data *...continued*

9.75 GHz ≤ f_{LO} ≤ 11.30 GHz; operating conditions of Table 6 apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_{conv}	conversion gain	f_{IF} = 1450 MHz				
		f_{LO} = 10.55 GHz	29.8	34.3	38.8	dB
		f_{LO} = 10.60 GHz	29.8	34.3	38.8	dB
s_{11}	input reflection coefficient	10.70 GHz ≤ f_{RF} ≤ 12.85 GHz	-	–10	-	dB
s_{22}	output reflection coefficient	950 MHz ≤ f_{IF} ≤ 2150 MHz; Z_0 = 75 Ω	-	–10	-	dB
$IP3_o$	output third-order intercept point	carrier power = –10 dBm (measured at output)				
		f_{IF} = 1450 MHz; 9.75 GHz ≤ f_{LO} ≤ 10.75 GHz	14	18	-	dBm
		f_{IF} = 1250 MHz; 11.25 GHz ≤ f_{LO} ≤ 11.30 GHz	14	18	-	dBm

[1] DC values.

[2] See Table 4 for specific values at certain settings of pins HB0, HB1 and HB2.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFF1024HN	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

6. Functional diagram

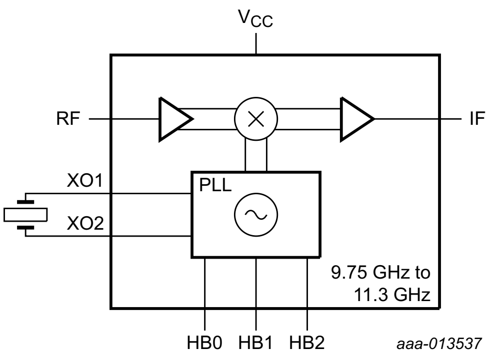


Fig 1. Functional diagram

7. Pinning information

7.1 Pinning

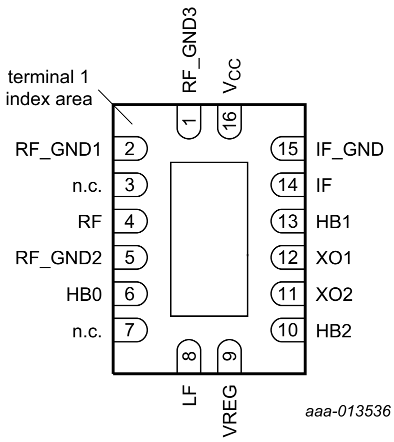


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	0	ground (exposed die pad)
RF_GND3	1	RF ground. Connect this pin to the exposed die pad landing.
RF_GND1	2	RF ground. Connect this pin to the exposed die pad landing and the RF input CPW line.
n.c.	3	not connected. Connect to RF on PCB. [1]
RF	4	RF input.
RF_GND2	5	RF ground. Connect this pin to the exposed die pad landing and the RF input CPW line.
HB0	6	LO frequency selection, LSB. Connect this pin to GND for "0", leave open for "1". Also see Table 4.
n.c.	7	not connected. Use this pin to route the ground layer on top of the PCB to the exposed die pad.
LF	8	Loop filter PLL. Connect loop filter between this pin and VREG (pin 9).
VREG	9	Regulated output voltage for PLL loop filter. Connect loop filter to this pin. Decouple against die pad via pin 7.
HB2	10	LO frequency selection, MSB. Connect this pin to GND for "0", leave open for "1". Also see Table 4.
XO2	11	Crystal connection 2. Connect crystal between this pin and XO1 (pin 12).
XO1	12	Crystal connection 1. Connect crystal between this pin and XO2 (pin 11).
HB1	13	LO frequency selection. Connect this pin to GND for "0", leave open for "1". Also see Table 4.
IF	14	IF output
IF_GND	15	IF output ground. Connect this pin to the exposed die pad landing and the output transmission line ground.
V_{CC}	16	Supply voltage

[1] The distance between the outer edges of pin 2 and pin 3 is 740 μm. This gives an optimum transition from a 1.1 mm wide, Z_0 = 50 Ω line to the TFF1024HN on a Rogers RO4223 Printed-Circuit Board (PCB) material of 0.5 mm height.

8. Functional description

8.1 LO frequency selection

Table 4. LO frequency selection table

See Figure 1 for the functional diagram.

f_{LO}	f_{xtal}	HB2	HB1	HB0	f_{RF} (GHz)		f_{IF} (MHz)	
(GHz)	(MHz)	(pin 10)	(pin 13)	(pin 6)	Min	Max	Min	Max
9.75	25	0	0	0	10.70	11.90	950	2150
10.00	25	0	0	1	10.95	12.15	950	2150
10.25	25	0	1	0	11.20	12.40	950	2150
10.45 [1]	24.76	0	1	1	11.40	12.60	950	2150
10.55	25	0	1	1	11.50	12.70	950	2150
10.60	25	1	0	0	11.55	12.75	950	2150
10.75	25	1	0	1	11.70	12.85	950	2100
11.25	25	1	1	0	12.20	12.85	950	1600
11.30	25	1	1	1	12.25	12.85	950	1550

[1] For frequencies that cannot be achieved using the 25 MHz crystal choose the closest frequency and adapt the crystal frequency. Example: 10.45 GHz. This can be achieved by choosing 10.55 GHz. The divider ratio is 422. 10.45 GHz will be achieved with a crystal frequency of 10.45 GHz / 422 = 24.76303 MHz.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+6	V
V_i	input voltage	on pin HB0	–0.5	+6	V
		on pin HB1	–0.5	+6	V
		on pin HB2	–0.5	+6	V
T_{stg}	storage temperature		–40	+125	°C

10. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	RF input and IF output AC coupled [1]	4.5	5	5.5	V
V_i	input voltage	on pin HB0	0	-	2.7	V
		on pin HB1	0	-	2.7	V
		on pin HB2	0	-	2.7	V
$I_{CC(startup)}$	start-up supply current	during 30 ms only at supply power-on	300	-	-	mA
T_{amb}	ambient temperature		–40	+25	+85	°C
Z_0	characteristic impedance		-	50	-	Ω
f_{RF}	RF frequency	[2]	10.70	-	12.85	GHz

Table 6. Operating conditions *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{LO}	LO frequency	HB2 = 0; HB1 = 0; HB0 = 0	[3]	-	9.75	-	GHz
		HB2 = 1; HB1 = 1; HB0 = 1	[4]	-	11.30	-	GHz
f_{IF}	IF frequency		[2]	950	-	2150	MHz
$C_{L(xtal)}$	crystal load capacitance			-	10	-	pF
ESR	equivalent series resistance			-	-	40	Ω
f_{xtal}	crystal frequency			-	25	-	MHz

[1] DC values.

[2] See Table 4 for specific values at certain settings of pins HB0, HB1 and HB2.

[3] The minimum LO frequency is specified. See Table 4 for other specific values at certain settings of pins HB0, HB1 and HB2.

[4] The maximum LO frequency is specified. See Table 4 for other specific values at certain settings of pins HB0, HB1 and HB2.

11. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		35	K/W

12. Characteristics

Table 8. Characteristics

9.75 GHz ≤ f_{LO} ≤ 11.30 GHz; operating conditions of Table 6 apply.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	supply current	RF input and IF output AC coupled	[1]	-	56	70	mA
$\varphi_{n\lambda(itg)RMS}$	RMS integrated phase noise density	loop bandwidth = crossover bandwidth; low ESR crystal used (ESR < 20 Ω)					
		integration offset frequency = 1 kHz to 1 MHz		-	1.2	2.2	deg
		integration offset frequency = 10 kHz to 13 MHz		-	1.2	2.2	deg
NF_{SSB}	single sideband noise figure	f_{IF} = 1450 MHz; T_{amb} = 25 °C					
		f_{LO} = 9.75 GHz		-	8.8	10.8	dB
		10.55 GHz ≤ f_{LO} ≤ 10.60 GHz		-	9.0	11.0	dB
		f_{IF} = 1250 MHz; T_{amb} = 25 °C					
		11.25 GHz ≤ f_{LO} ≤ 11.30 GHz		-	9.5	11.5	dB
G_{conv}	conversion gain	f_{IF} = 1450 MHz					
		f_{LO} = 9.75 GHz		29.6	34.1	38.6	dB
		f_{LO} = 10.00 GHz		29.5	34.0	38.5	dB
		f_{LO} = 10.25 GHz		29.5	34.0	38.5	dB
		f_{LO} = 10.55 GHz		29.8	34.3	38.8	dB
		f_{LO} = 10.60 GHz		29.8	34.3	38.8	dB
		f_{LO} = 10.75 GHz		30.2	34.7	39.2	dB
		f_{IF} = 1250 MHz					
		f_{LO} = 11.25 GHz		30.2	34.7	39.2	dB
		f_{LO} = 11.30 GHz		30.1	34.6	39.1	dB

Table 8. Characteristics *...continued*

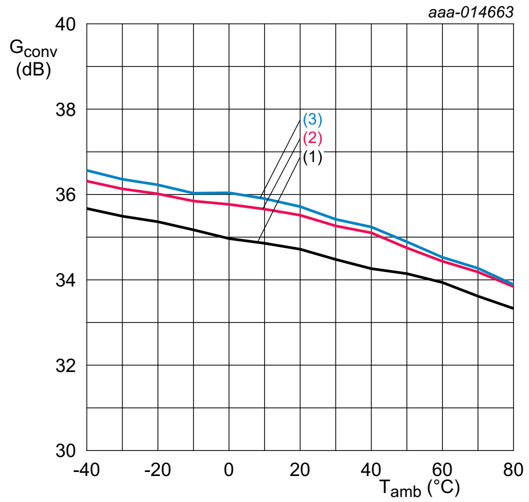
9.75 GHz ≤ f_{LO} ≤ 11.30 GHz; operating conditions of Table 6 apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta G_{conv}/\Delta f$	conversion gain variation with frequency	over IF band; –40 °C ≤ T_{amb} ≤ +85 °C; V_{CC} = 5.0 V				
		f_{LO} = 9.75 GHz [2]	-	-	2.5	dB
		f_{LO} = 10.00 GHz [2]	-	-	3.0	dB
		f_{LO} = 10.25 GHz [2]	-	-	3.6	dB
		f_{LO} = 10.55 GHz [2]	-	-	4.0	dB
		f_{LO} = 10.60 GHz [2]	-	-	4.0	dB
		f_{LO} = 10.75 GHz [2]	-	-	4.0	dB
		f_{LO} = 11.25 GHz [2]	-	-	3.0	dB
		f_{LO} = 11.30 GHz [2]	-	-	3.0	dB
		in every 36 MHz band; –40 °C ≤ T_{amb} ≤ +85 °C; V_{CC} = 5.0 V	-	-	0.6	dB
s_{11}	input reflection coefficient	10.70 GHz ≤ f_{RF} ≤ 12.85 GHz	-	–10	-	dB
s_{22}	output reflection coefficient	950 MHz ≤ f_{IF} ≤ 2150 MHz; Z_0 = 75 Ω	-	–10	-	dB
$IP3_o$	output third-order intercept point	carrier power is –10 dBm (measured at the output)				
		f_{IF} = 1450 MHz; 9.75 GHz ≤ f_{LO} ≤ 10.75 GHz	14	18	-	dBm
		f_{IF} = 1250 MHz; 11.25 GHz ≤ f_{LO} ≤ 11.30 GHz	14	18	-	dBm
$P_{L(1dB)}$	output power at 1 dB gain compression	measured at the output				
		f_{IF} = 1450 MHz; 9.75 GHz ≤ f_{LO} ≤ 10.75 GHz	2	6	-	dBm
		f_{IF} = 1250 MHz; 11.25 GHz ≤ f_{LO} ≤ 11.30 GHz	2	6	-	dBm
$\alpha_{L(RF)lo}$	local oscillator RF leakage	f_c = f_{LO}; span = 100 MHz; RBW = 50 kHz; VBW = 200 kHz	-	-	–35	dBm
V_{IL}	LOW-level input voltage	on pin HB0	-	-	0.8	V
		on pin HB1	-	-	0.8	V
		on pin HB2	-	-	0.8	V
V_{IH}	HIGH-level input voltage	on pin HB0	1.6	-	2.7	V
		on pin HB1	1.6	-	2.7	V
		on pin HB2	1.6	-	2.7	V
R_{pu}	pull-up resistance	on pin HB0	80	110	140	kΩ
		on pin HB1	80	110	140	kΩ
		on pin HB2	80	110	140	kΩ

[1] DC values.

[2] See Table 4 for the corresponding f_{IF} ranges.

12.1 Graphs



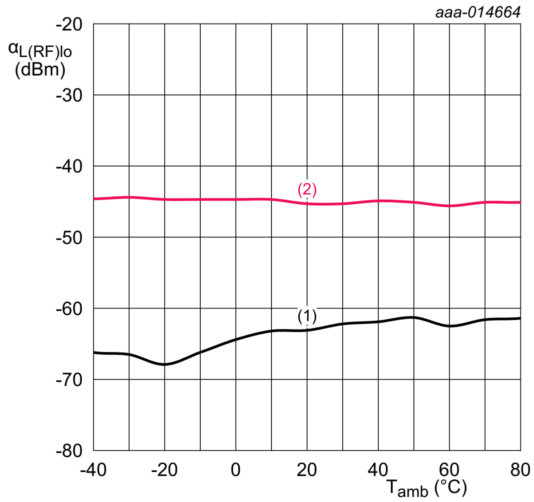
V_{CC} = 5 V; f_{IF} = 1550 MHz.

(1) f_{LO} = 9.75 GHz

(2) f_{LO} = 10.60 GHz

(3) f_{LO} = 11.30 GHz

Fig 3. Conversion gain as a function of ambient temperature; typical values

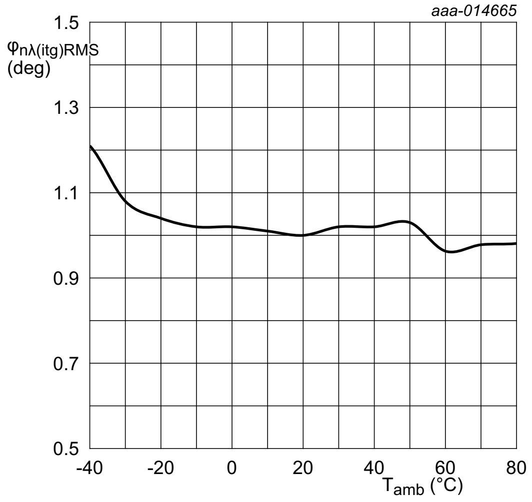


V_{CC} = 5 V.

(1) f_{LO} = 9.75 GHz

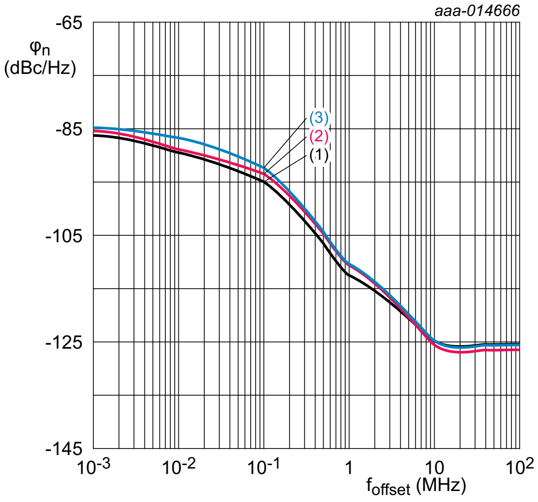
(2) f_{LO} = 11.30 GHz

Fig 4. Local oscillator RF leakage as a function of ambient temperature; typical values



V_{CC} = 5 V; f_{LO} = 10.55 GHz.

Fig 5. RMS integrated phase noise density as a function of ambient temperature; typical values



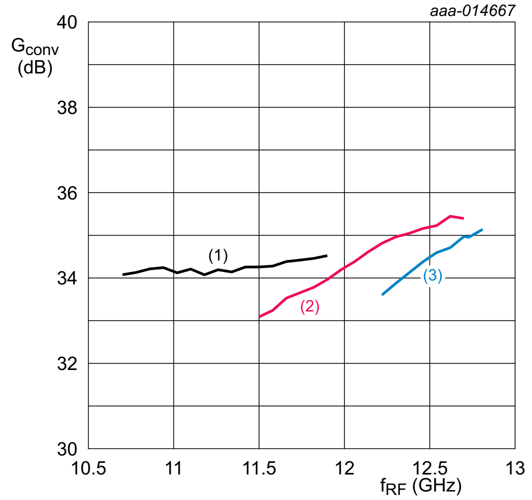
V_{CC} = 5 V; T_{amb} = 25 °C.

(1) f_{LO} = 9.75 GHz

(2) f_{LO} = 10.60 GHz

(3) f_{LO} = 11.30 GHz

Fig 6. Phase noise as a function of offset frequency; typical values



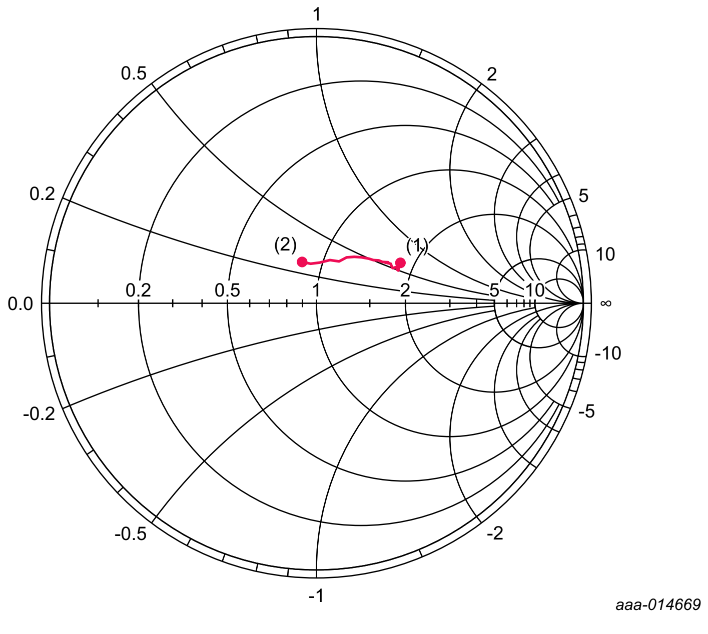
V_{CC} = 5 V.

(1) f_{LO} = 9.75 GHz

(2) f_{LO} = 10.60 GHz

(3) f_{LO} = 11.30 GHz

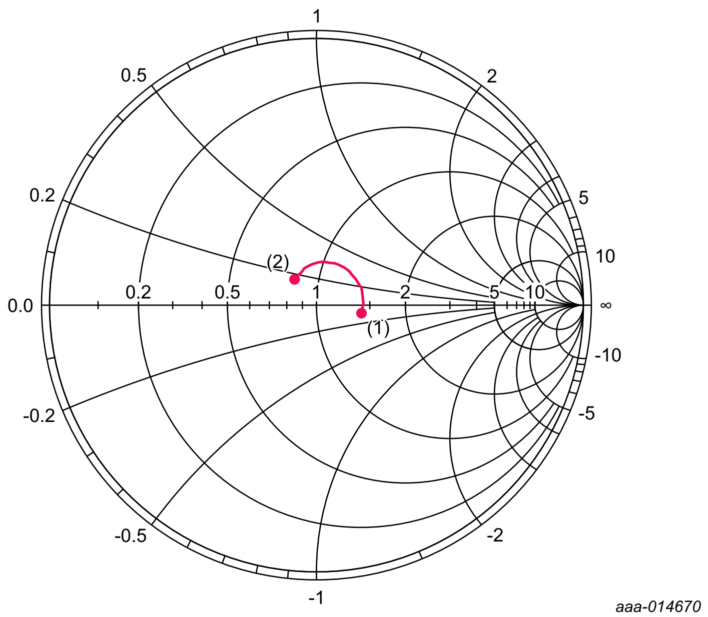
Fig 7. Conversion gain as a function of RF frequency; typical values



(1) f_{RF} = 10.70 GHz

(2) f_{RF} = 12.75 GHz

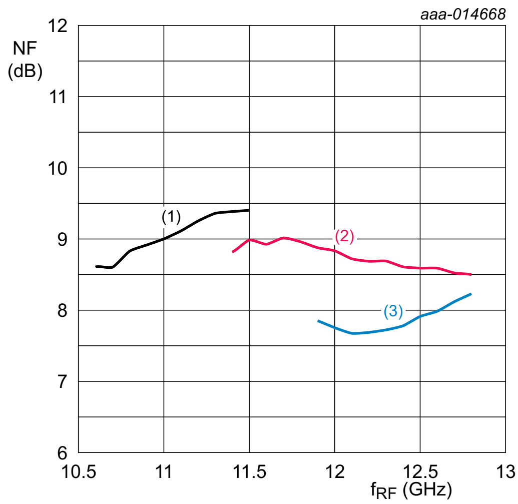
Fig 8. Input reflection coefficient (S_{11}); typical values



(1) f_{IF} = 250 MHz

(2) f_{IF} = 2150 MHz

Fig 9. Output reflection coefficient (S_{22}); typical values



V_{CC} = 5 V.

(1) f_{LO} = 9.75 GHz

(2) f_{LO} = 10.60 GHz

(3) f_{LO} = 11.30 GHz

Fig 10. Noise figure as function of RF frequency; typical values

13. Application information

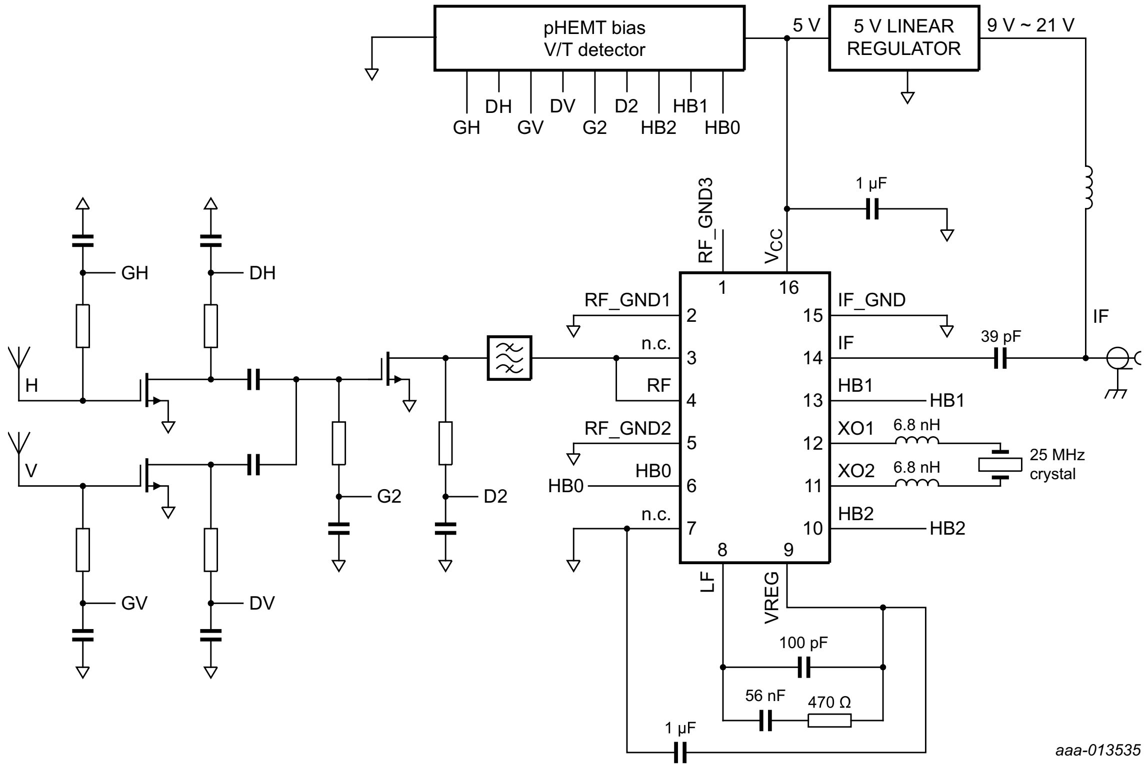


Fig 11. Application diagram of TFF1024HN

Table 9. List of netnames

See Figure 11.

Netname	Description
GH	Gate voltage of 1st stage LNA. Horizontal polarization
DH	Drain voltage of 1st stage LNA. Horizontal polarization
GV	Gate voltage of 1st stage LNA. Vertical polarization
DV	Drain voltage of 1st stage LNA. Vertical polarization
G2	Gate voltage of 2nd stage LNA
D2	Drain voltage of 2nd stage LNA
HB0	LO frequency selection, LSB
HB1	LO frequency selection
HB2	LO frequency selection, MSB

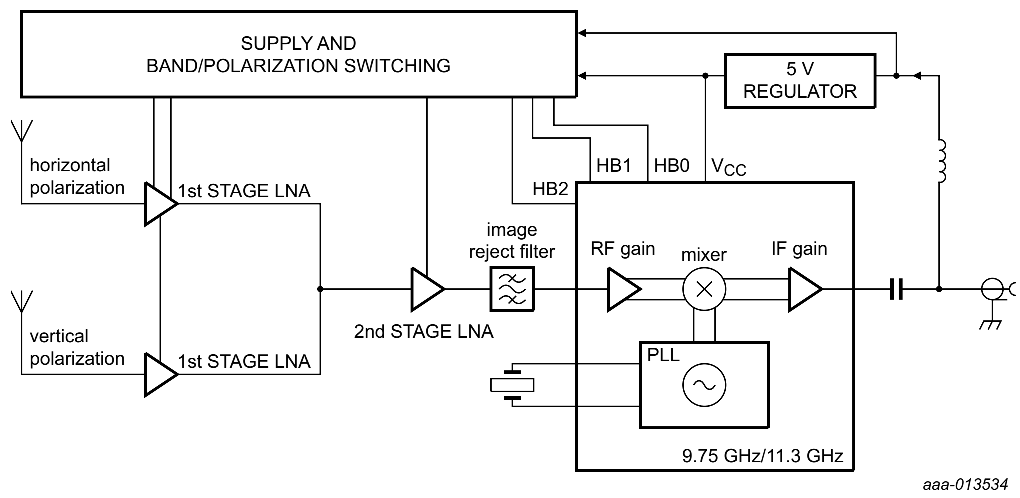
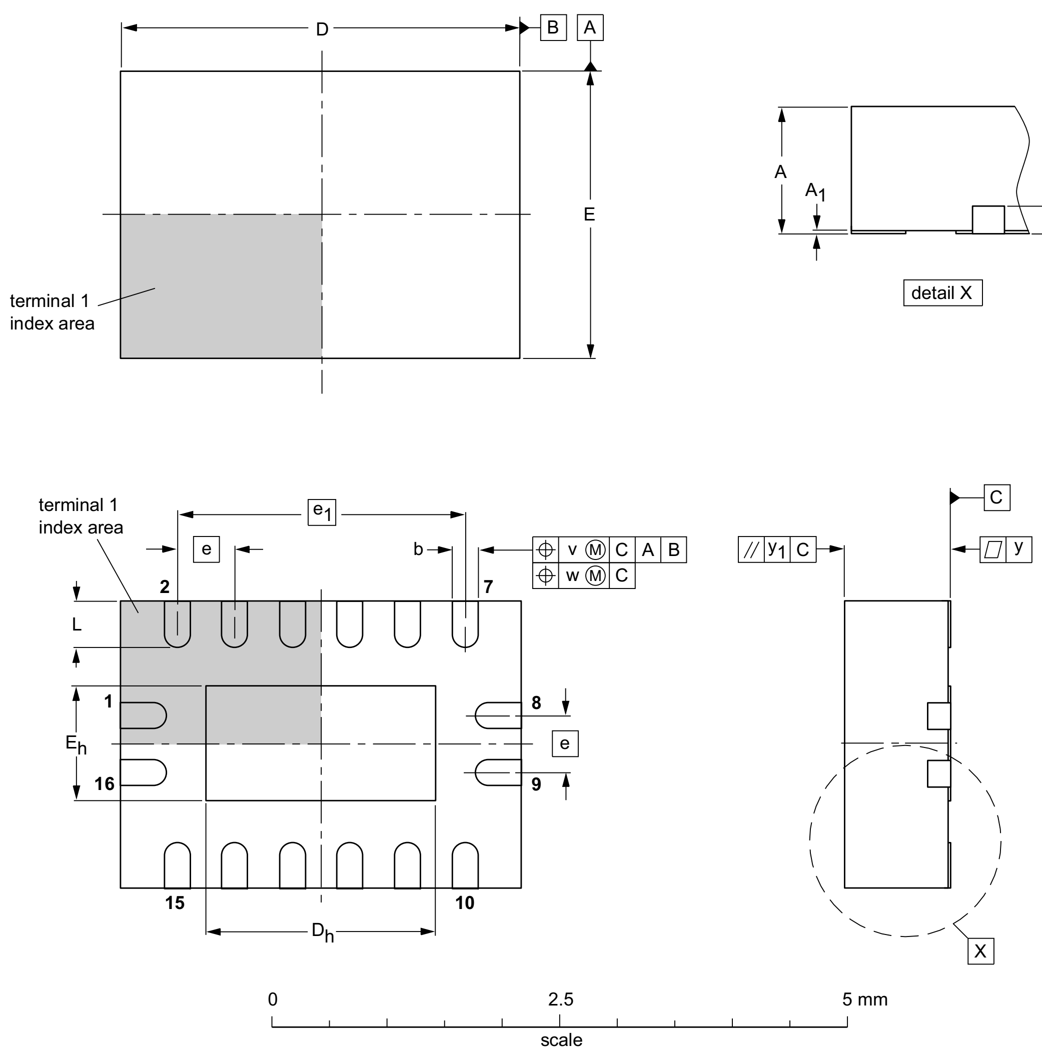


Fig 12. LNB system block diagram with TFF1024HN

14. Package outline

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT763-1

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CPW	CoPlanar Waveguide
DVB-S	Digital Video Broadcasting by Satellite
DVB-S2	Digital Video Broadcasting - Satellite - Second generation
ESD	ElectroStatic Discharge
IF	Intermediate Frequency
K_u band	K-under band
LNA	Low-Noise Amplifier
LNB	Low-Noise Block
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
pHEMT	Pseudomorphic High Electron Mobility Transistor
PLL	Phase-Locked Loop
RBW	Resolution BandWidth
VSAT	Very Small Aperture Terminal
V/T	Voltage / Tone
VBW	Video BandWidth

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFF1024HN v.1	20150113	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

19. Contents

Date of release: 13 January 2015

Document identifier: TFF1024HN