

# DATA SHEET



## **SAA7715AH** Digital Signal Processor

Preliminary specification

2003 Mar 13

**Digital Signal Processor****SAA7715AH**

|                 |                                                       |                                                                                     |
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### 1 FEATURES

#### 1.1 Hardware

- 24-bit Philips 70 MIPS DSP core (24-bit data path and 12/24-bit coefficient path)
- 1.5 kbyte of downloadable DSP program memory (PRAM)
- 2 kbyte of DSP program memory (PROM)
- 2.875 kbyte of re-programmable DSP data memory (XRAM)
- 1.5 kbyte of re-programmable DSP coefficient memory (YRAM)
- Four stereo digital serial inputs (8 channels) with common BCK and WS. To these inputs the I<sup>2</sup>S-bus format or LSB-justified formats can be applied
- One stereo bitstream DAC (2 channels) with 64 fold oversampling and noise shaping
- Selectable clock output (pin SYSCLOCK) for external slave devices (128f<sub>s</sub> to 512f<sub>s</sub>)
- Four stereo digital serial outputs (8 channels) with selectable I<sup>2</sup>S-bus or LSB-justified format
- Two SPDIF inputs combined with digital serial input
- On-board WS\_PLL generates clock for on-board DAC and output pin SYSCLOCK
- I<sup>2</sup>C-bus controlled (including fast mode)
- Programmable Phase-Locked Loop (PLL) derives the clock for the DSP from the CLK\_IN input
- -40 to +85 °C operating temperature range
- Supply voltage only 3.3 V
- All digital inputs are tolerant for 5 V input levels
- Power-down mode for low current consumption in standby mode
- Optimized pinning for applications with other Philips DACs (such as UDA1334, UDA1355 and UDA1328).

#### 1.2 Possible firmware

- Dolby®<sup>(1)</sup> Pro Logic decoding
- Smoothed volume control (without zipper noise)
- Automatic Volume Levelling (AVL)
- Dynamic bass enhancement
- Ultra bass

(1) **Dolby** — Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.



- Incredible surround
- Incredible mono (Imono)
- DPL virtualizer
- Dolby digital virtualizer (DVD post-processing)
- Dynamic compressor
- Spectral enhancer
- Equalizer with peaking/shelving filters
- DC filters
- Bass/treble control
- Dynamic loudness
- Tone/noise generator
- Graphical spectrum analyser
- Configurable Delay Unit (DLU)
- Sound steering/elevation for car applications
- Sample Rate Conversion (SRC).

### 2 APPLICATIONS

- As co-processor for a car radio DSP in a car radio application for additional acoustic enhancements (sound steering/sound elevation/signal processing)
- Multichannel audio: in DVD and Home theatre applications as post-processing device such as signal virtualization (virtual 3D surround) and acoustic enhancement, tone control, volume control and equalizers
- Multichannel decoding: Dolby Pro Logic and virtual 3D surround
- PC/USB audio applications: stereo widening (Incredible surround), sound steering, sound positioning and speaker equalization.

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**3 GENERAL DESCRIPTION**

The SAA7715AH is a cost effective and powerful high performance 24-bit programmable DSP for a variety of digital audio applications. This DSP device integrates a 24-bit DSP core with programmable memories (program RAM/ROM, data and coefficient RAM), 4 digital serial inputs, 4 digital serial outputs, 2 separate SPDIF receivers, a stereo FSDAC, a standard Philips I<sup>2</sup>C-bus interface, a phase-locked loop for the DSP clock generation and a second phase-locked loop for system clock generation (internal and external DAC clocks).

The SAA7715AH can be configured for various audio applications by downloading the dedicated DSP program code into the DSP program RAM or using the ROM or a combination of both. During the Power-down mode the contents of the memories and all other settings will keep their values. The SAA7715AH can be initialized using the I<sup>2</sup>C-bus interface.

Several system application examples, based on this existing SAA7715AH, are available for a wide range of audio applications (e.g car radio DSP, DVD post-processing, Dolby Pro Logic, PC/USB audio and more) which can be used as a reference design for customers.

**4 QUICK REFERENCE DATA**

| SYMBOL                     | PARAMETER                                                   | CONDITIONS                                                    | MIN.   | TYP.    | MAX.   | UNIT  |
|----------------------------|-------------------------------------------------------------|---------------------------------------------------------------|--------|---------|--------|-------|
| V <sub>DD</sub>            | operating supply voltage                                    | all pins V <sub>DD</sub> with respect to pins V <sub>SS</sub> | 3.15   | 3.3     | 3.45   | V     |
| I <sub>DDD</sub>           | supply current of the digital part                          | high activity of the DSP at DSPFREQ frequency                 | –      | 95      | –      | mA    |
| I <sub>DDA</sub>           | supply current of the analog part                           | zero input and output signal                                  | –      | 20      | –      | mA    |
| P <sub>tot</sub>           | total power dissipation                                     | high activity of the DSP at DSPFREQ frequency                 | –      | 380     | –      | mW    |
| I <sub>POWERDOWN</sub>     | DC supply current of the total chip in Power-down mode      | pin POWERDOWN enabled                                         | –      | 400     | –      | μA    |
| f <sub>s</sub>             | sample frequency                                            | at IIS_WS1, SPDIF1 or SPDIF2 input                            | 32     | 44.1    | 96     | kHz   |
| (THD + N)/S <sub>DAC</sub> | total harmonic distortion-plus-noise to signal ratio of DAC | at 0 dB                                                       | –      | –85     | –      | dB(A) |
|                            |                                                             | at –60 dB                                                     | –      | –37     | –      | dB(A) |
| S/N <sub>DAC</sub>         | signal-to-noise ratio of DAC                                | code = 0                                                      | –      | 100     | –      | dB(A) |
| f <sub>CLK_IN</sub>        | clock input frequency                                       | DIV_CLK_IN = LOW                                              | 8.192  | 11.2896 | 12.288 | MHz   |
|                            |                                                             | DIV_CLK_IN = HIGH                                             | 16.384 | –       | 24.576 | MHz   |
| DSPFREQ                    | maximum DSP clock frequency                                 |                                                               | –      | –       | 70     | MHz   |

**5 ORDERING INFORMATION**

| TYPE NUMBER | PACKAGE |                                                                                  |          |
|-------------|---------|----------------------------------------------------------------------------------|----------|
|             | NAME    | DESCRIPTION                                                                      | VERSION  |
| SAA7715AH   | QFP44   | plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm | SOT307-2 |

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## 6 BLOCK DIAGRAM

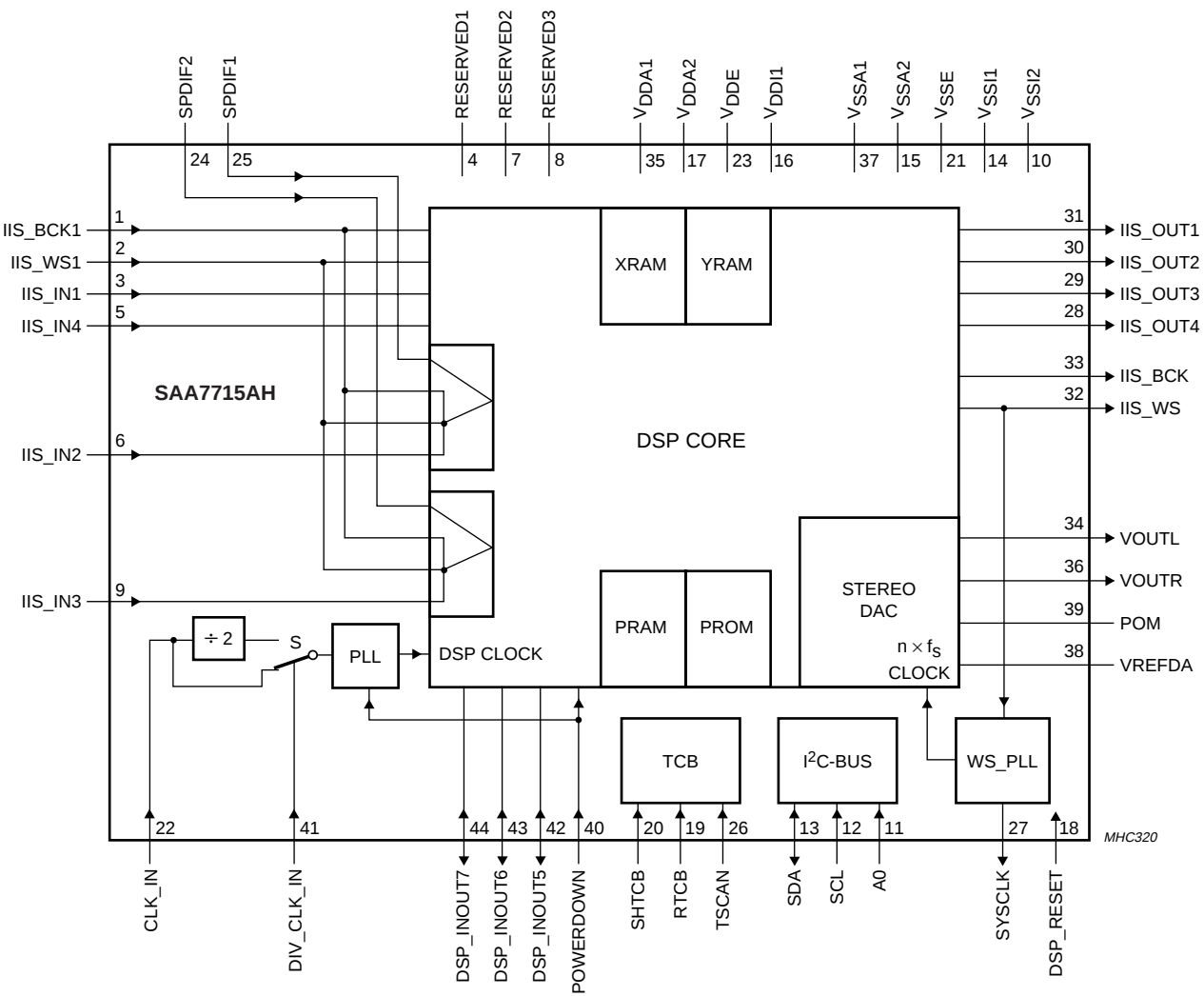


Fig.1 Block diagram.

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## 7 PINNING

| SYMBOL            | PIN | PIN TYPE    | DESCRIPTION                                                                           |
|-------------------|-----|-------------|---------------------------------------------------------------------------------------|
| IIS_BCK1          | 1   | ipthdt5v    | bit clock signal belonging to data of digital serial inputs 1 to 4                    |
| IIS_WS1           | 2   | ipthdt5v    | word select signal belonging to data of digital serial inputs 1 to 4                  |
| IIS_IN1           | 3   | ipthdt5v    | data pin of digital serial input 1                                                    |
| RESERVED1         | 4   | ipthdt5v    | not to be connected externally                                                        |
| IIS_IN4           | 5   | ipthdt5v    | data pin of digital serial input 4                                                    |
| IIS_IN2           | 6   | ipthdt5v    | data pin of digital serial input 2                                                    |
| RESERVED2         | 7   | ipthdt5v    | not to be connected externally                                                        |
| RESERVED3         | 8   | ipthdt5v    | not to be connected externally                                                        |
| IIS_IN3           | 9   | ipthdt5v    | data pin of digital serial input 3                                                    |
| V <sub>SSI2</sub> | 10  | vssi        | ground supply (core only) (bond out to 2 pads)                                        |
| A0                | 11  | ipthdt5v    | slave sub-address I <sup>2</sup> C-bus selection/serial data input test control block |
| SCL               | 12  | iptht5v     | clock input of I <sup>2</sup> C-bus                                                   |
| SDA               | 13  | iic400kt5v  | data input/output of I <sup>2</sup> C-bus                                             |
| V <sub>SSI1</sub> | 14  | vssis       | ground supply (core only)                                                             |
| V <sub>SSA2</sub> | 15  | vssco       | ground supply analog of PLL, WS_PLL, SPDIF input stage                                |
| V <sub>DDI1</sub> | 16  | vddi        | positive supply (core only) (bond out to 2 pads)                                      |
| V <sub>DDA2</sub> | 17  | vddco       | positive supply analog of PLL, WS_PLL, SPDIF input stage                              |
| DSP_RESET         | 18  | ipthut5v    | general reset of chip (active LOW)                                                    |
| RTCB              | 19  | ipthdt5v    | asynchronous reset test control block, connect to ground (internal pull down)         |
| SHTCB             | 20  | ipthdt5v    | shift clock test control block (internal pull down)                                   |
| V <sub>SSE</sub>  | 21  | vsse        | ground supply (peripheral cells only)                                                 |
| CLK_IN            | 22  | iptht5v     | system clock input                                                                    |
| V <sub>DDE</sub>  | 23  | vdde        | positive supply (peripheral cells only)                                               |
| SPDIF2            | 24  | apio        | SPDIF2 data input (internally multiplexed with digital serial input 3)                |
| SPDIF1            | 25  | apio        | SPDIF1 data input (internally multiplexed with digital serial input 2)                |
| TSCAN             | 26  | ipthdt5v    | scan control active HIGH (internal pull down)                                         |
| SYSCLK            | 27  | bpt4mthdt5v | $n \times f_s$ output of SAA7715AH                                                    |
| IIS_OUT4          | 28  | ops5c       | data pin of digital serial output 4                                                   |
| IIS_OUT3          | 29  | ops5c       | data pin of digital serial output 3                                                   |
| IIS_OUT2          | 30  | ops5c       | data pin of digital serial output 2                                                   |
| IIS_OUT1          | 31  | ops5c       | data pin of digital serial output 1                                                   |
| IIS_WS            | 32  | ops5c       | word select output belonging to digital serial output 1 to 4                          |
| IIS_BCK           | 33  | ops5c       | bit clock output belonging to digital serial output 1 to 4                            |
| VOU <sub>TL</sub> | 34  | apio        | analog left output pin.                                                               |
| V <sub>DDA1</sub> | 35  | vddo        | FSDAC positive supply voltage (bond out to 2 pads)                                    |
| VOU <sub>TR</sub> | 36  | apio        | analog right output pin                                                               |
| V <sub>SSA1</sub> | 37  | vsso        | FSDAC ground supply voltage (bond out to 2 pads)                                      |
| VREFDA            | 38  | apio        | voltage reference pin of FSDAC                                                        |
| POM               | 39  | apio        | power-on mute pin of FSDAC                                                            |
| POWERDOWN         | 40  | iptht5v     | standby mode of chip                                                                  |

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| SYMBOL     | PIN | PIN TYPE    | DESCRIPTION                                                           |
|------------|-----|-------------|-----------------------------------------------------------------------|
| DIV_CLK_IN | 41  | ipthdt5v    | divide the input frequency on pin CLK_IN by two                       |
| DSP_INOUT5 | 42  | bpts5thdt5v | digital input/output flag of the DSP-core (F5 of the status register) |
| DSP_INOUT6 | 43  | bpts5thdt5v | digital input/output flag of the DSP-core (F6 of the status register) |
| DSP_INOUT7 | 44  | bpts5thdt5v | digital input/output flag of the DSP-core (F7 of the status register) |

**Table 1** Brief explanation of used pin types

| PIN TYPE    | EXPLANATION                                                                                                                 |
|-------------|-----------------------------------------------------------------------------------------------------------------------------|
| apio        | analog I/O pad cell; actually pin type vddco                                                                                |
| bpts5thdt5v | 43 MHz bidirectional pad; push-pull input; 3-state output; 5 ns slew rate control; TTL; hysteresis; pull-down; 5 V tolerant |
| bpts5tht5v  | 43 MHz bidirectional pad; push-pull input; 3-state output; 5 ns slew rate control; TTL; hysteresis; 5 V tolerant            |
| bpt4mthdt5v | bidirectional pad; push-pull input; 3-state output; 4 mA output drive; TTL; hysteresis; pull-down; 5 V tolerant             |
| iic400kt5v  | I <sup>2</sup> C-bus pad; 400 kHz I <sup>2</sup> C-bus specification; 5 V tolerant                                          |
| ipthdt5v    | input pad buffer; TTL; hysteresis; pull-down; 5 V tolerant                                                                  |
| iptht5v     | input pad buffer; TTL; hysteresis; 5 V tolerant                                                                             |
| ipthut5v    | input pad buffer; TTL; hysteresis; pull-up; 5 V tolerant                                                                    |
| ops5c       | output pad; push-pull; 5 ns slew rate control; CMOS                                                                         |
| op4mc       | output pad; push-pull; 4 mA output drive                                                                                    |
| vddco       | V <sub>DD</sub> supply to core only                                                                                         |
| vdde        | V <sub>DD</sub> supply to peripheral only                                                                                   |
| vddi        | V <sub>DD</sub> supply to core only                                                                                         |
| vddo        | V <sub>DD</sub> supply to core only                                                                                         |
| vssco       | V <sub>SS</sub> supply to core only (vssco does not connect the substrate)                                                  |
| vsse        | V <sub>SS</sub> supply to peripheral only                                                                                   |
| vssi        | V <sub>SS</sub> supply to core and peripheral                                                                               |
| vssis       | V <sub>SS</sub> supply to core only; with substrate connection                                                              |
| vssso       | V <sub>SS</sub> supply to core only                                                                                         |

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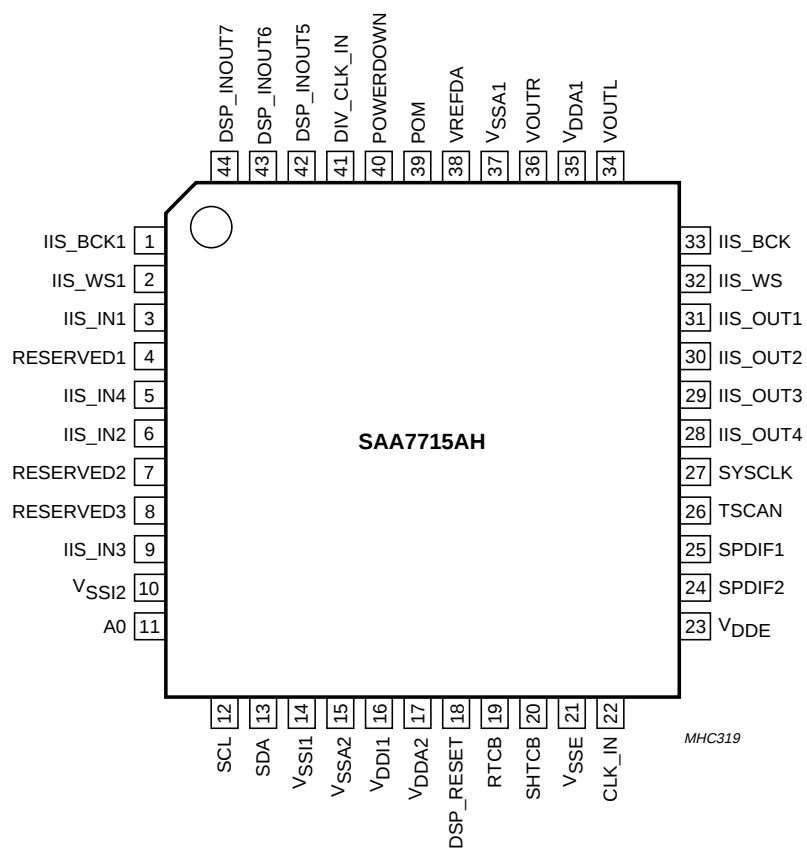


Fig.2 Pin configuration.

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## 8 FUNCTIONAL DESCRIPTION

## 8.1 PLL clock division factors for different clock inputs

An on-chip PLL generates the clock for the DSP. The DSP runs at a selectable frequency of maximum 70 MHz. The clock is generated with the PLL that uses the CLK\_IN of the chip to generate the DSP clock. Table 2 gives the PLL clock division factor and the values of the dsp\_turbo and the DIV\_CLK\_IN bits that need to be set via the I<sup>2</sup>C-bus (see Table 10).

**Table 2** PLL clock division factor per clock input.

| CLK_IN (MHz)             | pll_div[4:0] | N   | dsp_turbo | DIV_CLK_IN | DSP CLOCK (MHz) |
|--------------------------|--------------|-----|-----------|------------|-----------------|
| 8.192 (32 kHz × 256)     | 10H          | 272 | 1         | 0          | 69.632          |
| 9.728 (38 kHz × 256)     | 09H          | 227 | 1         | 0          | 69.008          |
| 11.2896 (44.1 kHz × 256) | 03H          | 198 | 1         | 0          | 69.854          |
| 12.288 (48 kHz × 256)    | 00H          | 181 | 1         | 0          | 69.504          |
| 16.384 (32 kHz × 512)    | 10H          | 272 | 1         | 1          | 69.632          |
| 18.432 (32 kHz × 576)    | 0BH          | 244 | 1         | 1          | 68.544          |
| 19.456 (38 kHz × 512)    | 09H          | 227 | 1         | 1          | 69.008          |
| 24.576 (96 kHz × 256)    | 00H          | 181 | 1         | 1          | 69.504          |

The above table does NOT imply that the clock input is restricted to the values given in this table. The clock input is restricted to be within the range of 8.192 to 12.228 MHz. For higher clock frequencies pin DIV\_CLK\_IN should be set to logic 1 performing a divide-by-2 of the CLK\_IN signal and thereby doubling the CLK\_IN frequency range that is allowed (16.384 to 24.576 MHz).

## 8.2 The word select PLL

A second on-chip PLL generates a selectable multiple of the sample rate frequency supplied on the word select pin IIS\_WS (= IIS\_WS1). The clock generated by this so called WS\_PLL is available for the user at pin SYSCLK. Tables 3 and 4 show the I<sup>2</sup>C-bus settings needed to generate the  $n \times f_s$  clock. The memory map of the I<sup>2</sup>C-bus bits is shown in Table 10.

**Table 3** Word select input range selection

| SAMPLE RATE OF $f_s$ (kHz) | sel_loop_div[1:0] |
|----------------------------|-------------------|
| 32 to 50                   | 01                |
| 50 to 96                   | 00                |

**Table 4** Selection of  $n \times f_s$  clock at SYSCLK output

| sel2 | sel1 | sel0 | SYSCLK ( $n \times$ IIS_WS1) | DUTY FACTOR                                               |
|------|------|------|------------------------------|-----------------------------------------------------------|
| 1    | 0    | 0    | 512                          | 50% for 32 to 50 kHz input;<br>66% for 50 to 96 kHz input |
| 0    | 1    | 1    | 384                          | 50%                                                       |
| 0    | 1    | 0    | 256                          | 50%                                                       |
| 0    | 0    | 1    | 192                          | 50%                                                       |
| 0    | 0    | 0    | 128                          | 50%                                                       |

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**8.3 The Filter Stream DAC (FSDAC)**

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

**8.3.1 INTERPOLATION FILTER**

The digital filter interpolates from 1 to  $64f_s$  by means of a cascade of a recursive filter and an FIR filter.

**Table 5** Digital interpolation filter characteristics

| ITEM             | CONDITIONS     | VALUE (dB) |
|------------------|----------------|------------|
| Pass band ripple | 0 to $0.45f_s$ | $\pm 0.03$ |
| Stop band        | $>0.55f_s$     | -50        |
| Dynamic range    | 0 to $0.45f_s$ | 116.5      |
| Gain             | DC             | -3.5       |

**8.3.2 NOISE SHAPER**

The 5th-order noise shaper operates at  $64f_s$ . It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

**8.3.3 FUNCTION OF PIN POM**

With pin POM it is possible to switch off the reference current of the DAC. The capacitor on pin POM determines the time after which this current has a soft switch-on. So at power-on the current audio signal outputs are always muted. The loading of the external capacitor is done in two stages via two different current sources. The loading starts at a current level that is lower than the current loading after the voltage on pin POM has passed a particular level. This results in an almost dB-linear behaviour. This prevents 'plop' effects during power on/off.

**8.3.4 POWER OFF PLOP SUPPRESSION**

To avoid plops in a power amplifier, the supply voltage of the analog part of the DAC and the rest of the chip can be fed from a separate supply of 3.3 V. A capacitor connected to this supply enables to provide power to the analog part at the moment the digital voltage is switching off fast. In this event the output voltage will decrease gradually allowing the power amplifier some extra time to switch off without audible plops.

**8.3.5 PIN VREFDA FOR INTERNAL REFERENCE**

With two internal resistors half the supply voltage  $V_{DDA1}$  is obtained and used as an internal reference. This reference voltage is used as DC voltage for the output operational amplifiers and as reference for the DAC. In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground, preferably close to the analog pin  $V_{SSA1}$ .

**8.3.6 SUPPLY OF THE ANALOG OUTPUTS**

The entire analog circuitry of the DACs and the OPAMPS are supplied by 2 supply pins,  $V_{DDA1}$  and  $V_{SSA1}$ . The  $V_{DDA1}$  must have sufficient decoupling to prevent THD degradation and to ensure a good Power Supply Rejection Ratio (PSRR). The digital part of the DAC is fully supplied from the chip core supply.

**8.4 External control pins**

The flags DSP\_INOUT5 to DSP\_INOUT7 are available as external pins. The flags can be used by the DSP depending on the downloaded software.

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### 8.5 Digital serial inputs/outputs and SPDIF inputs

#### 8.5.1 DIGITAL SERIAL INPUTS/OUTPUTS

For communication with external digital sources a digital serial bus is implemented. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7715AH acts as a slave, so the external source is master and supplies the clock.

For the I<sup>2</sup>S-bus format itself see the official specification from Philips.

The digital serial input is capable of handling Philips I<sup>2</sup>S-bus and LSB-justified formats of 16, 18, 20 and 24 bits word sizes. The sampling frequency can be 32 up to 96 kHz. See "9.8 I<sup>2</sup>C-bus memory map definition" for the bits that must be programmed, for selection of the desired serial format.

See Fig.3 for the general waveforms of the possible formats.

When the applied word length exceeds 24 bits, the LSBs are skipped.

The digital serial input/output circuitry is limited in handling the number of BCK pulses per WS period. The maximum allowed number of bit clocks per WS period is 256. Also the number of bit clocks during WS LOW and HIGH must be equal (50% WS duty factor) only for the LSB-justified formats.

There are two modes in which the digital inputs can be used (the mode is selectable via an I<sup>2</sup>C-bus bit):

- Use up to 4 digital serial inputs (8ch) with common WS and BCK signal (8ch IN and 8ch OUT + 2ch FSDAC output)
- Use one of the 2 SPDIF inputs as source instead of the use of the digital serial inputs (2ch IN and 8ch OUT + One 2ch FSDAC output).

#### 8.5.2 SPDIF INPUTS

Two separate SPDIF receivers are available, one shared with digital serial input 2 (SPDIF1) and one with the digital serial input 3 (SPDIF2). The sample frequency at which the SPDIF inputs can be used must be in the range of 32 to 96 kHz.

There are few control signals available from the SPDIF input stage. These are connected to flags of the DSP:

- A lock signal indicating if the SPDIF input 1 or 2 is in lock
- The pcm\_audio/non-pcm\_audio bit indicating if an audio or data stream is detected on SPDIF input 1 or 2. The FSDAC output will NOT be muted in the event of non-audio PCM stream. This status bit can be read via the I<sup>2</sup>C-bus, the microprocessor controller can decide to put the DAC into MUTE (via pin POM).

Handling of channel status bits: The first 40 (of 192) channel status bits of the selected SPDIF source (0FFBH, bit 20), will come available in the I<sup>2</sup>C-bus registers 0FF2H to 0FF5H. Two registers 0FF2H to 0FF3H contain the information for the right channel, the other two (0FF4H to 0FF5H) contain the information for the left channel. The information can be read via I<sup>2</sup>C-bus or by the DSP program.

The design fulfils the digital audio interface specification "IEC 60958-1 Ed2, part 1, general part IEC 60958-3 Ed2, part 3, consumer applications".

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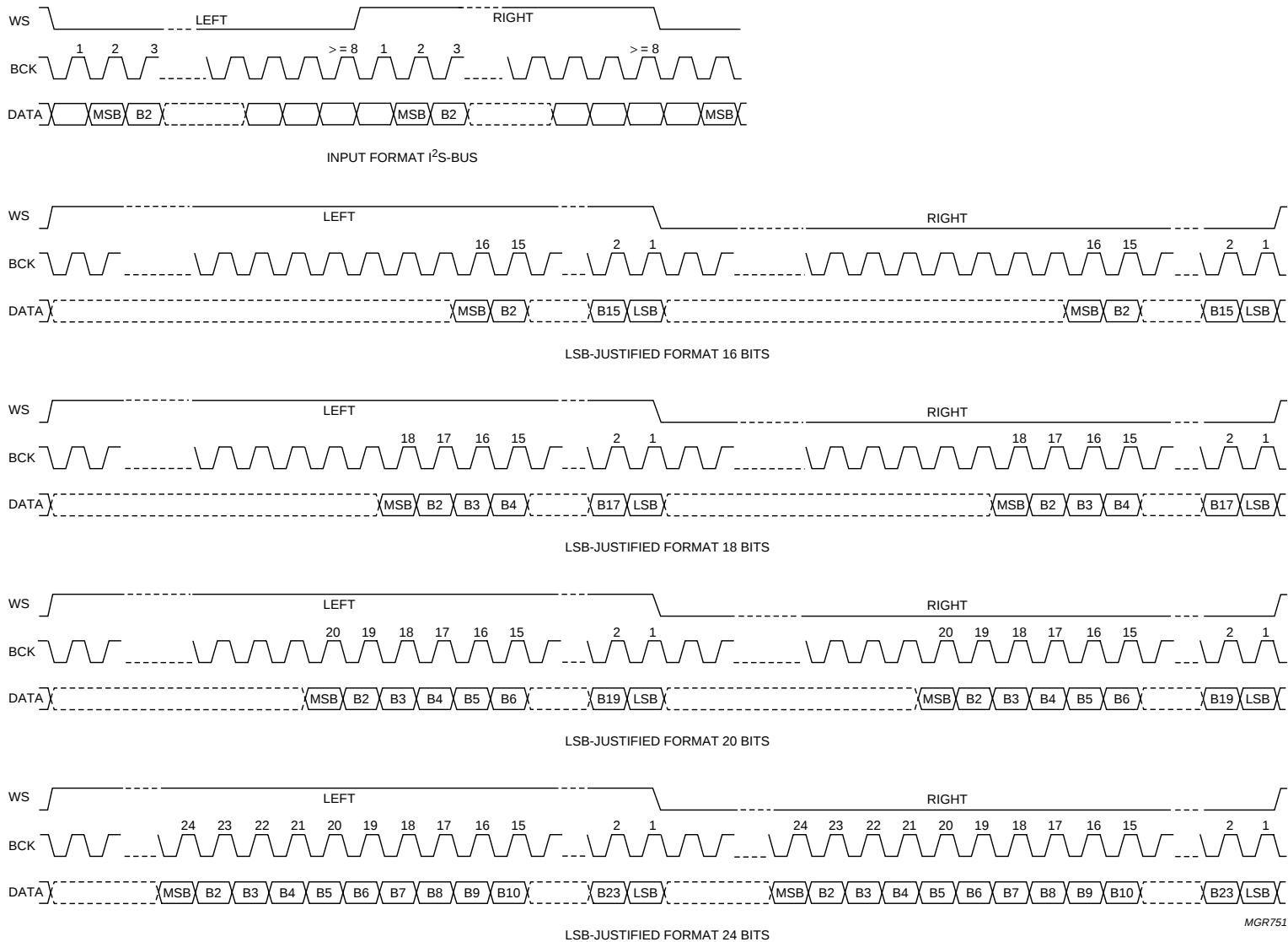


Fig.3 All serial data input/output formats.

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**8.6 I<sup>2</sup>C-bus interface (pins SCL and SDA)**

The I<sup>2</sup>C-bus format is described in "The I<sup>2</sup>C-bus and how to use it", order no. 9398 393 40011.

For the external control of the SAA7715AH a fast I<sup>2</sup>C-bus is implemented. This is a 400 kHz bus which is downward compatible with the standard 100 kHz bus.

There are two different types of control instructions:

- Loading of the Program RAM (PRAM) with the required DSP program
  - Programming the coefficient RAM (YRAM)
  - Instructions to control the DSP program.
- Selection of the digital serial input/output format to be used, the DSP clock speed.

The detailed description of the I<sup>2</sup>C-bus and the description of the different bits in the memory map is given in Chapter 9.

**8.7 Reset**

The reset (pin DSP\_RESET) is active LOW and needs an external 22 k $\Omega$  pull-up resistor. Between this pin and the V<sub>SSI</sub> ground a capacitor of 1  $\mu$ F should be connected to allow a proper switch-on of the supply voltage. The capacitor value is such that the chip is in reset as long as the power supply is not stabilized. A more or less fixed relationship between the DSP reset and the POM time constant is obligatory. The voltage on pin POM determines the current flowing in the DACs.

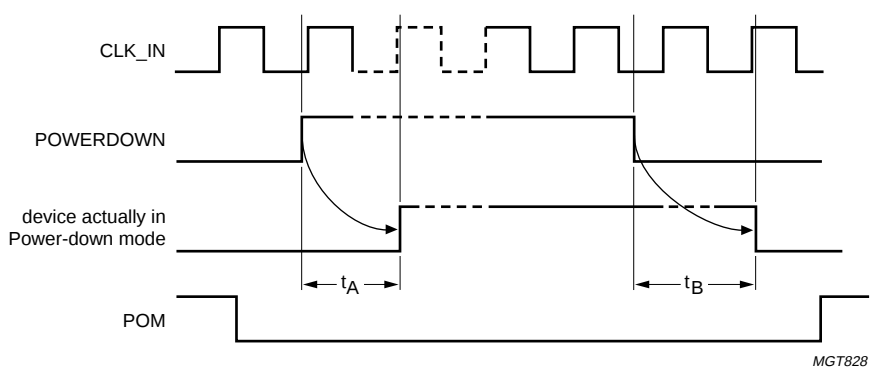
The reset sets all I<sup>2</sup>C-bus bits to their default value and it restarts the DSP program.

**8.8 Power-down mode**

The Power-down mode switches off all activity on the chip. The Power-down mode can be switched on and off using pin POWERDOWN. This pin needs to be connected to ground if not used. The following applies for the Power-down mode:

- Power-down mode may only be switched on when there is no I<sup>2</sup>C-bus activity to or from the SAA7715AH
- Power-down mode may not be switched on before the complete chip has been reset (DSP\_RESET active LOW)
- The clock signal on pin CLK\_IN should be running during Power-down mode
- It is advised to set pin POM to logic 0 before switching on the Power-down mode and set it back to logic 1 after the chip actually returns from Power-down mode as shown in Fig.4
- All on-chip registers and memories will keep their values during Power-down mode
- Digital serial outputs are not muted, the last value is kept on the output
- The SAA7715AH will not 'lock-up' the I<sup>2</sup>C-bus during Power-down mode (SDA line).

Figure 4 shows the time the chip actually is in Power-down mode after switching on/off pin POWERDOWN.



$$t_A = 4 \times (256/\text{CLK\_IN}); 8.192 \text{ MHz} < \text{CLK\_IN} < 12.288 \text{ MHz.}$$

$$t_A = 4 \times (512/\text{CLK\_IN}); 16.384 \text{ MHz} < \text{CLK\_IN} < 24.576 \text{ MHz.}$$

$$t_B = 128 \times (256/\text{CLK\_IN}); 8.192 \text{ MHz} < \text{CLK\_IN} < 12.288 \text{ MHz.}$$

$$t_B = 128 \times (512/\text{CLK\_IN}); 16.384 \text{ MHz} < \text{CLK\_IN} < 24.576 \text{ MHz.}$$

Fig.4 Power-down mode.

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**8.9 Power supply connection and EMC**

The digital part of the chip has in total 4 positive supply line connections and 5 ground connections. To minimize radiation the chip should be put on a double layer printed-circuit board with on one side a large ground plane. The ground supply lines should have a short connection to this ground plane. A coil/capacitor network in the positive supply line of the peripheral power supply line can be used as high frequency filter. The core supply lines ( $V_{DDI}$ ) have an on-chip decoupling capacitance, for EMC reasons an external decoupling capacitance must not be used on this pin. A series resistor plus capacitance is required for proper operation on pin  $V_{DDA2}$ , see Fig.9.

**8.10 Test mode connections (pins TSCAN, RTCB and SHTCB)**

Pins TSCAN, RTCB and SHTCB are used to put the chip in test mode and to test the internal connections. Each pin has an internal pull-down resistor to ground. In the application these pins can be left open or connected to ground.

**9 I<sup>2</sup>C-BUS PROTOCOL****9.1 Addressing**

Before any data is transmitted on the I<sup>2</sup>C-bus, the device that should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

**9.2 Slave address (pin A0)**

The SAA7715AH acts as a slave receiver or a slave transmitter. Therefore the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The slave address is shown in Table 6.

**Table 6** Slave address

| MSB |   |   |   |   |   |    | LSB |
|-----|---|---|---|---|---|----|-----|
| 0   | 0 | 1 | 1 | 1 | 1 | A0 | R/W |

The sub-address bit A0 corresponds to the hardware address pin A0 which allows the device to have 2 different addresses. The A0 input is also used in test mode as serial input of the test control block.

**9.3 Write cycles**

The I<sup>2</sup>C-bus configuration for a write cycle is shown in Fig.5. The write cycle is used to write the bytes to the DSP for manipulating the data and coefficients. More details can be found in the I<sup>2</sup>C-bus memory map, see Table 8.

The data length is 2, 3 or 4 bytes depending on the accessed memory. If the Y-memory is addressed the data length is 2 bytes, in the event of the X-memory the length is 3 bytes. The slave receiver detects the address and adjusts the number of bytes accordingly.

For this RAM-based product the internal P-memory (PRAM) can be accessed via the I<sup>2</sup>C-bus interface. The transmitted data stream should be 4 bytes.

**9.4 Read cycles**

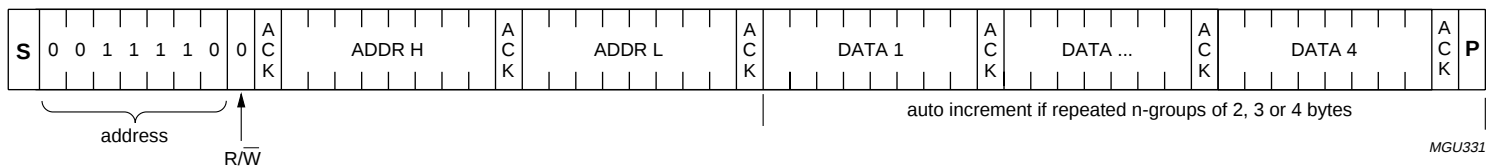
The I<sup>2</sup>C-bus configuration for a read cycle is shown in Fig.6. The read cycle is used to read the data values from XRAM, YRAM or PRAM. The master starts with a START condition S, the SAA7715AH address '0011110' and a logic 0 (write) for the read/write bit. This is followed by an acknowledge of the SAA7715AH. Then the master writes the high memory address (ADDR H) and low memory address (ADDR L) where the reading of the memory content of the SAA7715AH must start. The SAA7715AH acknowledges these addresses both.

The master generates a repeated START (Sr) and again the SAA7715AH address '0011110' but this time followed by a logic 1 (read) of the read/write bit. From this moment on the SAA7715AH will send the memory content in groups of 3 (X/Y-memory or registers) or 4 (P-memory) bytes to the I<sup>2</sup>C-bus each time acknowledged by the master. The master stops this cycle by generating a negative acknowledge, then the SAA7715AH frees the I<sup>2</sup>C-bus and the master can generate a STOP condition.

The data is transferred from the DSP register to the I<sup>2</sup>C-bus register at execution of the MPI instruction in the DSP program. Therefore at least once every DSP routine an MPI instruction should be added.

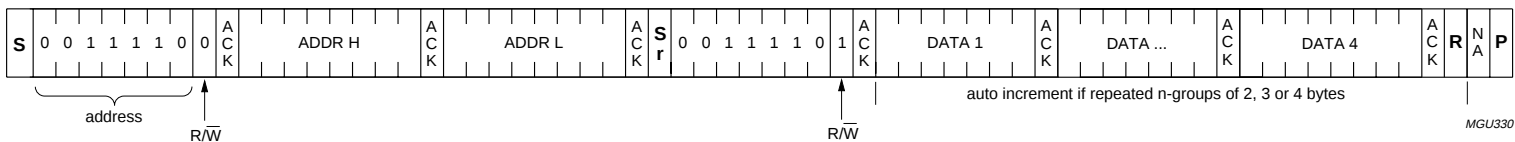
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S = START condition.  
 P = STOP condition.  
 ACK = acknowledge from SAA7715AH.  
 ADDR H and ADDR L = address DSP register.  
 DATA 1 to DATA 4 = 2, 3 or 4 bytes data word.

Fig.5 Master transmitter writes to the SAA7715AH registers.



S = START condition.  
 Sr = repeated START condition.  
 P = STOP condition.  
 ACK = acknowledge from SAA7715AH (SDA LOW).  
 R = repeat n-times the 2, 3 or 4 bytes data group.  
 NA = Negative Acknowledge master (SDA HIGH).  
 ADDR H and ADDR L = address DSP register.  
 DATA 1 to DATA 4 = 2, 3 or 4 bytes data word.

Fig.6 Master transmitter reads from the SAA7715AH registers.

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**9.5 Program RAM**

The SAA7715AH has a 1.5 kbyte PRAM to store the DSP instruction code into. Also a 2 kbyte PROM is on-chip available and can be accessed (memory mapped) without the need of selecting the PROM or PRAM. The DSP instruction code can be downloaded into the PRAM via the I<sup>2</sup>C-bus. The write and read cycle are shown in Figs 5 and 6 respectively.

The DSP has an instruction word width of 32 bits which means that this space should be accessed with 4 bytes in consecutive order and does have the auto-increment function.

**9.6 Data word alignment**

It is possible to transfer data via the I<sup>2</sup>C-bus to a destination where it can have different data word length. Those destinations with data word are shown in Table 7.

**Table 7** Data word alignment

| SOURCE               | DESTINATION                    | DATA WORD                          | BYTES (NUMBER) |
|----------------------|--------------------------------|------------------------------------|----------------|
| I <sup>2</sup> C-bus | DSP-PRAM                       | MBBB BBBB BBBB BBBB BBBB BBBB BBBL | 4              |
| I <sup>2</sup> C-bus | DSP and general control        | MBBB BBBB BBBB BBBB BBBB BBBL      | 3              |
| I <sup>2</sup> C-bus | I <sup>2</sup> C-bus registers | MBBB BBBB BBBB BBBB BBBB BBBL      | 3              |
| I <sup>2</sup> C-bus | DSP-XRAM                       | MBBB BBBB BBBB BBBB BBBB BBBL      | 3              |
| I <sup>2</sup> C-bus | DSP-YRAM                       | XXXX MBBB BBBB BBBL                | 2              |

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**9.7 I<sup>2</sup>C-bus memory map specification**

The I<sup>2</sup>C-bus memory map contains all defined I<sup>2</sup>C-bus bits. The map is split up in two different sections: the hardware memory registers and the RAM definitions. In Table 8 the preliminary memory map is depicted. The hardware registers are memory map on the XRAM of DSP. Table 9 shows the detailed memory map of those locations. All locations are acknowledged by the SAA7715AH even if the user tries to write to a reserved space. The data in these sections will be lost. Reading from these locations will result in undefined data words.

**Table 8** I<sup>2</sup>C-bus memory map

| ADDRESS               | FUNCTION                                            | SIZE             |
|-----------------------|-----------------------------------------------------|------------------|
| 8000H to 87FFH        | DSP to PROM (not readable via I <sup>2</sup> C-bus) | 2k × 32 bits     |
| 602FH                 | DSP and general control                             | 1 × 24 bits      |
| 2000H to 25FFH        | DSP to PRAM                                         | 1.5k × 32 bits   |
| 1000H to 15FFH        | DSP to YRAM                                         | 1.5k × 12 bits   |
| 0FF2H to 0FF5H, 0FFBH | I <sup>2</sup> C-bus register                       | 5 × 24 bits      |
| 0000H to 0B7FH        | DSP to XRAM                                         | 2.875k × 24 bits |

**Table 9** I<sup>2</sup>C-bus memory map overview

| ADDRESS                   | DESCRIPTION                              |
|---------------------------|------------------------------------------|
| <b>Hardware registers</b> |                                          |
| 0FFBH                     | Selector register 1                      |
| 0FF5H                     | SPDIF IN channel status register 1 left  |
| 0FF4H                     | SPDIF IN channel status register 2 left  |
| 0FF3H                     | SPDIF IN channel status register 1 right |
| 0FF2H                     | SPDIF IN channel status register 2 right |
| <b>DSP control</b>        |                                          |
| 602FH                     | DSP and general control register         |

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9.8 I<sup>2</sup>C-bus memory map definition

Table 10 DSP and general control register (602FH)

| NAME                       | SIZE (BITS) | DESCRIPTION                                                                                                                 | DEFAULT | BIT POSITION |
|----------------------------|-------------|-----------------------------------------------------------------------------------------------------------------------------|---------|--------------|
|                            | 1           | reserved                                                                                                                    | 0       | 0            |
| pll_div[4:0]               | 5           | PLL clock division factor according to Table 2                                                                              | 00011   | 5 to 1       |
| dsp_turbo                  | 1           | PLL output frequency<br>1: double<br>0: no doubling                                                                         | 1       | 6            |
|                            | 1           | reserved                                                                                                                    | 1       | 7            |
| pc_reset_dsp               | 1           | program counter reset DSP<br>1: reset on<br>0: reset off                                                                    | 0       | 8            |
|                            | 2           | reserved                                                                                                                    | 00      | 10 to 9      |
| sel[2:0]                   | 3           | selection of $n \times f_s$ clock at SYSCLK output according to Table 4                                                     | 010     | 13 to 11     |
| sel_loop_div[1:0]          | 2           | word select input range selection for WS_PLL according to Table 3                                                           | 01      | 15 to 14     |
|                            | 2           | reserved                                                                                                                    | 00      | 17 to 16     |
| sel_FSDAC_clk              | 2           | clock source for FSDAC<br>00: WS_PLL if no signal to pin CLK_IN<br>01: $512f_s$ to pin CLK_IN<br>11: $256f_s$ to pin CLK_IN | 00      | 19 to 18     |
| dis_SYSCLK                 | 1           | output on pin SYSCLK<br>1: disable<br>0: enable                                                                             | 0       | 20           |
| $256f_s \cdot n \cdot F_s$ | 1           | signal on pin SYSCLK<br>1: fixed $256f_s$ clock<br>0: $n \times f_s$ clock; determined by bits 13 to 11                     | 0       | 21           |
|                            | 2           | reserved                                                                                                                    | 00      | 23 to 22     |

Table 11 SPDIF IN channel status register 2 right (0FF2H)

| NAME                 | SIZE (BITS) | DESCRIPTION                                    | DEFAULT | BIT POSITION |
|----------------------|-------------|------------------------------------------------|---------|--------------|
| ch_stat_in right lsb | 20          | channel status SPDIF in right LSB bits 19 to 0 | 00000H  | 19 to 0      |

Table 12 SPDIF IN channel status register 1 right (0FF3H)

| NAME                 | SIZE (BITS) | DESCRIPTION                                     | DEFAULT | BIT POSITION |
|----------------------|-------------|-------------------------------------------------|---------|--------------|
| ch_stat_in right msb | 20          | channel status SPDIF in right MSB bits 39 to 20 | 00000H  | 19 to 0      |

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**Table 13** SPDIF IN channel status register 2 left (0FF4H)

| NAME                | SIZE (BITS) | DESCRIPTION                                    | DEFAULT | BIT POSITION |
|---------------------|-------------|------------------------------------------------|---------|--------------|
| ch_stat_in left lsb | 20          | channel status SPDIF in2 left LSB bits 19 to 0 | 00000H  | 19 to 0      |

**Table 14** SPDIF IN channel status register 1 left (0FF5H)

| NAME                | SIZE (BITS) | DESCRIPTION                                     | DEFAULT | BIT POSITION |
|---------------------|-------------|-------------------------------------------------|---------|--------------|
| ch_stat_in left msb | 20          | channel status SPDIF in2 left MSB bits 39 to 20 | 00000H  | 19 to 0      |

**Table 15** Selector register 1 (0FFBH)

| NAME               | SIZE (BITS) | DESCRIPTION                                                                                                                                                                                       | DEFAULT | BIT POSITION |
|--------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------|
| format_in1         | 3           | digital serial inputs 1 and 4 data format according to Table 17                                                                                                                                   | 011     | 2 to 0       |
| format_in2         | 3           | digital serial input 2 data format according to Table 17                                                                                                                                          | 011     | 5 to 3       |
| format_in3         | 3           | digital serial input 3 data format according to Table 17                                                                                                                                          | 011     | 8 to 6       |
| format_out         | 3           | digital serial outputs 1 to 4 data format according to Table 18                                                                                                                                   | 000     | 11 to 9      |
| en_output          | 1           | enable or disable digital serial outputs<br>1: enable<br>0: disable                                                                                                                               | 1       | 12           |
|                    | 1           | reserved                                                                                                                                                                                          | 0       | 13           |
| master_source      | 4           | source selection<br>0000: digital serial input 1<br>0101: digital serial input 2 or SPDIF 1 (see bit 18)<br>1010: digital serial input 3 or SPDIF 2 (see bit 19)<br>all other values are reserved | 0000    | 17 to 14     |
| spdif_sel1         | 1           | SPDIF1 or digital serial input 2                                                                                                                                                                  | 0       | 18           |
|                    |             | 1: SPDIF1                                                                                                                                                                                         |         |              |
|                    |             | 0: digital serial input 2                                                                                                                                                                         |         |              |
| spdif_sel2         | 1           | SPDIF2 or digital serial input 3                                                                                                                                                                  | 0       | 19           |
|                    |             | 1: SPDIF2                                                                                                                                                                                         |         |              |
|                    |             | 0: digital serial input 3                                                                                                                                                                         |         |              |
| sel_spdifin_chstat | 1           | select channel status information taken from SPDIF1 or SPDIF2                                                                                                                                     | 0       | 20           |
|                    |             | 1: from input SPDIF2                                                                                                                                                                              |         |              |
|                    |             | 0: from input SPDIF1                                                                                                                                                                              |         |              |
|                    | 3           | reserved                                                                                                                                                                                          | 000     | 23 to 21     |

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**Table 16** Default settings of I<sup>2</sup>C-bus registers after power-up and reset

| I <sup>2</sup> C-BUS ADDRESS | DEFAULT VALUE |
|------------------------------|---------------|
| 602FH                        | 0050C6H       |
| 0FFBH                        | 0010DBH       |
| 0FF5H                        | 000000H       |
| 0FF4H                        | 000000H       |
| 0FF3H                        | 000000H       |
| 0FF2H                        | 000000H       |

**9.9 Table definitions****Table 17** Digital serial format for inputs 1 to 4

| format_in1, 2 and 3 |       |       | INPUT                         |
|---------------------|-------|-------|-------------------------------|
| BIT 2               | BIT 1 | BIT 0 |                               |
| 0                   | 1     | 1     | standard I <sup>2</sup> S-bus |
| 1                   | 0     | 0     | LSB-justified, 16 bits        |
| 1                   | 0     | 1     | LSB-justified, 18 bits        |
| 1                   | 1     | 0     | LSB-justified, 20 bits        |
| 1                   | 1     | 1     | LSB-justified, 24 bits        |

**Table 18** Digital serial formats for outputs 1 to 4

| format_out |       |       | OUTPUT                        |
|------------|-------|-------|-------------------------------|
| BIT 2      | BIT 1 | BIT 0 |                               |
| 0          | 0     | 0     | standard I <sup>2</sup> S-bus |
| 1          | 0     | 0     | LSB-justified, 16 bits        |
| 1          | 0     | 1     | LSB-justified, 18 bits        |
| 1          | 1     | 0     | LSB-justified, 20 bits        |
| 1          | 1     | 1     | LSB-justified, 24 bits        |

**10 SOFTWARE IN ROM DESCRIPTION**

The function of this chip is related to the PROM code (ROM code dependent).

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**11 LIMITING VALUES**

In accordance with the Absolute Maximum Ratings System (IEC 60134).

| SYMBOL                      | PARAMETER                                   | CONDITIONS                                               | MIN. | MAX.     | UNIT |
|-----------------------------|---------------------------------------------|----------------------------------------------------------|------|----------|------|
| $V_{DD}$                    | supply voltage                              |                                                          | -0.5 | +3.6     | V    |
| $V_I$                       | input voltage                               |                                                          | -0.5 | +5.5     | V    |
| $I_{IK}$                    | input clamping diode current                | $V_I < -0.5 \text{ V}$ or $V_I > V_{DD} + 0.5 \text{ V}$ | –    | $\pm 10$ | mA   |
| $I_{OK}$                    | output clamping diode current               | $V_O < -0.5 \text{ V}$ or $V_O > V_{DD} + 0.5 \text{ V}$ | –    | $\pm 20$ | mA   |
| $I_{O(\text{sink/source})}$ | output source or sink current               | $-0.5 \text{ V} < V_O < V_{DD} + 0.5 \text{ V}$          | –    | $\pm 20$ | mA   |
| $I_{DD}, I_{SS}$            | $V_{DD}$ or $V_{SS}$ current per supply pin |                                                          | –    | $\pm 50$ | mA   |
| $T_{\text{amb}}$            | ambient temperature                         |                                                          | -40  | +85      | °C   |
| $T_{\text{stg}}$            | storage temperature                         |                                                          | -65  | +125     | °C   |
| $V_{\text{ESD}}$            | electrostatic handling voltage              | note 1                                                   | 200  | –        | V    |
|                             |                                             | note 2                                                   | 2000 | –        | V    |
| $I_{lu(\text{prot})}$       | latch-up protection current                 | CIC specification/test method                            | 100  | –        | mA   |
| $P_{\text{tot}}$            | total power dissipation                     |                                                          | –    | 600      | mW   |

**Notes**

- Machine model ( $R = 0 \text{ } \Omega$ ;  $C = 100 \text{ pF}$ ;  $L = 2.5 \text{ } \mu\text{H}$ ).
- Human body model ( $R = 1500 \text{ } \Omega$ ;  $C = 100 \text{ pF}$ ).

**12 THERMAL CHARACTERISTICS**

| SYMBOL        | PARAMETER                                   | CONDITIONS                       | VALUE | UNIT |
|---------------|---------------------------------------------|----------------------------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | mounted on printed-circuit board | 60    | K/W  |

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**13 CHARACTERISTICS** $V_{DD} = 3.15$  to  $3.45$  V; unless otherwise specified.

| SYMBOL                                                                                                                                               | PARAMETER                                                 | CONDITIONS                                      | MIN.           | TYP. | MAX. | UNIT |
|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|-------------------------------------------------|----------------|------|------|------|
| <b>Supplies; <math>T_{amb} = -40</math> to <math>+85</math> °C</b>                                                                                   |                                                           |                                                 |                |      |      |      |
| $V_{DD}$                                                                                                                                             | operating supply voltage                                  | all pins $V_{DD}$ with respect to pins $V_{SS}$ | 3.15           | 3.3  | 3.45 | V    |
| $I_{DD}$                                                                                                                                             | supply current of the digital part                        |                                                 | –              | 95   | –    | mA   |
| $I_{DD(core)}$                                                                                                                                       | supply current of the digital core part                   | high activity of the DSP at DSPFREQ frequency   | –              | 90   | –    | mA   |
| $I_{DD(peri)}$                                                                                                                                       | supply current of the digital periphery part              | no external load to ground                      | –              | 5    | –    | mA   |
| $I_{DDA}$                                                                                                                                            | supply current of the analog part                         | zero input and output signal                    | –              | 20   | –    | mA   |
| $I_{DDA(DAC)}$                                                                                                                                       | supply current of the DAC                                 | zero input and output signal                    | –              | 6.5  | 13   | mA   |
|                                                                                                                                                      |                                                           | Power-down mode                                 | –              | 250  | –    | µA   |
| $I_{DDA(SPDIF)}$                                                                                                                                     | supply current of the SPDIF inputs, on-chip PLL and WSPLL | zero input and output signals                   | –              | 13.5 | 27   | mA   |
| $P_{tot}$                                                                                                                                            | total power dissipation                                   |                                                 | –              | 380  | –    | mW   |
| $I_{POWERDOWN}$                                                                                                                                      | DC supply current of the total chip in Power-down mode    | pin POWERDOWN enabled                           | –              | 400  | –    | µA   |
| <b>Digital I/O; <math>T_{amb} = -40</math> to <math>+85</math> °C; <math>V_{DD} = 3.15</math> to <math>3.45</math> V; unless otherwise specified</b> |                                                           |                                                 |                |      |      |      |
| $V_{IH}$                                                                                                                                             | HIGH-level input voltage all digital inputs and I/Os      |                                                 | 2.0            | –    | –    | V    |
| $V_{IL}$                                                                                                                                             | LOW-level input voltage all digital inputs and I/Os       |                                                 | –              | –    | 0.8  | V    |
| $V_{hys}$                                                                                                                                            | Schmitt-trigger hysteresis                                |                                                 | 0.4            | –    | –    | V    |
| $V_{OH}$                                                                                                                                             | HIGH-level output voltage                                 | standard output; $I_O = -4$ mA                  | $V_{DD} - 0.4$ | –    | –    | V    |
|                                                                                                                                                      |                                                           | 5 ns slew rate output; $I_O = -4$ mA            | $V_{DD} - 0.4$ | –    | –    | V    |
|                                                                                                                                                      |                                                           | 10 ns slew rate output; $I_O = -2$ mA           | $V_{DD} - 0.4$ | –    | –    | V    |
|                                                                                                                                                      |                                                           | 20 ns slew rate output; $I_O = -1$ mA           | $V_{DD} - 0.4$ | –    | –    | V    |

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| SYMBOL                                                                                                                                                                                   | PARAMETER                                      | CONDITIONS                                              | MIN. | TYP. | MAX. | UNIT |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|---------------------------------------------------------|------|------|------|------|
| V <sub>OL</sub>                                                                                                                                                                          | LOW-level output voltage                       | standard output;<br>I <sub>O</sub> = 4 mA               | –    | –    | 0.4  | V    |
|                                                                                                                                                                                          |                                                | 5 ns slew rate output;<br>I <sub>O</sub> = 4 mA         | –    | –    | 0.4  | V    |
|                                                                                                                                                                                          |                                                | 10 ns slew rate<br>output; I <sub>O</sub> = 2 mA        | –    | –    | 0.4  | V    |
|                                                                                                                                                                                          |                                                | 20 ns slew rate<br>output; I <sub>O</sub> = 1 mA        | –    | –    | 0.4  | V    |
|                                                                                                                                                                                          |                                                | I <sup>2</sup> C-bus output;<br>I <sub>O</sub> = 4 mA   | –    | –    | 0.4  | V    |
| I <sub>LO</sub>                                                                                                                                                                          | output leakage current 3-state<br>outputs      | V <sub>O</sub> = 0 V or V <sub>DD</sub>                 | –    | –    | ±5   | μA   |
| R <sub>pd</sub>                                                                                                                                                                          | internal pull-down resistor to V <sub>SS</sub> |                                                         | 24   | 50   | 140  | kΩ   |
| R <sub>pu</sub>                                                                                                                                                                          | internal pull-up resistor to V <sub>DD</sub>   |                                                         | 30   | 50   | 100  | kΩ   |
| C <sub>i</sub>                                                                                                                                                                           | input capacitance                              |                                                         | –    | –    | 3.5  | pF   |
| t <sub>i(r)</sub> ,t <sub>i(f)</sub>                                                                                                                                                     | input rise and fall times                      | V <sub>DD</sub> = 3.45 V                                | –    | 6    | 200  | ns   |
| t <sub>o(t)</sub>                                                                                                                                                                        | output transition time                         | standard output;<br>C <sub>L</sub> = 30 pF              | –    | 3.5  | –    | ns   |
|                                                                                                                                                                                          |                                                | 5 ns slew rate output;<br>C <sub>L</sub> = 30 pF        | –    | 5    | –    | ns   |
|                                                                                                                                                                                          |                                                | 10 ns slew rate<br>output; C <sub>L</sub> = 30 pF       | –    | 10   | –    | ns   |
|                                                                                                                                                                                          |                                                | 20 ns slew rate<br>output; C <sub>L</sub> = 30 pF       | –    | 20   | –    | ns   |
|                                                                                                                                                                                          |                                                | I <sup>2</sup> C-bus output;<br>C <sub>L</sub> = 400 pF | 60   | –    | 300  | ns   |
| AC characteristics SPDIF1 and SPDIF2 inputs; T <sub>amb</sub> = 25 °C; V <sub>DDA2</sub> = 3.3 V; unless otherwise specified                                                             |                                                |                                                         |      |      |      |      |
| V <sub>i(p-p)</sub>                                                                                                                                                                      | AC input level (peak-to-peak level)            |                                                         | 0.2  | 0.5  | 3.3  | V    |
| R <sub>i</sub>                                                                                                                                                                           | input impedance                                | at 1 kHz                                                | –    | 6    | –    | kΩ   |
| V <sub>hys</sub>                                                                                                                                                                         | hysteresis of input voltage                    |                                                         | –    | 40   | –    | mV   |
| Analog DAC outputs; V <sub>DDA1</sub> = 3.3 V; f <sub>s</sub> = 44.1 kHz; T <sub>amb</sub> = 25 °C; R <sub>L</sub> = 5 kΩ; all voltages referenced to ground; unless otherwise specified |                                                |                                                         |      |      |      |      |
| DC CHARACTERISTICS                                                                                                                                                                       |                                                |                                                         |      |      |      |      |
| R <sub>O(DAC)</sub>                                                                                                                                                                      | DAC output resistance                          |                                                         | –    | 0.13 | 3.0  | Ω    |
| I <sub>o(max)</sub>                                                                                                                                                                      | maximum output current                         | (THD + N)/S < 0.1%<br>R <sub>L</sub> = 5 kΩ             | –    | 0.22 | –    | mA   |
| R <sub>L</sub>                                                                                                                                                                           | load resistance                                |                                                         | 3    | –    | –    | kΩ   |
| C <sub>L</sub>                                                                                                                                                                           | load capacitance                               |                                                         | –    | –    | 200  | pF   |
| R <sub>O(VREFDA)</sub>                                                                                                                                                                   | VREFDA output resistance                       |                                                         | –    | 28   | –    | kΩ   |
| AC CHARACTERISTICS                                                                                                                                                                       |                                                |                                                         |      |      |      |      |
| V <sub>o(rms)</sub>                                                                                                                                                                      | output voltage (RMS value)                     |                                                         | –    | 1000 | –    | mV   |
| ΔV <sub>o</sub>                                                                                                                                                                          | unbalance between channels                     |                                                         | –    | 0.1  | –    | dB   |

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| SYMBOL        | PARAMETER                                            | CONDITIONS                                                             | MIN. | TYP. | MAX. | UNIT  |
|---------------|------------------------------------------------------|------------------------------------------------------------------------|------|------|------|-------|
| (THD + N)/S   | total harmonic distortion plus noise-to-signal ratio | at 0 dB                                                                | –    | –85  | –    | dB(A) |
|               |                                                      | at –60 dB                                                              | –    | –37  | –    | dB(A) |
| S/N           | signal-to-noise ratio                                | code = 0                                                               | –    | 100  | –    | dB(A) |
| $\alpha_{CS}$ | channel separation                                   |                                                                        | –    | 80   | –    | dB    |
| PSRR          | power supply rejection ratio                         | $f_{\text{ripple}} = 1 \text{ kHz};$<br>$V_{\text{ripple(p-p)}} = 1\%$ | –    | 50   | –    | dB    |

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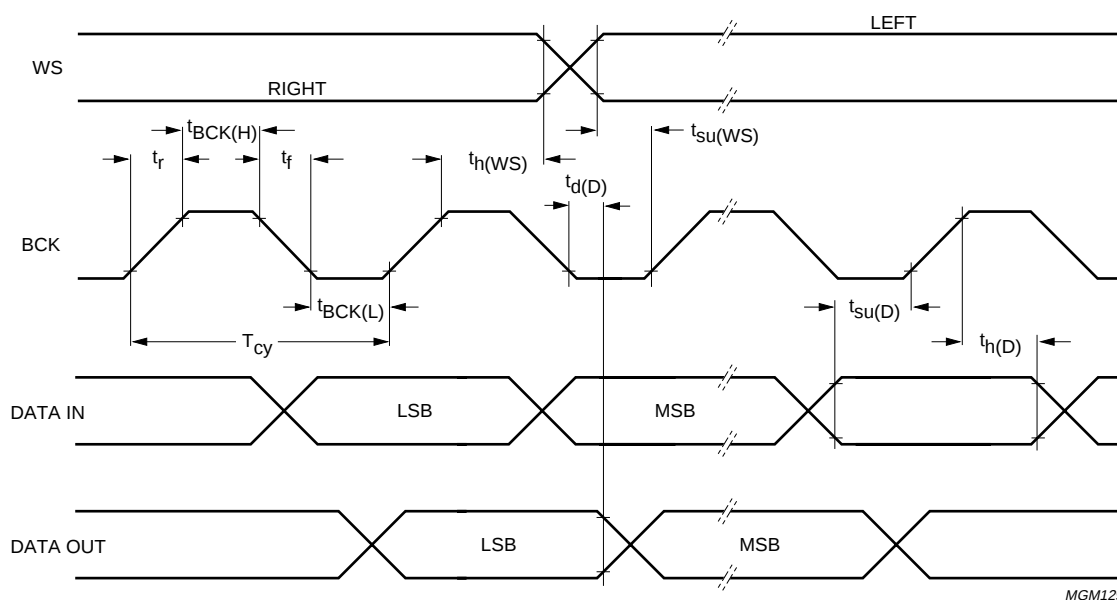
14 I<sup>2</sup>S-BUS TIMING

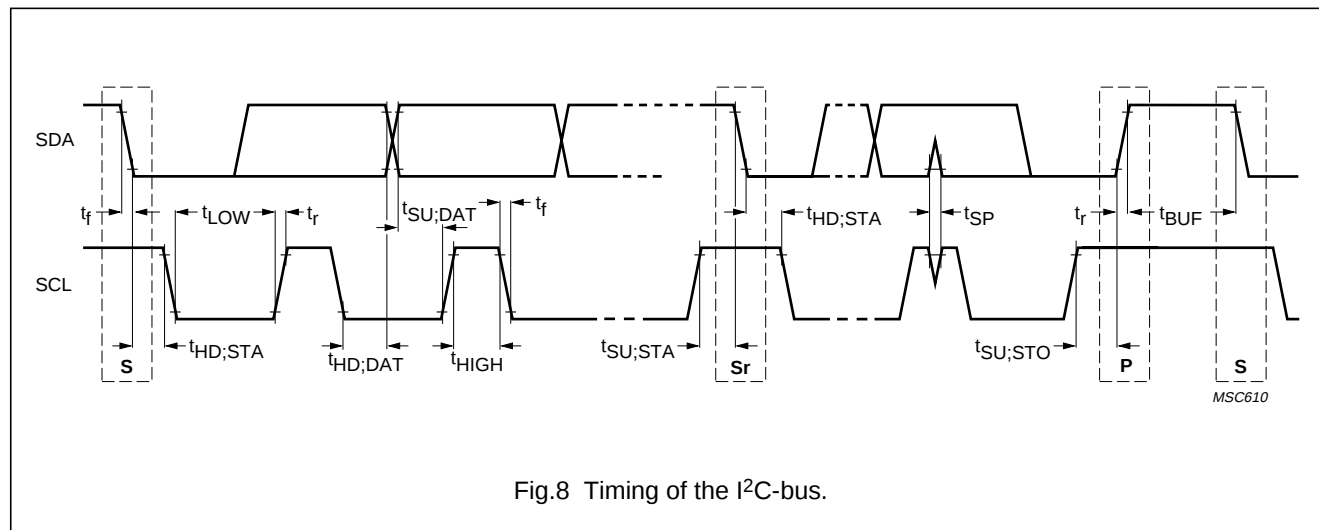
Fig.7 Timing of the digital serial audio data inputs and outputs.

**Table 19** Timing of the digital serial audio data inputs and outputs (see Fig.7)

| SYMBOL       | PARAMETER               | CONDITIONS               | MIN.         | TYP. | MAX.         | UNIT |
|--------------|-------------------------|--------------------------|--------------|------|--------------|------|
| $T_{cy}$     | bit clock cycle time    |                          | 162          | –    | –            | ns   |
| $t_r$        | rise time               | $T_{cy} = 50 \text{ ns}$ | –            | –    | $0.15T_{cy}$ | ns   |
| $t_f$        | fall time               | $T_{cy} = 50 \text{ ns}$ | –            | –    | $0.15T_{cy}$ | ns   |
| $t_{BCK(H)}$ | bit clock HIGH time     | $T_{cy} = 50 \text{ ns}$ | $0.35T_{cy}$ | –    | –            | ns   |
| $t_{BCK(L)}$ | bit clock LOW time      | $T_{cy} = 50 \text{ ns}$ | $0.35T_{cy}$ | –    | –            | ns   |
| $t_{su(D)}$  | data set-up time        | $T_{cy} = 50 \text{ ns}$ | $0.2T_{cy}$  | –    | –            | ns   |
| $t_{h(D)}$   | data hold time          | $T_{cy} = 50 \text{ ns}$ | $0.2T_{cy}$  | –    | –            | ns   |
| $t_{d(D)}$   | data delay time         | $T_{cy} = 50 \text{ ns}$ | –            | –    | $0.15T_{cy}$ | ns   |
| $t_{su(WS)}$ | word select set-up time | $T_{cy} = 50 \text{ ns}$ | $0.2T_{cy}$  | –    | –            | ns   |
| $t_{h(WS)}$  | word select hold time   | $T_{cy} = 50 \text{ ns}$ | $0.2T_{cy}$  | –    | –            | ns   |

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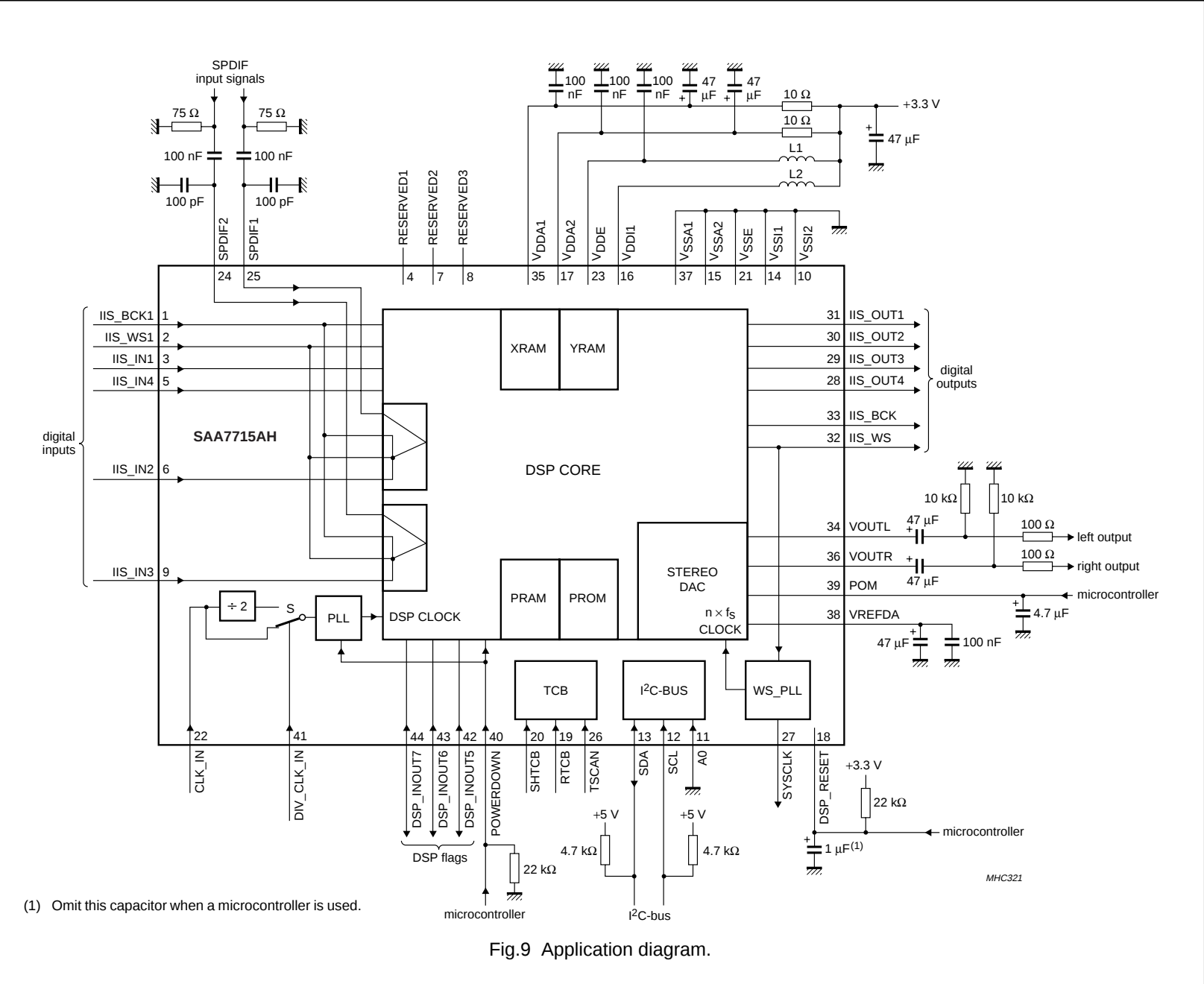
15 I<sup>2</sup>C-BUS TIMINGTable 20 Timing of the I<sup>2</sup>C-bus (see Fig.8)

| SYMBOL              | PARAMETER                                                                                   | CONDITIONS           | STANDARD MODE I <sup>2</sup> C-BUS |      | FAST MODE I <sup>2</sup> C-BUS |      | UNIT |
|---------------------|---------------------------------------------------------------------------------------------|----------------------|------------------------------------|------|--------------------------------|------|------|
|                     |                                                                                             |                      | MIN.                               | MAX. | MIN.                           | MAX. |      |
| f <sub>SCL</sub>    | SCL clock frequency                                                                         |                      | 0                                  | 100  | 0                              | 400  | kHz  |
| t <sub>BUF</sub>    | bus free time between a STOP and START condition                                            |                      | 4.7                                | —    | 1.3                            | —    | μs   |
| t <sub>HD;STA</sub> | hold time (repeated) START condition; after this period, the first clock pulse is generated |                      | 4.0                                | —    | 0.6                            | —    | μs   |
| t <sub>LOW</sub>    | SCL LOW period                                                                              |                      | 4.7                                | —    | 1.3                            | —    | μs   |
| t <sub>HIGH</sub>   | SCL HIGH period                                                                             |                      | 4.0                                | —    | 0.6                            | —    | μs   |
| t <sub>SU;STA</sub> | set-up time for a repeated START condition                                                  |                      | 4.7                                | —    | 0.6                            | —    | μs   |
| t <sub>HD;DAT</sub> | DATA hold time                                                                              |                      | 0                                  | —    | 0                              | 0.9  | μs   |
| t <sub>SU;DAT</sub> | DATA set-up time                                                                            |                      | 250                                | —    | 100                            | —    | ns   |
| t <sub>r</sub>      | rise time of both SDA and SCL signals                                                       | C <sub>b</sub> in pF | —                                  | 1000 | 20 + 0.1C <sub>b</sub>         | 300  | ns   |
| t <sub>f</sub>      | fall time of both SDA and SCL signals                                                       | C <sub>b</sub> in pF | —                                  | 300  | 20 + 0.1C <sub>b</sub>         | 300  | ns   |
| t <sub>SU;STO</sub> | set-up time for STOP condition                                                              |                      | 4.0                                | —    | 0.6                            | —    | μs   |
| C <sub>b</sub>      | capacitive load for each bus line                                                           |                      | —                                  | 400  | —                              | 400  | pF   |
| t <sub>SP</sub>     | pulse width of spikes to be suppressed by input filter                                      |                      | not applicable                     |      | 0                              | 50   | ns   |

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16 APPLICATION DIAGRAM



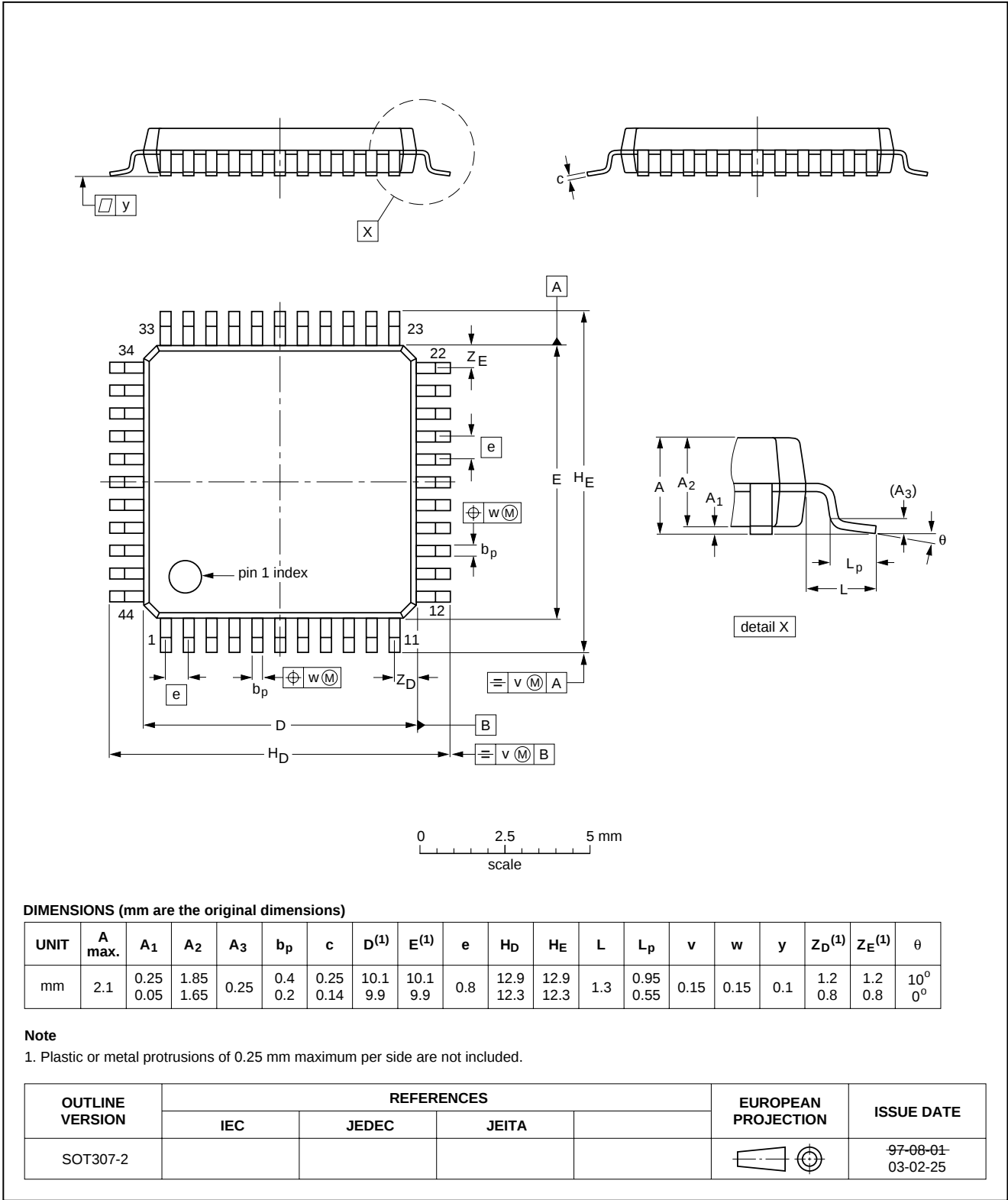
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17 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



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**18 SOLDERING****18.1 Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

**18.2 Reflow soldering**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

**18.3 Wave soldering**

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**18.4 Manual soldering**

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## 18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE <sup>(1)</sup>                                           | SOLDERING METHOD                  |                       |
|------------------------------------------------------------------|-----------------------------------|-----------------------|
|                                                                  | WAVE                              | REFLOW <sup>(2)</sup> |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA                             | not suitable                      | suitable              |
| HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable <sup>(3)</sup>       | suitable              |
| PLCC <sup>(4)</sup> , SO, SOJ                                    | suitable                          | suitable              |
| LQFP, QFP, TQFP                                                  | not recommended <sup>(4)(5)</sup> | suitable              |
| SSOP, TSSOP, VSO                                                 | not recommended <sup>(6)</sup>    | suitable              |

## Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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## 19 DATA SHEET STATUS

| DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)</sup> | DEFINITIONS                                                                                                                                                                                                                                                                                                            |
|----------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective data                   | Development                   | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.                                                                                                                            |
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