



# PCA9570

Remote 4-bit general purpose outputs for 1 MHz I<sup>2</sup>C-bus

Rev. 4 — 17 September 2014

Product data sheet

## 1. General description

---

The PCA9570 is a CMOS device that provides 4 bits of General Purpose parallel Output (GPO) expansion in low voltage processor and handheld battery powered mobile applications. It operates at 1 MHz I<sup>2</sup>C-bus speeds while maintaining backward compatibility to Fast-mode (400 kHz) and Standard-mode (100 kHz).

The PCA9570 is a streamlined GPO that consists of 4-bit push-pull outputs that offer low current consumption, small packaging options and a low operating voltage range of 1.1 V to 3.6 V. The latched outputs are symmetrical 4 mA current drive capability at 3.3 V to drive various control logic. The PCA9570 output expander provides a simple solution when additional outputs are needed while keeping interconnections and floor space to a minimum, for example, in battery powered mobile applications where PCBs are crowded for interfacing to sensors, push buttons, etc.

The PCA9570 contains an internal Power-On Reset (POR) and a Software Reset feature that initializes the device to its default state.

## 2. Features and benefits

---

- 1 MHz I<sup>2</sup>C-bus interface with 6 mA SDA sink capability for lightly loaded buses (<100 pF) and improved power consumption
- Compliant with the I<sup>2</sup>C-bus Fast and Standard modes
- 1.1 V to 3.6 V operation
- Latched outputs with a sink/source capability of 4 mA at 3.3 V
- Readable device ID (manufacturer, device type, and revision)
- Software Reset
- Power-On Reset
- Low standby current
- -40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP8, XQFN8 (0.4 mm lead pitch), XQFN8 (0.5 mm lead pitch)

## 3. Applications

---

- Smart phones and tablets
- Portable medical equipment
- Portable instrumentation and test measurement



## 4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9570DP <sup>[1]</sup>	P9570	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9570GM4 <sup>[1]</sup>	70	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.20 × 1.40 × 0.50 mm	SOT1309-1
PCA9570GM	P7X <sup>[2]</sup>	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2

[1] In development. Contact your NXP sales office for availability.

[2] 'X' changes based on date code.

### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9570DP <sup>[1]</sup>	PCA9570DPJ	TSSOP8	Reel 13" Q1/T1 *Standard mark SMD	2500	T <sub>amb</sub> = -40 °C to +85 °C
PCA9570GM4 <sup>[1]</sup>	PCA9570GM4H	XQFN8	Reel 7" Q3/T4 *Standard mark	4000	T <sub>amb</sub> = -40 °C to +85 °C
PCA9570GM	PCA9570GMH	XQFN8	Reel 7" Q3/T4 *Standard mark	4000	T <sub>amb</sub> = -40 °C to +85 °C

[1] In development. Contact your NXP sales office for availability.

### 5. Block diagram

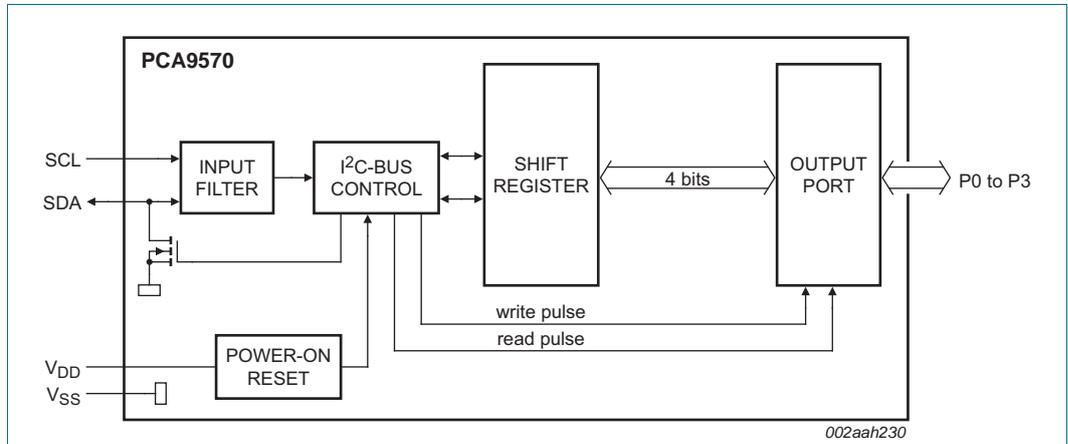


Fig 1. Block diagram of PCA9570

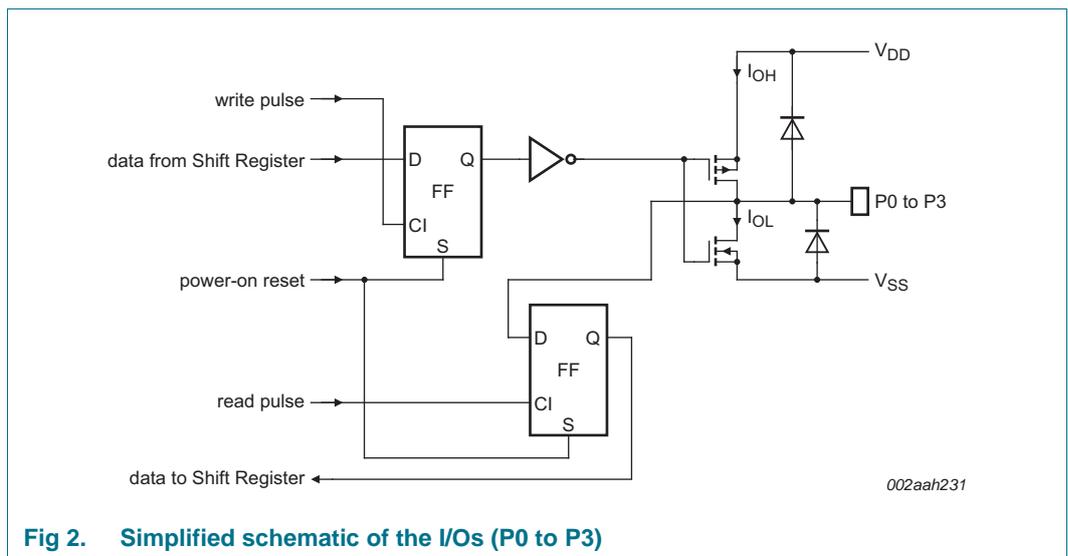
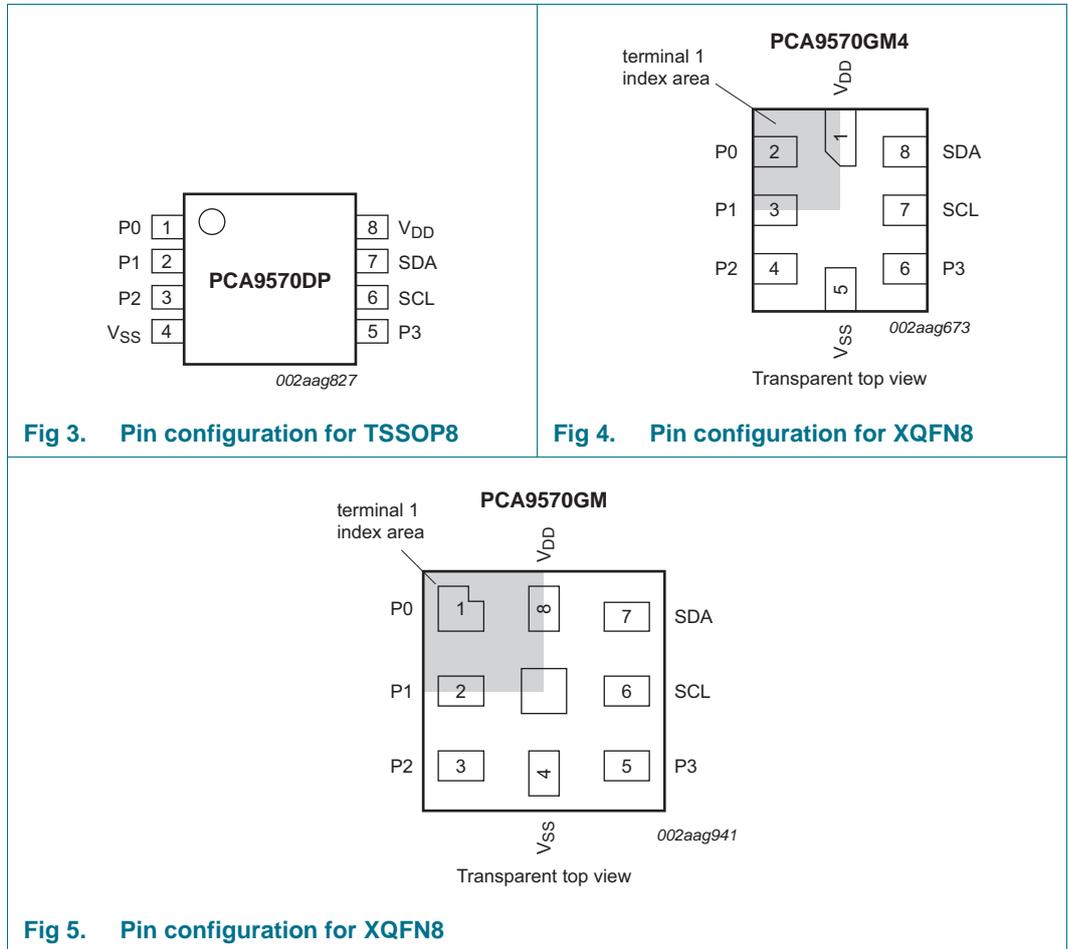


Fig 2. Simplified schematic of the I/Os (P0 to P3)

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3. Pin description

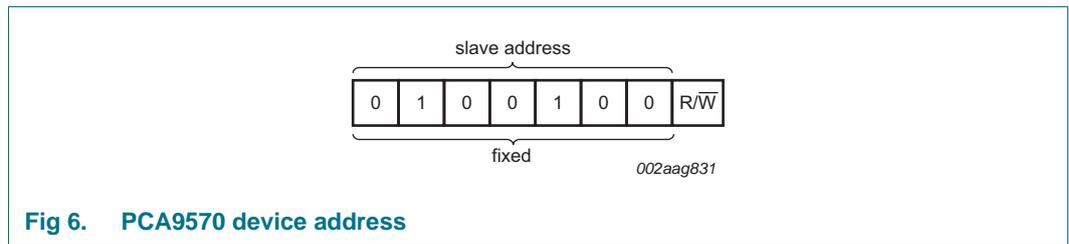
Symbol	Pin		Description
	XQFN8 (GM4)	TSSOP8, XQFN8 (GM)	
V <sub>DD</sub>	1	8	supply voltage
P0	2	1	input/output 0
P1	3	2	input/output 1
P2	4	3	input/output 2
V <sub>SS</sub>	5	4	supply ground
P3	6	5	input/output 3
SCL	7	6	serial clock line
SDA	8	7	serial data line

## 7. Functional description

Refer to [Figure 1 “Block diagram of PCA9570”](#).

### 7.1 Device address

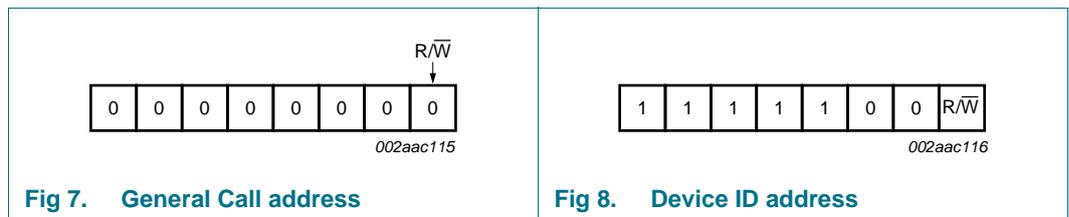
Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9570 is 48h as shown in [Figure 6](#).



### 7.2 Software Reset Call, and device ID addresses

Two other different addresses can be sent to the device.

- General Call address: allows resetting the device through the I<sup>2</sup>C-bus upon reception of the right I<sup>2</sup>C-bus sequence. See [Section 7.2.1 “Software Reset”](#) for more information.
- Device ID address: allows reading ID information from the device (manufacturer, part identification, revision). See [Section 7.2.2 “Device ID \(PCA9570 ID field\)”](#) for more information.



**7.2.1 Software Reset**

The Software Reset Call allows all the devices in the I<sup>2</sup>C-bus to be reset to the power-up state value through a specific formatted I<sup>2</sup>C-bus command. To be performed correctly, it implies that the I<sup>2</sup>C-bus is functional and that there is no device hanging the bus.

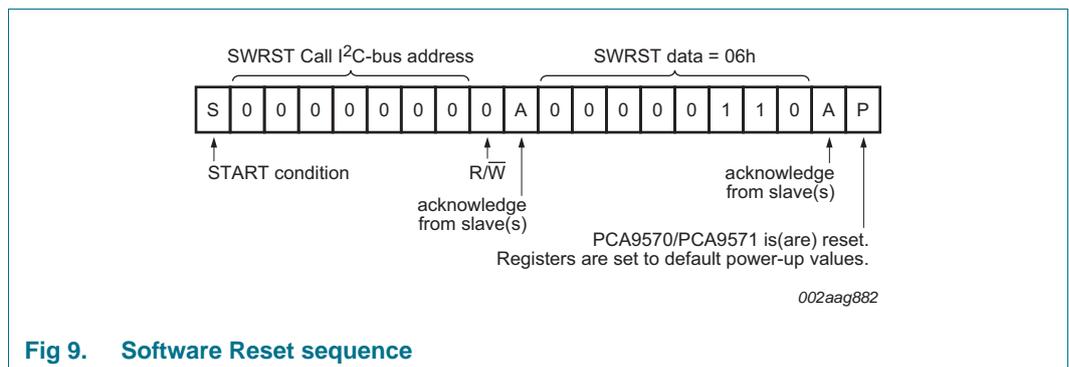
The Software Reset sequence is defined as following:

1. A START command is sent by the I<sup>2</sup>C-bus master.
2. The reserved General Call I<sup>2</sup>C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I<sup>2</sup>C-bus master.
3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I<sup>2</sup>C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
  - a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

If more than 1 byte of data is sent, the device does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I<sup>2</sup>C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in [Figure 9](#).



7.2.2 Device ID (PCA9570 ID field)

The Device ID field is a 3 byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer, the 7 MSBs with the category ID and the 6 LSBs with the feature ID (for example PCA9570 4-bit I/O expander).
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I<sup>2</sup>C-bus address followed by the R/W bit set to 0 (write): '1111 1000'.
3. The master sends the I<sup>2</sup>C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I<sup>2</sup>C-bus slave address).
4. The master sends a Re-START command.

**Remark:** A STOP command followed by a START command resets the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device resets the slave state machine and the Device ID Read cannot be performed.

5. The master sends the Reserved Device ID I<sup>2</sup>C-bus address followed by the R/W bit set to 1 (read): '1111 1001'.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

**Remark:** The reading of the Device ID can be stopped anytime by sending a NACK command.

If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCA9570, the Device ID is as shown in [Figure 10](#).

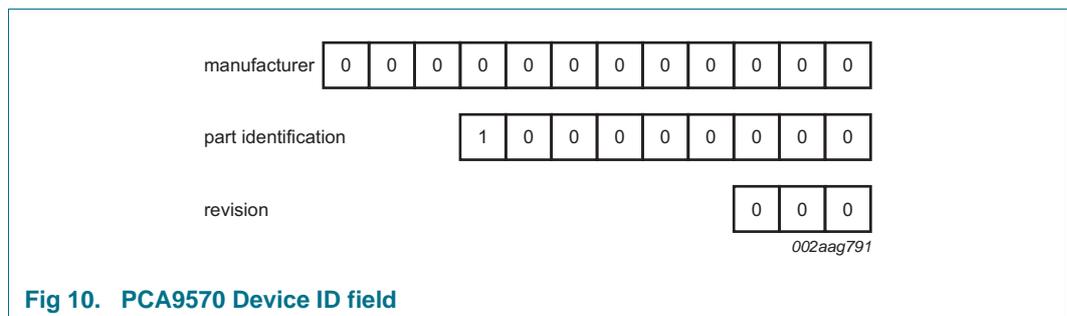
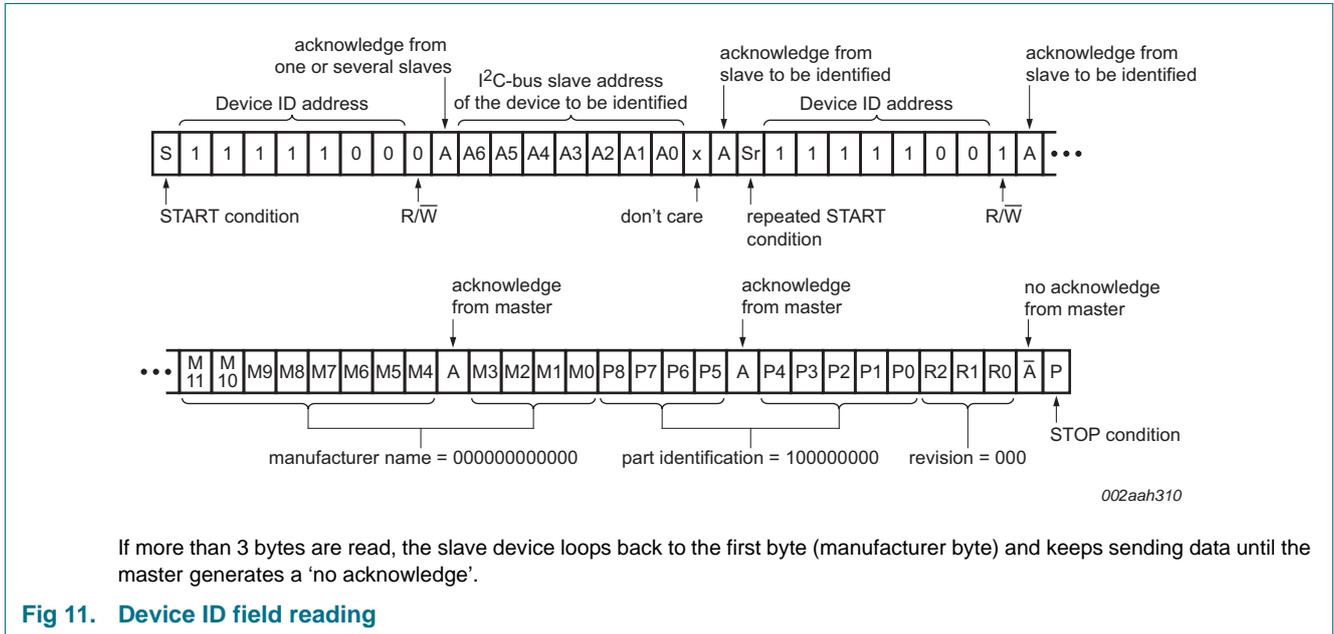


Fig 10. PCA9570 Device ID field



## 8. I/O programming

### 8.1 I/O architecture

The device ports (see [Figure 2](#)) are entirely independent and are output ports. The state of the ports at the pin is transferred from the ports to the microcontroller in the Read mode (see [Figure 13](#)). Output data is transmitted to the ports in the Write mode (see [Figure 12](#)).

At power-on all ports are HIGH. The state of the Output Port register determines if either Q1 or Q2 is on, driving the line either HIGH or LOW. A bit set to 1 in the data byte drives the line HIGH at the corresponding port. A bit set to 0 in the data byte drives the line LOW at the corresponding port.

If an external voltage is applied to an output, care should be exercised because of the low-impedance path that exists between the pin and either V<sub>DD</sub> or V<sub>SS</sub>.

### 8.2 Writing to the port (Output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0, the Write mode is entered. The device acknowledges and the master sends the data byte for P7 to P0 and is acknowledged by the device. Writes to P7 to P4 are ignored in the PCA9570 as only P3 through P0 are available. The 4-bit data is presented on the port lines after it has been acknowledged by the device. The number of data bytes that can be sent successively is not limited. The previous data is overwritten every time a data byte has been sent.

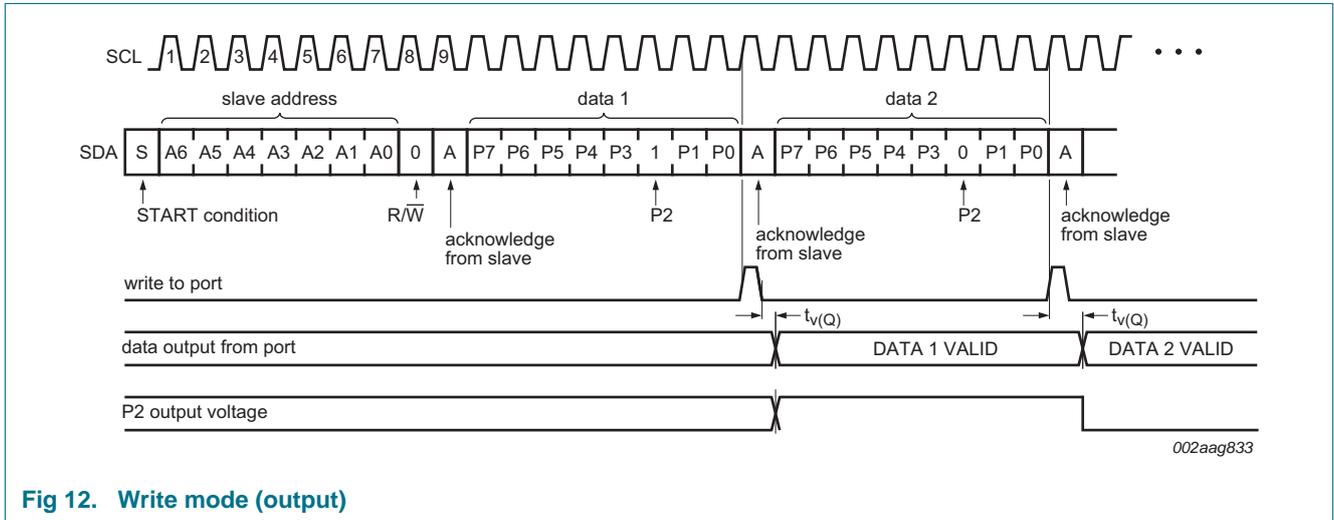


Fig 12. Write mode (output)

### 8.3 Reading from a port (Input mode)

All ports are outputs and cannot be used as inputs. When reading the device, the data returned is the port state at the pin. To read, the master (microcontroller) first addresses the slave device by setting the last bit of the byte containing the slave address to logic 1. The data byte that follows on the SDA is the value of the ports pins. There is no limit to the number of bytes read, and the state of the output port pins is updated at each acknowledge cycle. Logic 1 means that the port is HIGH. Logic 0 means that the port is LOW. When the PCA9570 is read, P7 through P4 return logic '1'.

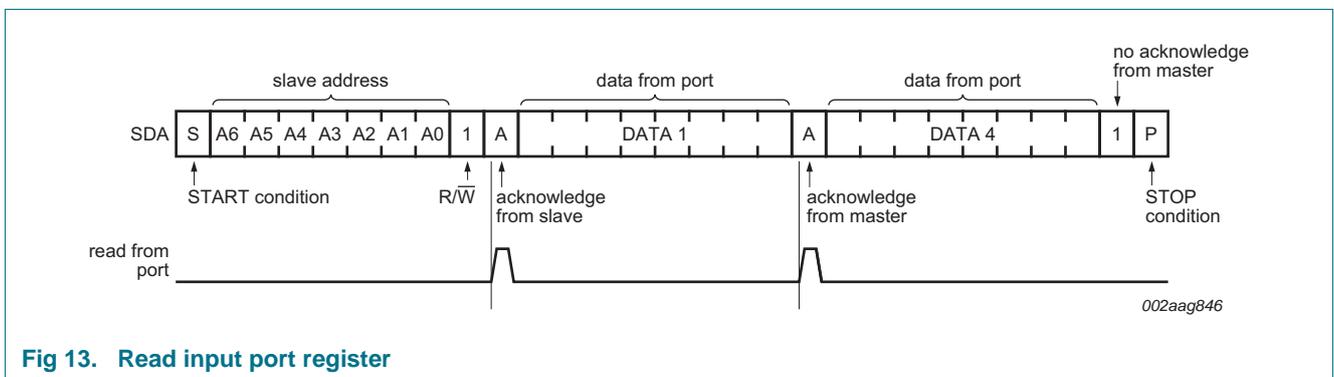


Fig 13. Read input port register

### 8.4 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the device in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the device registers and I<sup>2</sup>C-bus/SMBus state machine initialize to their default states. See [Section 14](#) for DC and AC characteristics of the POR function.

## 9. Application design-in information

### 9.1 I/O expander applications

Figure 14 shows a 4-bit output expander application. The desired HIGH or LOW logic levels are controlled by the master with speeds of up to 1 MHz on a lightly loaded bus (<100 pF). This allows the host processor to control various functions quickly and with very low overhead. The port read function of the device enables the host processor to poll the status of the output port pins. This is useful for system recovery operations or debugging.

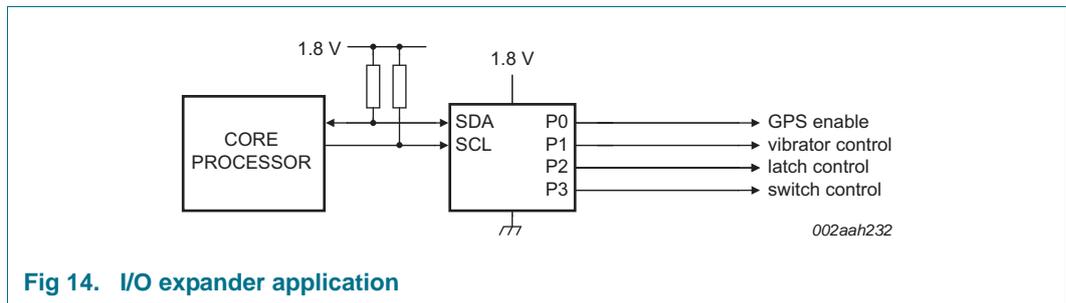


Fig 14. I/O expander application

## 10. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+4	V
V <sub>I</sub>	input voltage	SCL; SDA <a href="#">[1]</a>	-0.5	+4	V
I <sub>IK</sub>	input clamping current	SCL; V <sub>I</sub> < 0 V	-	±18	mA
I <sub>OK</sub>	output clamping current	P port; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>DD</sub>	-	±18	mA
		SDA; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>DD</sub>	-	±18	mA
I <sub>O</sub>	output current	continuous; P port	-	±25	mA
I <sub>OL</sub>	LOW-level output current	continuous; SDA; V <sub>O</sub> = 0 V to V <sub>DD</sub>	-	25	mA
I <sub>DD</sub>	supply current	continuous through V <sub>SS</sub>	-	100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		-	125	°C

[1] If the input and output current ratings are observed, the input negative-voltage and output voltage ratings may be exceeded

## 11. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Max	Unit
Z <sub>th(j-a)</sub>	transient thermal impedance from junction to ambient	TSSOP8 (SOT505-1) <a href="#">[1]</a>	88	K/W
		XQFN8 (SOT1039-1) <a href="#">[1]</a>	66	K/W
		XQFN8 (SOT902-2) <a href="#">[1]</a>	62	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

## 12. Static characteristics

**Table 6. Static characteristics**

$T_{amb} = -40\text{ °C to }+85\text{ °C}$ ;  $V_{DD} = 1.1\text{ V to }3.6\text{ V}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{IK}$	input clamping voltage	$I_I = -18\text{ mA}$	-1.2	-	-	V
$V_{DD}$	supply voltage		1.1	-	3.6	V
$V_{POR}$	power-on reset voltage	$V_I = V_{DD}\text{ or }V_{SS}$ ; $I_O = 0\text{ mA}$	-	0.7	1.0	V
$V_{OL}$	LOW-level output voltage	P port; $I_{OL} = 2\text{ mA}$ ; $V_{DD} = 1.65\text{ V}$	-	-	0.25	V
		P port; $I_{OL} = 3\text{ mA}$ ; $V_{DD} = 2.3\text{ V}$	-	-	0.25	V
		P port; $I_{OL} = 4\text{ mA}$ ; $V_{DD} = 3\text{ V}$	-	-	0.25	V
$V_{OH}$	HIGH-level output voltage	P port; $I_{OH} = 2\text{ mA}$ ; $V_{DD} = 1.65\text{ V}$	1.35	-	-	V
		P port; $I_{OH} = 3\text{ mA}$ ; $V_{DD} = 2.3\text{ V}$	2.0	-	-	V
		P port; $I_{OH} = 4\text{ mA}$ ; $V_{DD} = 3\text{ V}$	2.7	-	-	V
$I_{OL}$	LOW-level output current	SDA; $V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 2.1\text{ V to }3.6\text{ V}$	3	-	-	mA
		SDA; $V_{OL} = 0.2 \times V_{DD}$ ; $V_{DD} = 1.1\text{ V to }2.0\text{ V}$	1	-	-	mA
$V_{IH}$	HIGH-level input voltage	SCL, SDA; $V_{DD} = 1.1\text{ V to }1.2\text{ V}$	$0.8 \times V_{DD}$	-	1.2	V
		SCL, SDA; $V_{DD} = 1.2\text{ V to }3.6\text{ V}$	$0.7 \times V_{DD}$	-	3.6	V
$V_{IL}$	LOW-level input voltage	SCL, SDA; $V_{DD} = 1.1\text{ V to }1.2\text{ V}$	-0.5	-	$0.2 \times V_{DD}$	V
		SCL, SDA; $V_{DD} = 1.2\text{ V to }3.6\text{ V}$	-0.5	-	$0.3 \times V_{DD}$	V
$I_I$	input current	SCL, SDA; $V_{DD} = 1.1\text{ V to }3.6\text{ V}$ ; $V_I = V_{DD}\text{ or }V_{SS}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{DD}$	supply current	SDA, P port; $V_I$ on SDA = $V_{DD}\text{ or }V_{SS}$ ; $I_O = 0\text{ mA}$ ; $f_{SCL} = 400\text{ kHz}$				
		$V_{DD} = 2.3\text{ V to }3.6\text{ V}$	-	6.5	15	$\mu\text{A}$
		$V_{DD} = 1.1\text{ V to }2.3\text{ V}$	-	4	9	$\mu\text{A}$
		SCL, SDA, P port; $V_I$ on SCL, SDA = $V_{DD}\text{ or }V_{SS}$ ; $I_O = 0\text{ mA}$ ; $f_{SCL} = 0\text{ kHz}$				
		$V_{DD} = 2.3\text{ V to }3.6\text{ V}$	-	1	3.2	$\mu\text{A}$
		$V_{DD} = 1.1\text{ V to }2.3\text{ V}$	-	0.6	1.7	$\mu\text{A}$
		Active mode: SCL, SDA, P port; $I_O = 0\text{ mA}$ ; $f_{SCL} = 400\text{ kHz}$ ; continuous register read				
$C_i$	input capacitance	$V_I = V_{DD}\text{ or }V_{SS}$	-	6	7	pF
$C_o$	output capacitance	$V_O = V_{DD}\text{ or }V_{SS}$	-	3	5	pF
$T_{amb}$	ambient temperature	operating in free air	-40	-	+85	$^{\circ}\text{C}$

[1] The typical values are at  $V_{DD} = 2.2\text{ V}$  and  $T_{amb} = 25\text{ °C}$ .

12.1 Typical characteristics

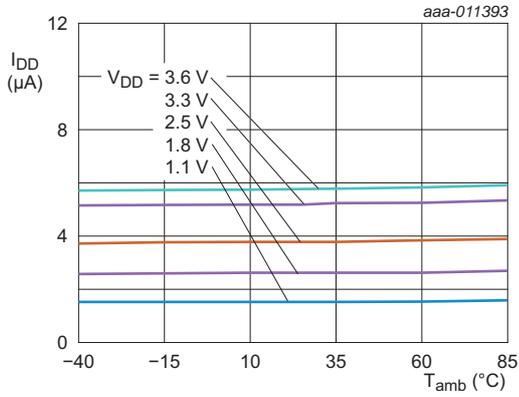


Fig 15. Supply current versus ambient temperature

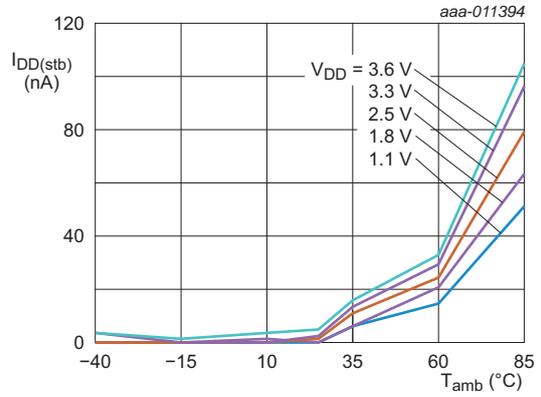
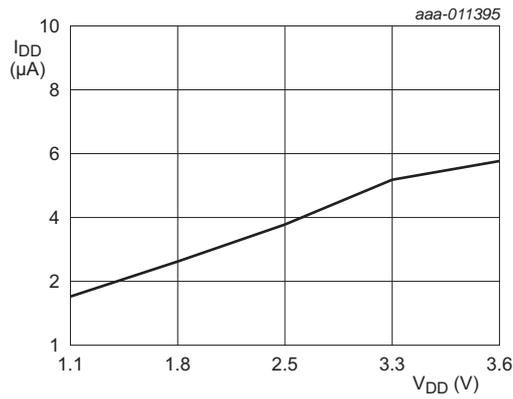
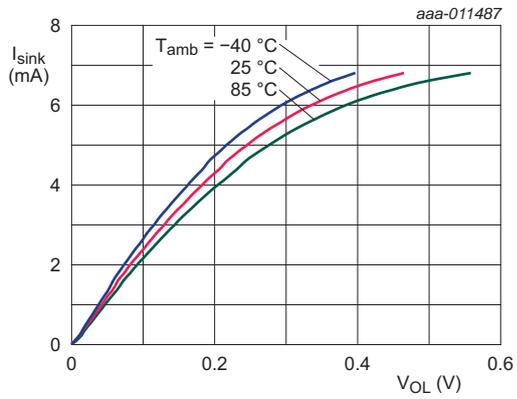


Fig 16. Standby supply current versus ambient temperature

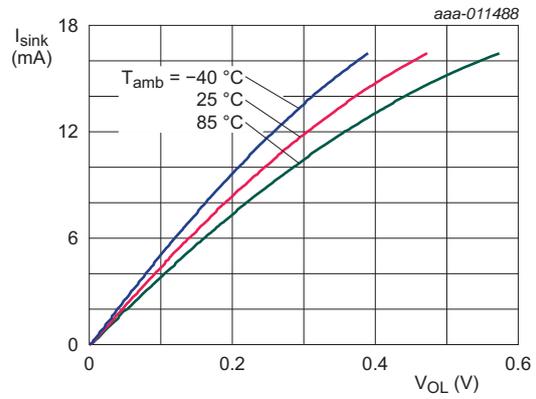


$T_{amb} = 25$  °C

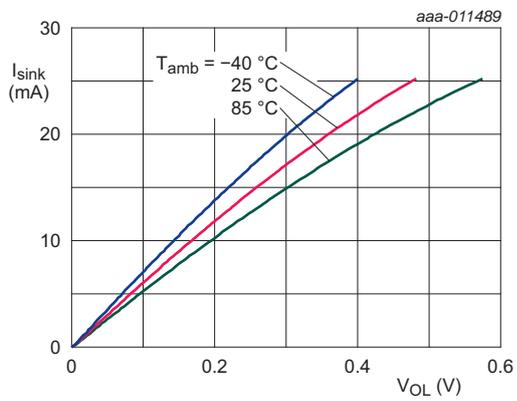
Fig 17. Supply current versus supply voltage



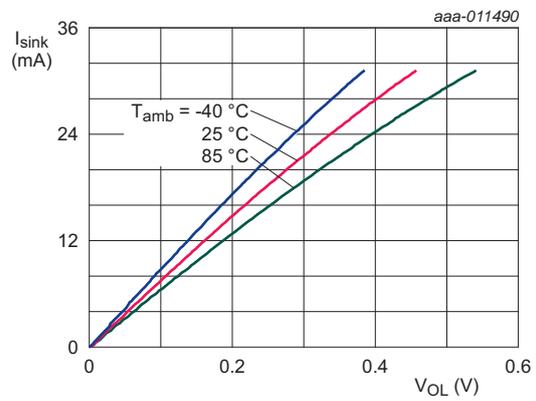
a.  $V_{DD} = 1.2\text{ V}$



b.  $V_{DD} = 1.8\text{ V}$

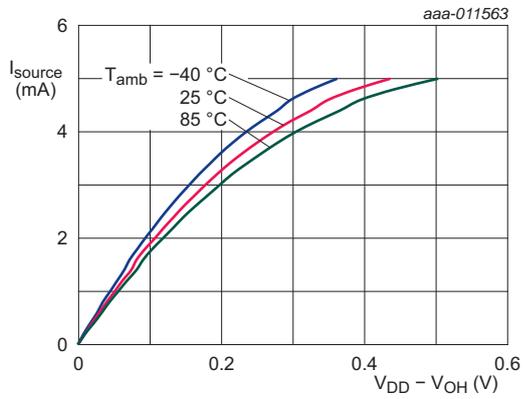


c.  $V_{DD} = 2.5\text{ V}$

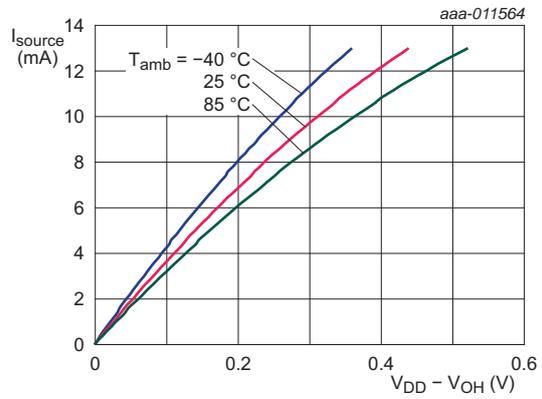


d.  $V_{DD} = 3.3\text{ V}$

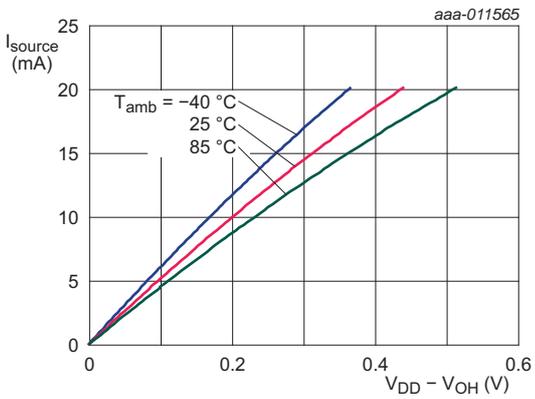
**Fig 18. I/O sink current versus LOW-level output voltage**



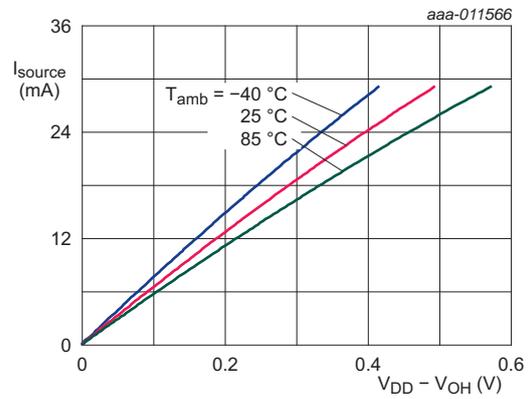
a.  $V_{DD} = 1.2\text{ V}$



b.  $V_{DD} = 1.8\text{ V}$

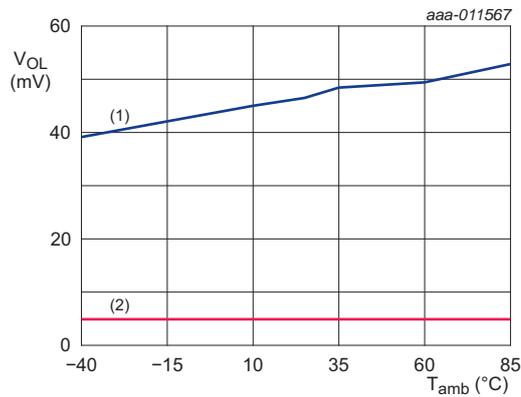


c.  $V_{DD} = 2.5\text{ V}$



d.  $V_{DD} = 3.3\text{ V}$

**Fig 19. I/O source current versus HIGH-level output voltage**



- (1)  $V_{DD} = 1.8\text{ V}; I_{\text{sink}} = 2\text{ mA}$
- (2)  $V_{DD} = 1.8\text{ V}; I_{\text{sink}} = 100\text{ }\mu\text{A}$

**Fig 20. LOW-level output voltage versus temperature**

### 13. Dynamic characteristics

**Table 7. Dynamic characteristics**
 $V_{DD} = 1.1\text{ V to }3.6\text{ V}; V_{SS} = 0\text{ V}; T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C};$  unless otherwise specified.

Symbol	Parameter	Conditions	Standard mode I <sup>2</sup> C-bus		Fast mode I <sup>2</sup> C-bus		1 MHz I <sup>2</sup> C-bus <sup>[1]</sup>		Unit
			Min	Max	Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	0	1000	kHz
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	μs
t <sub>HD,STA</sub>	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	μs
t <sub>SU,STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	μs
t <sub>SU,STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	μs
t <sub>HD,DAT</sub>	data hold time		0	-	0	-	0	-	ns
t <sub>VD,ACK</sub>	data valid acknowledge time	[2]	-	3.45	-	0.9	-	0.45	μs
t <sub>VD,DAT</sub>	data valid time	[3]	-	3.45	-	0.9	-	0.45	μs
t <sub>SU,DAT</sub>	data set-up time		250	-	100	-	50	-	ns
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	μs
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	20 × (V <sub>DD</sub> / 5.5 V)	300	20 × (V <sub>DD</sub> / 5.5 V)	120	ns
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	20	300	-	120	ns
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter	[4]	-	50	-	50	-	50	ns
<b>Port timing</b>									
t <sub>V(Q)</sub>	data output valid time		-	200	-	200	-	200	ns

[1] Fm+ mode on a non-standard, lightly loaded bus (<100 pF).

[2] t<sub>VD,ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[3] t<sub>VD,DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.

[4] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

### 14. Power-on reset requirements

In the event of a glitch or data corruption, the device can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

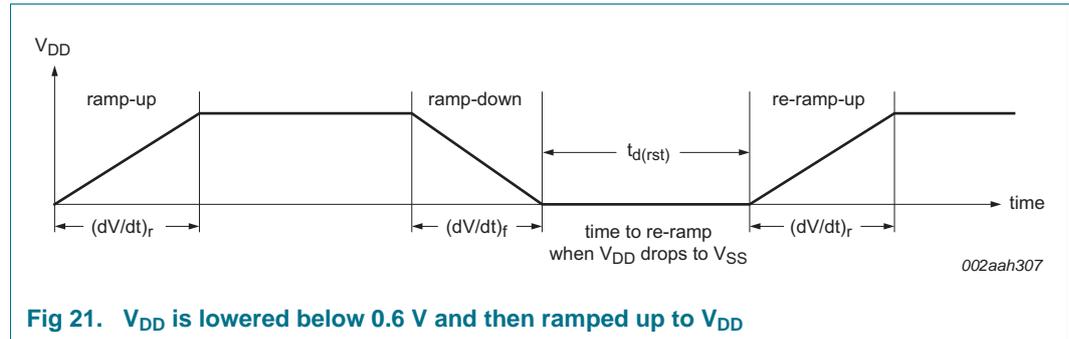


Fig 21. V<sub>DD</sub> is lowered below 0.6 V and then ramped up to V<sub>DD</sub>

Table 8. Recommended supply sequencing and ramp rates

T<sub>amb</sub> = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
(dV/dt) <sub>f</sub>	fall rate of change of voltage	Figure 21	0.1	-	2000	ms
(dV/dt) <sub>r</sub>	rise rate of change of voltage	Figure 21	0.1	-	2000	ms
t <sub>d(rst)</sub>	reset delay time	Figure 21; when V <sub>DD</sub> drops to V <sub>SS</sub>	1	-	-	μs
ΔV <sub>DD(gl)</sub>	glitch supply voltage difference	Figure 22 [1]				
		V <sub>DD</sub> = 2.1 V to 3.6 V	-	-	1.2	V
		V <sub>DD</sub> = 1.1 V to 2.1 V	-	-	V <sub>DD</sub> - 0.9	V
t <sub>w(gl)VDD</sub>	supply voltage glitch pulse width	Figure 22 [2]	-	-	10	μs
V <sub>POR(trip)</sub>	power-on reset trip voltage	rising V <sub>DD</sub>	-	0.7	1.0	V

[1] Level that V<sub>DD</sub> can glitch down to with a ramp rate of 0.4 μs/V, but not cause a functional disruption when t<sub>gw(VDD)</sub> = 1 μs.

[2] Glitch width that does not cause a functional disruption when V<sub>DD</sub> = 1.8 V to 3.6 V, ΔV<sub>DD(gl)</sub> = 0.5 × V<sub>DD</sub>; V<sub>DD</sub> = 1.1 V to 1.8 V, ΔV<sub>DD(gl)</sub> = V<sub>DD</sub> - 0.9 V.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t<sub>w(gl)VDD</sub>) and glitch height (ΔV<sub>DD(gl)</sub>) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 22 and Table 8 provide more information on how to measure these specifications.

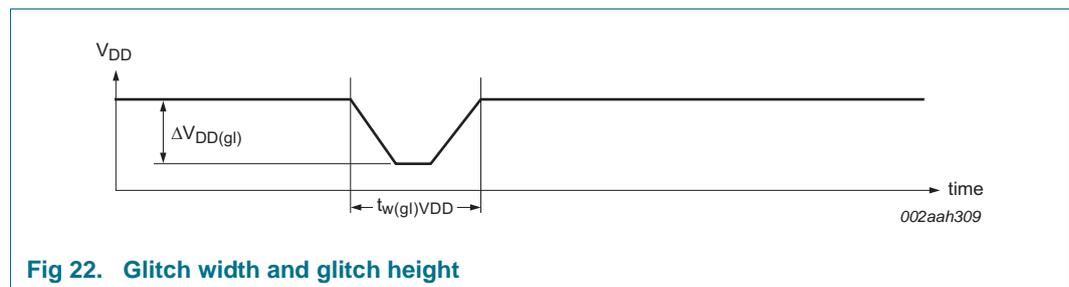
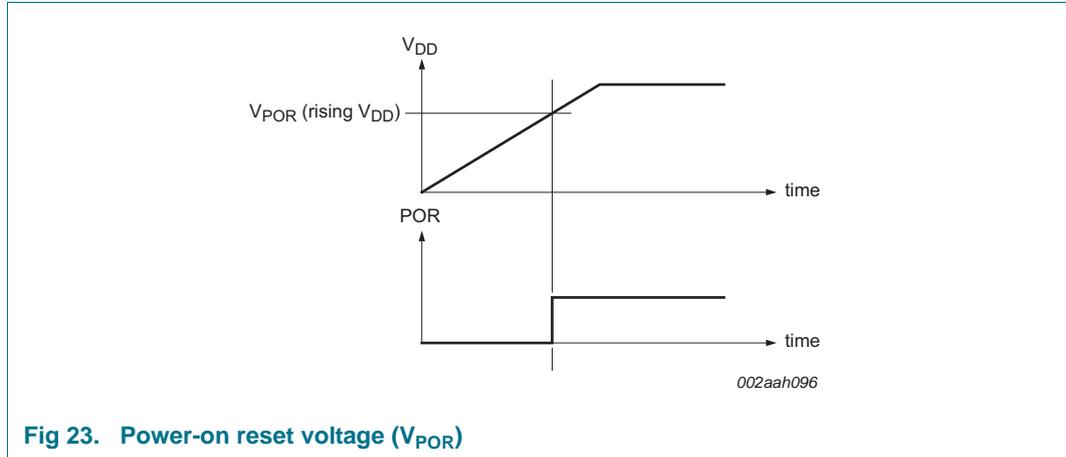


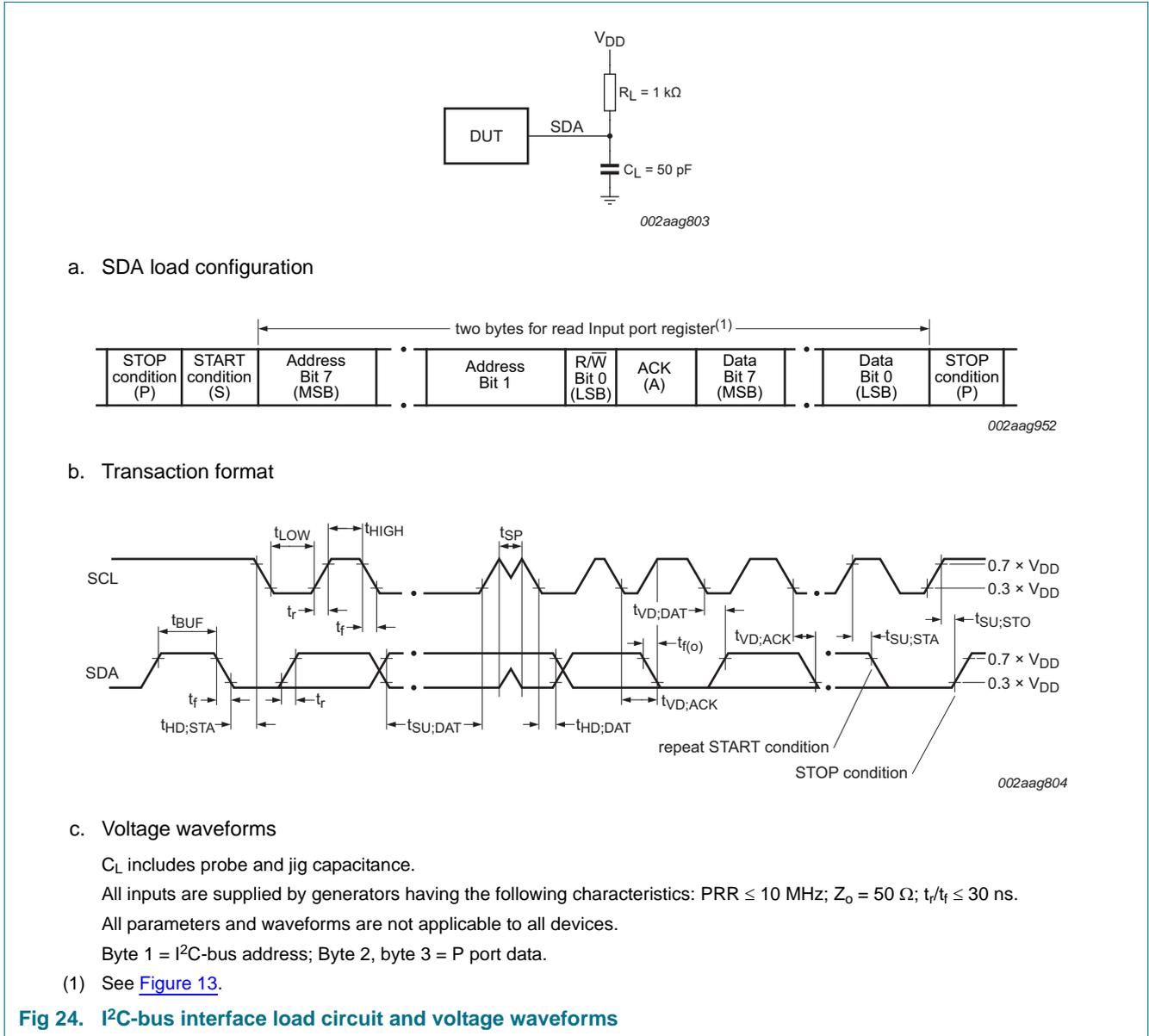
Fig 22. Glitch width and glitch height

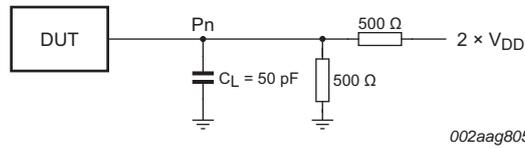
V<sub>POR</sub> is critical to the power-on reset. V<sub>POR</sub> is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C-bus/SMBus state machine are initialized to their default states. [Figure 23](#) and [Table 8](#) provide more details on this specification.



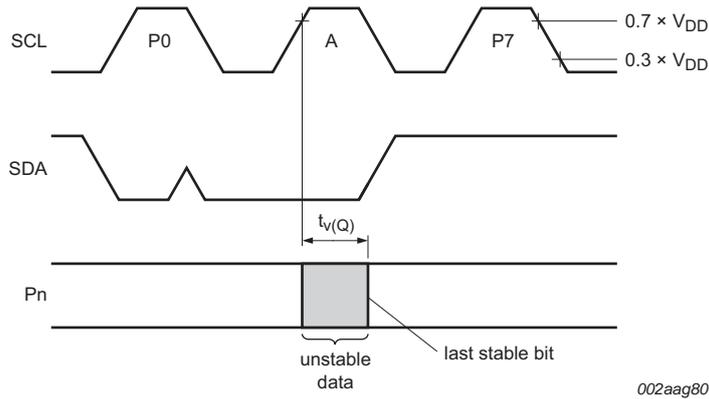
**Fig 23. Power-on reset voltage (V<sub>POR</sub>)**

15. Parameter measurement information

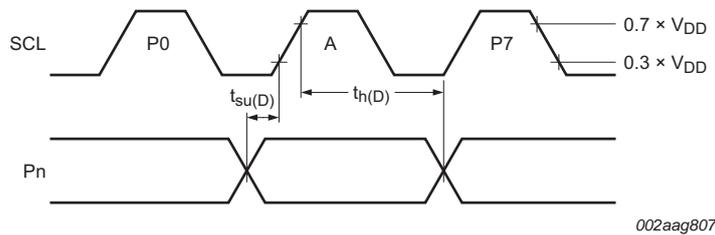




a. P port load configuration



b. Write mode ( $\overline{R/\overline{W}} = 0$ )



c. Read mode ( $\overline{R/\overline{W}} = 1$ )

$C_L$  includes probe and jig capacitance.

$t_{V(Q)}$  is measured from  $0.7 \times V_{DD}$  on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz;  $Z_o = 50 \Omega$ ;  $t_r/t_f \leq 30$  ns.

The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig 25. P port load circuit and voltage waveforms

16. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

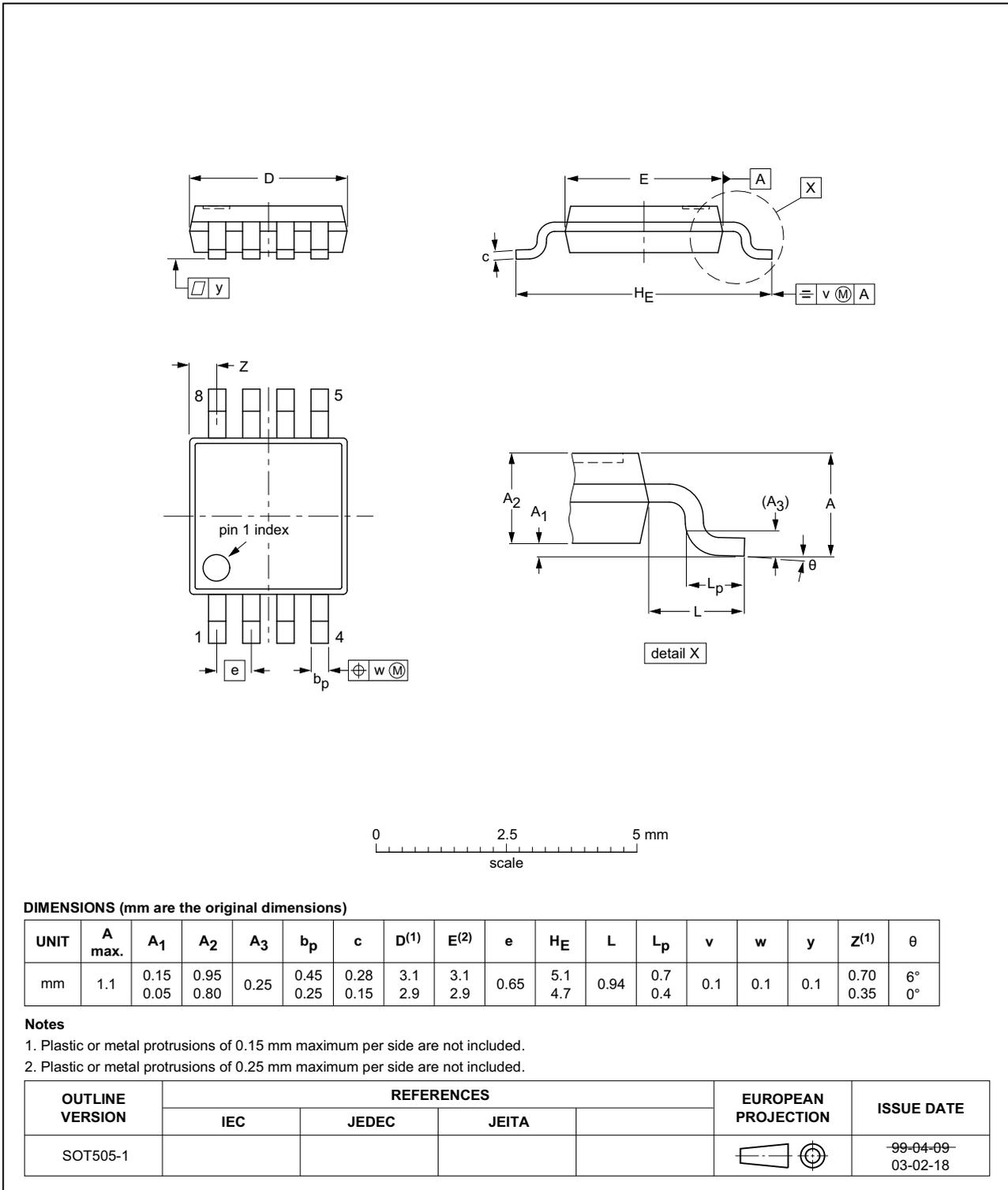


Fig 26. Package outline SOT505-1 (TSSOP8)

XQFN8: plastic, extremely thin quad flat package; no leads;  
8 terminals; body 1.4 x 1.2 x 0.5 mm

SOT1309-1

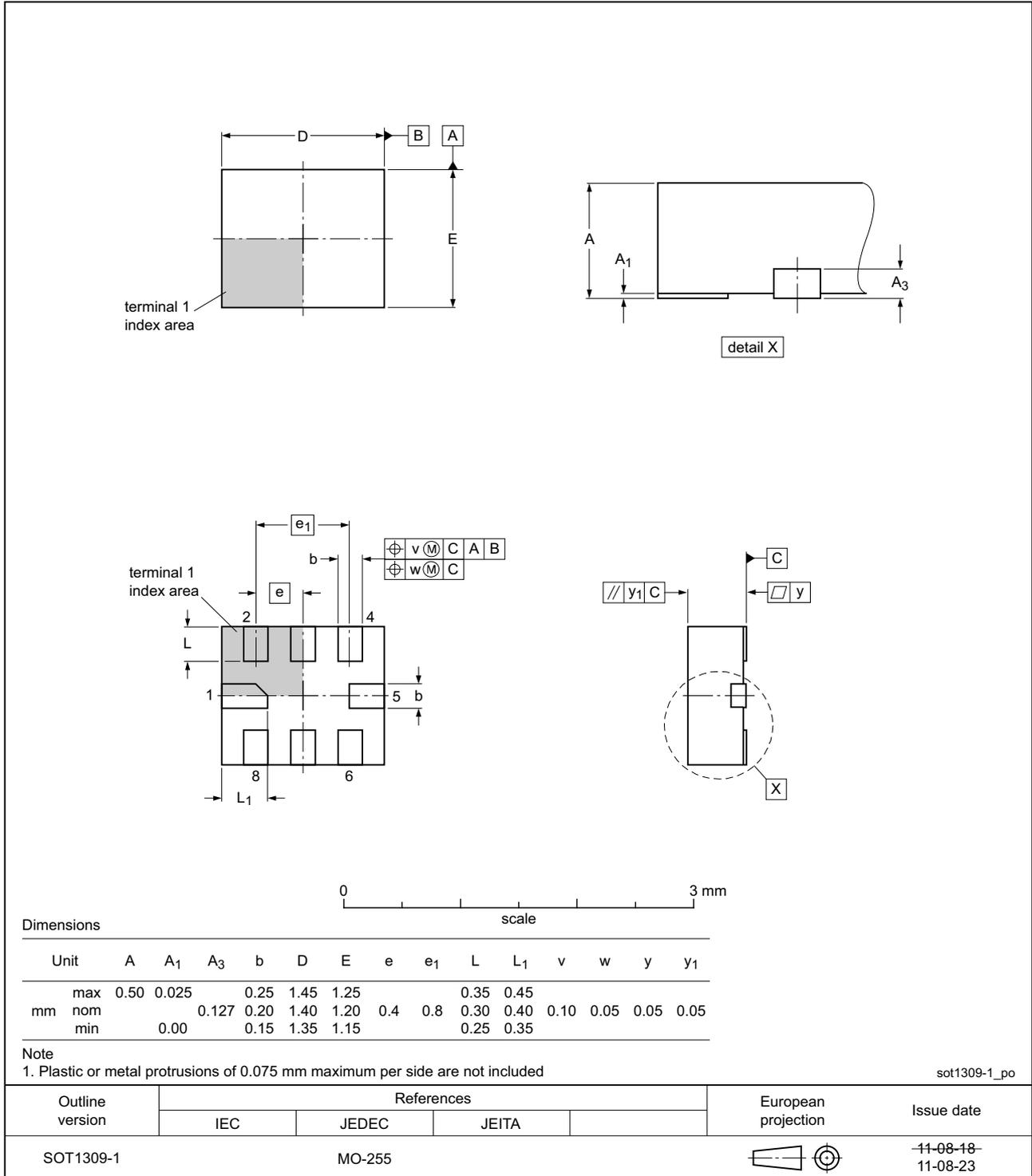


Fig 27. Package outline SOT1309-1 (XQFN8)

**XQFN8: plastic, extremely thin quad flat package; no leads;**  
**8 terminals; body 1.6 x 1.6 x 0.5 mm**

SOT902-2

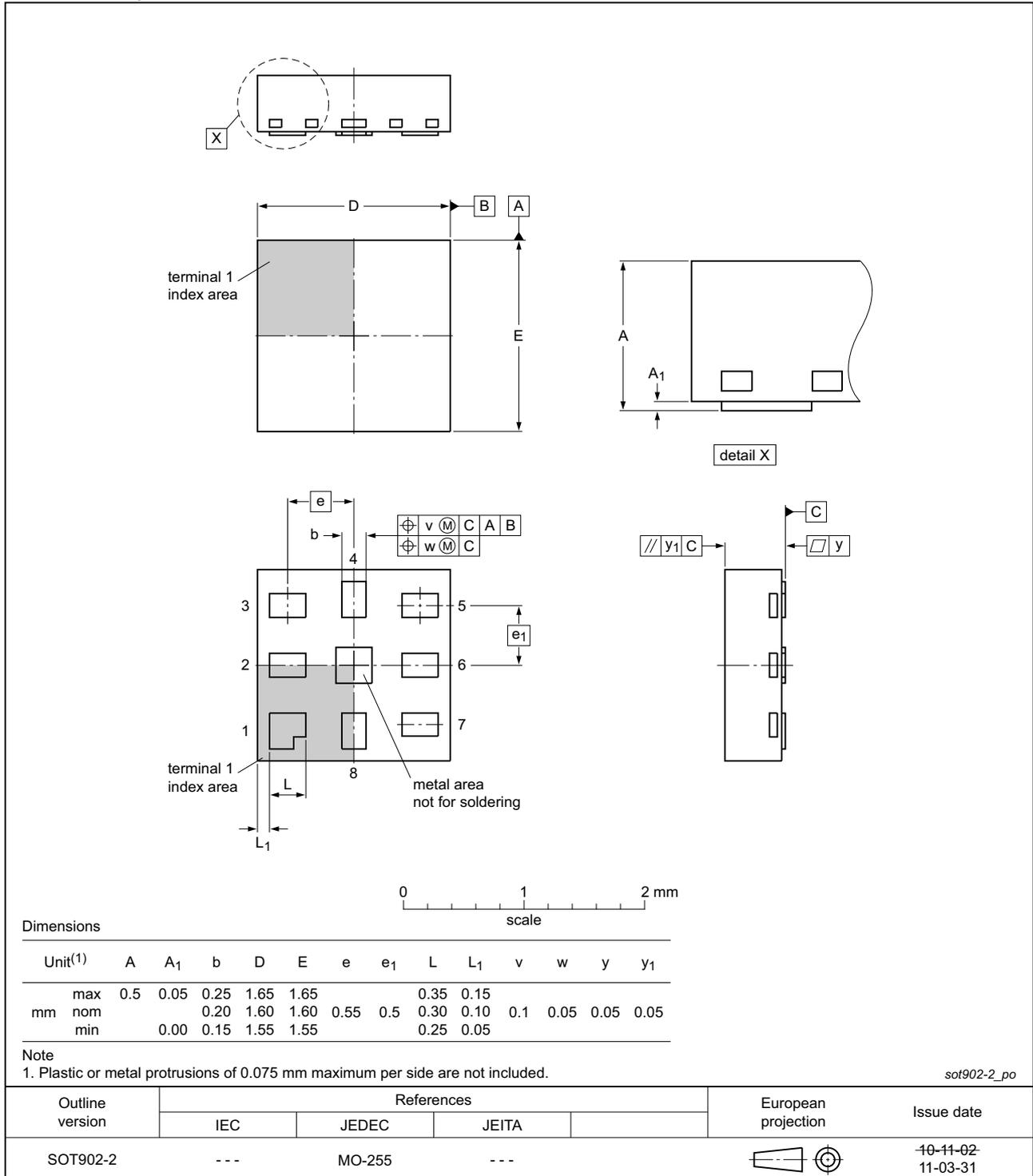


Fig 28. Package outline SOT902-2 (XQFN8)

## 17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

**18.4 Reflow soldering**

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 29](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 9](#) and [10](#)

**Table 9. SnPb eutectic process (from J-STD-020D)**

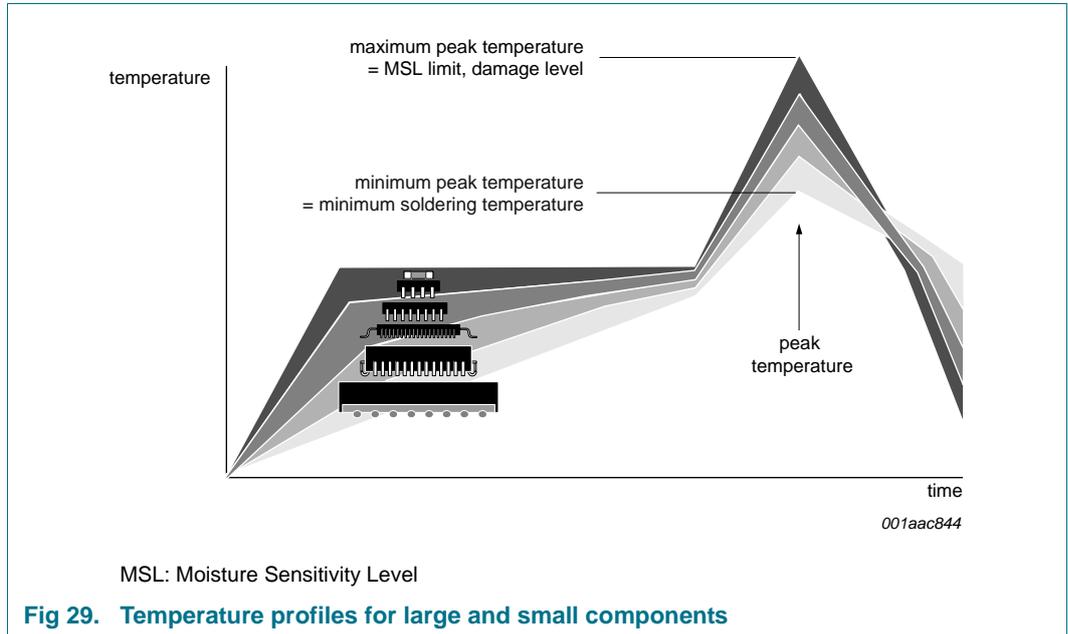
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 10. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

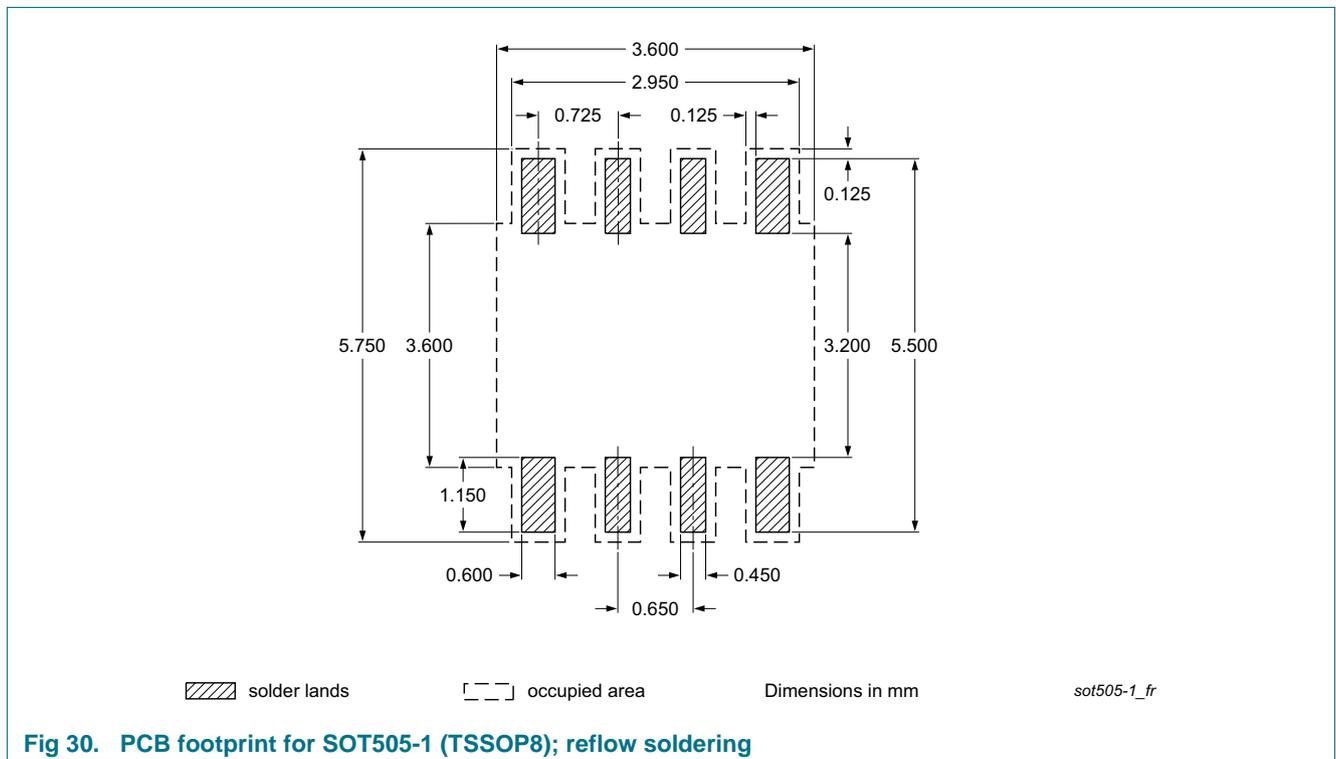
Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 29](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 19. Soldering: PCB footprints



Footprint information for reflow soldering of SOT1309 package

SOT1309-1

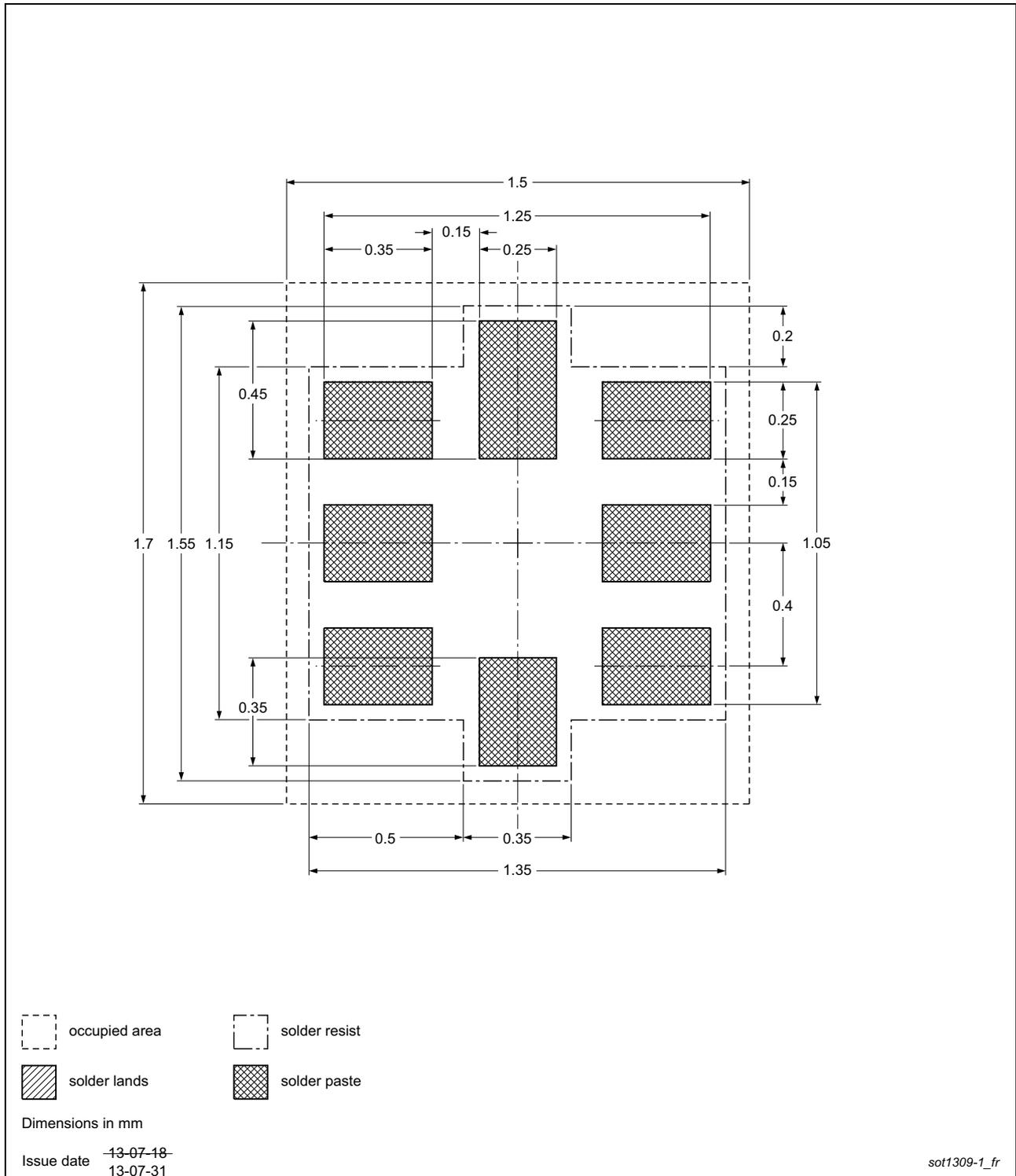


Fig 31. PCB footprint for SOT1309-1 (XQFN8); reflow soldering

Footprint information for reflow soldering of XQFN8 package

SOT902-2

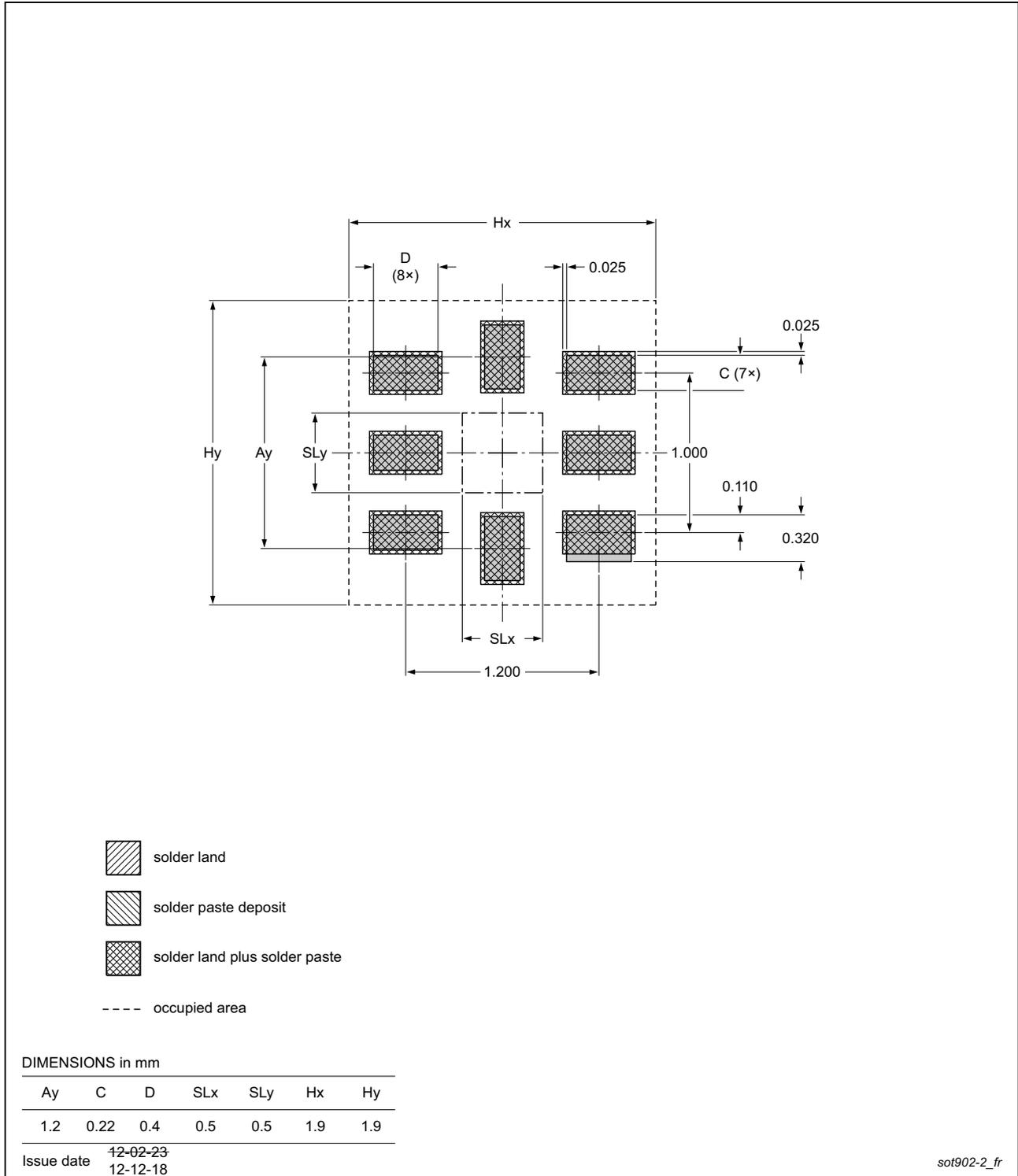


Fig 32. PCB footprint for SOT902-2 (XQFN8); reflow soldering

## 20. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
FM	Frequency Modulation
GPIO	General Purpose Input/Output
GPS	Global Positioning Satellite
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
IC	Integrated Circuit
ID	Identification
LED	Light Emitting Diode
LSB	Least Significant Bit
MP3	MPEG audio layer 3
MSB	Most Significant Bit
SMBus	System Management Bus

## 21. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9570 v.4	20140917	Product data sheet	-	PCA9570 v.3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 1 “Ordering information”</a>: Added table note <a href="#">[1]</a>.</li> <li>• <a href="#">Table 2 “Ordering options”</a>: Added table note <a href="#">[1]</a>.</li> <li>• <a href="#">Table 4 “Limiting values”</a>, I<sub>DD</sub>; changed max from “200” to “100”.</li> <li>• <a href="#">Section 14 “Power-on reset requirements”</a>: Deleted paragraphs 2 and 3; deleted Fig 22.</li> <li>• <a href="#">Table 8 “Recommended supply sequencing and ramp rates”</a>: <ul style="list-style-type: none"> <li>– t<sub>d(rst)</sub>: Deleted 2nd row</li> <li>– ΔV<sub>DD(g)</sub>: Changed V<sub>DD</sub> condition from “1.8 V” to “2.1 V”</li> </ul> </li> </ul>			
PCA9570 v.3	20140515	Product data sheet	-	PCA9570 v.2
PCA9570 v.2	20140204	Product data sheet	-	PCA9570 v.1
PCA9570 v.1	20130910	Product data sheet	-	-

## 22. Legal information

### 22.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 22.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 22.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 22.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP Semiconductors N.V.

## 23. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 24. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>	<b>23</b>	<b>Contact information</b> .....	<b>31</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>	<b>24</b>	<b>Contents</b> .....	<b>32</b>
<b>3</b>	<b>Applications</b> .....	<b>1</b>			
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>			
4.1	Ordering options .....	2			
<b>5</b>	<b>Block diagram</b> .....	<b>3</b>			
<b>6</b>	<b>Pinning information</b> .....	<b>4</b>			
6.1	Pinning .....	4			
6.2	Pin description .....	4			
<b>7</b>	<b>Functional description</b> .....	<b>5</b>			
7.1	Device address .....	5			
7.2	Software Reset Call, and device ID addresses	5			
7.2.1	Software Reset .....	6			
7.2.2	Device ID (PCA9570 ID field) .....	7			
<b>8</b>	<b>I/O programming</b> .....	<b>8</b>			
8.1	I/O architecture .....	8			
8.2	Writing to the port (Output mode) .....	8			
8.3	Reading from a port (Input mode) .....	9			
8.4	Power-on reset .....	9			
<b>9</b>	<b>Application design-in information</b> .....	<b>10</b>			
9.1	I/O expander applications .....	10			
<b>10</b>	<b>Limiting values</b> .....	<b>11</b>			
<b>11</b>	<b>Thermal characteristics</b> .....	<b>11</b>			
<b>12</b>	<b>Static characteristics</b> .....	<b>12</b>			
12.1	Typical characteristics .....	13			
<b>13</b>	<b>Dynamic characteristics</b> .....	<b>16</b>			
<b>14</b>	<b>Power-on reset requirements</b> .....	<b>17</b>			
<b>15</b>	<b>Parameter measurement information</b> .....	<b>19</b>			
<b>16</b>	<b>Package outline</b> .....	<b>21</b>			
<b>17</b>	<b>Handling information</b> .....	<b>24</b>			
<b>18</b>	<b>Soldering of SMD packages</b> .....	<b>24</b>			
18.1	Introduction to soldering .....	24			
18.2	Wave and reflow soldering .....	24			
18.3	Wave soldering .....	24			
18.4	Reflow soldering .....	25			
<b>19</b>	<b>Soldering: PCB footprints</b> .....	<b>26</b>			
<b>20</b>	<b>Abbreviations</b> .....	<b>29</b>			
<b>21</b>	<b>Revision history</b> .....	<b>29</b>			
<b>22</b>	<b>Legal information</b> .....	<b>30</b>			
22.1	Data sheet status .....	30			
22.2	Definitions .....	30			
22.3	Disclaimers .....	30			
22.4	Trademarks .....	31			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2014.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 17 September 2014

Document identifier: PCA9570