

TIC206A, TIC206B, TIC206D, TIC206M, TIC206N, TIC206S

SILICON BIDIRECTIONAL TRIODE THYRISTOR

- 4 A RMS
- Glass Passivated Wafer
- 100 V to 800 V Off-State Voltage
- Max I_{GT} of 5 mA (Quadrants 1-3)
- Sensitive gate triacs
- Compliance to ROHS

DESCRIPTION

This device is a bidirectional triode thyristor (triac) which may be triggered from the off-state to the on-state by either polarity of gate signal with main Terminal 2 at either polarity.

ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings	Value						Unit
		A	B	D	M	S	N	
V_{DRM}	Repetitive peak off-state voltage (see Note1)	100	200	400	600	700	800	V
$I_{T(RMS)}$	Full-cycle RMS on-state current at (or below) 70°C case temperature (see note2)	4						A
I_{TSM}	Peak on-state surge current full-sine-wave (see Note3)	25						A
I_{TSM}	Peak on-state surge current half-sine-wave (see Note4)	30						A
I_{GM}	Peak gate current	± 0.2						A
P_{GM}	Peak gate power dissipation at (or below) 85°C case temperature (pulse width $\leq 200 \mu s$)	1.3						W
$P_{G(AV)}$	Average gate power dissipation at (or below) 85°C case (see Note5)	0.3						W
T_C	Operating case temperature range	-40 to +110						°C
T_{stg}	Storage temperature range	-40 to +125						°C
T_L	Lead temperature 1.6 mm from case for 10 seconds	230						°C

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THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
$R_{\theta JC}$	Junction to case thermal resistance	≤ 7.8	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Junction to free air thermal resistance	≤ 62.5	

ELECTRICAL CHARACTERISTICS

TC=25°C unless otherwise noted

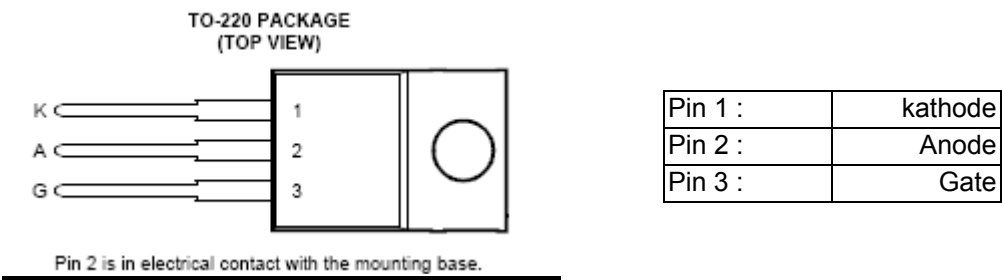
Symbol	Ratings	Test Condition(s)	Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = \text{Rated } V_{\text{DRM}}, I_G = 0$ $T_C = 110^{\circ}\text{C}$	-	-	± 1	mA
I_{GT}	Gate trigger current	$V_{\text{supply}} = +12 \text{ V}\dagger, R_L = 10 \Omega, t_{p(g)} = > 20 \mu\text{s}$	-	0.5	5	mA
		$V_{\text{supply}} = +12 \text{ V}\dagger, R_L = 10 \Omega, t_{p(g)} = > 20 \mu\text{s}$	-	-1.5	-5	
		$V_{\text{supply}} = -12 \text{ V}\dagger, R_L = 10 \Omega, t_{p(g)} = > 20 \mu\text{s}$	-	-2	-5	
		$V_{\text{supply}} = -12 \text{ V}\dagger, R_L = 10 \Omega, t_{p(g)} = > 20 \mu\text{s}$	-	3.6	10	
V_{GT}	Gate trigger voltage	$V_{\text{supply}} = +12 \text{ V}\dagger, R_L = 10 \Omega, t_{p(g)} = > 20 \mu\text{s}$	-	0.7	2	V
		$V_{\text{supply}} = +12 \text{ V}\dagger, R_L = 10 \Omega, t_{p(g)} = > 20 \mu\text{s}$	-	-0.7	-2	
		$V_{\text{supply}} = -12 \text{ V}\dagger, R_L = 10 \Omega, t_{p(g)} = > 20 \mu\text{s}$	-	-0.8	-2	
		$V_{\text{supply}} = -12 \text{ V}\dagger, R_L = 10 \Omega, t_{p(g)} = > 20 \mu\text{s}$	-	0.8	2	
I_{H}	Holding current	$V_{\text{supply}} = +12 \text{ V}\dagger, I_G = 0$ initiating $I_{\text{TM}} = 100 \text{ mA}$	-	2	15	mA
		$V_{\text{supply}} = -12 \text{ V}\dagger, I_G = 0$ initiating $I_{\text{TM}} = -100 \text{ mA}$	-	-4	-15	
I_{L}	Latching current	$V_{\text{supply}} = +12 \text{ V}\dagger$ (see Note 7)	-	-	30	mA
		$V_{\text{supply}} = -12 \text{ V}\dagger$ (see Note 7)	-	-	-30	
V_{TM}	Peak on-state voltage	$I_{\text{TM}} = \pm 4.2 \text{ A}, I_G = 50 \text{ mA}$ (see Note 6)	-	± 1.3	± 2.2	V
dv/dt	Critical rate of rise of off-state voltage	$V_{\text{DRM}} = \text{Rated } V_{\text{DRM}}, I_G = 0$ $T_C = 110^{\circ}\text{C}$	-	± 50	-	V/ μs
dv/dt_{c}	Critical rise of communication voltage	$V_{\text{DRM}} = \text{Rated } V_{\text{DRM}}, I_{\text{TRM}} = \pm 4.2 \text{ A}$ $T_C = 85^{\circ}\text{C}$	± 1	± 1.3	± 2.5	

$\dagger$ All voltages are with respect to Main Terminal 1.



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PINNING



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