

VFJA400

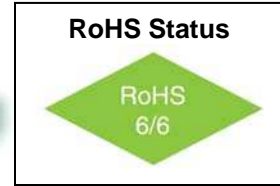
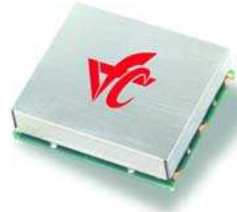
Quad Input to 200MHz

Jitter Attenuator w/ F_{OUT} to 200MHz



Features

- 10MHz to 200MHz Output Frequency Range
- 8KHz to 200MHz Input Frequency Range
- Ultra Low Jitter and Phase Noise: -130 dBc/Hz @ 1KHz
- Low Power: < 150mW typical

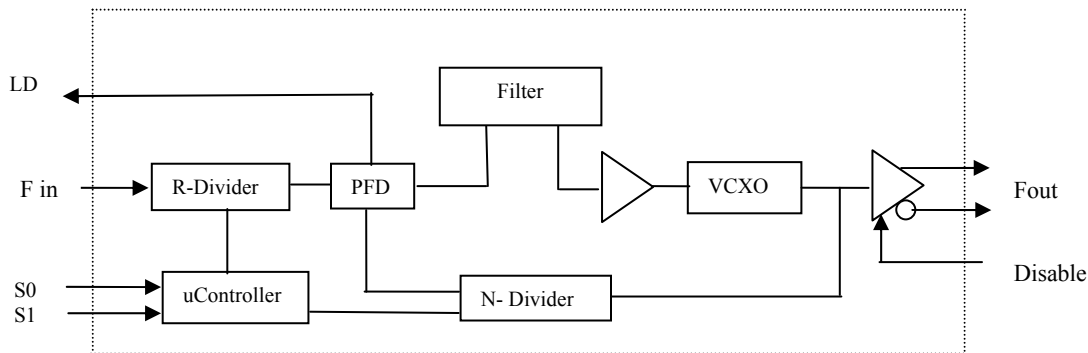


Applications

- Sonet / SDH / ATM
- 10 Gigabit Ethernet
- Wireless Infrastructure

Description

The VFJA400 is a Jitter Attenuator capable of providing an output frequency up to 200MHz. Two select inputs [S1,S0] allow the user to select 1 of 4 preset input frequencies. A Lock Detect signal indicates when the output signal is frequency locked to the input. Operating with a +3.3 volt power supply the device typically consumes 150mW. The output is configured as a differential LVPECL signal and requires external termination resistors. The VFJA400 is available in a 19.5mm x 15.5mm surface mount package.



Block Diagram

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Break Down Voltage	V _{cc}		-0.5		5.5	V	
Storage Temperature	T _s		-55		+105°	°C	

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note	
Output Frequency Range	F _{out}		10		200	MHz	See Table 2	
Input Frequency Range	F _{in}	2.5 V / ns (min) Rising edge triggered	0.008		200	MHz	See Table 2	
Input Level	V _{in}	AC coupled internally	0.4		3.3	V p-p		
Output Level Logic "1"	V _{oh}	50 Ohm to V _{cc} -2V or Thevenin Equivalent	V _{cc} -0.96		V _{cc} -0.81	V		
Output Level Logic "0"	V _{ol}		V _{cc} -1.85		V _{cc} -1.65	V		
Phase Jitter		12KHz to 20MHz		0.20	0.5	ps(rms)		
SSB Phase Noise	Φ _n	100Hz 1KHz 10KHz 100KHz		-100 -130 -145 -150		dBc/Hz	@ 155.52MHz	
APR			± 32			ppm		
Modulation BW			10			Hz	Note 1	
Duty Cycle		@ 50%	45	50	55	%		
Rise / Fall Time	Tr/Tf	20% to 80%			0.6	ns		
Start up time				3		s		
Supply Voltage	V _{cc}		3.15	3.30	3.45	V		
Input Current	I _{cc}			45	55	mA		
Operating Temperature Range	T _a		-40°		+85°	°C		
Lock Detect	LD	Output HIGH (> 2.5 V) : In Lock; Output LOW (< .5V): Out of Lock						LVC MOS
Enable / Disable Function		Input HIGH (>2.5V): Output Disabled Input LOW (<0.5V) or floating: Output Enabled						LVC MOS
Enable / Disable Time	Te/Td				100	ns		

Notes:

1. Consult factory for Bandwidth options

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How to Order

VFJA400 — Suffix

Standard Frequencies **Table 2**

P/N suffix	S1:S0	Input Frequency (MHz)	Output Frequency (MHz)	P/N suffix	S1:S0	Input Frequency (MHz)	Output Frequency (MHz)
-001	00	0.008	25.00	-002	00	0.008	125.00
	01	19.44	25.00		01	19.44	125.00
	10	25	25.00		10	25	125.00
	11	125	25.00		11	125	125.00
-003	00	19.44	155.52	-004	00	19.44	161.1328125
	01	125.0	155.52		01	19.44	161.1328125
	10	155.52	155.52		10	19.44	161.1328125
	11	156.25	155.52		11	19.44	161.1328125
-005	00	132.81	84.774	-006	00	169.548	156.25
	01	153.60	84.774		01	169.548	156.25
	10	155.52	84.774		10	169.548	156.25
	11	156.25	84.774		11	169.548	156.25
-007	00	10	200				
	01	10	200				
	10	10	200				
	11	10	200				

Once Input and Output frequencies have been submitted and approved, the Factory will assign a part number.

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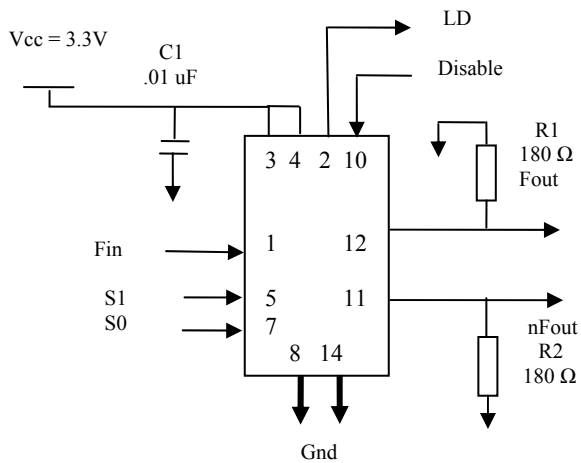
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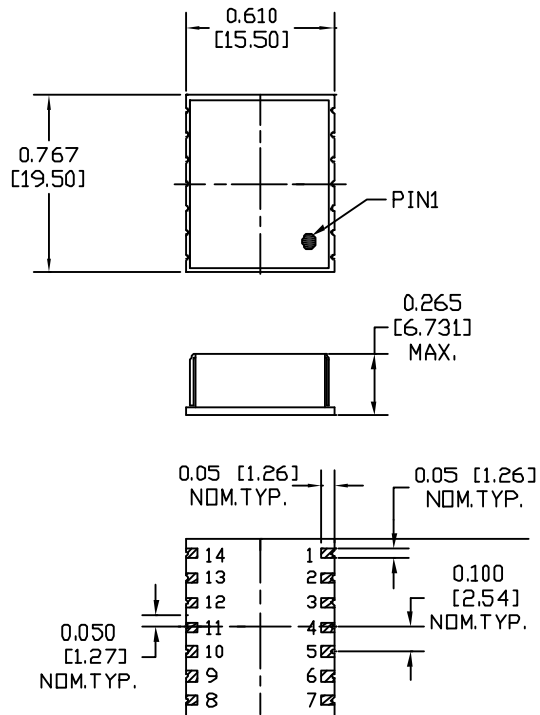
Environmental and Mechanical

Parameter	Specification
Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Vibration	Per MIL-STD-883, Method 2007, Condition A
Soldering Conditions	260°C for 10s max
Hermetic Seal	Leak rate less than 5×10^{-8} atm.cc/s of helium (crystal only)

Connection Diagram



Mechanical Outline



Pin #	Description
1	Fin
2	Lock Detect
3	Vcc
4	Vcc
5	S1
6	DNC
7	S0
8	Gnd
9	N/C
10	Disable
11	nFout
12	Fout
13	N/C
14	Gnd