

MR36V01G52B

64M-Word × 16-Bit or 128M-Word × 8-Bit Page Mode **P2ROM**

FEATURES

64Mx16 or 128Mx8-bit
electrically switchable configuration

- Page size of 8-word x 16-Bit or 16-word x 8-Bit
- 3.0 V to 3.6V power supply
- Random Access time 110 ns MAX
- Page Access time 25 ns MAX
- Operating current 50 mA MAX
- Standby current 25 mA MAX
- Input/Output TTL compatible
- Three-state output

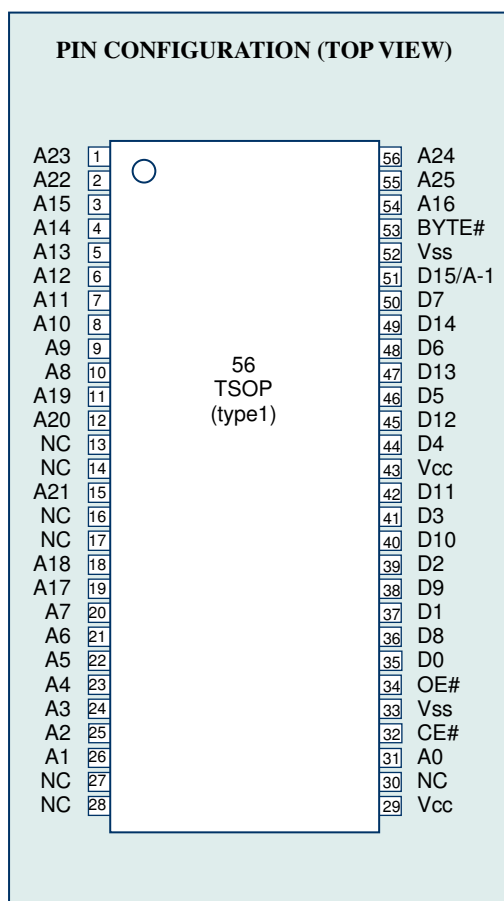
PACKAGES

- 56-pin plastic TSOP (TSOP(1)56-P-1420-0.50-K-MC)

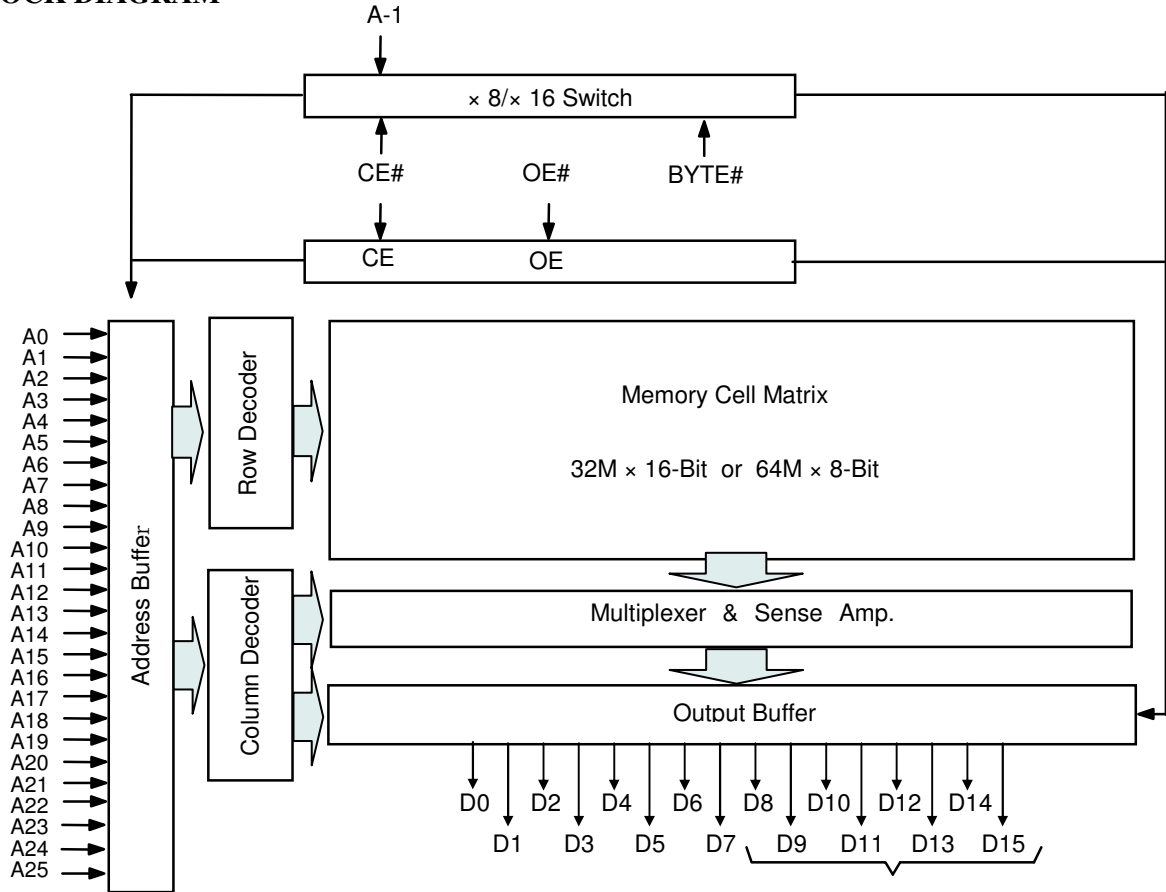
P2ROM ADVANCED TECHNOLOGY

P2ROM stands for Production Programmed ROM. This exclusive LAPIS Semiconductor technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- **No additional programming charge**, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- **Custom Marking is** available at no additional charge.



BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions
D15 / A-1	Data output / Address input
A0 to A25	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V _{CC}	Power supply voltage
V _{SS}	Ground
NC	No connect

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V _{CC}	D0 to D7	D8 to D15	A-1
Read (16-Bit)	L	L	H	3.3 V	D _{OUT}		*
Read (8-Bit)	L	L	L		D _{OUT}	Hi-Z	L/H
Output disable	L	H	H		Hi-Z		*
			L				
Standby	H	*	H		Hi-Z		*
			L				

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T _a	—	0 to 70	°C
Storage temperature	T _{stg}		-55 to 125	°C
Input voltage	V _I	relative to V _{SS}	-0.5 to V _{CC} +0.5	V
Output voltage	V _O		-0.5 to V _{CC} +0.5	V
Power supply voltage	V _{CC}		-0.5 to 5	V
Output short circuit current	I _{OS}	—	10	mA
Power dissipation per package	P _D	T _a =25°C	1.0	W

RECOMMENDED OPERATING CONDITIONS

(T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V _{CC} power supply voltage	V _{CC}	V _{CC} = 3.0 to 3.6 V	3.0	—	3.6	V
Input "H" level	V _{IH}		2.2	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}		-0.5**	—	0.6	V

Voltage is relative to V_{SS}.

* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.3 V, T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input(except BYTE#)	C _{IN1}	V _I = 0 V	—	—	20	pF
Output	C _{OUT}		—	—	20	

ELECTRICAL CHARACTERISTICS**DC CHARACTERISTICS**(V_{CC} = 3.3 V ± 0.3 V, T_a = 0 to 70°C)

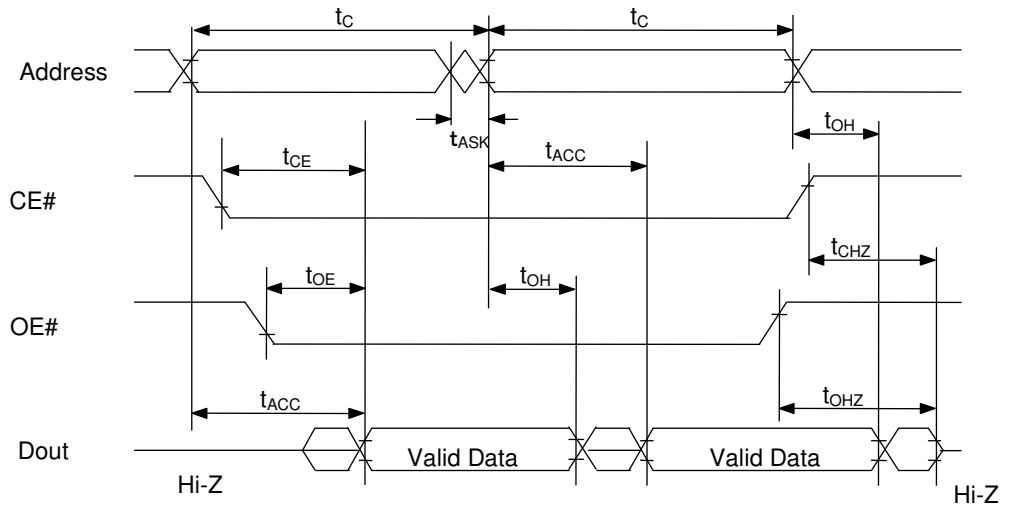
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I = 0 to V _{CC}	—	—	20	μA
Output leakage current	I _{LO}	V _O = 0 to V _{CC}	—	—	20	μA
V _{CC} power supply current (Standby)	I _{CCSC}	CE# = Add.=V _{CC}	—	—	25	mA
	I _{CCST}	CE# = Add.=V _{IH}	—	—	25	mA
V _{CC} power supply current (Read)	I _{CCA1}	CE# = V _{IL} OE# = V _{IH} tc = 200 ns	—	—	50	mA
Input "H" level	V _{IH}	—	2.2	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}	—	-0.5**	—	0.6	V
Output "H" level	V _{OH}	I _{OH} = -2 mA	2.4	—	—	V
Output "L" level	V _{OL}	I _{OL} = 2 mA	—	—	0.4	V

Voltage is relative to V_{SS}.* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

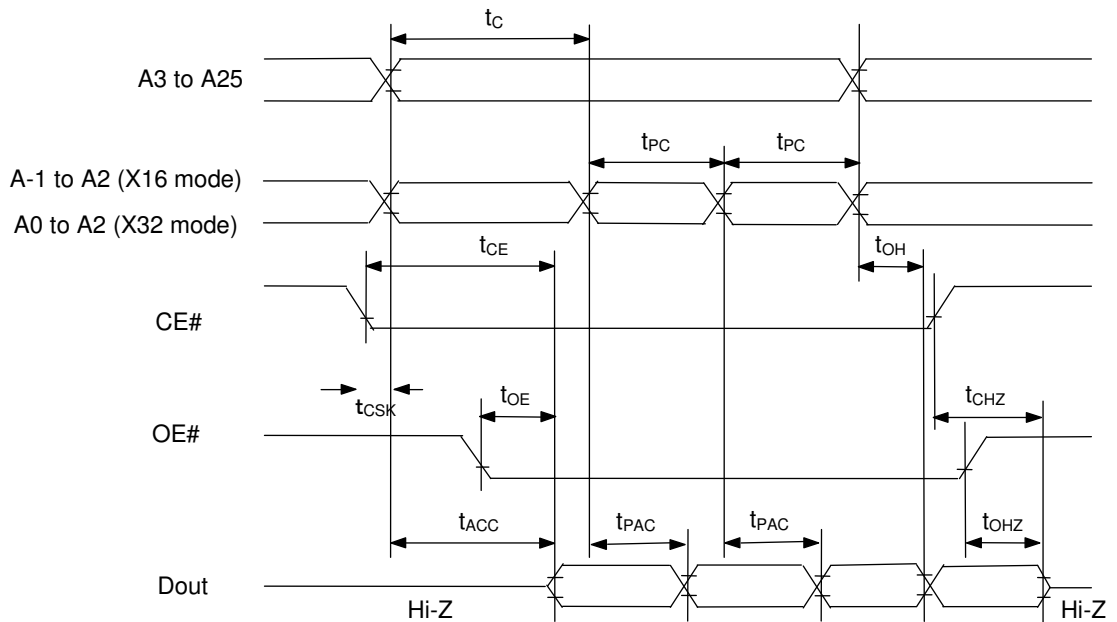
** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

TIMING CHART (READ CYCLE)

Random Access Mode Read Cycle



Page Access Mode Read Cycle

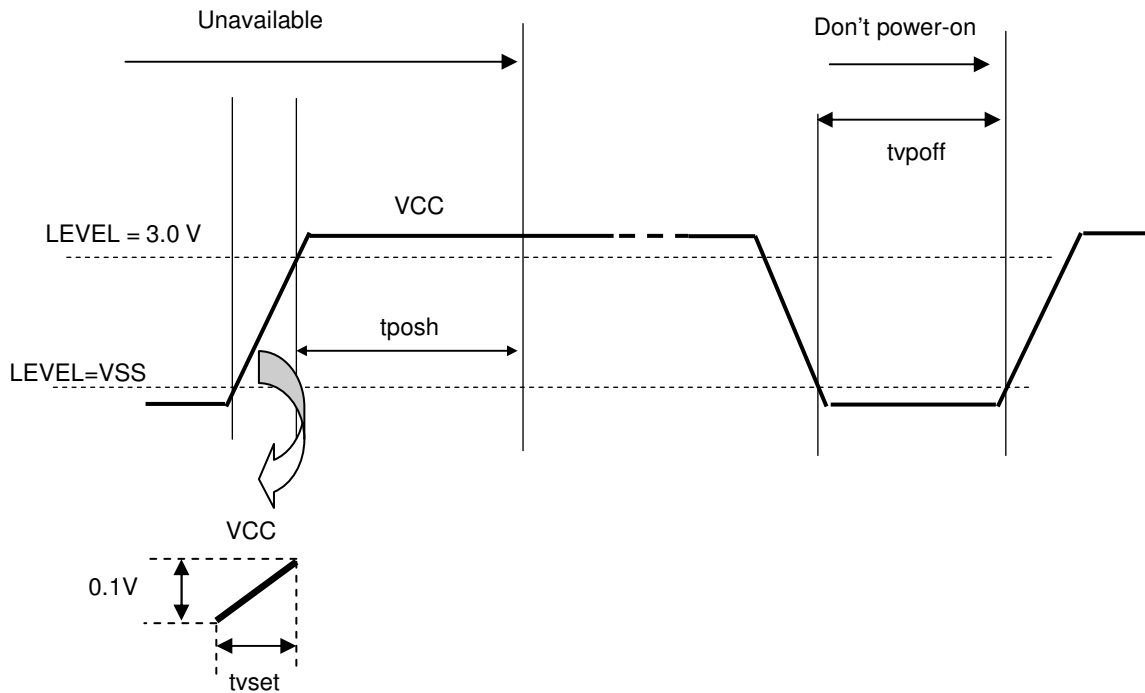


POWER ON CHARACTERISTICS

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $T_a = 0\text{ to }70^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Max.	Unit
VCC set up time	tvset	—	5	270	us
Power on sequence hold time	tposh	—	1	—	ms
Power off hold time	tpoff	—	1	—	ms

TIMING CHART (POWER ON)



Note: A start-up delay of 1ms is required after power-on.
 If you power-off VCC, you must wait 1ms to power-on.
 CE# must be HIGH while VCC power on sequence.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR36V01G52B-002-01	Nov. 18,2009	-	-	Final edition 1

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