ML9461B

Segment Driver for Dot Matrix STN Liquid Crystal Display

1. Product Overview

1.1 General Description

The ML9461B is a 320-output segment driver for driving a dot matrix LCD panel.
The driver enables switching between 320 outputs and 240 outputs and 200 outputs. The ML9461B is used in combination with the common driver ML9460.

1.2 Features

- 320-channel common driver
- Display duty: Up to 1/240
- Liquid crystal drive voltage: 2.6 to 5.5 V
- Automatically generates a chip enable signal internally
- Operating voltage: 2.5 to 5.5 V
- Number of data bits: 4-/8-bits
- Built-in standby function
- Can switch output modes: 320-output mode/240-output mode/200-output mode
- Shift clock speed: 15 MHz max. @ 2.7 to 4.5 V, 20 MHz max. @ 4.5 to 5.5 V
- Package

Au Bump Chip	Product name: ML9461BCVWA
TCP	Product name: ML9461ADVVA

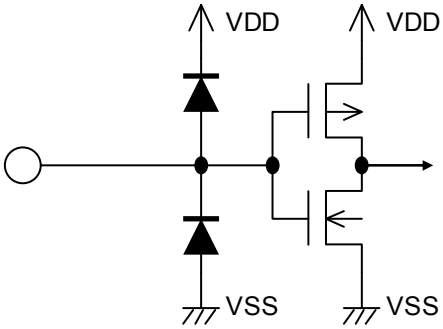
2. Pin Description

2.1 Pin Description

Pin name	I/O	Polarity	Descripiton	Initial value	Handling when not used	Attribute	Remarks
VDD	—	—	Logic power supply pin	—	—	Power	
VSS	—	—	Logic power supply pin	—	—	Power	
V1L V1R	I	—	Power supply pins for liquid crystal drive level output.	—	—	Power	V1L and V1R are connected internally with each other.
VCL VCR	I	—	Power supply pins for liquid crystal drive level output.	—	—	Power	VCL and VCR are connected internally with each other.
MV1L MV1R	I	—	Power supply pins for liquid crystal drive level output.	—	—	Power	MV1L and MV1R are connected internally with each other.
LP	I	↓	Display data latch signal pin	Low	—	Digital	
$\overline{\text{SCL}}$	I	↓	Display data fetch signal pin.	Low	—	Digital	
FR	I	—	Input-output pin for alternating signal for liquid crystal drive output	Low or High	—	Digital	
D0 to D7	I	—	Display data input pins	Low or High	In 4-bit input mode, tie D4–D7 to VSS.	Digital	See Section 4.1.4, “Latch Circuit 1.”
SHL	I	—	Data output inversion control pin	Low or High	—	Digital	See Section 4.1.6.1, “Data Output Destination Switching (SHL).”
$\overline{\text{EIO1}}$	I/O	Negative	Enable signal input-output pin	Low or High	—	Digital	
$\overline{\text{EIO2}}$	I/O	Negative	Enable signal input-output pin	Low or High	—	Digital	
$\overline{\text{DSPOF}}$	I	Negative	Display OFF signal control pin. A VSS level on this pin sets each of the liquid crystal drive outputs O1–O320 to the VC level.	Low	—	Digital	
DMS	I	—	Display data input bit count switching pin	Low or High	—	Digital	
SEL1	I	—	Display data input bit count switching pin	Low or High	—	Digital	
DFR	I	—	FR signal control switching pin.	Low or High	Connect to VSS	Digital	
SEL2	I	—	Display data input bit count switching pin	Low or High	Connect to VSS	Digital	
O1 to O320	O	—	Liquid crystal drive output pins. When $\overline{\text{DSPOF}}$ is set to the VDD level, either one of the two levels (V1 and MV1) is selected and output according to the combination of the M signal and display data.	—	Pins that are made disabled by the SEL1 pin will output the nonselective level signal (VC). Those disabled pins should be left open.	Analog	See Section 4.1.1, “Liquid Crystal Drive Circuit.”

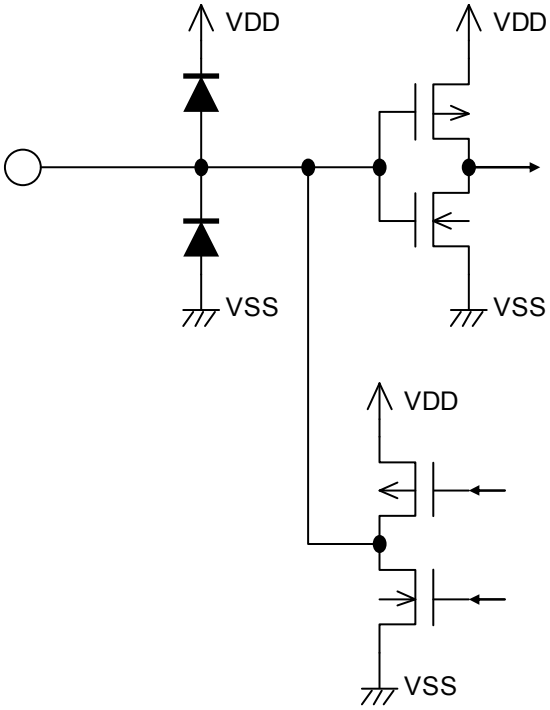
Note:
In the initial value column,
- A dash “—” for an input pin indicates that the initial value is Don’t Care.
- A dash “—” for an output pin indicates that the initial value is undefined.

2.2 Inupt and Output Configuration

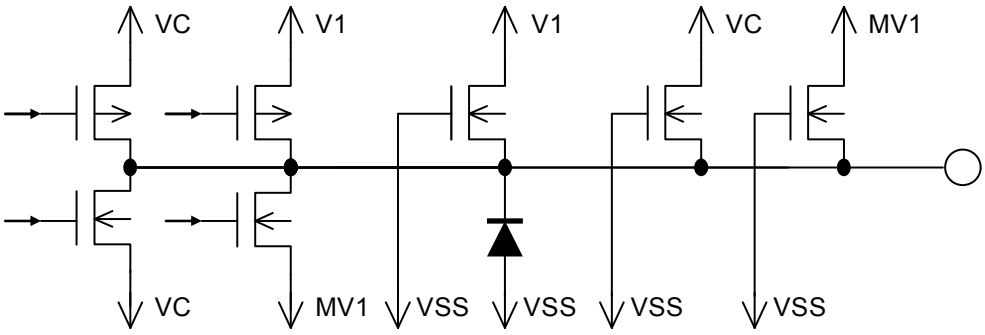


Applicable to pins
LP,$\overline{\text{SCL}}$,FR,SHL,$\overline{\text{DSPOF}}$,
DMS,SEL1,DFR,SEL2,
and D0～D7.

※ For the terminal D0～D8,
the second is not INV gate,
but NAND gate.

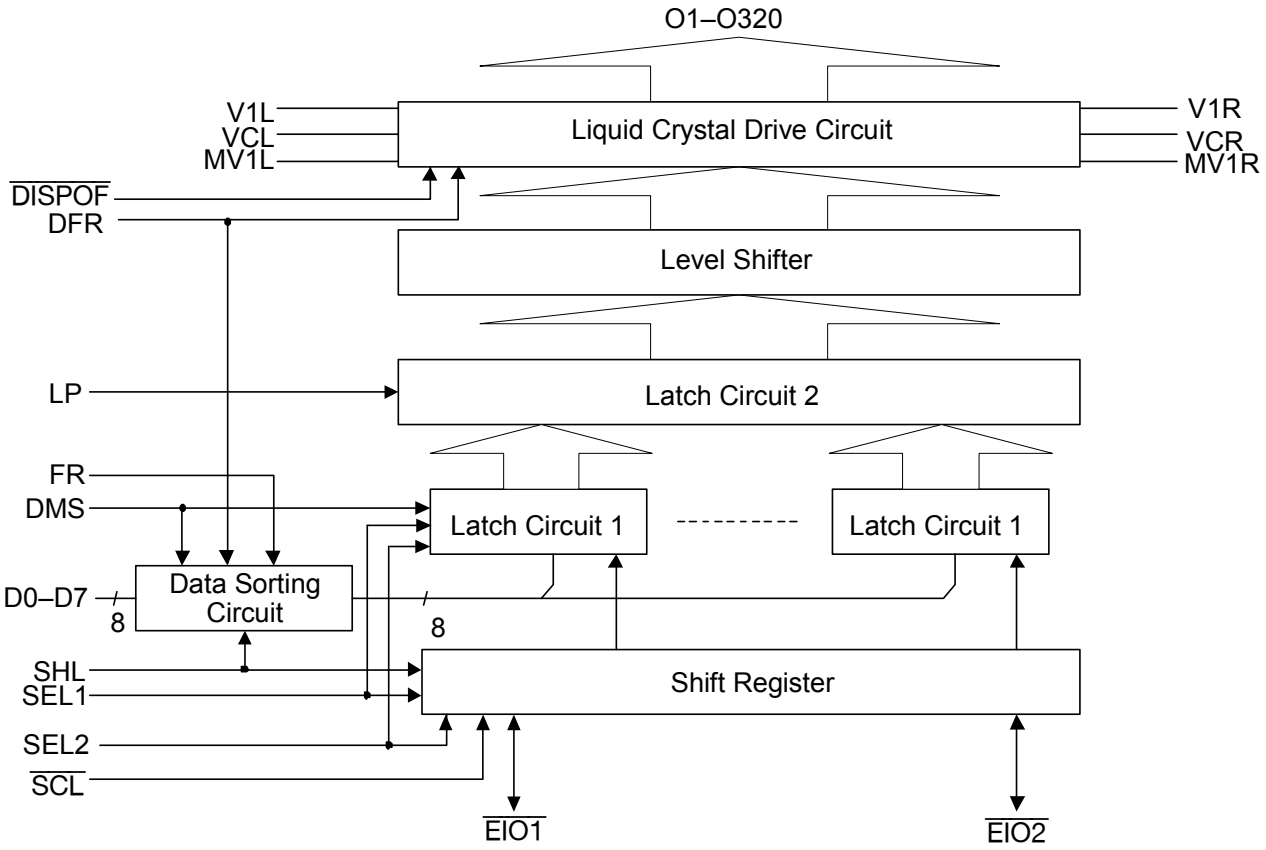


Applicable to pins $\overline{\text{EIO1}}$and $\overline{\text{EIO2}}$.



Applicable to pins O1～O320.

3. Block Diagram



4. Functional Description

4.1 Internal Blocks

4.1.1 Liquid Crystal Drive Circuit

The liquid crystal drive circuit selects one of the three levels for liquid crystal drive and outputs it. One of the three liquid crystal drive levels (V1, VC, MV1) is selected and output according to the combination of the data stored in the latch circuit 2, FR, and $\overline{DSPOF}$.

FR	Display data	$\overline{DSPOF}$	Output level
*	*	"L"	VC
"L"	"L"	"H"	V1
"L"	"H"	"H"	MV1
"H"	"L"	"H"	MV1
"H"	"H"	"H"	V1

*: Don't care

The number of output pins and Shift direction is set by the SEL1, SEL2, SHL pin setting, as shown below.

SEL2	SEL1	SHL	Number of output pins	Shift direction
"L"	"L"	"L"	240Outputs (O41,O42,O43 … O279,O280)	O41→O280
"L"	"L"	"H"	240 Outputs (O41,O42,O43 … O279,O280)	O280→O41
"L"	"H"	"L"	320 Outputs (O1,O2,O3 … O319,O320)	O1→O320
"L"	"H"	"H"	320 Outputs (O1,O2,O3 … O319,O320)	O320→O1
"H"	"L"	"L"	200 Outputs (O57,O58,O59 … O255,O256)	O57→O256
"H"	"L"	"H"	200 Outputs (O57,O58,O59 … O255,O256)	O256→O57
"H"	"H"	"L"	200 Outputs (O121,O122,O123 … O319,O320)	O121→O320
"H"	"H"	"H"	200 Outputs (O1,O2,O3 … O119,O200)	O200→O1

Pins that are made disabled by the SEL1 ,SEL2,SHL pin will output the nonselective level signal (VC). Those pins should be left open.

4.1.2 Level Shifter

The level shifter boosts logic signals to high-voltage signals (5 V) for liquid crystal drive.

4.1.3 Latch Circuit 2

The latch circuit 2 is a 320-bit latch circuit. It latches the data in the latch circuit 1 on the falling edge of LP, then transfers the outputs to the level shifter.

4.1.4 Latch Circuit 1

The latch circuit 1 is a 4-/8-bit parallel data latch circuit. It fetches display data D0–D7 according to the signal from the shift register.
The number of input bits of display data is switched according to the DMS pin setting, as shown below.

DMS	Input bit mode
"H"	8-bit input mode
"L"	4-bit input mode (Fetches data from D0–D3.)

If 4-bit input mode is selected, tie pins D4–D7 to VSS.

4.1.5 Shift Register

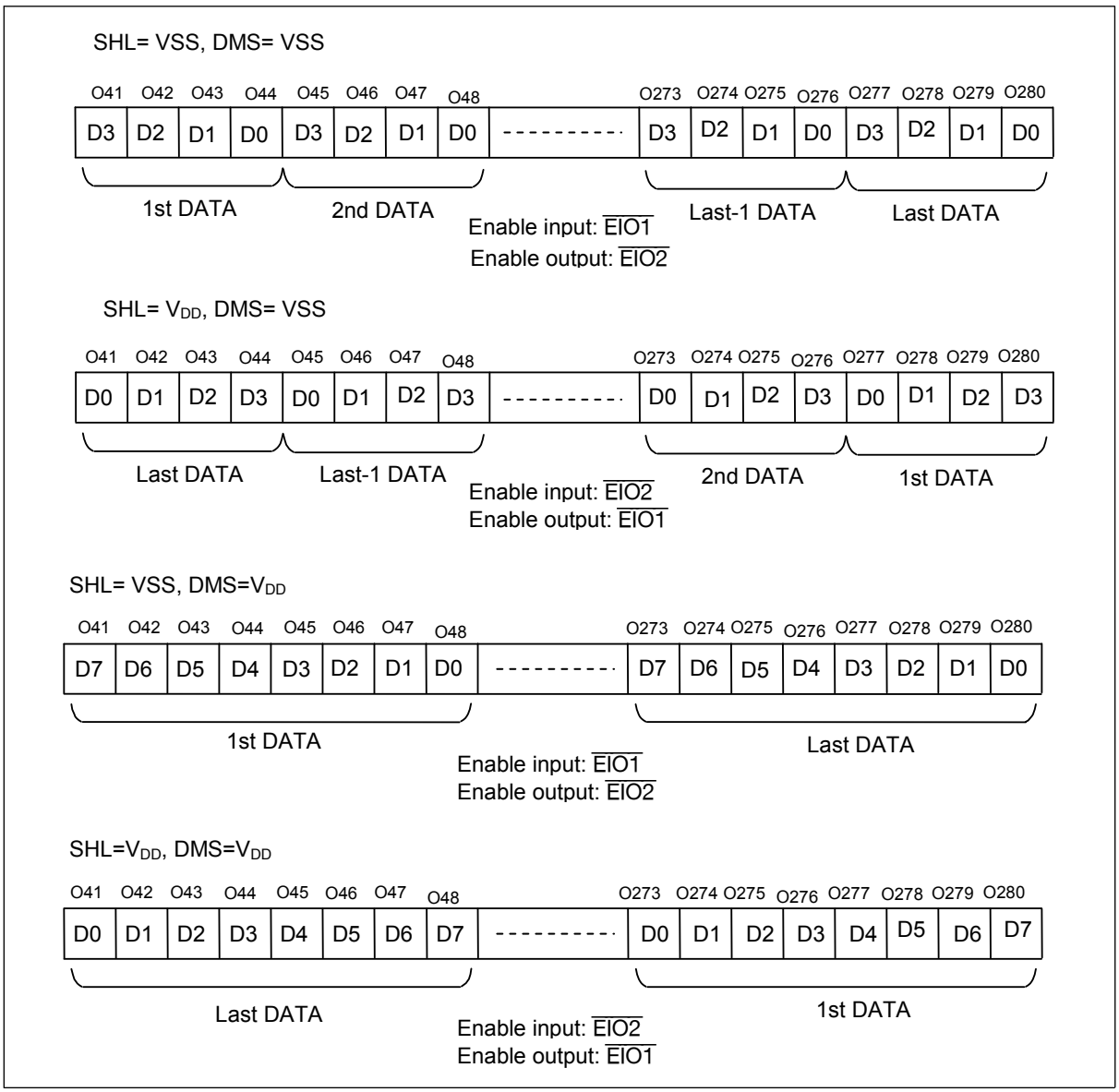
The ML9461B has an 80-bit shift register, which generates a signal used for fetching data in the latch circuit 1 on the falling edge of $\overline{SCL}$.

4.1.6 Data Sorting Circuit

This data sorting circuit inverts data by flipping the order of data output right/left (like a mirror image) (according to the SHL signal).

4.1.6.1 Data Output Destination Switching (SHL):SEL2=L, SEL1=L

The data sorting circuit flips the order of data output right/left according to the SHL signal. At this time, the enable signal input-output pins are switched.

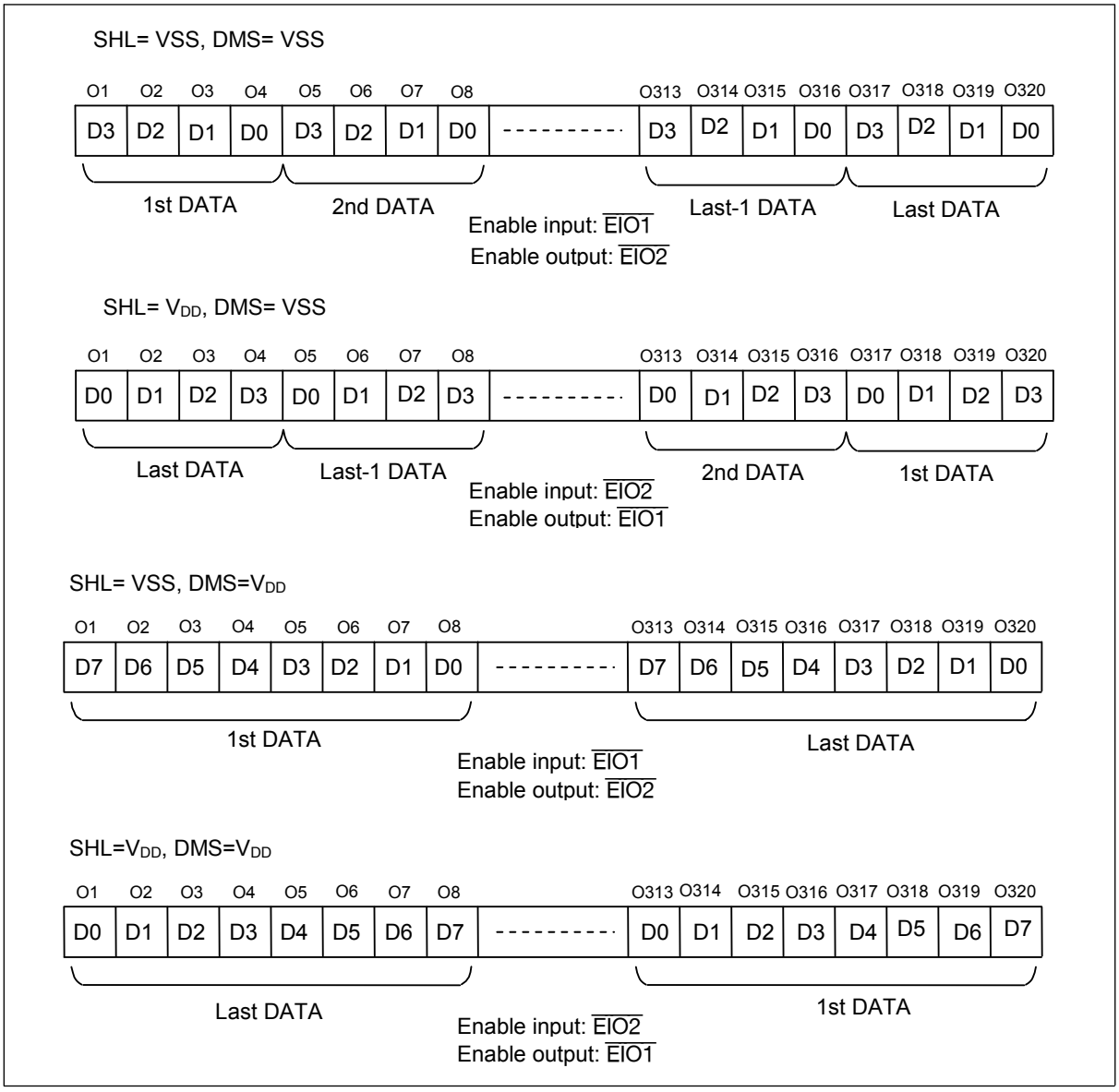


Enable input: Tie the enable input at the first stage to VSS and connect the remaining enable inputs to the enable outputs at their (= the remaining inputs') respective preceding stages.

Enable output: During cascade output, connect each enable output to the corresponding enable input at the next stage.

4.1.6.2 Data Output Destination Switching (SHL):SEL2=L, SEL1=H

The data sorting circuit flips the order of data output right/left according to the SHL signal. At this time, the enable signal input-output pins are switched.

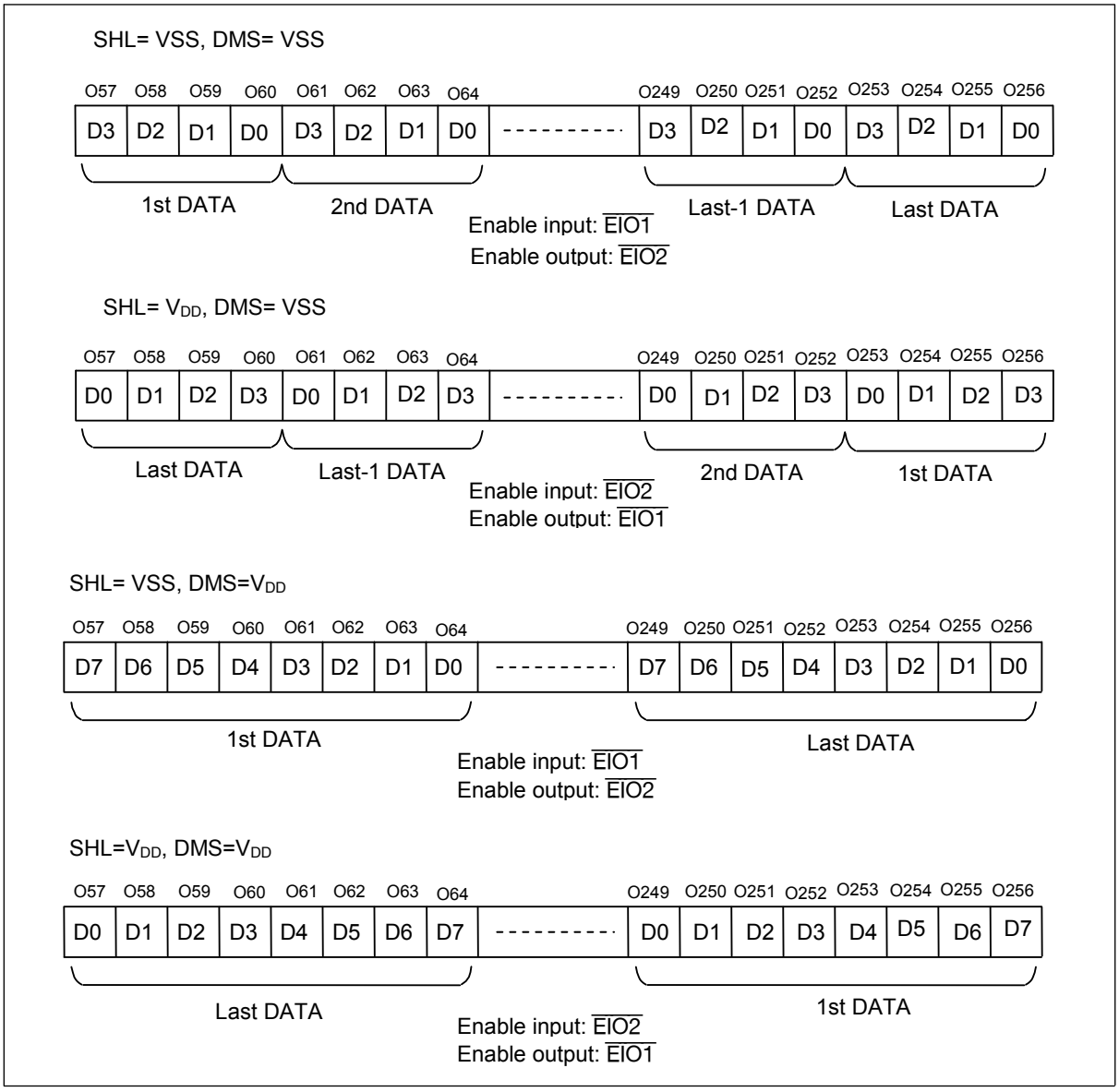


Enable input: Tie the enable input at the first stage to VSS and connect the remaining enable inputs to the enable outputs at their (= the remaining inputs') respective preceding stages.

Enable output: During cascade output, connect each enable output to the corresponding enable input at the next stage.

4.1.6.3 Data Output Destination Switching (SHL):SEL2=H, SEL1=L

The data sorting circuit flips the order of data output right/left according to the SHL signal. At this time, the enable signal input-output pins are switched.

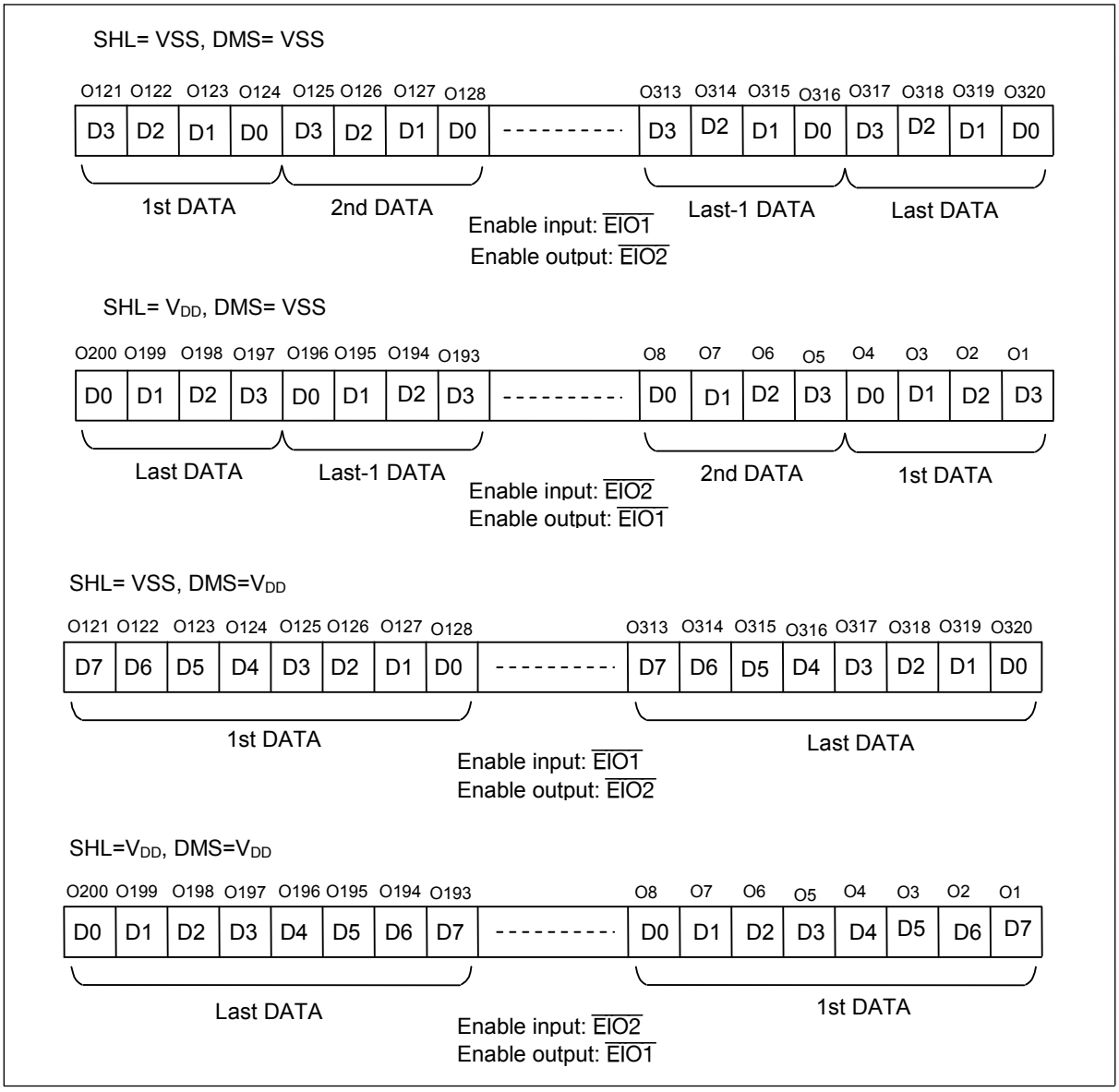


Enable input: Tie the enable input at the first stage to VSS and connect the remaining enable inputs to the enable outputs at their (= the remaining inputs') respective preceding stages.

Enable output: During cascade output, connect each enable output to the corresponding enable input at the next stage.

4.1.6.4 Data Output Destination Switching (SHL):SEL2=H, SEL1=H

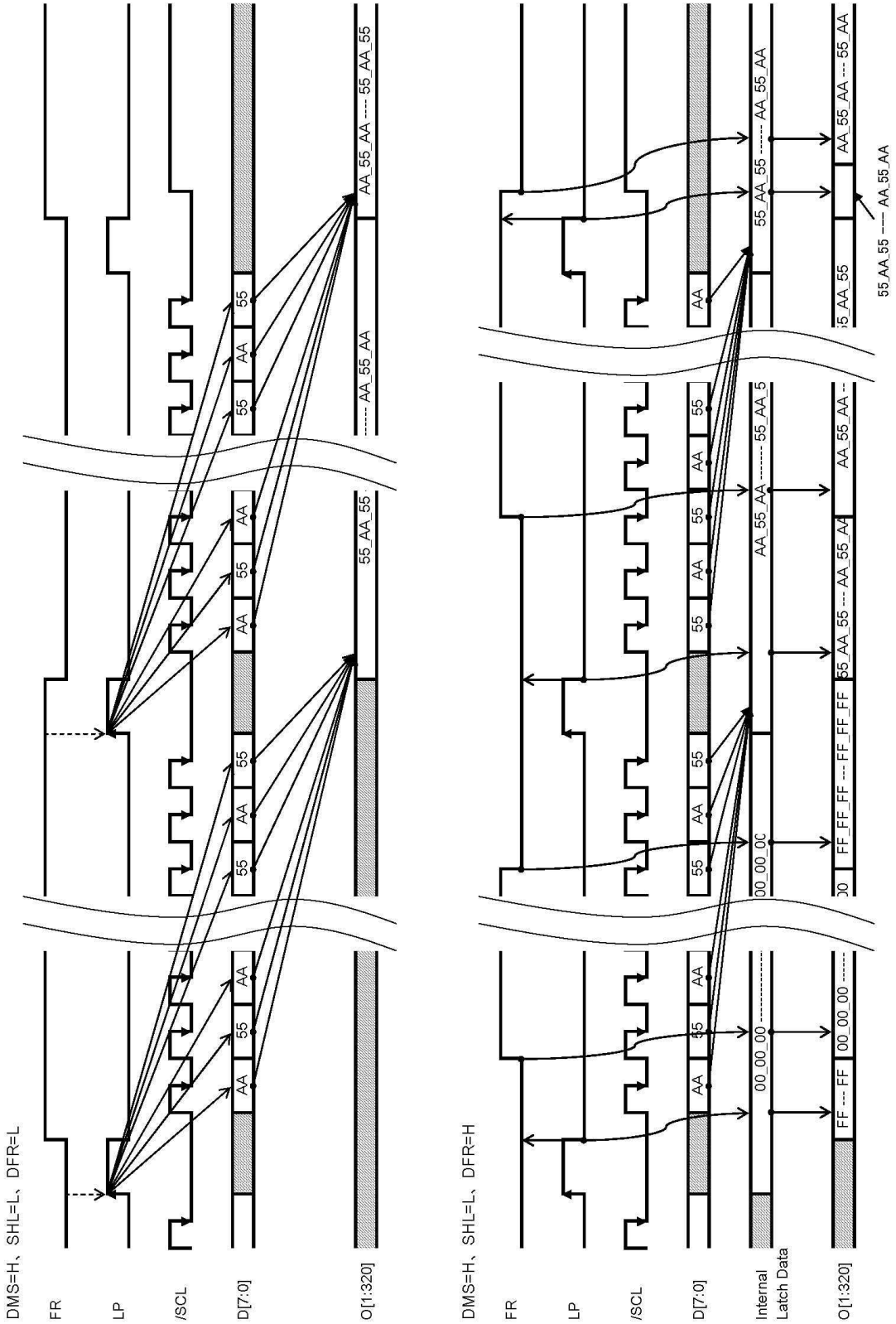
The data sorting circuit flips the order of data output right/left according to the SHL signal. At this time, the enable signal input-output pins are switched.



Enable input: Tie the enable input at the first stage to VSS and connect the remaining enable inputs to the enable outputs at their (= the remaining inputs') respective preceding stages.

Enable output: During cascade output, connect each enable output to the corresponding enable input at the next stage.

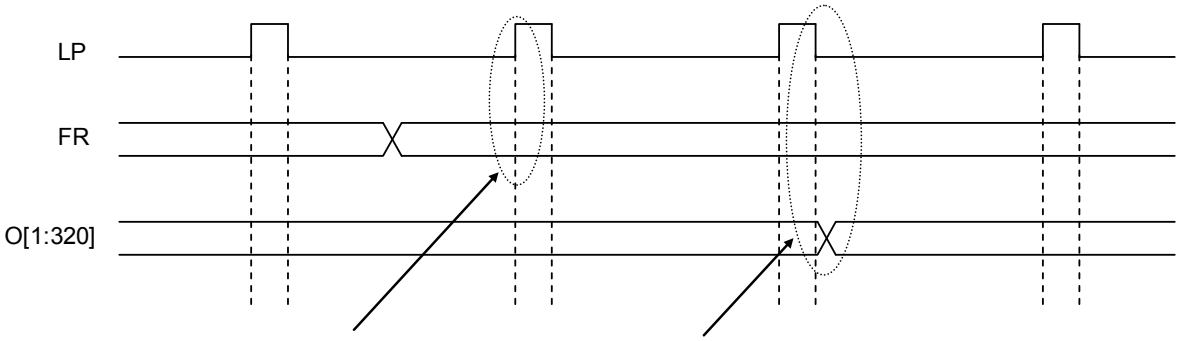
4.1.7 Output control function by DFR pin.



4.1.7 Output control function by DFR pin.（Supplement Explanation.）

◆Timing of liquid crystal exchange making signal FR and driver output.（in the case of DFR=L）

・By the state of the FR signal when an LP signal rise, interchange inversion is set.

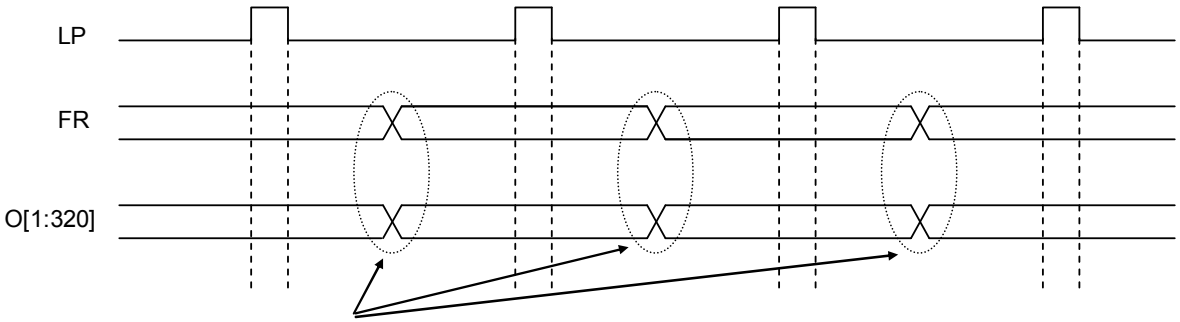


The FR signal is latched to inside by the timing of the LP signal rising.

By the timing of next LP signal's falling, it is transmitted to the output.

◆Timing of liquid crystal exchange making signal FR and driver output.（in the case of DFR=H）

・By an FR signal only, interchange inversion is set.

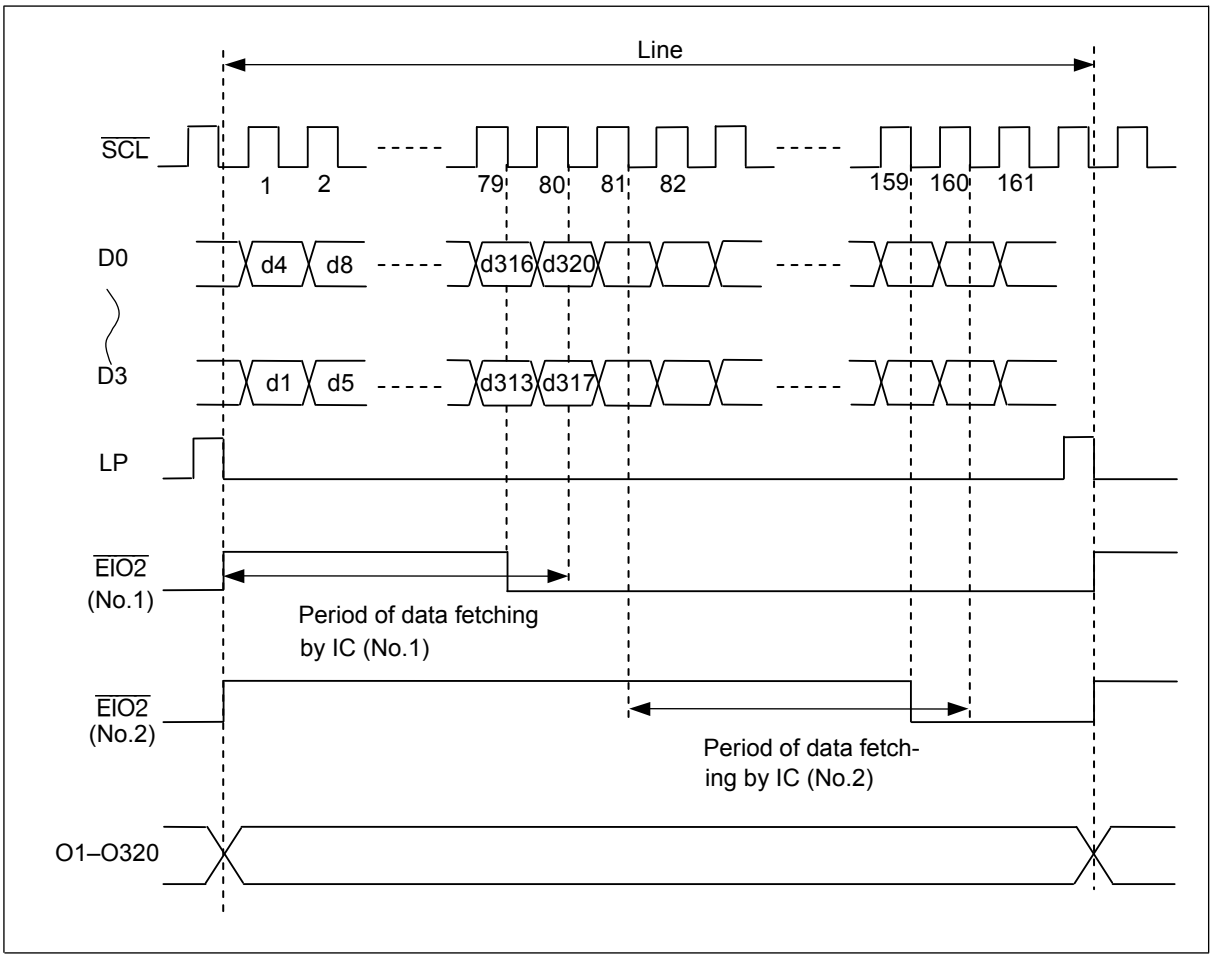


By an FR signal only, interchange inversion is set.

4.2 Timing Diagram

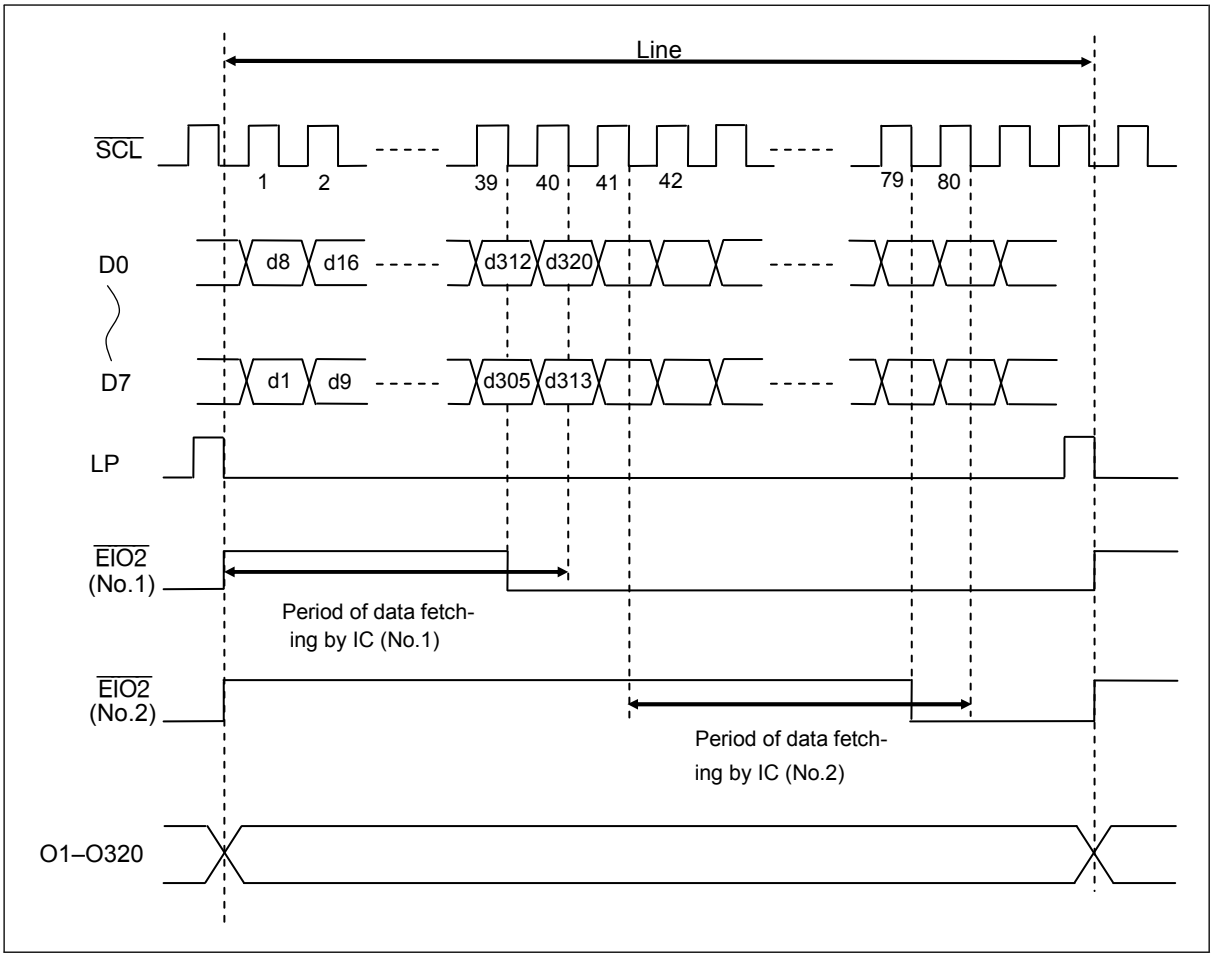
4.2.1 Data Fetch Timing (4-bit fetch; 640 dots per line)

At DMS = VSS, the device is in 4-bit fetch mode.
Releasing a data standby state is enabled when the data fetch enable signal (when SHL = VSS: $\overline{EIO1}$) is at a Low level, and the standby state is actually released by the next data fetch clock ($\overline{SCL}$). Four bits of data are fetched simultaneously at the falling edge of $\overline{SCL}$. At completion of fetching of 316 bits, the enable signal (when SHL = VSS: $\overline{EIO2}$) is set to the VSS level. At completion of fetching 320 bits, the operation stops automatically (standby state). By connecting the $\overline{EIO2}$ pin to the $\overline{EIO1}$ pin of the next stage, the IC of the next stage is activated.
As for the output destination of fetched data, d1 is output to output pin O1 and d320 to O320 when SHL = VSS. When SHL = V_{DD}, d1 is output to O320 and d320 to O1.



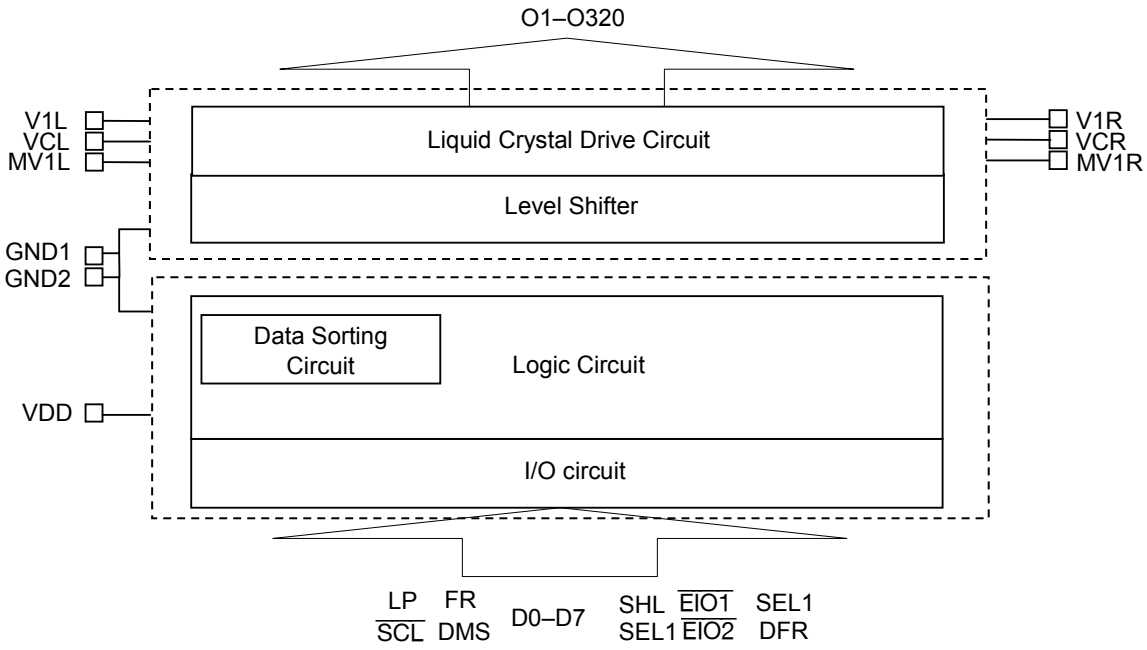
4.2.2 Data Fetch Timing (8-bit fetch; 640 dots per line)

At DMS = VDD, the device is in 8-bit fetch mode.
Eight bits of display data are fetched simultaneously at the falling edge of $\overline{SCL}$. Other basic operations are the same as in 4-bit fetch mode.



5. Power Supply System

5.1 Power Supply Group



This LSI does completely separate liquid crystal power supply and logic power supply on its circuit architecture. But,if the noise of the liquid crystal power supply in the LCD module rounds to the logic power supply,there is the possibility that VDD is less than 2.5V. Then this LSI may malfunction. Since there is a possibility that Input voltage of V1L/V1R drops down temporality at charging/discharging depending on load capacity of an LCD panel,calibration of CB that Liquid crystal drive voltage doesn't go lower point(2.6V) is necessary. Insert bypass capacitors CA,CB by referring to the Application Circuit described later so that power supplies will be stabilized. It is recommended that 0.1 μF CA capacitors (JIS (Japanese Industrial Standards) FJ(F) equivalent) be used .

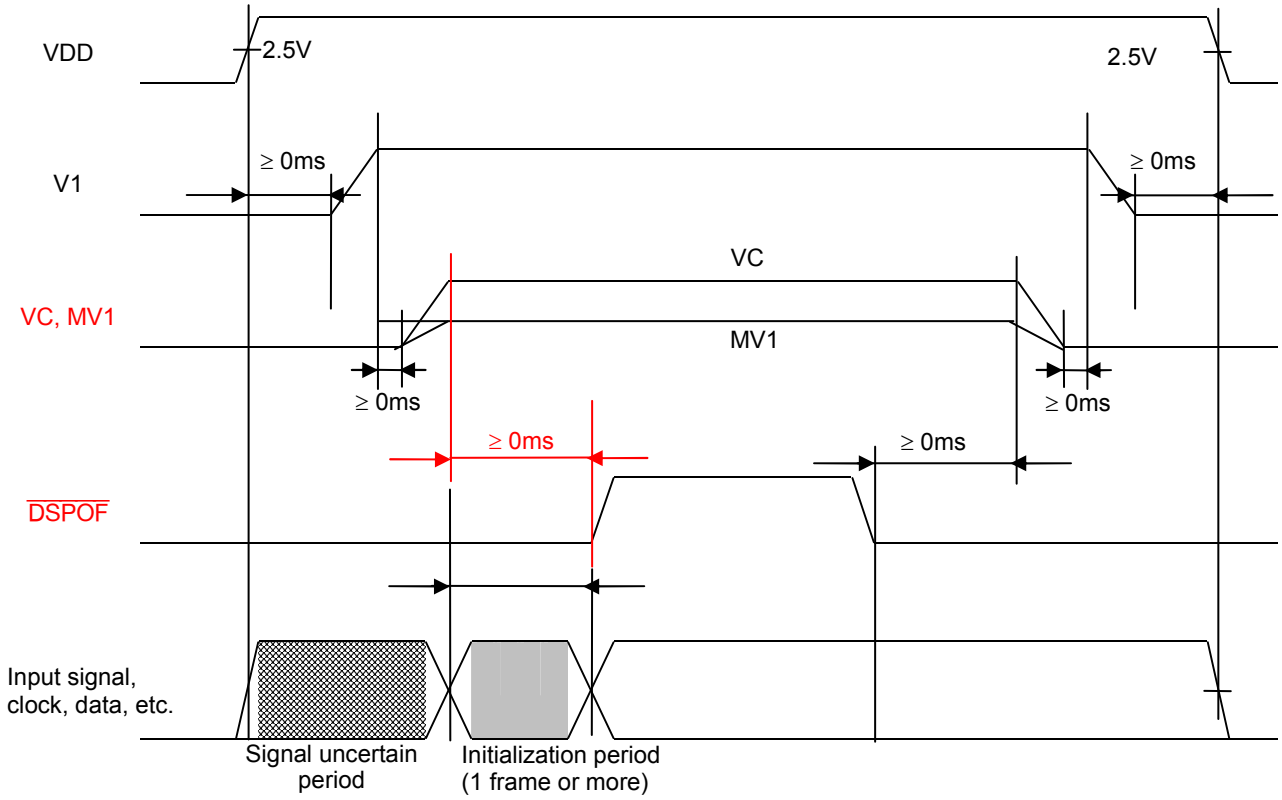
5.2 Power-On/Shutdown Sequence

5.2.1 Power-On Sequence

1. Apply power to (1)VSS–VDD, (2)VSS–V1, and (3)VC, MV1 in this order with the VSS potential being input to the $\overline{\text{DSPOF}}$ pin.
2. The O1–O240 pins forcibly outputs the VC level by the DISPOFF function.
3. Even if an input signal is disturbed immediately after VDD is applied, priority is given to the DISPOFF function.
4. Input the predetermined signal(s) to initialize the registers in the driver. In this case, take at least one frame for the initialization period.
5. Input the VDD voltage to the $\overline{\text{DSPOF}}$ pin to release the DISPOFF function. At this point, the levels of the V1, VC, and MV1 pin must have reached their respective predetermined potentials.

5.2.2 Shutdown Sequence

1. The $\overline{\text{DSPOF}}$ pin must remain set to the VSS potential.
2. Shut down the power supplies for liquid crystal in the order of (1)VC, MV1 and (2)VSS–V1.
3. Reduce the voltage of (3)VDD and the levels of the input signals to the VSS potential. At this point, the V1, VC, and MV1 pin must completely drop to 0 V.



6. Electrical Specifications

6.1 Absolute Maximum Ratings

VSS = 0V

Parameter		Symbol	Condition	Rating	Unit	Applicable pins
Power supply voltage	Logic circuit	V_{DD}	Tj = –30°C to +75°C	–0.3 to +6.5	V	VDD
	liquid crystal drive circuit	V1	Tj = –30°C to +75°C	–0.3 to +6.5	V	V1L, V1R
Input voltage (1)		V_{t1}	Tj = –30°C to +75°C	–0.3 to V_{DD}+0.3	V	LP, $\overline{SCL}$, FR, D0–D7, SHL, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DSPOF}$, DMS, SEL1, SEL2,DFR
Input voltage (2)		V_{t2}	Tj = –30°C to +75°C	–0.3 to V1+0.3	V	VCL, VCR, MV1L, MV1R
Output current/output short-circuit current		I_O	Tj = –30°C to +75°C	3	mA	$\overline{EIO1}$, $\overline{EIO2}$, O1–O320
Junction temperature		Tj	—	–55 to +110	°C	—
Storate temperature range		T_{stg}	—	–55 to +110	°C	—

6.2 Recommended Operating Conditions (Guaranteed Operating Range)

VSS = 0V, V1 = 2.6 to 5.5V

Parameter	Symbol	Condition	Range			Unit	Applicable pins
			Min.	Typ.	Max.		
Power supply voltage	V_{DD}	—	2.5	—	5.5	V	VDD
“H” Input voltage	V_{IH}	—	0.8×V_{DD}	—	V_{DD}	V	LP, $\overline{SCL}$, FR, D0–D7, SHL, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DSPOF}$, DMS, SEL1,SEL2,DFR
“L” Input voltage	V_{IL}	—	0	—	0.2×V_{DD}	V	
Operating frequency1	f_{CK1}	V_{DD} = 2.5 to 4.5V	— (*1)	—	15	MHz	LP, $\overline{SCL}$
Operating frequency2	f_{CK2}	V_{DD} = 4.5 to 5.5V	— (*1)	—	20	MHz	LP, $\overline{SCL}$
Operating temperature	Tjop	—	–30	—	75	°C	—
Load condition 1	C_{L1}	—	—	—	10	pF	$\overline{EIO1}$, $\overline{EIO2}$
Load condition 2	C_{L2}	—	—	—	100	pF	O1–O320
Input rise waveform	t_r	—	—	—	30	ns	LP, $\overline{SCL}$
Input fall waveform	t_f	—	—	—	30	ns	LP, $\overline{SCL}$

“—” indicates that no particular value is specified.

*1: 5 kHz is specified for the test condition.

Notes:

1. Insert bypass capacitors CA,CB by referring to the Application Circuit described later so that power supplies will be stabilized. It is recommended that 0.1 μF CA capacitors (JIS (Japanese Industrial Standards) FJ(F) equivalent) be used .
2. Observe the following magnitude relationship:
   V1 ≥ VC ≥ MV1 ≥ VSS

6.3 DC Characteristics

Unless otherwise specified, VSS = 0V, V_{DD} = 2.5 to 5.5V, V1 = 2.6 to 5.5V, Tj = –30 to +75°C

No.	Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pins	Remarks
1	"H" level input voltage	V_{IH}	—		V_{DD}×0.8	—	V_{DD}	V	LP, $\overline{SCL}$, FR, D0–D7, SHL, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DSPOF}$, DMS, SEL1,SEL2, DFR	
2	"L" level input voltage	V_{IL}	—		0	—	V_{DD}×0.2	V		
3	"H" level output voltage	V_{OH}	I_{OH} = –0.4mA		V_{DD}–0.4	—	—	V	$\overline{EIO1}$, $\overline{EIO2}$	
4	"L" level output voltage	V_{OL}	I_{OL} = 0.4mA		—	—	0.4	V		
5	Dynamic supply current VDD	I_{DD1}	f_{FR} = 70Hz f_{LP} = 16.8kHz f_{SCL} = 672kHz DMS = H SEL1 = H Ta = 25°C	VDD = 3.0V V1 = 3.0V	—	140	280	μA	VDD	(*1)
		I_{DD2}		VDD = 5.0V V1 = 3.0V	—	240	480	μA	VDD	(*1)
6	Dynamic supply current V1	I_{V11}	f_{FR} = 70Hz f_{LP} = 16.8kHz f_{SCL} = 672kHz DMS = H SEL1 = H Ta = 25°C No Load Checker	VDD = 3.0V V1 = 3.0V	—	80	240	μA	V1L, V1R	(*1)
		I_{V12}		VDD = 3.0V V1 = 5.5V	—	140	420	μA	V1L, V1R	(*1)
7	Static supply current	IDDS	Ta = 25°C		—	—	5	μA	VDD	(*1)
		IV1S	Ta = 25°C		—	—	5	μA	V1L, V1R	(*1)
		IVC1S	Ta = 25°C		—	—	5	μA	VCL, VCR	(*1)
8	Input leakage current (1)	I_{IL1}	V_{IN} = V_{DD} to VSS		–5	—	5	μA	LP, $\overline{SCL}$, FR, D0–D7, SHL, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DSPOF}$, DMS, SEL1,SEL2, DFS	
9	Input leakage current (2)	I_{IL2}	V_{IN} = V_1 to VSS		–25	—	25	μA	VCL, VCR, MV1L, MV1R	
10	ON resistance between Vi and Oj	R_{ON}	I_{ON} = 150 μA		—	0.7	2.0	kΩ	O1–O320, V1L,V1R	(*2)
					—	2.0	3.0	kΩ	O1–O320, VCL, VCR	
					—	0.7	2.0	kΩ	O1–O320, MV1L, MV1R	

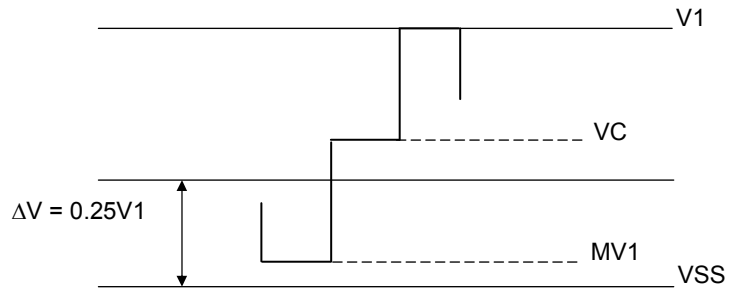
Values in the Typ. column are for reference only.
"—" indicates that no particular value is specified.

*1: The current that the input and output sections carry is excluded. In a CMOS device, if an input goes into an intermediate level, a through current will flow into the input circuit, so that power supply current will be increased. Therefore, use this device with V_{IH} = VDD level and V_{IL} = VSS level.

*2: The ON resistance between Vi and Oj indicates the resistance value between the O and V pins when a load current is applied to one of the pins O1–O320. The following conditions are defined:

V1 – VSS = 5.5 V
VC = (V1 + MV1)/2
MV1 = VSS + 1.0

The voltage range of the power supplies for liquid crystal drive level output should be as follows:
Apply a voltage near VSS to MV1 and a voltage near the intermediate level between MV1 and V1 to VC. Use MV1 within the voltage range of ΔV = 0.25V1. This range specifies the range where the value of the driver output impedance R_{ON} will stabilize.



Relationship between a driver output waveform and each liquid crystal drive level voltage

6.4 AC Characteristics

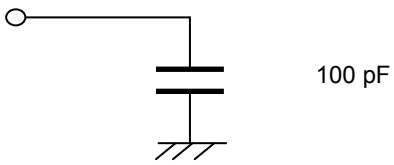
6.4.1 AC Characteristics 1

Unless otherwise specified, VSS = 0V, V_{DD} = 2.5 to 4.5V, V1 = 2.6 to 5.5V, Tj = –30 to +75°C

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
1	Clock cycle time	t_{CYC}	—	68	—	—	ns	$\overline{SCL}$
2	$\overline{SCL}$ "H" level width	t_{CWH2}	—	15	—	—	ns	$\overline{SCL}$
3	$\overline{SCL}$ "L" level width	t_{CWL2}	—	20	—	—	ns	$\overline{SCL}$
4	LP "H" level width	t_{CWH1}	—	25	—	—	ns	LP
5	$\overline{SCL}$ rise time	t_r	—	—	—	30	ns	LP, $\overline{SCL}$
6	$\overline{SCL}$ fall time	t_f	—	—	—	30	ns	LP, $\overline{SCL}$
7	$\overline{SCL}$ setup time	t_{SCL}	—	45	—	—	ns	LP, $\overline{SCL}$
8	$\overline{SCL}$ hold time	t_{HCL}	—	45	—	—	ns	LP, $\overline{SCL}$
9	Dta setup time	t_{DS}	—	15	—	—	ns	D0–D7, $\overline{SCL}$
10	Data hold time	t_{DH}	—	15	—	—	ns	D0–D7, $\overline{SCL}$
11	FR setup time	t_{FRS}	—	15	—	—	ns	FR, LP
12	FR hold time	t_{FRH}	—	15	—	—	ns	FR, LP
13	Output delay time	t_{pd1}	(*1)	—	—	1000	ns	O1–O320, LP,FR

Values in the Typ. column are for reference only.
"—" indicates that no particular value is specified.

*1: Load condition



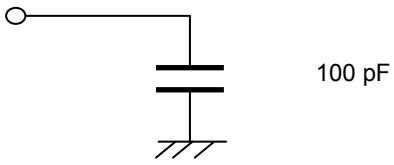
6.4.2 AC Characteristics 2

Unless otherwise specified, VSS = 0V, V_{DD} = 4.5 to 5.5V, V1 = 2.6 to 5.5V, Tj = –30 to +75°C

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
1	Clock cycle time	t_{CYC}	—	50	—	—	ns	$\overline{SCL}$
2	$\overline{SCL}$ "H" level width	t_{CWH2}	—	15	—	—	ns	$\overline{SCL}$
3	$\overline{SCL}$ "L" level width	t_{CWL2}	—	15	—	—	ns	$\overline{SCL}$
4	LP "H" level width	t_{CWH1}	—	15	—	—	ns	LP
5	$\overline{SCL}$ rise time	t_r	—	—	—	30	ns	LP, $\overline{SCL}$
6	$\overline{SCL}$ fall time	t_f	—	—	—	30	ns	LP, $\overline{SCL}$
7	$\overline{SCL}$ setup time	t_{SCL}	—	45	—	—	ns	LP, $\overline{SCL}$
8	$\overline{SCL}$ hold time	t_{HCL}	—	45	—	—	ns	LP, $\overline{SCL}$
9	Dta setup time	t_{DS}	—	15	—	—	ns	D0–D7, $\overline{SCL}$
10	Data hold time	t_{DH}	—	15	—	—	ns	D0–D7, $\overline{SCL}$
11	FR setup time	t_{FRS}	—	15	—	—	ns	FR, LP
12	FR hold time	t_{FRH}	—	15	—	—	ns	FR, LP
13	Output delay time	t_{pd1}	(*1)	—	—	1000	ns	O1–O320, LP,FR

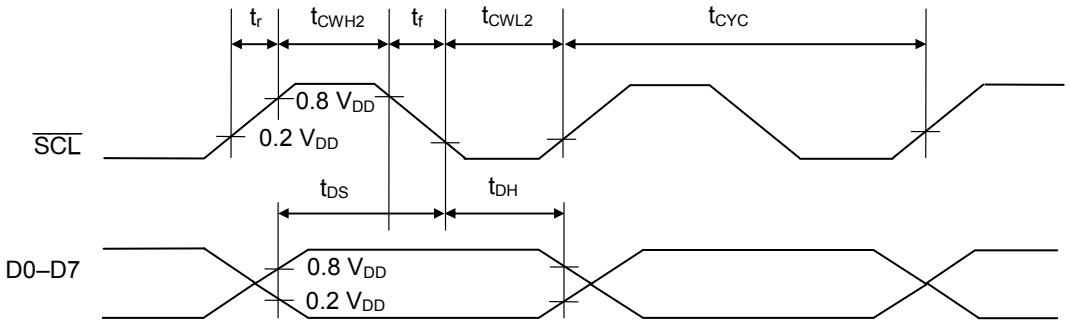
Values in the Typ. column are for reference only.
"—" indicates that no particular value is specified.

*1: Load condition

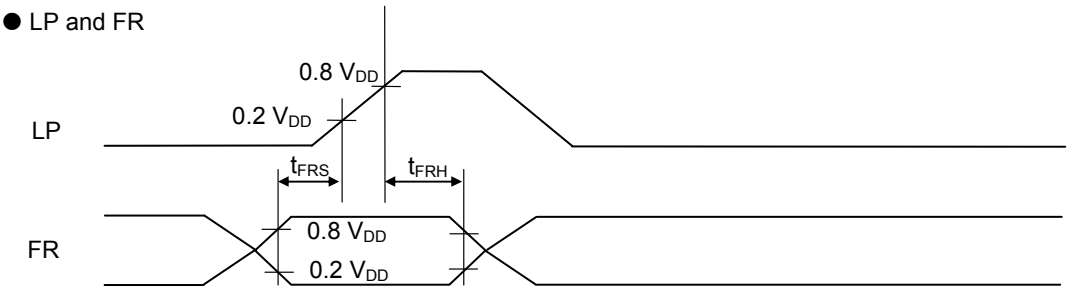


6.4.3 Timing Waveforms of AC Characteristics

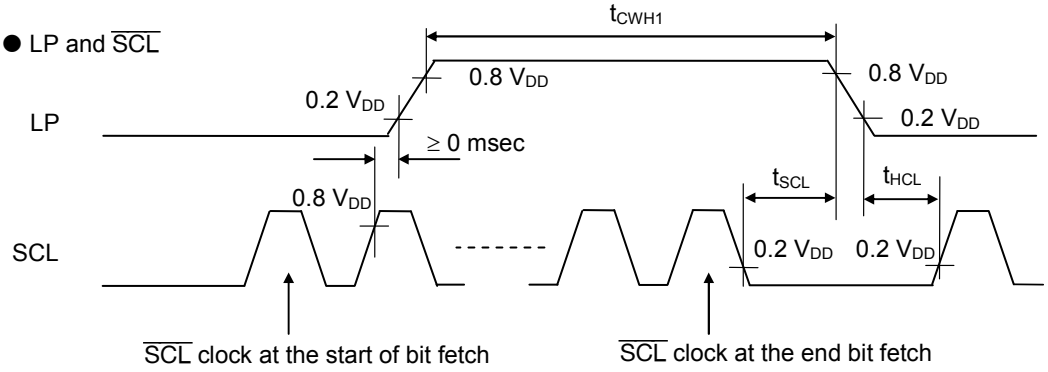
● $\overline{SCL}$ and D0–D7



● LP and FR

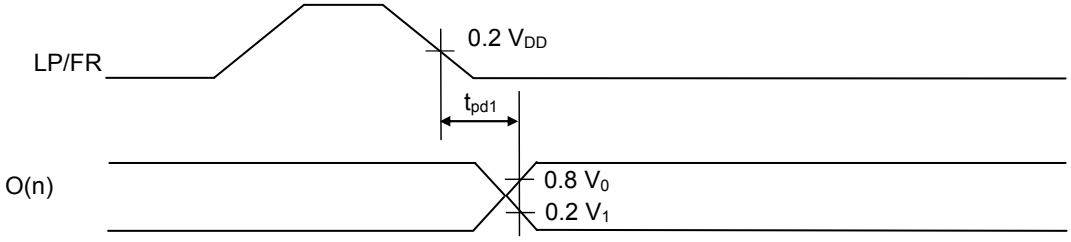


● LP and $\overline{SCL}$



* Keep the following relationships between LP and SCL:
- LP must rise on or after the rise of the $\overline{SCL}$ clock at the second bit after the $\overline{SCL}$ clock at the start of bit fetch.
- LP must rise after the tSCL period following the fall of the $\overline{SCL}$ clock at the end of bit fetch.
- $\overline{SCL}$ mus rise after the tHCL period after LP falls.

● LP and O(n), FR and O(n):DFR=H



7. PAD CONFIGURATION

7.1 Pad Coordinates (Au Bump Chip: ML9461BCVWA)

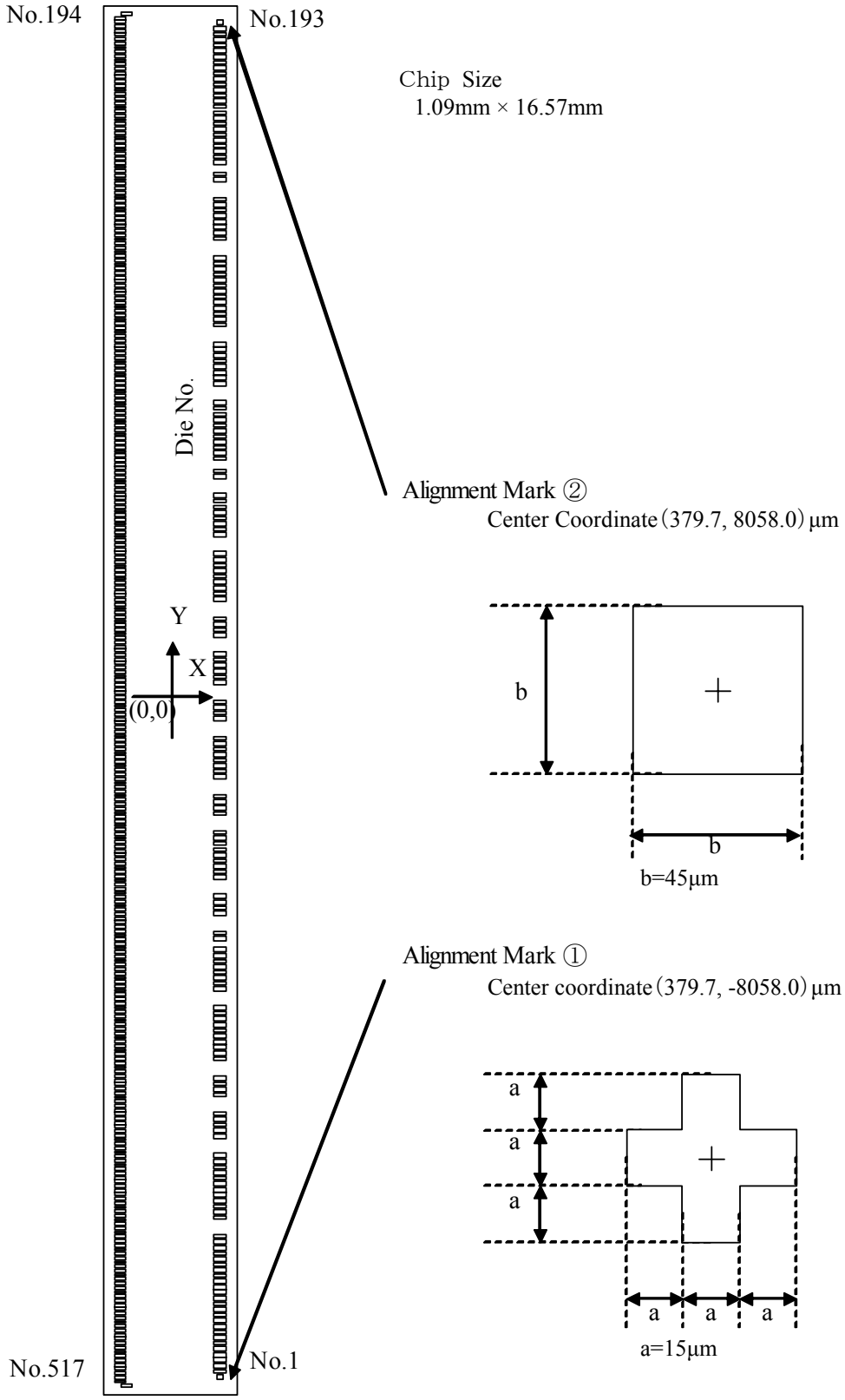
No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]
1	DUMMY	389.7	-7974.1	81	DUMMY	389.7	-1336.5	161	DUMMY	389.7	5632.0	241	O275	-398.0	5727.8
2	DUMMY	389.7	-7908.1	82	DUMMY	389.7	-1270.5	162	DUMMY	389.7	5698.0	242	O274	-398.0	5677.8
3	VCL	389.7	-7842.1	83	DUMMY	389.7	-1204.5	163	DUMMY	389.7	5764.0	243	O273	-398.0	5627.8
4	VCL	389.7	-7776.1	84	DUMMY	389.7	-1138.5	164	DUMMY	389.7	5830.0	244	O272	-398.0	5577.8
5	VCL	389.7	-7710.1	85	D1	389.7	-911.1	165	DUMMY	389.7	5896.0	245	O271	-398.0	5527.7
6	V1L	389.7	-7644.1	86	D1	389.7	-845.1	166	$\overline{\text{EIO2}}$	389.7	6123.4	246	O270	-398.0	5477.7
7	V1L	389.7	-7578.1	87	DUMMY	389.7	-779.1	167	$\overline{\text{EIO2}}$	389.7	6189.4	247	O269	-398.0	5427.7
8	V1L	389.7	-7512.1	88	DUMMY	389.7	-713.1	168	DUMMY	389.7	6324.0	248	O268	-398.0	5377.7
9	MV1L	389.7	-7446.1	89	DUMMY	389.7	-647.1	169	DUMMY	389.7	6390.0	249	O267	-398.0	5327.6
10	MV1L	389.7	-7380.1	90	DUMMY	389.7	-581.1	170	DUMMY	389.7	6456.0	250	O266	-398.0	5277.6
11	MV1L	389.7	-7314.1	91	D2	389.7	-515.1	171	DUMMY	389.7	6522.0	251	O265	-398.0	5227.6
12	VDD	389.7	-7248.1	92	D2	389.7	-449.1	172	DUMMY	389.7	6588.0	252	O264	-398.0	5177.6
13	VDD	389.7	-7182.1	93	DUMMY	389.7	-221.7	173	DUMMY	389.7	6654.0	253	O263	-398.0	5127.5
14	VDD	389.7	-7116.1	94	DUMMY	389.7	-155.7	174	DUMMY	389.7	6720.0	254	O262	-398.0	5077.5
15	DUMMY	389.7	-7050.1	95	DUMMY	389.7	-89.7	175	DUMMY	389.7	6786.0	255	O261	-398.0	5027.5
16	DUMMY	389.7	-6984.1	96	DUMMY	389.7	-23.7	176	DUMMY	389.7	6852.0	256	O260	-398.0	4977.5
17	DUMMY	389.7	-6918.1	97	D3	389.7	203.7	177	DUMMY	389.7	6918.0	257	O259	-398.0	4927.4
18	DUMMY	389.7	-6852.1	98	D3	389.7	269.7	178	DUMMY	389.7	6984.0	258	O258	-398.0	4877.4
19	DUMMY	389.7	-6786.1	99	DUMMY	389.7	335.7	179	DUMMY	389.7	7050.0	259	O257	-398.0	4827.4
20	DUMMY	389.7	-6720.1	100	DUMMY	389.7	401.7	180	VSS	389.7	7116.0	260	O256	-398.0	4777.4
21	DUMMY	389.7	-6654.1	101	D4	389.7	467.7	181	VSS	389.7	7182.0	261	O255	-398.0	4727.3
22	DUMMY	389.7	-6588.1	102	D4	389.7	533.7	182	VSS	389.7	7248.0	262	O254	-398.0	4677.3
23	DUMMY	389.7	-6522.1	103	DUMMY	389.7	761.1	183	MV1R	389.7	7314.0	263	O253	-398.0	4627.3
24	DUMMY	389.7	-6456.1	104	DUMMY	389.7	827.1	184	MV1R	389.7	7380.0	264	O252	-398.0	4577.3
25	DUMMY	389.7	-6390.1	105	DUMMY	389.7	893.1	185	MV1R	389.7	7446.0	265	O251	-398.0	4527.2
26	DUMMY	389.7	-6324.1	106	DUMMY	389.7	959.1	186	V1R	389.7	7512.0	266	O250	-398.0	4477.2
27	SEL1	389.7	-6096.7	107	D5	389.7	1186.5	187	V1R	389.7	7578.0	267	O249	-398.0	4427.2
28	SEL1	389.7	-6030.7	108	D5	389.7	1252.5	188	V1R	389.7	7644.0	268	O248	-398.0	4377.2
29	DUMMY	389.7	-5964.7	109	DUMMY	389.7	1318.5	189	VCR	389.7	7710.0	269	O247	-398.0	4327.1
30	DUMMY	389.7	-5898.7	110	DUMMY	389.7	1384.5	190	VCR	389.7	7776.0	270	O246	-398.0	4277.1
31	DUMMY	389.7	-5832.7	111	DUMMY	389.7	1450.5	191	VCR	389.7	7842.0	271	O245	-398.0	4227.1
32	DUMMY	389.7	-5766.7	112	DUMMY	389.7	1516.5	192	DUMMY	389.7	7908.0	272	O244	-398.0	4177.1
33	DUMMY	389.7	-5700.7	113	DUMMY	389.7	1582.5	193	DUMMY	389.7	7974.0	273	O243	-398.0	4127.0
34	DUMMY	389.7	-5634.7	114	D6	389.7	1648.5	194	DUMMY	-350.2	8079.0	274	O242	-398.0	4077.0
35	DUMMY	389.7	-5568.7	115	D6	389.7	1714.5	195	DUMMY	-398.0	8029.0	275	O241	-398.0	4027.0
36	DUMMY	389.7	-5502.7	116	DUMMY	389.7	1941.9	196	O320	-398.0	7979.0	276	O240	-398.0	3977.0
37	DMS	389.7	-5436.7	117	DUMMY	389.7	2007.9	197	O319	-398.0	7928.9	277	O239	-398.0	3926.9
38	DMS	389.7	-5370.7	118	DUMMY	389.7	2073.9	198	O318	-398.0	7878.9	278	O238	-398.0	3876.9
39	DUMMY	389.7	-5143.3	119	DUMMY	389.7	2139.9	199	O317	-398.0	7828.9	279	O237	-398.0	3826.9
40	DUMMY	389.7	-5077.3	120	DUMMY	389.7	2205.9	200	O316	-398.0	7778.9	280	O236	-398.0	3776.9
41	DUMMY	389.7	-5011.3	121	DUMMY	389.7	2271.9	201	O315	-398.0	7728.8	281	O235	-398.0	3726.8
42	DUMMY	389.7	-4945.3	122	DUMMY	389.7	2337.9	202	O314	-398.0	7678.8	282	O234	-398.0	3676.8
43	DUMMY	389.7	-4879.3	123	DUMMY	389.7	2403.9	203	O313	-398.0	7628.8	283	O233	-398.0	3626.8
44	DFR	389.7	-4651.9	124	D7	389.7	2631.3	204	O312	-398.0	7578.8	284	O232	-398.0	3576.8
45	DFR	389.7	-4585.9	125	D7	389.7	2697.3	205	O311	-398.0	7528.7	285	O231	-398.0	3526.7
46	SEL2	389.7	-4519.9	126	DUMMY	389.7	2837.8	206	O310	-398.0	7478.7	286	O230	-398.0	3476.7
47	SEL2	389.7	-4453.9	127	DUMMY	389.7	2903.8	207	O309	-398.0	7428.7	287	O229	-398.0	3426.7
48	DUMMY	389.7	-4226.5	128	DUMMY	389.7	2969.8	208	O308	-398.0	7378.7	288	O228	-398.0	3376.7
49	DUMMY	389.7	-4160.5	129	DUMMY	389.7	3035.8	209	O307	-398.0	7328.6	289	O227	-398.0	3326.6
50	VSS	389.7	-4094.5	130	DUMMY	389.7	3101.8	210	O306	-398.0	7278.6	290	O226	-398.0	3276.6
51	VSS	389.7	-4028.5	131	DUMMY	389.7	3167.8	211	O305	-398.0	7228.6	291	O225	-398.0	3226.6
52	VSS	389.7	-3962.5	132	DUMMY	389.7	3233.8	212	O304	-398.0	7178.6	292	O224	-398.0	3176.6
53	DUMMY	389.7	-3896.5	133	DUMMY	389.7	3299.8	213	O303	-398.0	7128.5	293	O223	-398.0	3126.5
54	DUMMY	389.7	-3830.5	134	DUMMY	389.7	3365.8	214	O302	-398.0	7078.5	294	O222	-398.0	3076.5
55	DUMMY	389.7	-3764.5	135	$\overline{\text{SCL}}$	389.7	3431.8	215	O301	-398.0	7028.5	295	O221	-398.0	3026.5
56	DUMMY	389.7	-3698.5	136	$\overline{\text{SCL}}$	389.7	3497.8	216	O300	-398.0	6978.5	296	O220	-398.0	2976.5
57	DUMMY	389.7	-3632.5	137	DUMMY	389.7	3725.2	217	O299	-398.0	6928.4	297	O219	-398.0	2926.4
58	SHL	389.7	-3405.1	138	DUMMY	389.7	3791.2	218	O298	-398.0	6878.4	298	O218	-398.0	2876.4
59	SHL	389.7	-3339.1	139	DUMMY	389.7	3857.2	219	O297	-398.0	6828.4	299	O217	-398.0	2826.4
60	DUMMY	389.7	-3273.1	140	DUMMY	389.7	3923.2	220	O296	-398.0	6778.4	300	O216	-398.0	2776.4
61	DUMMY	389.7	-3207.1	141	DUMMY	389.7	3989.2	221	O295	-398.0	6728.3	301	O215	-398.0	2726.3
62	DUMMY	389.7	-3141.1	142	DUMMY	389.7	4055.2	222	O294	-398.0	6678.3	302	O214	-398.0	2676.3
63	DUMMY	389.7	-3075.1	143	DUMMY	389.7	4121.2	223	O293	-398.0	6628.3	303	O213	-398.0	2626.3
64	DUMMY	389.7	-3009.1	144	DUMMY	389.7	4187.2	224	O292	-398.0	6578.3	304	O212	-398.0	2576.3
65	DUMMY	389.7	-2943.1	145	LP	389.7	4414.6	225	O291	-398.0	6528.2	305	O211	-398.0	2526.2
66	$\overline{\text{EIO1}}$	389.7	-2808.5	146	LP	389.7	4480.6	226	O290	-398.0	6478.2	306	O210	-398.0	2476.2
67	$\overline{\text{EIO1}}$	389.7	-2742.5	147	DUMMY	389.7	4546.6	227	O289	-398.0	6428.2	307	O209	-398.0	2426.2
68	DUMMY	389.7	-2517.3	148	DUMMY	389.7	4612.6	228	O288	-398.0	6378.2	308	O208	-398.0	2376.2
69	DUMMY	389.7	-2451.3	149	DUMMY	389.7	4678.6	229	O287	-398.0	6328.1	309	O207	-398.0	2326.1
70	DUMMY	389.7	-2385.3	150	DUMMY	389.7	4744.6	230	O286	-398.0	6278.1	310	O206	-398.0	2276.1
71	DUMMY	389.7	-2319.3	151	DUMMY	389.7	4810.6	231	O285	-398.0	6228.1	311	O205	-398.0	2226.1
72	$\overline{\text{DSPOF}}$	389.7	-2091.9	152	DUMMY	389.7	4876.6	232	O284	-398.0	6178.1	312	O204	-398.0	2176.1
73	$\overline{\text{DSPOF}}$	389.7	-2025.9	153	DUMMY	389.7	4942.6	233	O283	-398.0	6128.0	313	O203	-398.0	2126.0
74	DUMMY	389.7	-1959.9	154	DUMMY	389.7	5008.6	234	O282	-398.0	6078.0	314	O202	-398.0	2076.0
75	DUMMY	389.7	-1893.9	155	DUMMY	389.7	5074.6	235	O281	-398.0	6028.0	315	O201	-398.0	2026.0
76	DUMMY	389.7	-1827.9	156	FR	389.7	5140.6	236	O280	-398.0	5978.0	316	O200	-398.0	1976.0
77	DUMMY	389.7	-1761.9	157	FR	389.7	5206.6	237	O279	-398.0	5927.9	317	O199	-398.0	1925.9
78	DUMMY	389.7	-1695.9	158	DUMMY	389.7	5434.0	238	O278	-398.0	5877.9	318	O198	-398.0	1875.9
79	D0	389.7	-1629.9	159	DUMMY	389.7	5500.0	239	O277	-398.0	5827.9	319	O197	-398.0	1825.9
80	D0	389.7	-1563.9	160	DUMMY	389.7	5566.0	240	O276	-398.0	5777.9	320	O196	-398.0	1775.9

Note: Leave DUMMY pads open.

No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]	No.	Pad name	x-coordinate [μm]	y-coordinate [μm]
321	O195	-398.0	1725.8	371	O145	-398.0	-775.4	421	O95	-398.0	-3276.7	471	O45	-398.0	-5777.9
322	O194	-398.0	1675.8	372	O144	-398.0	-825.5	422	O94	-398.0	-3326.7	472	O44	-398.0	-5828.0
323	O193	-398.0	1625.8	373	O143	-398.0	-875.5	423	O93	-398.0	-3376.7	473	O43	-398.0	-5878.0
324	O192	-398.0	1575.8	374	O142	-398.0	-925.5	424	O92	-398.0	-3426.8	474	O42	-398.0	-5928.0
325	O191	-398.0	1525.7	375	O141	-398.0	-975.5	425	O91	-398.0	-3476.8	475	O41	-398.0	-5978.0
326	O190	-398.0	1475.7	376	O140	-398.0	-1025.6	426	O90	-398.0	-3526.8	476	O40	-398.0	-6028.1
327	O189	-398.0	1425.7	377	O139	-398.0	-1075.6	427	O89	-398.0	-3576.8	477	O39	-398.0	-6078.1
328	O188	-398.0	1375.7	378	O138	-398.0	-1125.6	428	O88	-398.0	-3626.9	478	O38	-398.0	-6128.1
329	O187	-398.0	1325.6	379	O137	-398.0	-1175.6	429	O87	-398.0	-3676.9	479	O37	-398.0	-6178.1
330	O186	-398.0	1275.6	380	O136	-398.0	-1225.7	430	O86	-398.0	-3726.9	480	O36	-398.0	-6228.2
331	O185	-398.0	1225.6	381	O135	-398.0	-1275.7	431	O85	-398.0	-3776.9	481	O35	-398.0	-6278.2
332	O184	-398.0	1175.6	382	O134	-398.0	-1325.7	432	O84	-398.0	-3827.0	482	O34	-398.0	-6328.2
333	O183	-398.0	1125.5	383	O133	-398.0	-1375.7	433	O83	-398.0	-3877.0	483	O33	-398.0	-6378.2
334	O182	-398.0	1075.5	384	O132	-398.0	-1425.8	434	O82	-398.0	-3927.0	484	O32	-398.0	-6428.3
335	O181	-398.0	1025.5	385	O131	-398.0	-1475.8	435	O81	-398.0	-3977.0	485	O31	-398.0	-6478.3
336	O180	-398.0	975.5	386	O130	-398.0	-1525.8	436	O80	-398.0	-4027.1	486	O30	-398.0	-6528.3
337	O179	-398.0	925.4	387	O129	-398.0	-1575.8	437	O79	-398.0	-4077.1	487	O29	-398.0	-6578.3
338	O178	-398.0	875.4	388	O128	-398.0	-1625.9	438	O78	-398.0	-4127.1	488	O28	-398.0	-6628.4
339	O177	-398.0	825.4	389	O127	-398.0	-1675.9	439	O77	-398.0	-4177.1	489	O27	-398.0	-6678.4
340	O176	-398.0	775.4	390	O126	-398.0	-1725.9	440	O76	-398.0	-4227.2	490	O26	-398.0	-6728.4
341	O175	-398.0	725.3	391	O125	-398.0	-1775.9	441	O75	-398.0	-4277.2	491	O25	-398.0	-6778.4
342	O174	-398.0	675.3	392	O124	-398.0	-1826.0	442	O74	-398.0	-4327.2	492	O24	-398.0	-6828.5
343	O173	-398.0	625.3	393	O123	-398.0	-1876.0	443	O73	-398.0	-4377.2	493	O23	-398.0	-6878.5
344	O172	-398.0	575.3	394	O122	-398.0	-1926.0	444	O72	-398.0	-4427.3	494	O22	-398.0	-6928.5
345	O171	-398.0	525.2	395	O121	-398.0	-1976.0	445	O71	-398.0	-4477.3	495	O21	-398.0	-6978.5
346	O170	-398.0	475.2	396	O120	-398.0	-2026.1	446	O70	-398.0	-4527.3	496	O20	-398.0	-7028.6
347	O169	-398.0	425.2	397	O119	-398.0	-2076.1	447	O69	-398.0	-4577.3	497	O19	-398.0	-7078.6
348	O168	-398.0	375.2	398	O118	-398.0	-2126.1	448	O68	-398.0	-4627.4	498	O18	-398.0	-7128.6
349	O167	-398.0	325.1	399	O117	-398.0	-2176.1	449	O67	-398.0	-4677.4	499	O17	-398.0	-7178.6
350	O166	-398.0	275.1	400	O116	-398.0	-2226.2	450	O66	-398.0	-4727.4	500	O16	-398.0	-7228.7
351	O165	-398.0	225.1	401	O115	-398.0	-2276.2	451	O65	-398.0	-4777.4	501	O15	-398.0	-7278.7
352	O164	-398.0	175.1	402	O114	-398.0	-2326.2	452	O64	-398.0	-4827.5	502	O14	-398.0	-7328.7
353	O163	-398.0	125.0	403	O113	-398.0	-2376.2	453	O63	-398.0	-4877.5	503	O13	-398.0	-7378.7
354	O162	-398.0	75.0	404	O112	-398.0	-2426.3	454	O62	-398.0	-4927.5	504	O12	-398.0	-7428.8
355	O161	-398.0	25.0	405	O111	-398.0	-2476.3	455	O61	-398.0	-4977.5	505	O11	-398.0	-7478.8
356	O160	-398.0	-25.1	406	O110	-398.0	-2526.3	456	O60	-398.0	-5027.6	506	O10	-398.0	-7528.8
357	O159	-398.0	-75.1	407	O109	-398.0	-2576.3	457	O59	-398.0	-5077.6	507	O9	-398.0	-7578.8
358	O158	-398.0	-125.1	408	O108	-398.0	-2626.4	458	O58	-398.0	-5127.6	508	O8	-398.0	-7628.9
359	O157	-398.0	-175.1	409	O107	-398.0	-2676.4	459	O57	-398.0	-5177.6	509	O7	-398.0	-7678.9
360	O156	-398.0	-225.2	410	O106	-398.0	-2726.4	460	O56	-398.0	-5227.7	510	O6	-398.0	-7728.9
361	O155	-398.0	-275.2	411	O105	-398.0	-2776.4	461	O55	-398.0	-5277.7	511	O5	-398.0	-7778.9
362	O154	-398.0	-325.2	412	O104	-398.0	-2826.5	462	O54	-398.0	-5327.7	512	O4	-398.0	-7829.0
363	O153	-398.0	-375.2	413	O103	-398.0	-2876.5	463	O53	-398.0	-5377.7	513	O3	-398.0	-7879.0
364	O152	-398.0	-425.3	414	O102	-398.0	-2926.5	464	O52	-398.0	-5427.8	514	O2	-398.0	-7929.0
365	O151	-398.0	-475.3	415	O101	-398.0	-2976.5	465	O51	-398.0	-5477.8	515	O1	-398.0	-7979.0
366	O150	-398.0	-525.3	416	O100	-398.0	-3026.6	466	O50	-398.0	-5527.8	516	DUMMY	-398.0	-8029.1
367	O149	-398.0	-575.3	417	O99	-398.0	-3076.6	467	O49	-398.0	-5577.8	517	DUMMY	-350.2	-8079.1
368	O148	-398.0	-625.4	418	O98	-398.0	-3126.6	468	O48	-398.0	-5627.9				
369	O147	-398.0	-675.4	419	O97	-398.0	-3176.6	469	O47	-398.0	-5677.9				
370	O146	-398.0	-725.4	420	O96	-398.0	-3226.7	470	O46	-398.0	-5727.9				

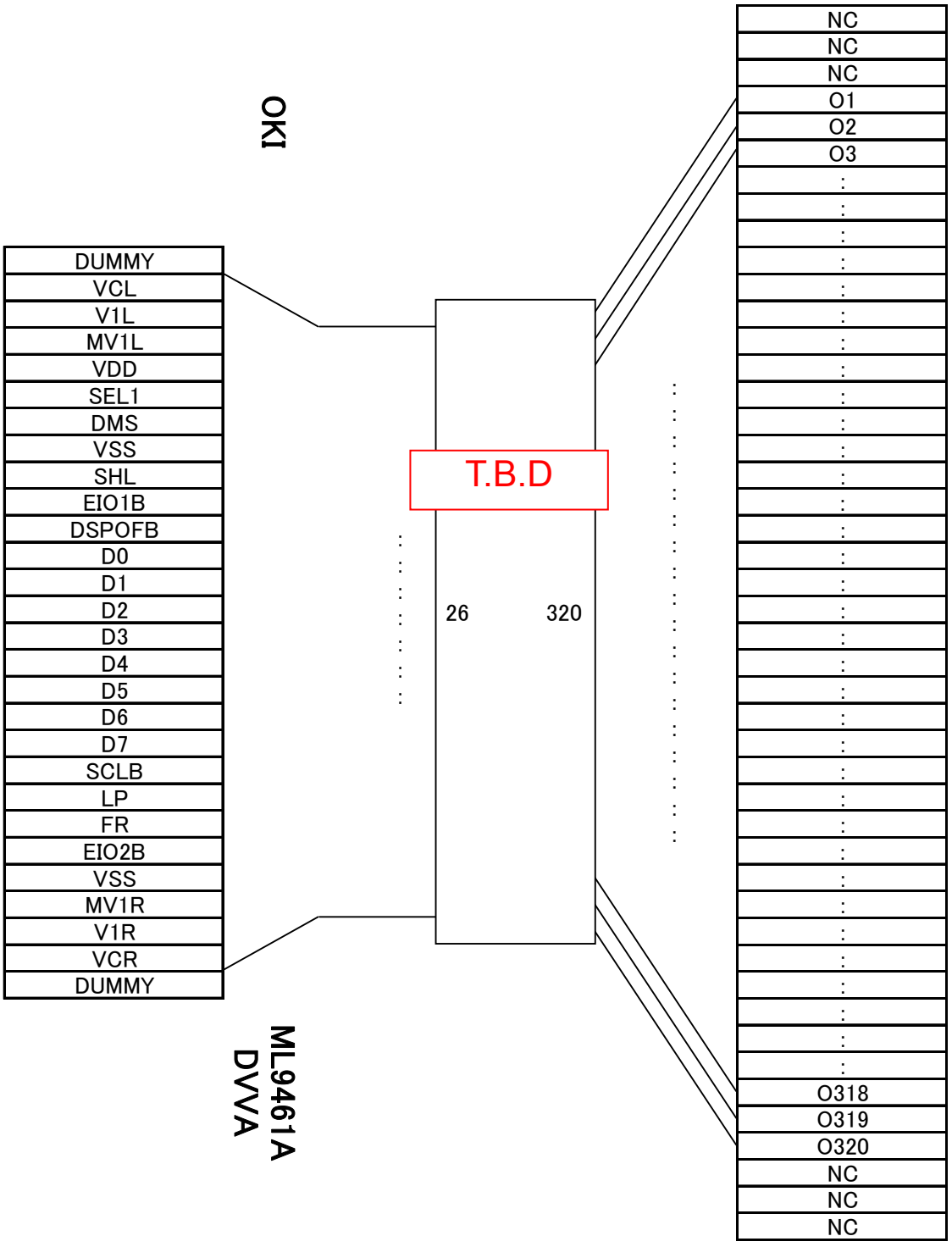
Note: Leave DUMMY pads open.

Alignment Mark Information



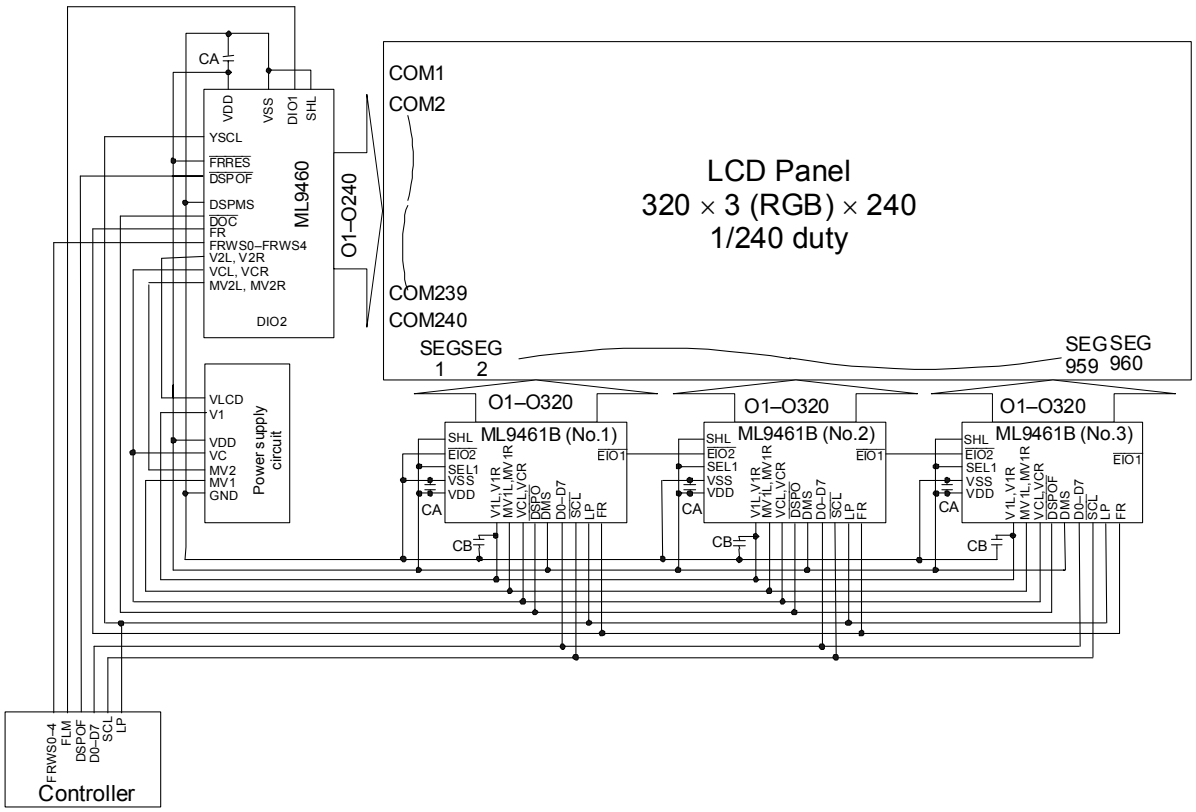
7.2 Pin Configuration (TCP: ML9461ADVVA)

TOP VIEW



The drawing shown does not specify the exact outline of the TCP;it only specifies the pin layout.

8. Application Circuit (With External Components Connected)



Insert a capacitor CA,CB specified in the Recommended Operating Conditions (Guaranteed Operating Range).
It is recommended that 0.1 μF CA capacitors (JIS (Japanese Industrial Standards) FJ(F) equivalent) be used.

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9461-01	May 21, 2007	–	–	Preliminary edition 1
PEDL9461-02	Dec 5, 2007	1	1	Au Bump Chip product name DVWA→CVWA
		6-9	6-9	Changed the data allocation at DMS=H.
		13	13	Additional comment.
		14	14	Shutdown Sequence 0.8VDD→2.5V
		15	15	Changed Note.
		16	16	Additional condition of supply current. TBD→provide spec.
		18	18	SCL “L” level width 15ns→20ns
		20	20	Additional comment.
		-	23	Additional 7.2 Pin Configuration.
		23	24	Changed Application Circuit.
PEDL9461-03	Dec 17,2008	–	–	Changed to OKI semiconductor’s format
				ML9461→ML9461B
FEDL9461-01	Jan 29,2009	–	–	Final edition 1
		–	3	Additional 2.2 Inupt and Output Configuration.
		–	12	Additional 4.1.7 Output control function by DFR pin. （Supplement Explanation.）
		13	15	Changed explanation
		14	16	Changed Time Chart
		–	25	Additional Alignment Mark Information.

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