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# ML7074-004

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## VoIP CODEC

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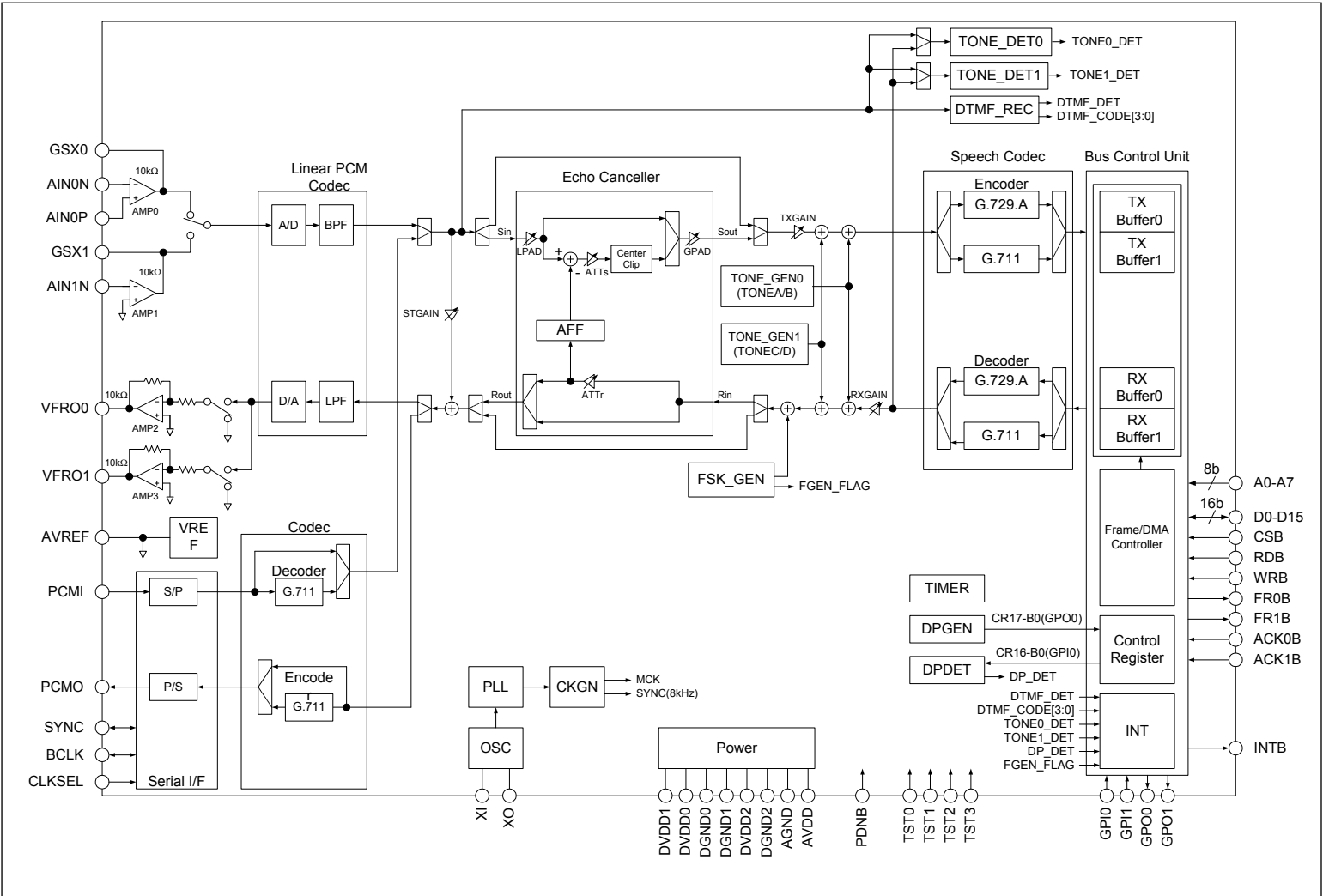
### GENERAL DESCRIPTION

The ML7074-004 is a speech CODEC for VoIP. This LSI allows selection of G.729.A, or G.711 standard as a speech CODEC. The LSI is optimum for adding VoIP functions to TAs, routers, etc., since it has the functions of an echo canceller for 32 ms delay, DTMF detection, tone detection, tone generation, etc.

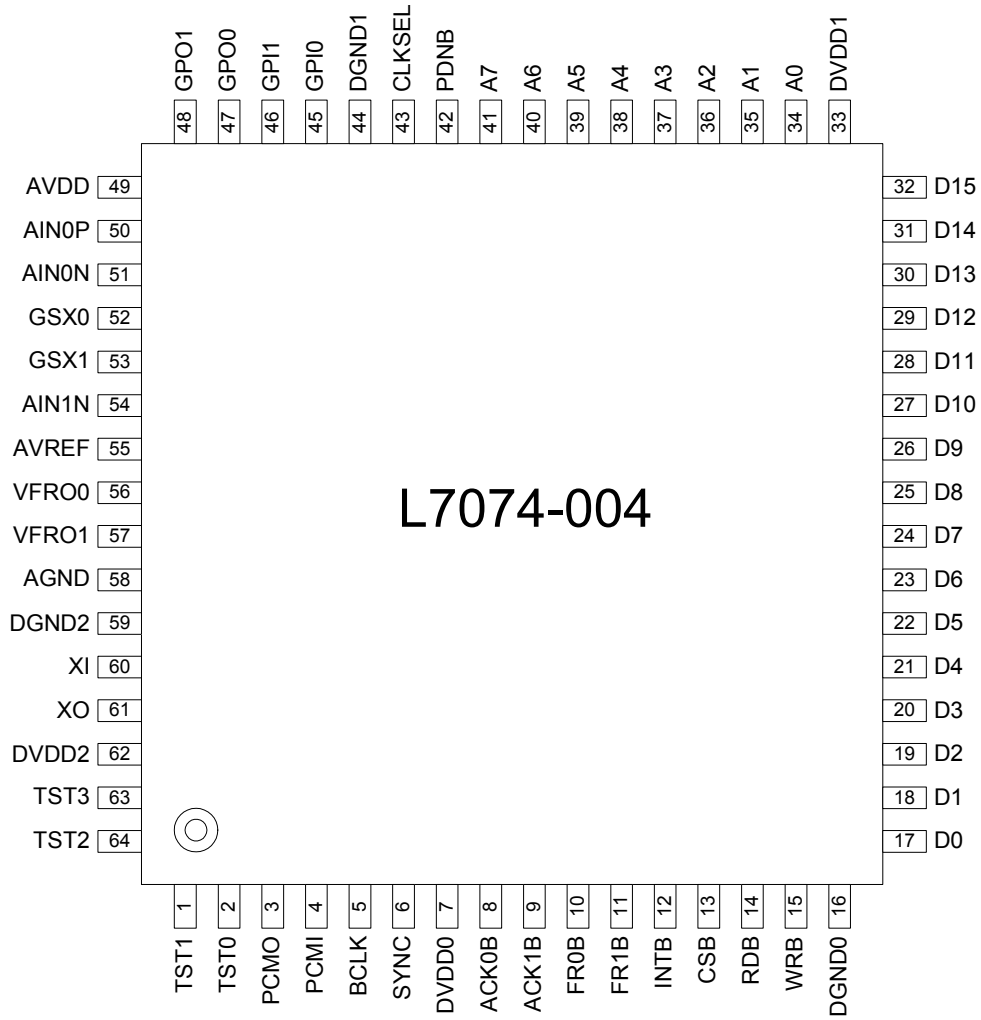
### FEATURES

- Single 3.3 V power supply operation ( $DV_{DD0, 1, 2}, AV_{DD}$ : 3.0 to 3.6 V)
- Speech CODEC:
  - Selectable among G.729.A (8 kbps), G.711 (64 kbps)  $\mu$ -law, and A-law
  - Supports PLC (Packet Loss Concealment) function conforming to ITU-T G.711 Appendix I
- Echo canceller for 32 ms delay
- DTMF detect function
- Tone detect function: 2 systems (1650 Hz, 2100 Hz: Detect frequency can be changed.)
- Tone generate function: 2 systems
- FSK generation function
- Dial pulse detect function
- Dial pulse transmit function
- Internal 1-channel 16-bit timer
- Built-in FIFO buffers (640 bytes) for transferring transmit and receive data
  - Frame/DMA (slave) interface selectable.
- Master clock frequency: 4.096 MHz (crystal oscillation or external input)
- Hardware or software power down operation possible.
- Analog input/output type:
  - Two built-in input amplifiers
  - Two built-in output amplifiers, 10 k $\Omega$  driving
- Package:
  - 64-pin plastic QFP (QFP64-P-1414-0.80-BK)
- Ordering part number:
  - ML7074-004GA

**BLOCK DIAGRAM**



**PIN ASSIGNMENT (TOP VIEW)**



**64-pin plastic QFP**

## PIN DESCRIPTIONS

Pin No.	Symbol	I/O	PDNB = "0"	Description
1	TST1	I	"0"	Test control input 1: Normally input "0".
2	TST0	I	"0"	Test control input 0: Normally input "0".
3	PCMO	O	"Hi-z"	PCM data output
4	PCMI	I	I	PCM data input
5	BCLK	I/O	I	CLKSEL = "0" PCM shift clock input
			"L"	CLKSEL = "1" PCM shift clock output
6	SYNC	I/O	I	CLKSEL = "0" PCM sync signal 8 kHz input
			"L"	CLKSEL = "1" PCM sync signal 8 kHz output
7	DV <sub>DD0</sub>	—	—	Digital power supply
8	ACK0B	I	I	Transmit buffer DMA access acknowledge signal input
9	ACK1B	I	I	Receive buffer DMA access acknowledge signal input
10	FR0B (DMARQ0B)	O	"H"	FR0B: (CR11-B7 = "0") Transmit buffer frame signal output
				DMARQ0B: (CR11-B7 = "1") Transmit buffer DMA access request signal output
11	FR1B (DMARQ1B)	O	"H"	FR1B: (CR11-B7 = "0") Receive buffer frame signal output
				DMARQ1B: (CR11-B7 = "1") Receive buffer DMA access request signal output
12	INTB	O	"H"	Interrupt request output "L" level is output for about 1.0 μs when an interrupt is generated.
13	CSB	I	I	Chip select control input
14	RDB	I	I	Read control input
15	WRB	I	I	Write control input
16	DGND0	—	I	Digital ground (0.0 V)
17	D0	I/O	I	Data input/output
18	D1	I/O	I	Data input/output
19	D2	I/O	I	Data input/output
20	D3	I/O	I	Data input/output
21	D4	I/O	I	Data input/output
22	D5	I/O	I	Data input/output
23	D6	I/O	I	Data input/output
24	D7	I/O	I	Data input/output
25	D8	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").
26	D9	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").
27	D10	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").
28	D11	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").
29	D12	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").
30	D13	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").
31	D14	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").
32	D15	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").

Pin No.	Symbol	I/O	PDNB = "0"	Description
33	DV <sub>DD1</sub>	—	—	Digital power supply
34	A0	I	I	Address input
35	A1	I	I	Address input
36	A2	I	I	Address input
37	A3	I	I	Address input
38	A4	I	I	Address input
39	A5	I	I	Address input
40	A6	I	I	Address input
41	A7	I	I	Address input
42	PDNB	I	"0"	Power down input "0": Power down reset "1": Normal operation
43	CLKSEL	I	I	SYNC and BCLK I/O control input "0": SYNC and BCLK become inputs "1": SYNC and BCLK become outputs
44	DGND1	—	—	Digital ground (0.0 V)
45	GPI0	I	I	General-purpose input pin 0 (5 V tolerant input) /Secondary function: Dial pulse detect input pin
46	GPI1	I	I	General-purpose input pin 1 (5 V tolerant input)
47	GPO0	O	"L"	General-purpose output pin 0 (5 V tolerant output, can be pulled up externally) /Secondary function: Dial pulse transmit pin
48	GPO1	O	"L"	General-purpose output pin 1 (5 V tolerant output, can be pulled up externally)
49	AV <sub>DD</sub>	—	—	Analog power supply
50	AIN0P	I	I	AMP0 non-inverted input
51	AIN0N	I	I	AMP0 inverted input
52	GSX0	O	"Hi-z"	AMP0 output (10 kΩ driving)
53	GSX1	O	"Hi-z"	AMP1 output (10 kΩ driving)
54	AIN1N	I	I	AMP1 inverted input
55	AVREF	O	"L"	Analog signal ground (1.4 V)
56	VFRO0	O	"Hi-z"	AMP2 Output (10 kΩ driving)
57	VFRO1	O	"Hi-z"	AMP3 Output (10 kΩ driving)
58	AGND	—	—	Analog ground (0.0 V)
59	DGND2	—	—	Digital ground (0.0 V)
60	XI	I	I	4.096 MHz crystal oscillator I/F, 4.096 MHz clock input
61	XO	O	"H"	4.096 MHz crystal oscillator I/F
62	DV <sub>DD2</sub>	—	—	Digital power supply
63	TST3	I	"0"	Test control input 3: Normally input "0".
64	TST2	I	"0"	Test control input 2: Normally input "0".

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Rating	Unit
Analog power supply voltage	VDA	—	-0.3 to 5.0	V
Digital power supply voltage	V <sub>DD</sub>	—	-0.3 to 5.0	V
Analog input voltage	VAIN	Analog pins	-0.3 to V <sub>DD</sub> + 0.3	V
Digital input voltage	VDIN1	Normal digital pins	-0.3 to V <sub>DD</sub> + 0.3	V
	VDIN2	5 V tolerant pins	-0.3 to 6.0	V
Storage temperature range	Tstg	—	-55 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

(Unless otherwise specified, AV<sub>DD</sub> = 3.0 to 3.6 V, DV<sub>DD</sub>0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = -20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Analog power supply voltage	VDA	—	3.0	3.3	3.6	V
Digital power supply voltage	V <sub>DD</sub>	—	3.0	3.3	3.6	V
Operating temperature range	Ta	—	-20	—	60	°C
Digital high level input voltage	VIH1	Digital input pins	2.0	—	V <sub>DD</sub> +0.3	V
	VIH2	GPI0 and GPI1 pins	2.0	—	5.5	V
Digital low level input voltage	VIL	Digital pins	-0.3	—	0.8	V
Digital input rise time	tIR	Digital pins	—	2	20	ns
Digital input fall time	tIF	Digital pins	—	2	20	ns
Digital output load capacitance	CDL	Digital pins	—	—	50	pF
Capacitance of bypass capacitor for AVREF	Cvref	Between AVREF and AGND	2.2+0.1	—	4.7+0.1	μF
Master clock frequency	Fmck	MCK	-0.01%	4.096	+0.01%	MHz
PCM shift clock frequency	Fbclk	BCLK (at input)	64	—	2048	kHz
PCM sync signal frequency	Fsync	SYNC (at input)	—	8.0	—	kHz
Clock duty ratio	DRCLK	MCK, BCLK (at input)	40	50	60	%
PCM sync timing	tBS	BCLK to SYNC (at input)	100	—	—	ns
	tSB	SYNC to BCLK (at input)	100	—	—	ns
PCM sync signal width	tWS	SYNC (at input)	1BCLK	—	100	μs

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

(Unless otherwise specified,  $V_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply current	I <sub>SS</sub>	Standby state (PDNB = "0", $V_{DD} = 3.3$ V, $T_a = 25^\circ\text{C}$ )	—	5.0	20.0	$\mu\text{A}$
	I <sub>DD1</sub>	Operating state 1 In the PCM/IF mode (SC_EN = "1", PCMIF_EN = "1", AFE_EN = "1") Connect a 4.096 MHz crystal oscillator between XI and XO.	—	45.0	55.0	mA
	I <sub>DD2</sub>	Operating state 2 When operating the whole system (SC_EN = "1", PCMIF_EN = "0", AFE_EN = "0") Connect a 4.096 MHz crystal oscillator between XI and XO.	—	50.0	65.0	mA
Digital input pin input leakage current	I <sub>IH</sub>	$V_{in} = DV_{DD}$	—	0.01	1.0	$\mu\text{A}$
	I <sub>IL</sub>	$V_{in} = DGND$	-1.0	-0.01	—	$\mu\text{A}$
Digital I/O pin output leakage current	I <sub>OZH</sub>	$V_{out} = DV_{DD}$	—	0.01	1.0	$\mu\text{A}$
	I <sub>OZL</sub>	$V_{out} = DGND$	-1.0	-0.01	—	$\mu\text{A}$
High level output voltage	V <sub>OH</sub>	Digital output pins, I/O pins I <sub>OH</sub> = 4.0 mA I <sub>OH</sub> = 1.0 mA (XO pin)	2.2	—	—	V
Low level output voltage	V <sub>OL</sub>	Digital output pins, I/O pins I <sub>OL</sub> = -4.0 mA I <sub>OL</sub> = -1.0 mA (XO pin)	—	—	0.4	V
Input capacitance *1	C <sub>IN</sub>	Input pins	—	8	12	pF

Note: \*1 Guaranteed design value

**Analog Interface**

(Unless otherwise specified,  $AV_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input resistance *1	RIN	AIN0N, AIN0P, AIN1N	10	—	—	M $\Omega$
Output load resistance	RL	GSX0, GSX1, VFRO0, VFRO1	10	—	—	k $\Omega$
Output load capacitance	CL	Analog output pins	—	—	50	pF
Offset voltage	VOF	VFRO0, VFRO1	-40	—	40	mV
Output voltage level *2	VO	GSX0, GSX1, VFRO0, VFRO1 RL = 10 k $\Omega$	—	—	1.3	Vpp

**Notes:**

\*1 Guaranteed design value

\*2  $-7.7$  dBm ( $600\Omega$ ) = 0 dBm0,  $+3.17$  dBm0 = 1.3 Vpp

## AC Characteristics

**CODEC (Speech CODEC in G.711 ( $\mu$ -law) Mode)**

(Unless otherwise specified, AV<sub>DD</sub> = 3.0 to 3.6 V, DV<sub>DD0</sub>, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = -20 to +60°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)				
Transmit frequency characteristics	LT1	0 to 60	0	25	—	—	dB
	LT2	300 to 3000		-0.15	—	0.20	dB
	LT3	1020		Reference value			—
	LT4	3300		-0.15	—	0.80	dB
	LT5	3400		0	—	0.80	dB
	LT6	3968.75		13	—	—	dB
Receive frequency characteristics	LR2	0 to 3000	0	-0.15	—	0.20	dB
	LR3	1020		Reference value			—
	LR4	3300		-0.15	—	0.80	dB
	LR5	3400		0	—	0.80	dB
	LR6	3968.75		13	—	—	dB
Transmit signal to noise ratio [*1]	SDT1	1020	3	35	—	—	dBp
	SDT2		0	35	—	—	dBp
	SDT3		-30	35	—	—	dBp
	SDT4		-40	28	—	—	dBp
	SDT5		-45	23	—	—	dBp
Receive signal to noise ratio [*1]	SDR1	1020	3	35	—	—	dBp
	SDR2		0	35	—	—	dBp
	SDR3		-30	35	—	—	dBp
	SDR4		-40	28	—	—	dBp
	SDR5		-45	23	—	—	dBp
Transmit inter-level loss error	GTT1	1020	3	-0.2	—	0.2	dB
	GTT2		-10	Reference value			—
	GTT3		-40	-0.2	—	0.2	dB
	GTT4		-50	-0.6	—	0.6	dB
	GTT5		-55	-1.2	—	1.2	dB
Receive inter-level loss error	GTR1	1020	3	-0.2	—	0.2	dB
	GTR2		-10	Reference value			—
	GTR3		-40	-0.2	—	0.2	dB
	GTR4		-50	-0.6	—	0.6	dB
	GTR5		-55	-1.2	—	1.2	dB
Idle channel noise [*1]	NIDL <sub>T</sub>	—	Analog input = AVREF	—	—	-68	dBm0p
	NIDL <sub>R</sub>	—	PCMI = "1"	—	—	-72	dBm0p
Transmit absolute level [*2]	AVT	1020	0	0.285	0.320	0.359	Vrms
Receive absolute level [*2]	AVR	1020	0	0.285	0.320	0.359	Vrms
Power supply noise reject ratio	PSRRT	Noise frequency range: 0 to 50 kHz Noise level: 50mVpp	—	30	—	—	dB
	PSRRR		—	30	—	—	dB

Notes: \*1 Using P-message filter

\*2 0.320 Vrms = 0 dBm0 = -7.7 dBm (600Ω)

**Gain Setting (Speech CODEC in G.711 ( $\mu$ -law) Mode)**

(Unless otherwise specified,  $AV_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transmit and receive gain setting accuracy	GAC	—	-1.0	—	1.0	dB

**Tone Output (Speech CODEC in G.711 ( $\mu$ -law) Mode)**

(Unless otherwise specified,  $AV_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency deviation	fDFT	Relative to set frequency	-1.5	—	1.5	%
Output level	oLEV	Relative to set gain	-2.0	—	2.0	dB

**DTMF Detector, Other Detectors (Speech CODEC in G.711 ( $\mu$ -law) Mode)**

(Unless otherwise specified,  $AV_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

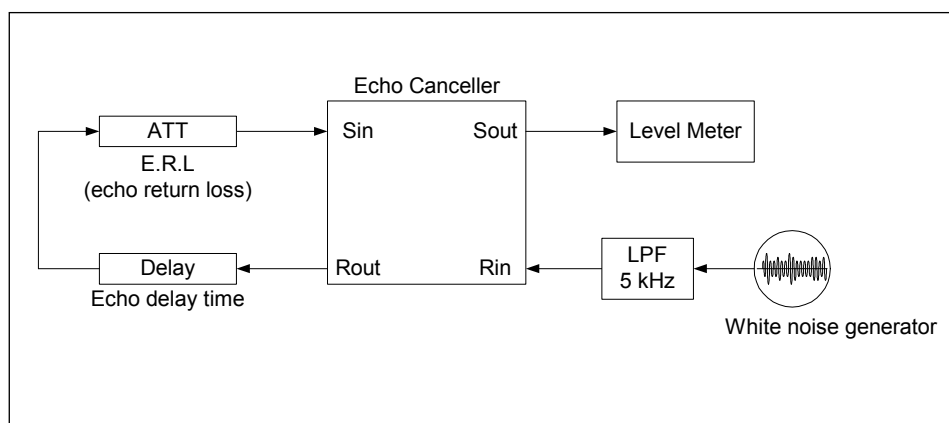
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detect level accuracy	dLAC	Relative to set detect level	-2.5	—	2.5	dB

**Echo Canceller**

(Unless otherwise specified,  $AV_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Echo attenuation	eRES	In the analog I/F mode	—	35	—	dB
		In the PCM I/F (16-bit linear) mode		30		
		In the PCM I/F (G.711) mode				
Erasable echo delay time	tECT	—	—	32	ms	

Measurement method

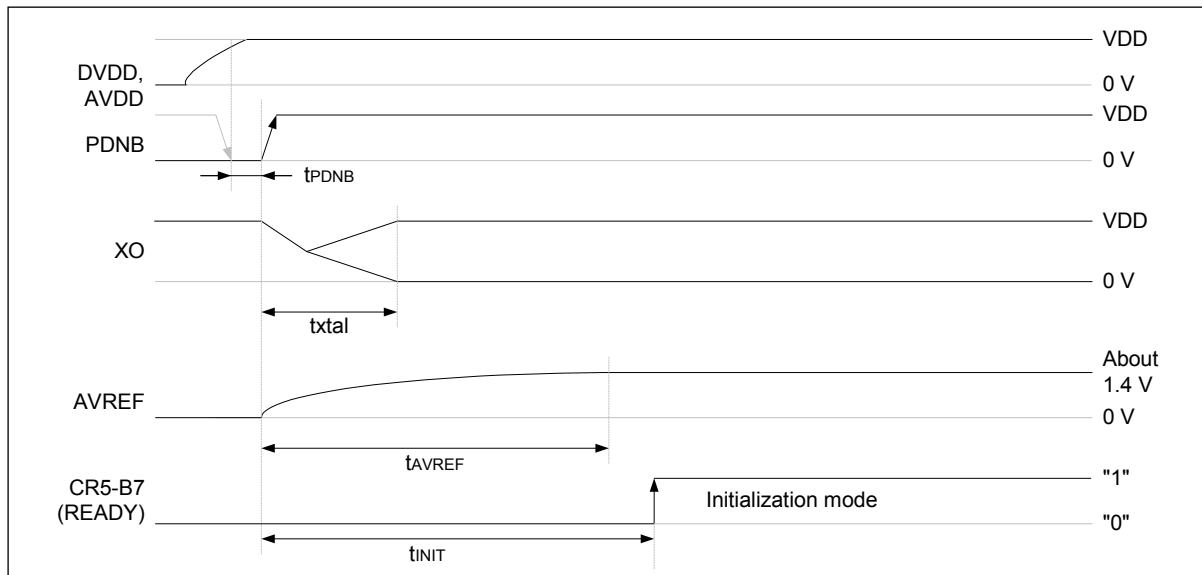


**PDNB, XO, AVREF Timings**

(Unless otherwise specified,  $AV_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power down signal pulse width	tPDNB	PDNB pin	1	—	—	$\mu\text{s}$
Oscillation start-up time	txtal	—	—	$2+\alpha$	100	ms
AVREF rise time	tAVREF	AVREF = 1.4 (90%) C5 = 4.7 $\mu\text{F}$ , C6 = 0.1 $\mu\text{F}$ (See Fig. 9.)	—	—	600	ms
Initialization mode start-up time	tINIT	—	—	1	—	s

\*  $\alpha$  is a value that depends on the oscillation stabilizing time when using a crystal oscillator.

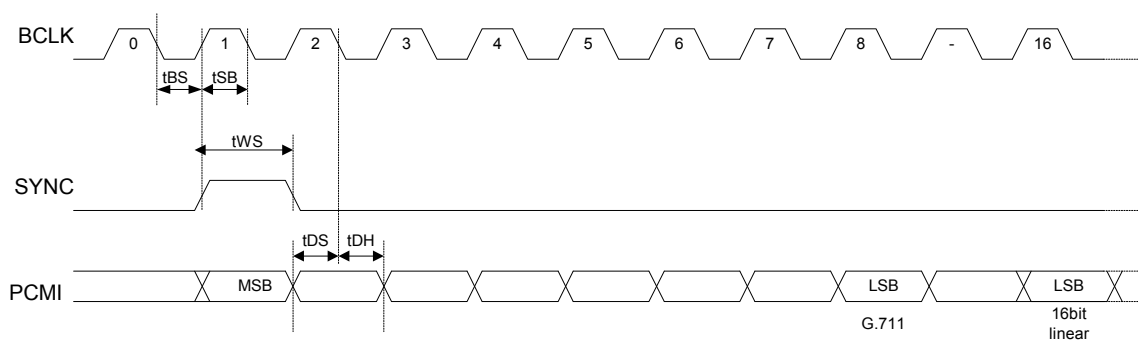


**Fig. 1 PDNB, XO, and AVREF timings**

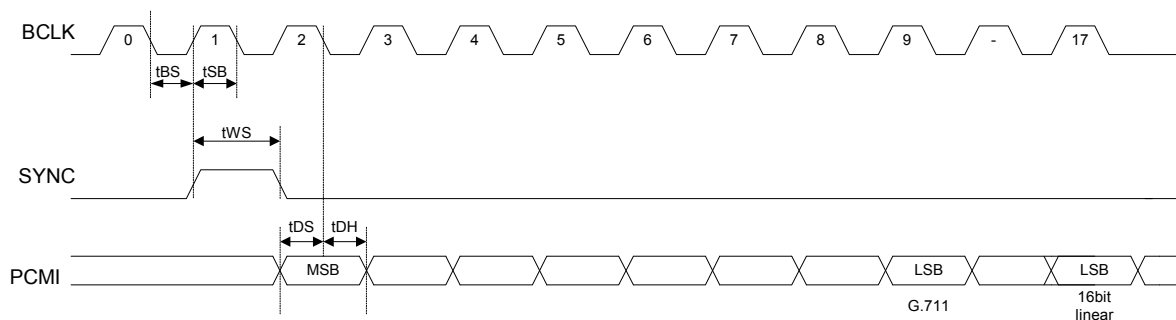
**PCM I/F Mode**

(Unless otherwise specified,  $AV_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bit clock frequency	fBCLK	CDL = 20pF(at output)	-0.1%	64	+0.1%	kHz
Bit clock duty ratio	dBCLK	CDL = 20pF(at output)	45	50	55	%
Sync signal frequency	fSYNC	CDL = 20pF(at output)	-0.1%	8	+0.1%	kHz
Sync signal duty ratio	dSYNC1	CDL = 20pF(at output) At 64 kHz output	12.4	12.5	12.6	%
	dSYNC2	CDL = 20pF(at output) At 128 kHz output	6.24	6.25	6.26	%
Transmit/receive signal sync timing	tBS	BCLK to SYNC (at output)	100	—	—	ns
	tSB	SYNC to BCLK (at output)	100	—	—	ns
Input setup time	tDS	—	100	—	—	ns
Input hold time	tDH	—	100	—	—	ns
Digital output delay time	tSDX	PCMO pin Pull-up, pull-down resistors RDL = 1 k $\Omega$ , CDL = 50 pF	—	—	100	ns
	tXD1		—	—	100	ns
	tXD2		—	—	100	ns
Digital output hold time	tXD3	—	—	100	ns	



**Fig. 2 PCM I/F mode input timing (long frame)**



**Fig. 3 PCM I/F mode input timing (short frame)**

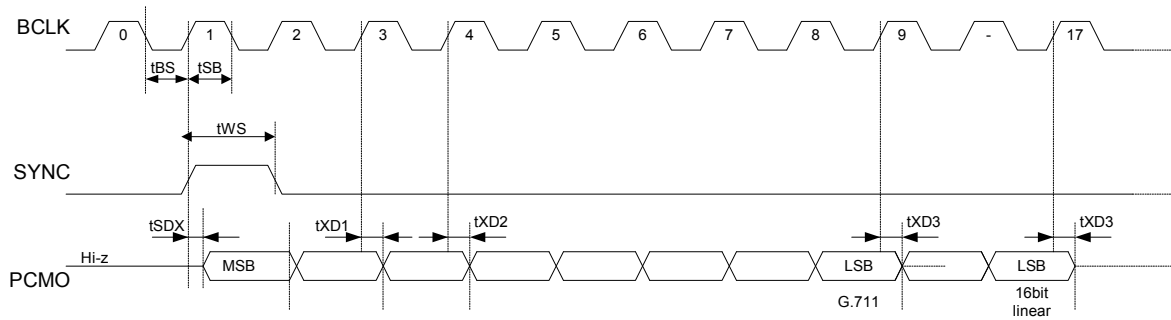


Fig. 4 PCM I/F mode output timing (long frame)

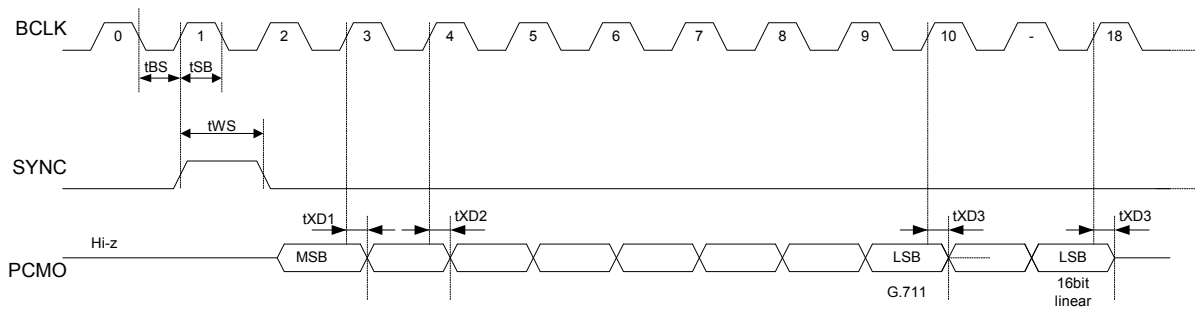
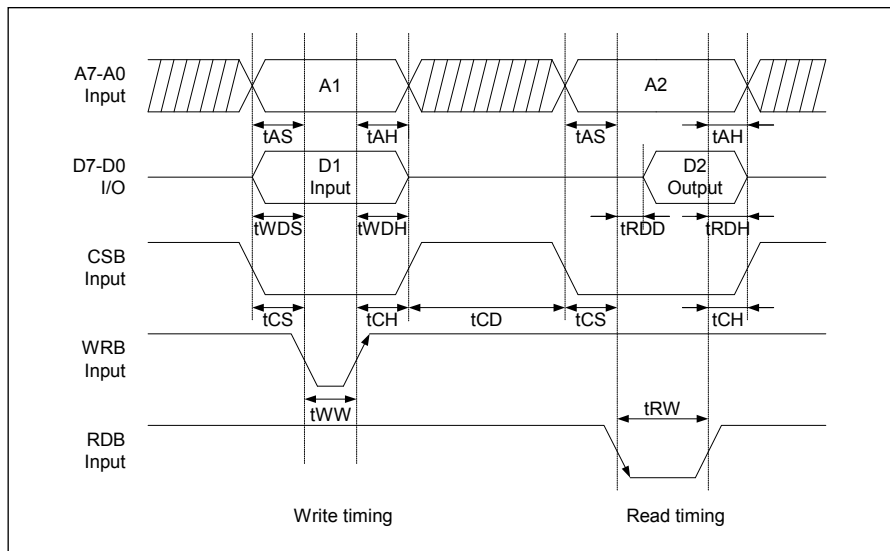


Fig. 5 PCM I/F mode output timing (short frame)

**Control Register Interface**

(Unless otherwise specified,  $AV_{DD} = 3.0$  to  $3.6$  V,  $DV_{DD0, 1, 2} = 3.0$  to  $3.6$  V,  $AGND = DGND0, 1, 2 = 0.0$  V,  $T_a = -20$  to  $+60^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address setup time	tAS	CL = 50 pF	10	—	—	ns
Address hold time	tAH		10	—	—	ns
Write data setup time	tWDS		10	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time	tCS		10	—	—	ns
CSB hold time	tCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
Read data output delay time	tRDD		—	—	20	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		25	—	—	ns
CSB disable time	tCD		10	—	—	ns

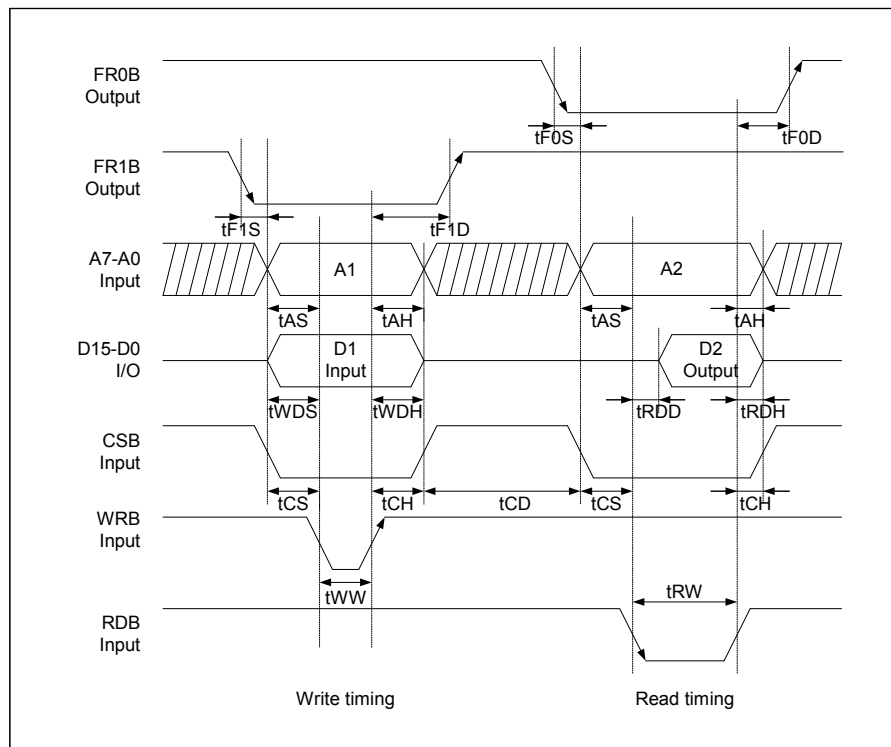


**Fig. 6 Control register interface**

**Transmit and Receive Buffer Interface (in Frame Mode)**

(Unless otherwise specified, AV<sub>DD</sub> = 3.0 to 3.6 V, DV<sub>DD0</sub>, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = -20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
FR1B setup time	tF1S	CL = 50 pF	3	—	—	ns
FR1B output delay time	tF1D		—	—	20	ns
Address setup time	tAS		10	—	—	ns
Address hold time	tAH		10	—	—	ns
Write data setup time	tWDS		10	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time	tCS		10	—	—	ns
CSB hold time	tCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
FR0B setup time	tF0S		3	—	—	ns
FR0B output delay time	tF0D		—	—	20	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
CSB disable time	tCD		10	—	—	ns

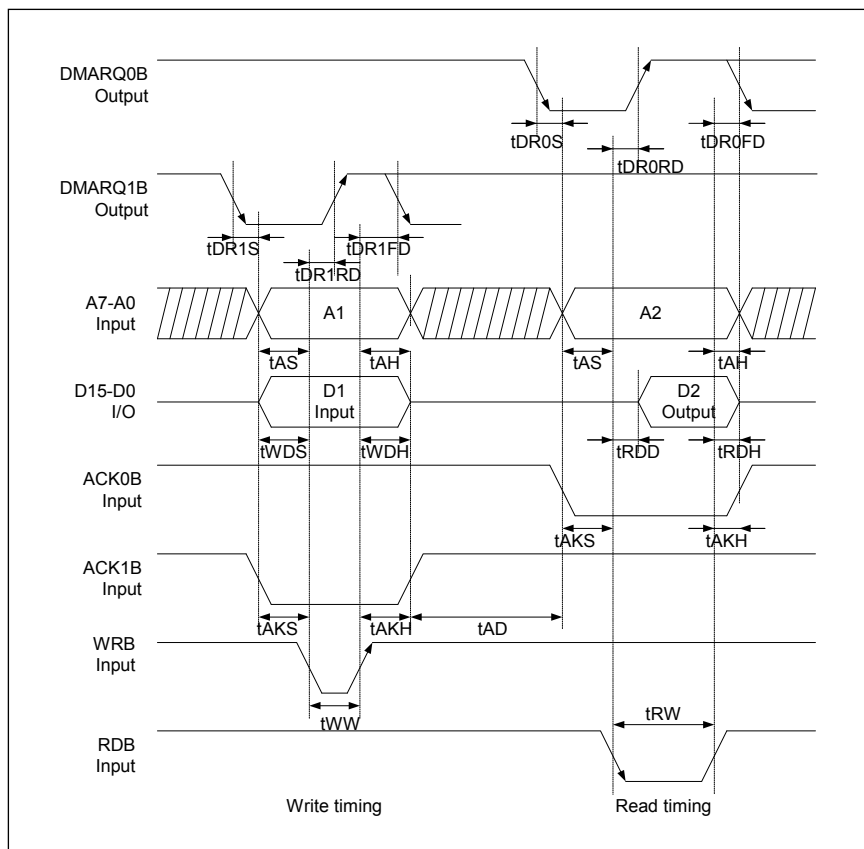


**Fig. 7 Transmit and receive buffer interface (in frame mode)**

**Transmit and Receive Buffer Interface (in DMA Mode)**

(Unless otherwise specified, AV<sub>DD</sub> = 3.0 to 3.6 V, DV<sub>DD0</sub>, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = -20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DMARQ1B setup time	tDR1S	CL = 50 pF	3	—	—	ns
DMARQ1B output delay time	tDR1RD		—	—	25	ns
	tDR1FD		—	—	25	ns
Address setup time	tAS		10	—	—	ns
Address hold time	tAH		10	—	—	ns
Write data setup time	tWDS		10	—	—	ns
Write data hold time	tWDH		10	—	—	ns
ACK setup time	tAKS		10	—	—	ns
ACK hold time	tAKH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
DMARQ0B setup time	tDR0S		3	—	—	ns
DMARQ0B output delay time	tDR0RD		—	—	20	ns
	tDR0FD		—	—	25	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
ACKB disable time	tAD		10	—	—	ns



**Fig. 8 Transmit and receive buffer interface (in DMA mode)**

## PIN FUNCTION DESCRIPTIONS

### AIN0N, AIN0P, GSX0, AIN1N, GSX1

These are the analog transmit input and transmit level adjust pins. Each of AIN0N and AIN1N is connected to each of the inverting input pins of the built-in transmit amplifiers AMP0 and AMP1, and AIN0P is connected to the non-inverting input pin of AMP0. In addition, GSX0 and GSX1 are connected to the output pins of AMP0 and AMP1, respectively. The selection between AMP0 and AMP1 is made by CR10-B0. See Fig. 9 for the method of making level adjustment. During the power down mode (when PDNB = "0" or CR0-B7 = "1"), the outputs of GSX0 and GSX1 go to the high impedance state. If AMP0 is not used in the specific application of this LSI, short GSX0 with AIN0N and connect AIN0P with AVREF. When AMP1 is not used, short GSX1 with AIN1N.

#### Notice:

It is recommended to select the amplifier to be used before the conversation starts, since a small amount of noise will be generated if the amplifier selection is changed while conversation is in progress.

### VFRO0, VFRO1

These are analog receive output pins and are connected to the output pins of the built-in receive amplifiers AMP2 and AMP3, respectively. The output signals of VFRO0 and VFRO1 can be selected using CR10-B1 and CR10-B2, respectively. When selected ("1"), the received signal will be output, and when deselected ("0"), the AVREF signal (about 1.4 V) will be output. In the power down mode, these pins will be in the high impedance state. It is recommended to use these output signals via DC coupling capacitors.

#### Notice:

It is recommended to select the amplifier to be used before the conversation starts, since a small amount of noise is generated if the output selection is changed while the conversation is in progress.

At the time of resetting or releasing from the reset state, it is recommended to select the AVREF as outputs of VFRO0 and VFRO1.

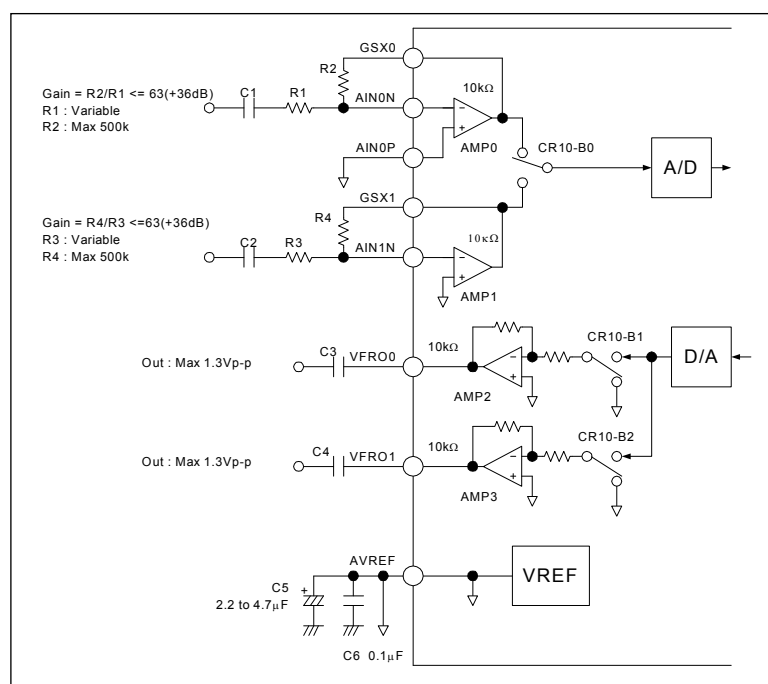


Fig. 9 Analog interface

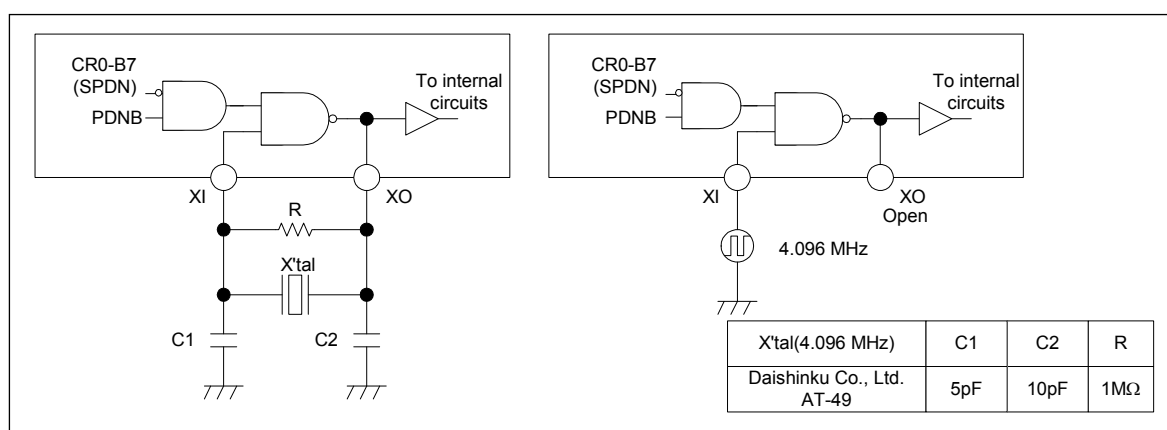
**AVREF**

This is the output pin for the analog signal ground potential. The output potential at this pin will be about 1.4 V. Connect a 2.2 to 4.7  $\mu\text{F}$  (aluminum electrolytic type) capacitor and a 0.1  $\mu\text{F}$  (ceramic type) capacitor in parallel between this pin and the GND pin as bypass capacitors. The output at the AVREF pin goes to 0.0 V in the power down mode. The voltage starts rising after the power down mode is released (PDNB = "1" and also CR0-B7 = "0"). The rise time is about 0.6 seconds.

**XI, XO**

These are the pins for either connecting the crystal oscillator for the master clock or for inputting an external master clock signal.

The oscillations of the master clock oscillator will be stopped during a power down due to the PDNB signal or during a software power down due to CR0-B7 (SPDN). The oscillations start when the power down condition is released, and the internal clock supply of the LSI will be started after counting up the oscillation stabilization period (of about 16 ms). Examples of crystal oscillator connection and external master clock input are shown in Fig. 10.



**Fig. 10 Examples of oscillator circuit and clock input**

**PDNB**

This is the power down control input pin. The power down mode is entered when this pin goes to "0". In addition, this pin also has the function of resetting the LSI. In order to prevent wrong operation of the LSI, carry out the initial power-down reset after switching on the power using this PDNB pin. Also, keep the PDNB pin at "0" level for 1  $\mu\text{s}$  or more to initiate the power down state.

Further, it is possible to carry out a power down reset of the LSI when the power is being supplied by performing control of CR0-B7 (SPDN) in the sequence "0"  $\rightarrow$  "1"  $\rightarrow$  "0".

The READY signal (CR5-B7) goes to "1" about 1.0 second after the power down mode is released thereby entering the mode of setting various functions (initialization mode). See Fig. 1 for the timings of PDNB and AVREF, XO, and the initialization mode.

Notice: At the time of switching on the power, start from the power down mode using PDNB.

**DV<sub>DD0</sub>, DV<sub>DD1</sub>, DV<sub>DD2</sub>, AV<sub>DD</sub>**

These are power supply pins. DV<sub>DD0</sub>, 1, 2 are the power supply pins for the digital circuits while AV<sub>DD</sub> is the power supply pin for the analog circuits of the LSI. Connect these pins together in the neighborhood of the LSI and connect as bypass capacitors a 10  $\mu\text{F}$  electrolytic capacitor and a 0.1  $\mu\text{F}$  ceramic capacitor in parallel between the DGND and AGND pins.

**DGND0, DGND1, DGND2, AGND**

These are ground pins. DGND0, 1, 2 are the ground pins for the digital circuits and AGND is the ground pin for the analog circuits of the LSI. Connect these pins together in the neighborhood of the LSI.

**TST0, TST1, TST2, TST3**

These are input pins for testing purposes only. Keep the inputs to these pins at the “0” level during normal use conditions.

**INTB**

This is the interrupt request output pin. An “L” level is output for a duration of about 1.0  $\mu$ s at this pin when there is a change in state of an interrupt cause.

This output will be maintained at the “H” level when there is no change in state of any of the interrupt causes. The actual interrupt cause generating the interrupt can be verified by reading CR3, CR4, and CR5. The different interrupt causes are described below.

- Underflow error (CR3-B0)
  - An interrupt is generated when an internal read from the receive buffer occurs before the writing into the receive buffer from the MCU has been completed.
  - An interrupt is generated when a normal writing is made in the receive buffer by the MCU and the underflow error is released.
- Overrun error (CR3-B1)
  - An interrupt is generated when an internal write of the next data into the transmit buffer occurs before the transmit buffer data read out from the MCU has been completed.
  - An interrupt is generated when a normal read out is made from the transmit buffer by the MCU and the overrun error is released.
- When a dial pulse is detected (CR4-B6).
- When a DTMF signal is detected (CR4-B4).
- When DTMF\_CODECO, 1, 2, 3 are detected (CR4-B0, B1, B2, B3).
  - An interrupt is generated when a DTMF signal is detected.
  - An interrupt is generated when there is a change from the DTMF signal detected state to the no-detected state.
  - An interrupt is generated when there is a change in the detected code (CR4-B0, B1, B2, B3) in the condition in which a DTMF signal is being detected.
- When TONE0 is detected (CR3-B3).
  - An interrupt is generated when a 1650 Hz tone signal is detected.
  - An interrupt is generated when there is a change to the non-detection condition in the tone signal detection condition.
- When TONE1 is detected (CR3-B4).
  - An interrupt is generated when a 2100 Hz tone signal is detected.
  - An interrupt is generated when there is a change to the non-detection condition in the tone signal detection condition.
- When DSP\_ERR is detected (CR3-B7).
  - An interrupt is generated when any error occurs in the DSP inside the LSI.
- When FGEN\_FLAG is cleared (CR5-B0).
  - FGEN\_FLAG is cleared to “0” and an interrupt is generated when data settings are enabled to output data setting register FGEN\_D[7:0] (CR18) in the FSK generator.

**A0 to A7**

These are the address input pins for use during an access of the frame, DMA, or control registers. The different addresses will be the following.

Transmit buffer (TX Buffer)

A7 to A0 = 10xxxxxb (the lower 6 bits are not valid)

Receive buffer (RX Buffer)

A7 to A0 = 01xxxxxb (the lower 6 bits are not valid)

Control register (CR)

A7 to A0 = 00xxxxxb

**D0 to D15**

These are the data input/output pins for use during an access of the frame, DMA, or control registers. Connect pull-up resistors to these pins since they are I/O pins. When the 8-bit bus access method is selected by CR11-B5, only D0 to D7 become valid. Since the higher 8 bits D8 to D15 will always be in the input state when the 8-bit bus access method is selected (CR11-B5 = "1"), tie them to "0" or "1" inputs.

**CSB**

This is the chip select input pin for use during a frame or control register access.

**RDB**

This is the read enable input pin for use during a frame, DMA, or control register access.

**WRB**

This is the write enable input pin for use during a frame, DMA, or control register access.

**FR0B (DMARQ0B)**

- FR0B (In frame mode, CR11-B7 = "0")  
This is the transmit frame output pin which outputs the signal when the transmit buffer is full during frame access. This pin outputs an "L" level when the transmit buffer becomes full, and maintains that "L" level output until a specific number of words are read out from the MCU.
- DMARQ0B (In DMA mode, CR11-B7 = "1")  
This is the DMA request output pin which outputs the signal when the transmit buffer is full during DMA access. This output becomes "L" when the transmit buffer becomes full, and returns to the "H" level automatically on the falling edge of the read enable signal (RDB = "1" → "0") when there is an acknowledgement signal (ACK0B = "0") from the MCU. This relationship is repeated until a specific number of words are read out from the MCU.

**FR1B (DMARQ1B)**

- FR1B (In frame mode, CR11-B7 = "0")  
This is the receive frame output pin which outputs the signal when the receive buffer is empty during frame access. This pin outputs an "L" level when the receive buffer becomes empty, and maintains that "L" level output until a specific number of words are written from the MCU.
- DMARQ1B (In DMA mode, CR11-B7 = "1")  
This is the DMA request output pin which outputs the signal when the receive buffer is empty during DMA access. This output becomes "L" when the receive buffer becomes empty, and returns to the "H" level automatically on the falling edge of the write enable signal (WRB = "1" → "0") when there is an acknowledgement signal (ACK1B = "0") from the MCU. This relationship is repeated until a specific number of words are written from the MCU.

**ACK0B**

This is the DMA acknowledgement input pin for the DMARQ0B signal during DMA access of the transmit buffer and becomes valid in the DMA mode (CR11-B7 = "1").

Tie this pin to "1" when using this LSI in the frame access mode (CR11-B7 = "0").

**ACK1B**

This is the DMA acknowledgement input pin for the DMARQ1B signal during DMA access of the receive buffer and becomes valid in the DMA mode (CR11-B7 = "1").

Tie this pin to "1" when using this LSI in the frame access mode (CR11-B7 = "0").

**GPI0, GPI1**

These are general-purpose input pins. The state ("1" or "0") of each of these GPI0 and GPI1 pins can be read out respectively from CR16-B0 and CR16-B1. Further, GPI0 becomes the input pin for the dial pulse detector (DPDET) in the secondary functions.

**GPO0, GPO1**

These are general-purpose output pins. The values set in CR17-B0 and CR17-B1 are output at these pins GPO0 and GPO1, respectively. Further, GPO0 becomes the output pin for the dial pulse generator (DPGEN) in the secondary functions.

**CLKSEL**

This is the input/output control input pin of SYNC and BCLK. The pin becomes input at “0” level and output at “1” level.

**SYNC**

This is the 8 kHz sync signal input/output pin of PCM signals. When CLKSEL is “0”, input continuously an 8 kHz clock synchronous with BCLK. Further, when CLKSEL is “1”, this pin outputs an 8 kHz clock synchronous with BCLK. Long frame synchronization is used when CR0-B1 (LONG/SHORT) is “0” and short frame synchronization is used when it is “1”.

**BCLK**

This is the shift clock input/output pin for the PCM signal. When CLKSEL is “0”, it is necessary to input to this pin a clock signal that is synchronous with SYNC. Input a 64 to 2048 kHz clock when the G.711 mode has been selected, and input a 128 to 2048 kHz clock when the 16-bit linear mode has been selected. When CLKSEL is “1”, this pin outputs a clock that is synchronous with SYNC. This pin outputs a 64 kHz clock when the G.711 mode has been selected, and outputs an 128 kHz clock when the 16-bit linear mode or G.729.A mode has been selected.

Note: The input/output control and frequencies of the above SYNC and BCLK signals will be as shown in Table 1 below.

**Table 1 Input/output control of SYNC and BCLK**

CLKSEL	SYNC	BCLK	Remarks
“0”	Input (8 kHz)	Input (64 kHz to 2048 kHz)	Input a continuous clock after starting the power supply. Input a 64 to 2048 kHz clock when G.711 is selected. Input a 128 to 2048 kHz clock when 16-bit linear mode is selected.
“1”	Output (8 kHz)	Output (64 kHz or 128 kHz)	An “L” level is output during the power down mode. A 64 kHz clock is output when G.711 is selected. A 128 kHz clock is output when G.729.A or 16-bit linear mode is selected.

**PCMO**

This is the PCM signal output pin for the transmitting section. The PCM signal is output in synchronization with the rising edges of SYNC and BCLK. The PCMO outputs the data only during the valid data segment in the selected coding format and goes to the high impedance state during all other segments. The basic timing chart of the PCM I/F mode is shown in Fig. 11. The PCMO output will be in the high impedance state when the PCM I/F mode is not used (CR12-B0 = “0”).

**PCMI**

This is the PCM signal input pin for the receiving section. The data is entered starting from the MSB by shift on the falling edge of BCLK.

The basic timing chart of the PCM I/F mode is shown in Fig. 11.

Fix input to “0” or “1” when the PCM I/F mode (CR12-B0 = “0”) is not used.

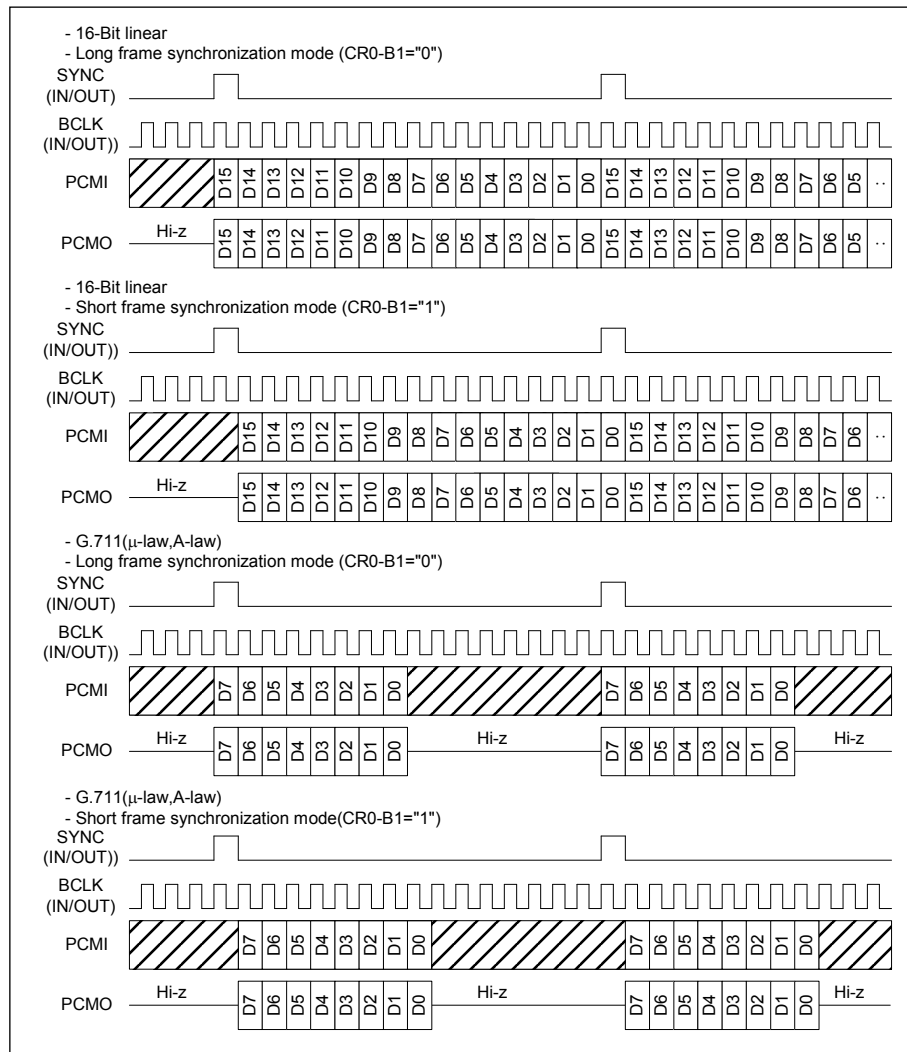


Fig. 11 PCM I/F mode timing diagram

## FUNCTION DESCRIPTION

### On the Transmit and Receive Buffers

The controllable parameters of the transmit and receive buffers are shown in Table 2 below.

**Table 2 Controllable parameters of transmit and receive buffers**

Content	Changeable parameter	Initial value	Remarks
Speech CODEC	G.729.A/G.711( $\mu$ -law, A-law)	G.729.A	The buffering size of the FIFO is changed automatically depending on the speech CODEC type.
Buffering time	10 ms/20 ms	10 ms	The number of words is changed automatically depending on the buffering time.
Accessing method	Frame or DMA	Frame	—
FIFO data width	16-bit/8-bit	16-bit	The number of words is changed automatically depending on the data width.

### Transmit and Receive Buffer Sizes

The transmit and receive buffers have a double buffer configuration of the FIFO (First In First Out) type, and one buffer can buffer data of 10 ms or 20 ms.

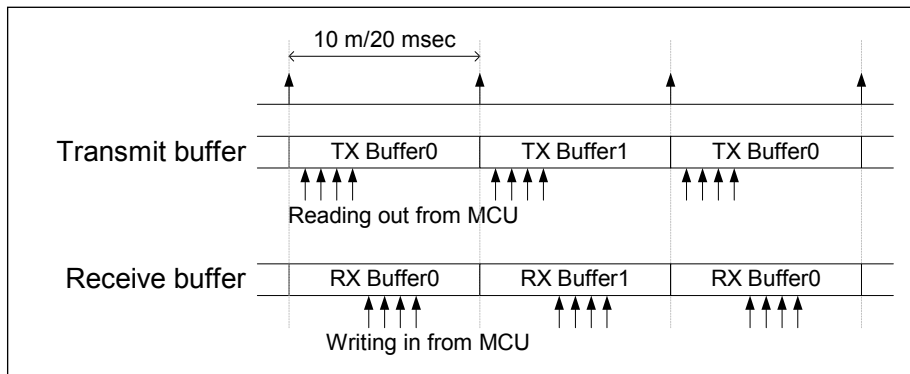
The timing of generation of the frame signals (FR0B, FR1B) requested to the MCU when the transmit buffer is full or the receive buffer is empty, and the timing of generation of the DMA request signals (DMARQ0B, DMARQ1B) depend on the buffering time. Further, the number of words of FIFO is changed automatically depending on the selected speech CODEC type and the FIFO data width. The buffer size and the number of words for the different speech CODEC types and data widths are shown in Table 3.

**Table 3 Buffer size and number of words of transmit and receive buffers**

Speech CODEC	10 ms mode			20 ms mode		
	Buffer size	16-bit	8-bit	Buffer size	16-bit	8-bit
G.729.A (8 kbps)	10 bytes	5 words	10 words	20 bytes	10 words	20 words
G.711 (64 kbps)	80 bytes	40 words	80 words	160 bytes	80 words	160 words

### Transmit and Receive Buffers Configuration

The timings of accessing the transmit and receive buffers are shown in Fig. 12. Although both transmit and receive buffers have a double buffer configuration, they can be accessed as a single buffer from the MCU.



**Fig. 12 Timings of accessing the transmit and receive buffers**

**Data Width Selection (16-Bit Mode, 8-Bit Mode)**

In the method of accessing the transmit and receive buffers, it is possible to select data width of 16 bits or 8 bits using the control register bit CR11-B5.

During the 16-bit mode, the access is made with a data width of 16 bits and the data bits D15 to D0 are accessed. In the 8-bit mode, the transmit and receive data are input or output to D7 to D0. During the 8-bit access mode, the bits D15 to D8 will always be in the input state.

**Data Storage Format**

The data storage formats during transmission and reception depending on the settings of the different parameters are shown in Fig. 13 and Fig. 14.

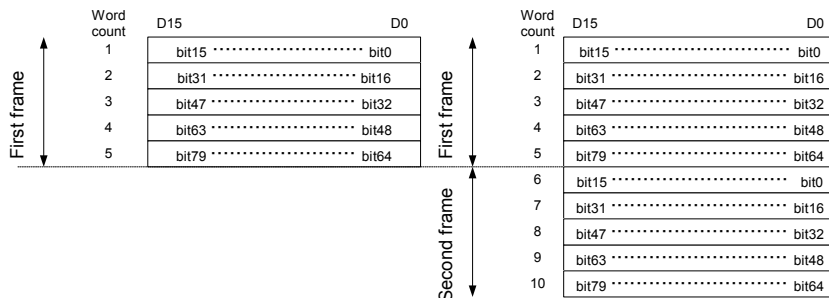
A. G.729.A

G.729.A(8 kbps)  
 1 frame 80-bit/10 ms  
 2 frames 160-bit/20 ms

**G.729.A coding, Word configuration**

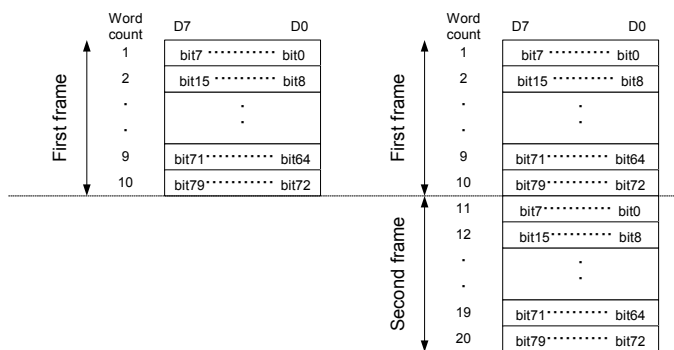
Symbol name bit No.																
Word count	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	L0	L1	L1	L1	L1	L1	L1	L1	L2	L2	L2	L2	L2	L3	L3	L3
2	L3	L3	P1	P1	P1	P1	P1	P1	P1	P0	C1	C1	C1	C1	C1	
3	C1	C1	C1	C1	C1	C1	C1	S1	S1	S1	S1	GA1	GA1	GA1	GB1	
4	GB1	GB1	P2	P2	P2	P2	P2	C2	C2	C2	C2	C2	C2	C2	C2	
5	C2	C2	C2	C2	S2	S2	S2	S2	GA2	GA2	GA2	GA2	GB2	GB2	GB2	

**Word configuration**



(a) 10 ms/16-bit mode

(b) 20 ms/16-bit mode



(c) 10 ms/8-bit mode

(d) 20 ms/8-bit mode

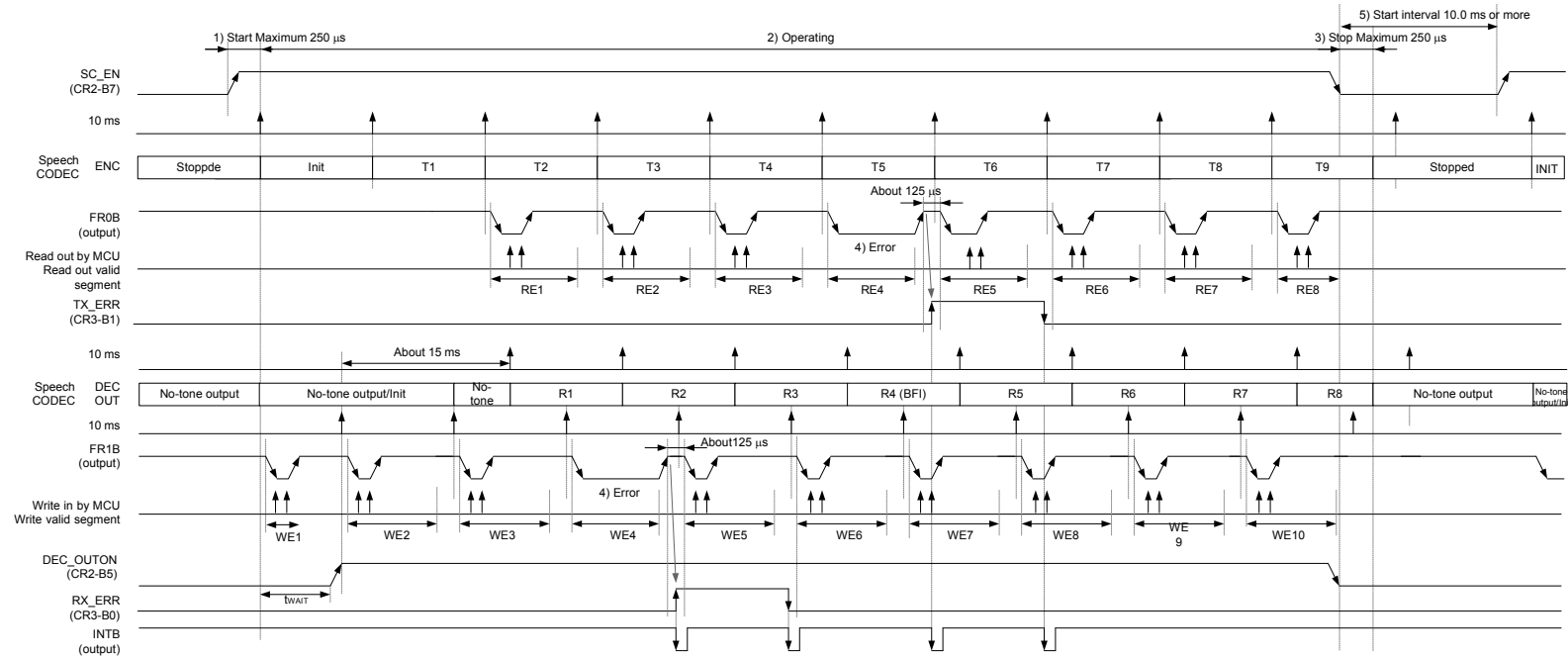
**Fig. 13 G.729.A data format**



## Transmit and Receive Buffer Control Method

The methods of controlling the transmit and receive buffers depending on the different parameters are shown in Figs. 15 to 18.

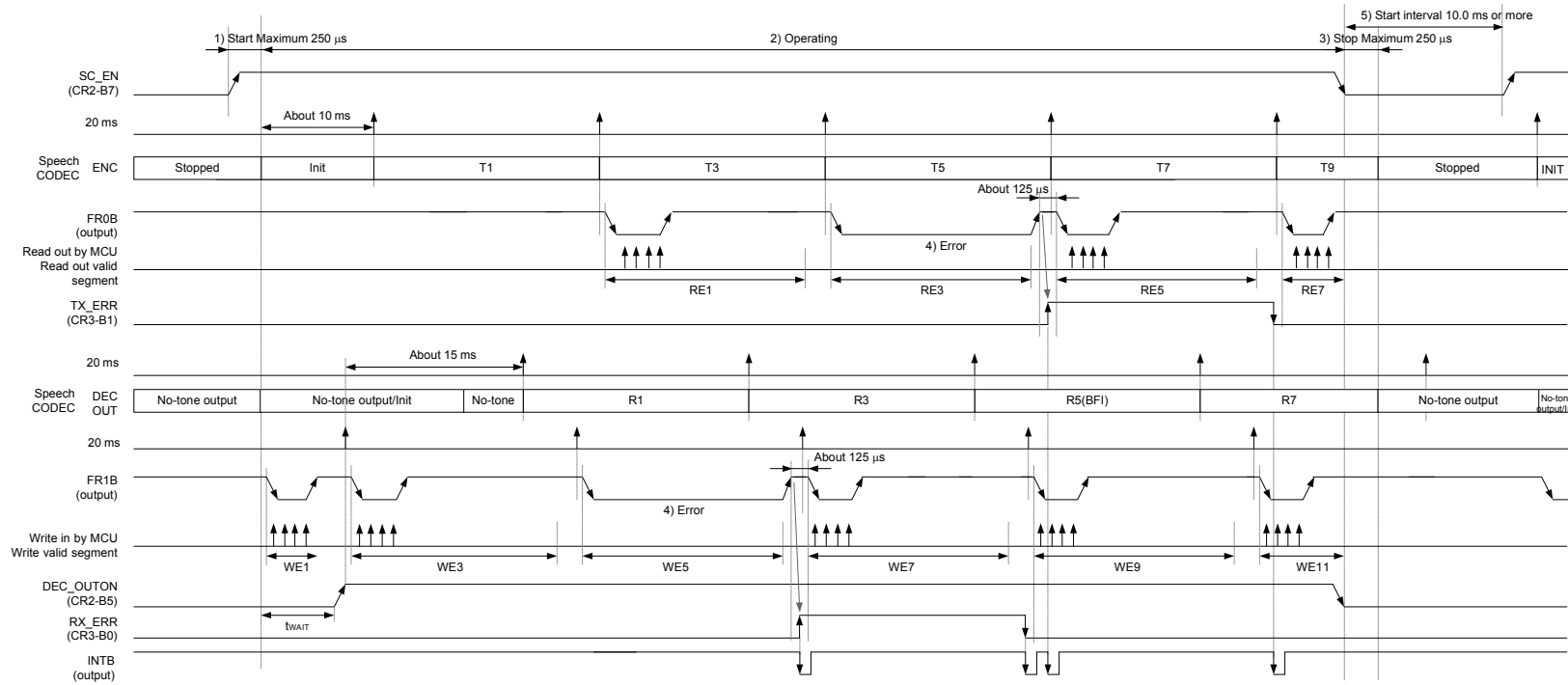
### A. G.729.A (10 ms/frame mode)



- 1) Start DEC\_OUTON "0", SC\_EN "0" → "1"  
The speech CODEC starts within about 250 μs after SC\_EN has been set to "1". The encoder is initialized during the first 10 ms period, and starts encoding with the T1 segment. The decoder carries out initialization after the speech CODEC has been started, and outputs no-tone data. If the first receive data has been written and the tWAIT wait time has elapsed, the DEC output control bit (DEC\_OUTON) can be set to "1". (tWAIT = 1 ms or more)
- 2) Operating  
The data encoded during encode segment Tn is read by the MCU during read valid segment RE<sub>n</sub>. This operation is repeated until the speech CODEC is stopped. (n = 1, 2, 3, 4, ...)  
The data written by the MCU during write valid segment WE<sub>n</sub> is output during decoder output segment Rn. This operation is repeated until the speech CODEC is stopped. (n = 1, 2, 3, 4, ...)
- 3) Stop Set SC\_EN "1" → "0", DEC\_OUTON "1" → "0"  
Encoding and decoding after the stoppage of the speech CODEC is disabled.  
Within about 250 μs after SC\_EN has been set to "1", the encoder stops writing data, and the decoder stops and then outputs no-tone data.
- 4) Error processing  
Receive error:  
In the figure above, an example of a receive error occurrence is shown in the write valid segment WE4.  
If data writing is not completed within a write valid segment, RX\_ERR is set to "1" and an interrupt is generated. The state of RX\_ERR will be maintained during and after the next write valid segment until just before the end of a frame that has been written normally into the RX buffer.  
If an error occurs in the write valid segment WE4, the loss-of-frame compensation processing (BFI: Bad Frame Indicator) specified in G.729A will be performed.  
Transmit error:  
In the figure above, an example of a transmit error occurrence is shown in the read valid segment RE5.  
If data reading is not completed within a read valid segment, TX\_ERR is set to "1" and an interrupt is generated. The state of TX\_ERR will be maintained during and after the next read valid segment until just before the end of a frame that has been read normally from the transmit buffer. Even if data reading is not completed, the data in the transmit buffer is updated as usual.
- 5) Start interval  
An interval of 10.0 ms or more is required after the speech CODEC has stopped before it is started again. During this interval, it is possible to change the speech CODEC.  
Write valid segment: There is no restriction of time on the first write valid segment (WE1) after the speech CODEC is started.  
For the write valid segment WE2 and after, complete the writing of data to the RX buffer within 9.0 ms from the falling edge of FR1B.  
Read valid segment: Complete the reading of data from the TX buffer within 9.0 ms from the falling edge of FR0B.

Fig. 15 G.729.A control timing (10 ms/frame mode)

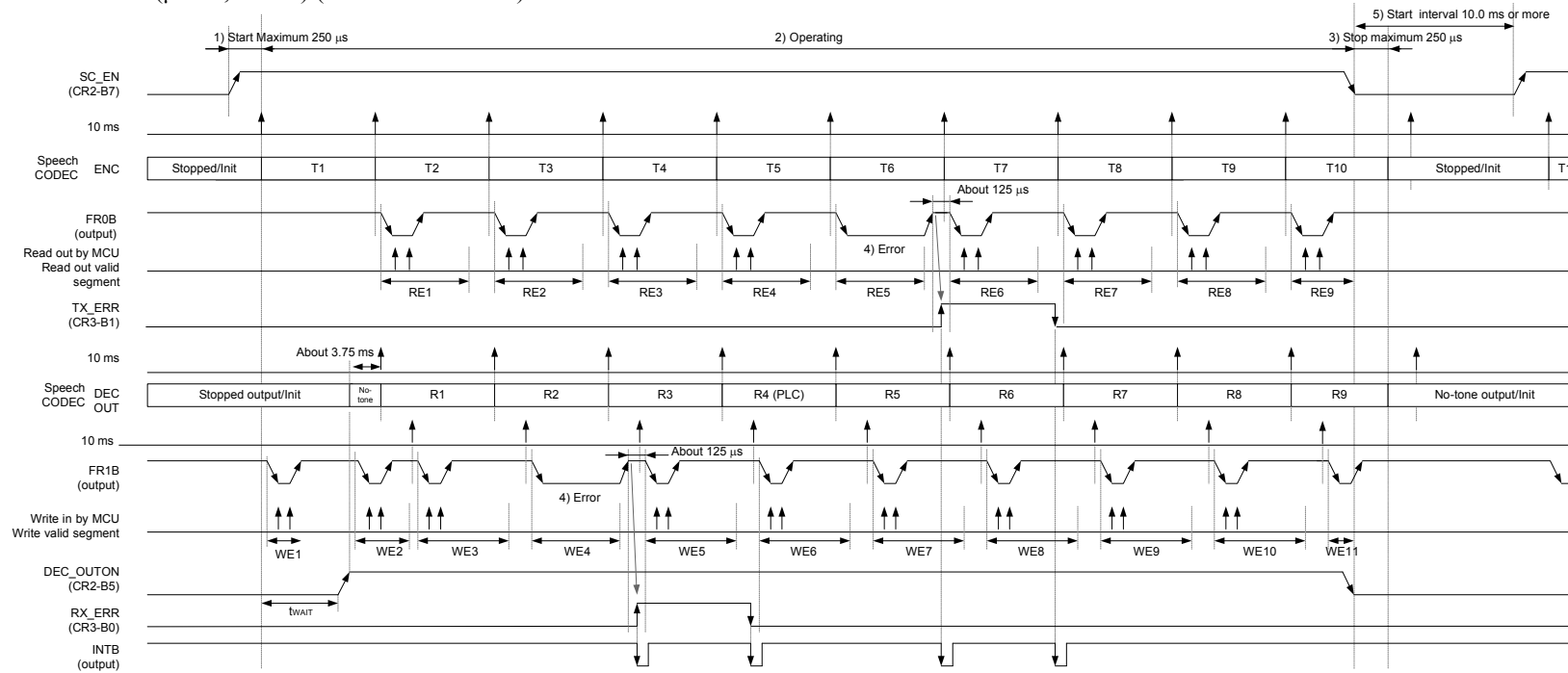
## B. G.729.A (20 ms/frame mode)



- 1) Start
  - DEC\_OUTON "0", SC\_EN "0" → "1"
  - The speech CODEC starts within about 250 μs after SC\_EN has been set to "1". The encoder is initialized during the first 10 ms period, and starts encoding with the T1 segment.
  - The decoder carries out initialization after the speech CODEC has been started, and outputs no-tone data.
  - If the first receive data has been written and the  $t_{WAIT}$  wait time has elapsed, the DEC output control bit (DEC\_OUTON) can be set to "1". ( $t_{WAIT}$  = 1 ms or more)
  - The decoder starts decoder output about 15 ms after DEC\_OUTON is set to "1".
- 2) Operating
  - The data encoded during encode segment Tn is read by the MCU during read valid segment RE<sub>n</sub>. This operation is repeated until the speech CODEC is stopped. (n = 1, 2, 3, 4, ...)
  - The data written by the MCU during write valid segment WE<sub>n</sub> is output during decoder output segment R<sub>n</sub>. This operation is repeated until the speech CODEC is stopped. (n = 1, 2, 3, 4, ...)
- 3) Stop
  - Set SC\_EN "1" → "0", DEC\_OUTON "1" → "0"
  - Encoding and decoding after the stoppage of the speech CODEC is disabled.
  - Within about 250 μs after SC\_EN has been set to "1", the encoder stops writing data, and the decoder stops and then outputs no-tone data.
- 4) Error processing
  - Receive error:
    - In the figure above, an example of a receive error occurrence is shown in the write valid segment WE5.
    - If data writing is not completed within a write valid segment, RX\_ERR is set to "1" and an interrupt is generated. The state of RX\_ERR will be maintained during and after the next write valid segment until just before the end of a frame that has been written normally into the RX buffer.
    - If an error occurs in the write valid segment WE5, the loss-of-frame compensation processing (BFI: Bad Frame Indicator) specified in G.729A will be performed.
  - Transmit error:
    - In the figure above, an example of a transmit error occurrence is shown in the read valid segment RE5.
    - If data reading is not completed within a read valid segment, TX\_ERR is set to "1" and an interrupt is generated. The state of TX\_ERR will be maintained during and after the next read valid segment until just before the end of a frame that has been read normally from the transmit buffer. Even if data reading is not completed, the data in the transmit buffer is updated as usual.
- 5) Start interval
  - An interval of 10.0 ms or more is required after the speech CODEC has stopped before it is started again. During this interval, it is possible to change the speech CODEC.
  - Write valid segment: There is no restriction of time on the first write valid segment (WE1) after the speech CODEC is started.
  - For the write valid segment WE3 and after, complete the writing of data to the RX buffer within 18.0 ms from the falling edge of FR1B.
  - Read valid segment: Complete the reading of data from the TX buffer within 18.0 ms from the falling edge of FR0B.

Fig. 16 G.729.A control timing (20 ms/frame mode)

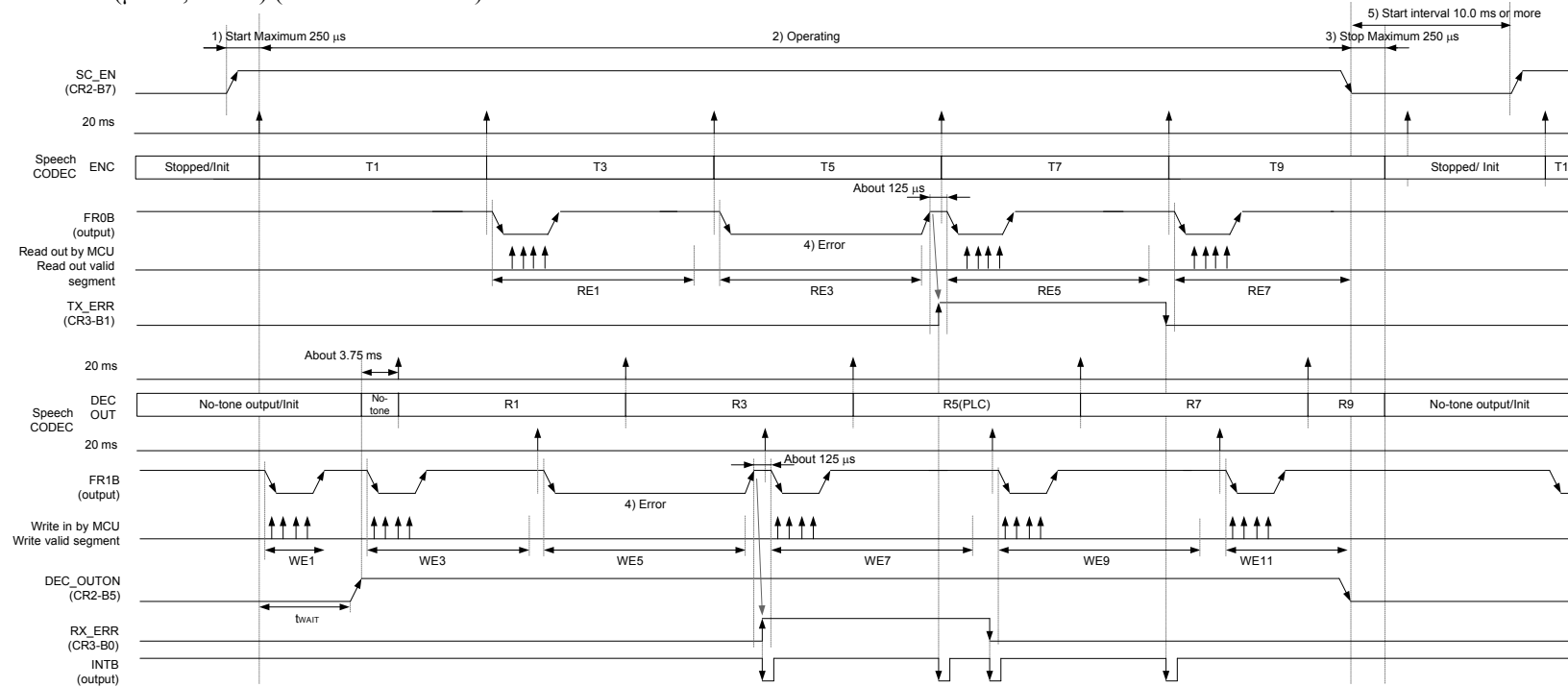
### C. G.711 ( $\mu$ -law, A-law) (10 ms/frame mode)



- 1) Start  
 DEC\_OUTON "0", SC\_EN "0" → "1"  
 The speech CODEC starts within about 250  $\mu$ s after SC\_EN has been set to "1". The encoder starts in the already initialized condition and starts encoding immediately after the speech CODEC has been started. The decoder carries out initialization after the speech CODEC has been started, and outputs no-tone data.  
 If the first receive data has been written and the tWAIT wait time has elapsed, the DEC output control bit (DEC\_OUTON) can be set to "1". (tWAIT = 1 ms or more)  
 After setting DEC\_OUTON to "1", the decoder outputs no-tone data for about 3.75 ms, and then starts decoder output.  
 However, if the PLC function has been disabled, the decoder starts decoder output after setting DEC\_OUT\_ON to "1".
- 2) Operating  
 The data encoded during encode segment Tn is read by the MCU during read valid segment REN. This operation is repeated until the speech CODEC is stopped. (n = 1, 2, 3, 4, ...)  
 The data written by the MCU during write valid segment WEn is output during decoder output segment Rn. This operation is repeated until the speech CODEC is stopped. (n = 1, 2, 3, 4, ...)
- 3) Stop  
 Set SC\_EN "1" → "0", DEC\_OUTON "1" → "0"  
 Encoding and decoding after the stoppage of the speech CODEC is disabled.  
 Within about 250  $\mu$ s after SC\_EN has been set to "1", the encoder stops writing data, and the decoder stops and then outputs no-tone data.
- 4) Error processing  
 Receive error:  
 In the figure above, an example of a receive error occurrence is shown in the write valid segment WE4.  
 If data writing is not completed within a write valid segment, RX\_ERR is set to "1" and an interrupt is generated. The state of RX\_ERR will be maintained during and after the next write valid segment until just before the end of a frame that has been written normally into the RX buffer.  
 If an error occurs in the write valid segment WE4, data generated according to the PLC algorithm specified in G.711 Appendix I is output during the decoder output segment R4. However, if the G.711 PCL function has been set disabled, no-tone data will be output.  
 Transmit error:  
 In the figure above, an example of a transmit error occurrence is shown in the read valid segment RE5.  
 If data reading is not completed within a read valid segment, TX\_ERR is set to "1" and an interrupt is generated. The state of TX\_ERR will be maintained during and after the next read valid segment until just before the end of a frame that has been read normally from the transmit buffer. Even if data reading is not completed, the data in the transmit buffer is updated as usual.
- 5) Start interval  
 An interval of 10.0 ms or more is required after the speech CODEC has stopped before it is started again. During this interval, it is possible to change the speech CODEC.  
 Write valid segment: There is no restriction of time on the first write valid segment (WE1) after the speech CODEC is started.  
 For the write valid segment WE2, complete the writing of data to the RX buffer within 4.0 ms from the falling edge of FR1B.  
 For the write valid segment WE3 and after, complete the writing of data to the RX buffer within 9.0 ms from the falling edge of FR1B.  
 Read valid segment: Complete the reading of data from the TX buffer within 9.0 ms from the falling edge of FR0B.

Fig. 17 G.711 ( $\mu$ -law, A-law) control timing (10 ms/frame mode)

### D. G.711 ( $\mu$ -law, A-law) (20 ms/frame mode)



- 1) Start
  - DEC\_OUTON "0", SC\_EN "0"  $\rightarrow$  "1"
  - The speech CODEC starts within about 250  $\mu$ s after SC\_EN has been set to "1". The encoder starts in the already initialized condition and starts encoding immediately after the speech CODEC has been started.
  - The decoder carries out initialization after the speech CODEC has been started, and outputs no-tone data.
  - If the first receive data has been written and the tWAIT wait time has elapsed, the DEC output control bit (DEC\_OUTON) can be set to "1".
  - After setting DEC\_OUTON to "1", the decoder outputs no-tone data for about 3.75 ms, and then starts decoder output.
  - However, if the PLC function has been disabled, the decoder starts decoder output after setting DEC\_OUT\_ON to "1".
- 2) Operating
  - The data encoded during encode segment Tn is read by the MCU during read valid segment REn. This operation is repeated until the speech CODEC is stopped (n = 1, 3, 5, ...).
  - The data written by the MCU during write valid segment WE<sub>n</sub> is output during decoder output segment Rn. This operation is repeated until the speech CODEC is stopped (n = 1, 3, 5, ...).
- 3) Stop
  - Set SC\_EN "1"  $\rightarrow$  "0", DEC\_OUTON "1"  $\rightarrow$  "0"
  - Encoding and decoding after the stoppage of the speech CODEC is disabled.
  - Within about 250  $\mu$ s after SC\_EN has been set to "1", the encoder stops writing data, and the decoder stops and then outputs no-tone data.
- 4) Error processing
  - Receive error:
    - In the figure above, an example of a receive error occurrence is shown in the write valid segment WE5.
    - If data writing is not completed within a write valid segment, RX\_ERR is set to "1" and an interrupt is generated. The state of RX\_ERR will be maintained during and after the next write valid segment until just before the normal end of a frame that has been written into the RX buffer.
    - If an error occurs in the write valid segment WE5, data generated according to the PLC algorithm specified in G.711 Appendix I is output during the decoder output segment R5. However, if the G.711 PCL function has been set disabled, no-tone data will be output.
  - Transmit error:
    - In the figure above, an example of a transmit error occurrence is shown in the read valid segment RE5.
    - If data reading is not completed within a read valid segment, TX\_ERR is set to "1" and an interrupt is generated. The state of TX\_ERR will be maintained during and after the next read valid segment until just before the normal end of a frame that has been read from the transmit buffer. Even if data reading is not completed, the data in the transmit buffer is updated as usual.
- 5) Start interval
  - An interval of 10.0 ms or more is required after the speech CODEC has stopped before it is started again. During this interval, it is possible to change the speech CODEC.
  - Write valid segment: There is no restriction of time on the first write valid segment (WE1) after the speech CODEC is started.
  - For the write valid segment WE3, complete the writing of data to the RX buffer within 15.0 ms from the falling edge of FR1B.
  - For the write valid segment WE5 and after, complete the writing of data to the RX buffer within 18.0 ms from the falling edge of FR1B.
  - Read valid segment: Complete the reading of data from the TX buffer within 18.0 ms from the falling edge of FR0B.

Fig. 18 G.711 ( $\mu$ -law, A-law) control timing (20 ms/frame mode)

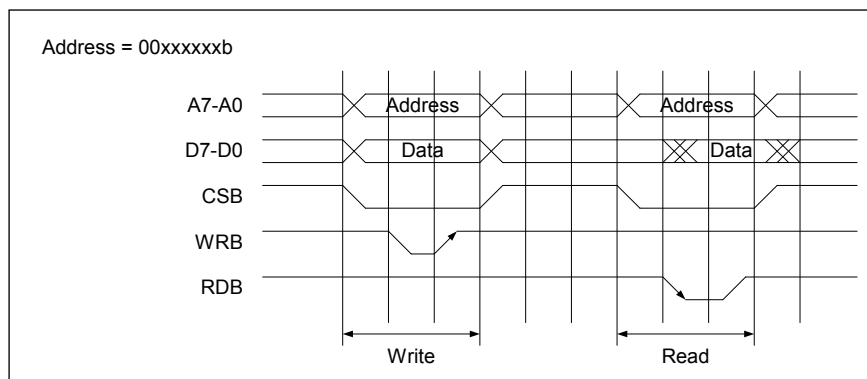
### Method of Controlling Control Registers

The method of controlling the control registers is shown in Fig. 19.

This LSI contains 21 control registers CR0 to CR20 for carrying out various controls. Further, the control bit (CR1-B7) assigned within such a control register, the address (CR6, CR7), and the data (CR8, CR9) are used to modify and control the data memory inside the DSP in this LSI.

See the section on “Method of Accessing and Controlling the Internal Data Memory” for details on how to access the data memory inside the DSP of this LSI.

The higher two bits of the address of a control register will be “0”. Irrespective of the 16-bit or 8-bit data width selected in CR11-B5 (16b/8b), all control operations of control registers are made with an 8-bit data width using only data bits D7 to D0. When the data bus is being accessed in the 16-bit access mode, data bits D15 to D8 are configured as inputs while the data is written to the control register, and are configured as outputs while the data is read from the control register. When a control register write is being made, “1” or “0” is input to D15 to D8, and “1” is read out during a control register read.

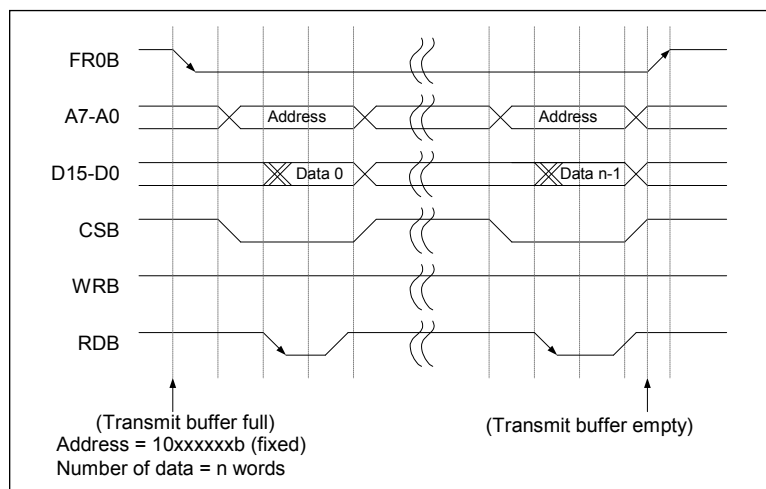


**Fig. 19 Method of controlling the control registers**

**Method of Accessing Transmit and Receive Buffers**

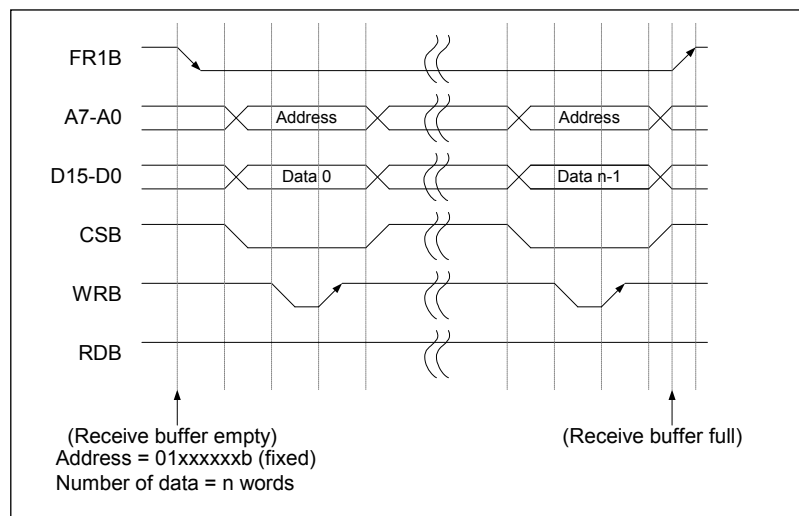
A. In the Frame Mode (CR11-B7 = "0")

The control timing and the method of accessing the transmit buffer (TX Buffer) during the frame mode are shown in Fig. 20. When the transmit buffer, which stores the compressed speech data of the transmit side (the speech compressing side), becomes full, a read request is made to the MPU by taking FR0B from the "H" state to the "L" state. Read the data in the transmit buffer during the following timing. The read address of the transmit buffer during the following timing. The read address of the transmit buffer is "10xxxxxxb" in which the lower 6 bits are ignored. Further, FR0B will be maintained in the "L" state until all the data bytes in the transmit buffer are read out.



**Fig. 20 Transmit buffer control timing**

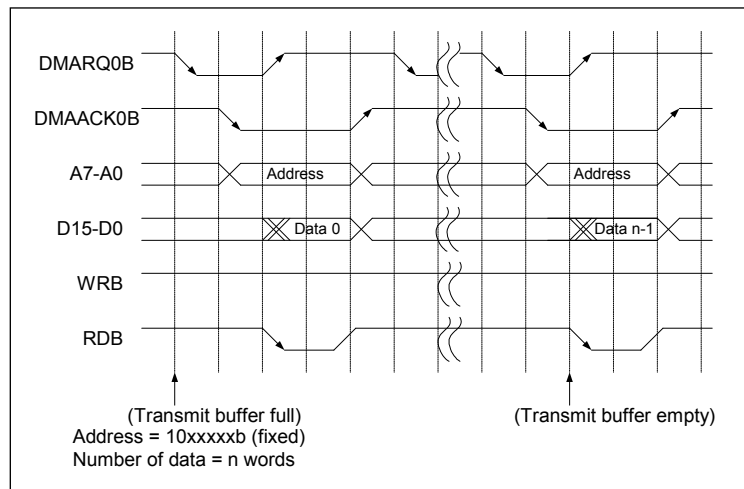
The control timing of the receive buffer (RX buffer) in the frame mode is shown in Fig. 21. A write request is made to the MPU by taking FR1B from the "H" state to the "L" state indicating that the receive buffer for storing the speech compression data of the receive side (the speech decompression side) has become empty. Write data into the receive buffer at the following timing. The write address of the receive buffer is "01xxxxxxb" in which the lower 6 bits are ignored. Further, FR1B will be maintained in the "L" state until the receive buffer is written to become full.



**Fig. 21 Receive buffer control timing**

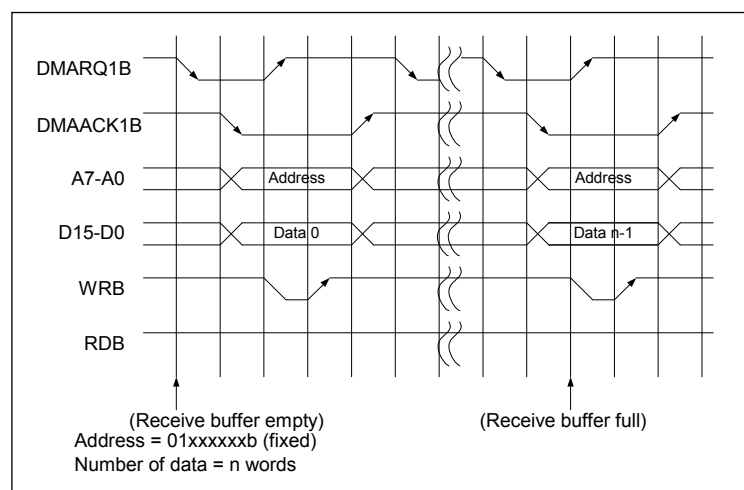
## B. In the DMA mode (CR11-B7 = "1")

The control timing of the transmit buffer in the DMA mode is shown in Fig. 22. A DMA request is made to the MPU by taking DMARQ0B from the "H" state to the "L" state when the transmit buffer storing the compressed speech data of the transmit side (the speech compressing side) becomes full. After the DMA request is made, an acknowledgement is input by changing the acknowledgement signal DMAACK0B to "0" from "1", and also, this DMARQ0B will be cleared automatically ("L" → "H") when a falling edge of the read enable signal is accepted (RDB = "1" → "0"). Read the data in the transmit buffer at the following timing simultaneously with the acknowledgement input. DMARQ0B repeats the DMA request until all the data in the transmit buffer has been read out.



**Fig. 22 Transmit buffer control timing in the DMA mode**

The control timing of the receive buffer during the DMA transfer mode is shown in Fig. 23. A DMA transfer request is made to the MPU by taking DMARQ1B from the "H" state to the "L" state when the receive buffer for storing the speech compression data of the receive side (the speech decompression side) has become empty. After the DMA transfer request is made, an acknowledgement is input by changing the acknowledgement signal DMAACK1B from "1" to "0", and also, this acknowledgement signal DMAACK1B will be cleared automatically ("L" → "H") when a falling edge of the read enable signal is accepted (RDB = "1" → "0"). Write data into the receive buffer at the following timing simultaneously with the acknowledgement input. DMARQ1B repeats the DMA transfer request until data has been written into the receive buffer to make it full.



**Fig. 23 Receive buffer control timing in the DMA mode**

**Control Registers**

Table 4 shows a map of the control registers. CR6 to CR9 are used for accessing the data memory inside the DSP. In addition, the changeable mode of operation is shown below the name of the register assigned to each bit.

**Table 4 Map of control registers**

Reg Name	Address A7 to A0	Contents								R/W
		B7	B6	B5	B4	B3	B2	B1	B0	
CR0	00h	SPDN	#	AFE_EN	#	#	#	LONG/ SHORT	OPE STAT	R/W
		/E	—	/I	—	—	—	—	/I	
CR1	01h	XDMWR	XDMRD	#	#	#	#	#	#	R/W
		/E	/E	—	—	—	—	—	—	
CR2	02h	SC_EN	FGEN _EN	DEC_ OUTON	TDET1 _EN	TDET0 _EN	DTMF _EN	EC_EN	#	R/W
		/E	/E	/E	/E	/E	/E	/E	—	
CR3	03h	DSP _ERR	#	#	TONE1 _DET	TONE0 _DET	#	TX _ERR	RX _ERR	R/
		—	—	—	—	—	—	—	—	
CR4	04h	INT	DP_DET	#	DTMF _DET	DTMF_ CODE3	DTMF_ CODE2	DTMF_ CODE1	DTMF_ CODE0	R/
		—	—	—	—	—	—	—	—	
CR5	05h	READY	#	#	#	#	#	#	FGEN FLAG	R/W
		—	—	—	—	—	—	—	/E	
CR6	06h	Internal data memory access (higher address)								/W
		A15	A14	A13	A12	A11	A10	A9	A8	
CR7	07h	Internal data memory access (lower address)								/W
		A7	A6	A5	A4	A3	A2	A1	A0	
CR8	08h	Internal data memory access (higher data)								R/W
		D15	D14	D13	D12	D11	D10	D9	D8	
CR9	09h	Internal data memory access (lower data)								R/W
		D7	D6	D5	D4	D3	D2	D1	D0	
CR10	0Ah	#	DPDET _EN	#	TDET1 _SEL	TDET0 _SEL	VFRO1 _SEL	VFRO0 _SEL	AIN _SEL	R/W
		—	/E	—	/I	/I	/E	/E	/E	
CR11	0Bh	FRAME/ DMA	10ms /20ms	16B /8B	#	#	SC _SEL1	SC _SEL0	G711_ PLCDIS	R/W
		/I	/I	/I	—	—	/E	/E	/E	

CR12	0Ch	#	#	#	#	#	PSC _SEL1	PSC _SEL0	PCMIF _EN	/W
		—	—	—	—	—	I/E	I/E	I/	
CR13	0Dh	\$	\$	\$	\$	\$	\$	\$	\$	/
CR14	0Eh	\$	\$	\$	\$	\$	\$	\$	\$	/
CR15	0Fh	TA2	TA1	TA0	\$	\$	\$	\$	\$	R/W
		I/	I/	I/	—	—	—	—	—	
CR16	10h	#	#	#	#	#	#	GPI1	GPI0	R/
		—	—	—	—	—	—	—	—	
CR17	11h	#	#	#	#	#	#	GPO1	GPO0	R/W
		—	—	—	—	—	—	I/E	I/E	
CR18	12h	FGEN _D7	FGEN _D6	FGEN _D5	FGEN _D4	FGEN _D3	FGEN _D2	FGEN _D1	FGEN _D0	R/W
		I/E								
CR19	13h	TGEN0 _RX	TGEN0 _TX	TGEN0 _CNT5	TGEN0 _CNT4	TGEN0 _CNT3	TGEN0 _CNT2	TGEN0 _CNT1	TGEN0 _CNT0	R/W
		I/E								
CR20	14h	TGEN1 _RX	TGEN1 _TX	TGEN1 _CNT5	TGEN1 _CNT4	TGEN1 _CNT3	TGEN1 _CNT2	TGEN1 _CNT1	TGEN1 _CNT0	R/W
		I/E								
—	15h-3Fh	\$	\$	\$	\$	\$	\$	\$	\$	/

## Notes:

## Register names

#: Reserved bit. Do not change the initial value of "0".

\$: Access-prohibited bit. Do not read or write this bit.

## Changeable operating mode:

I/E: Can be changed in either the initialization mode or the operating mode.

I/: Can be changed only in the initialization mode.

/E: Can be changed only in the operating mode.

## R/W

R/W: Both read and write are possible.

/W: Write only

R/: Read only

/: Access prohibited

## Notice:

Since the reading is made in synchronization with the SYNC signal (8 kHz) when the following control registers are set in the operating mode, maintain the condition for 250 μs or more.

CR1, CR2, CR5, CR10, CR11, CR12, CR19, CR20

See the method of accessing and controlling the internal data memory for the method of setting the following control registers.

CR6, CR7, CR8, CR9

## (1) CR0

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR0	SPDN	#	AFE _EN	#	#	#	LONG/ SHORT	OP _STAT	
Mode in which the setting can be changed	/E	—	I/	—	—	—	I/	I/	R/W
Initial value	0	0	0	0	1*	0	0	0	

## B7: Software power down reset control

0: Normal operation mode

1: Power down reset

The power down reset state can be initiated by setting this bit to “1” for 200 ns or longer. During the power down reset, all the contents of the control registers and of the internal data memory will be cleared automatically. The power down reset state is released by setting this bit to “1” first and then resetting it to “0”.

B6: Reserved bit. Do not change the initial value.

## B5: Analog front-end power down control

0: Normal operation mode

1: Power down state (excluding AVREF)

When using the PCM I/F mode, it is recommended to set this bit to “1” since the analog front-end function is not used in these modes. In addition, when setting this bit to “1”, simultaneously set the VFRO0 and VFRO1 outputs to the AVREF side (CR10-B2, B1 = “0”).

B4-2: Reserved bits. Do not change the initial values.

## B1: SYNC frame control

0: Long frame synchronization signal

1: Short frame synchronization signal

## B0: Operation start control

0: Operation hold

1: Operation start

The initialization mode is entered after releasing the power down reset state. In the initialization mode, it becomes possible to modify the contents of the control registers and the internal data memory. Read out the READY bit (CR5-B7) repeatedly and start modifying the contents of the control registers and the internal data memory after detecting a “1” in this bit.

When this bit is set to “1” after completing the writing of data in the control registers and the internal data memory, the LSI goes into the READY state (CR5-B7 = “0”) and the normal operation mode is initiated.

Carry out modifications of the control registers and the internal data memory after changing to the normal operation mode.

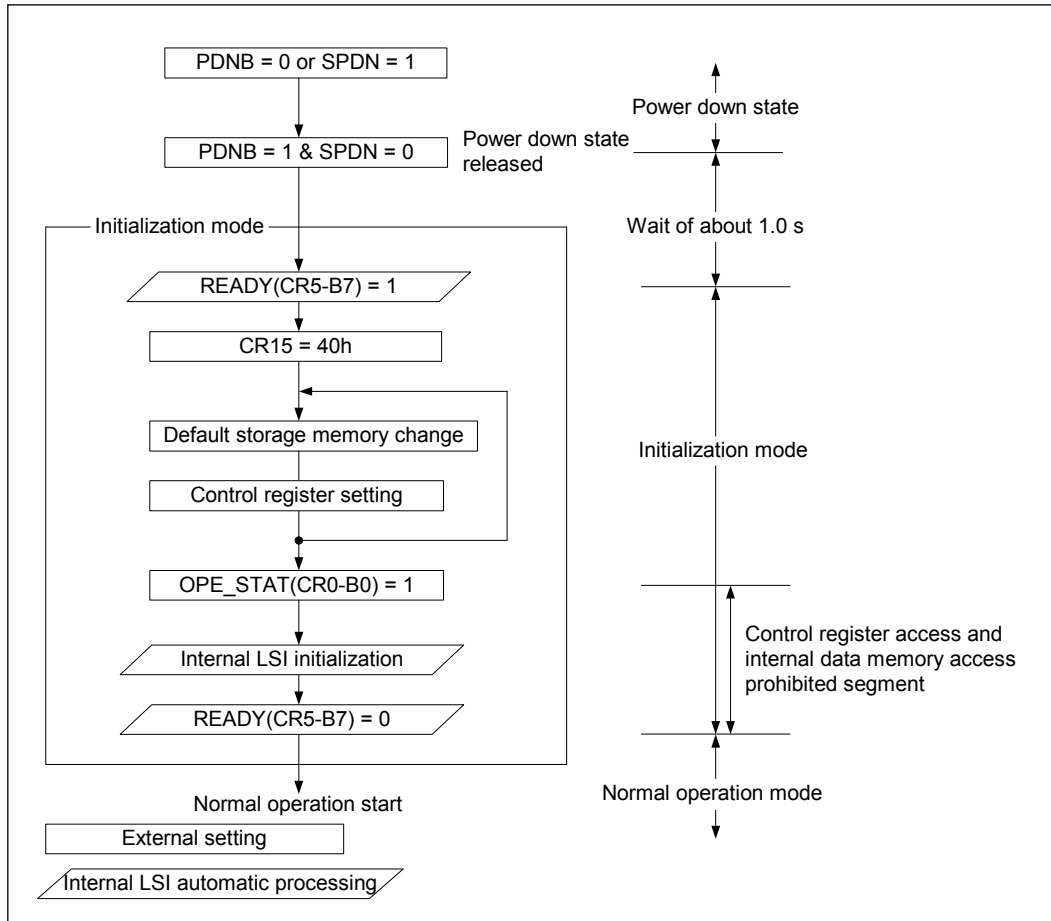
The method of changing the contents of the internal data memory is described later.

The flowchart of the initialization mode is shown in Fig. 24.

## Note: \*

Although the initial value of this bit is “0”, it will be set to “1” automatically before starting the initialization mode. Further, a “0” will be set in this bit automatically after the initialization mode if PCMIF\_EN (CR12-B0) is “1”.

When setting this register, make sure that the above value is not changed.



**Fig. 24 Initialization mode flowchart**

## (2) CR1

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR1	XDMWR	XDMRD	#	#	#	#	#	#	R/W
Mode in which the setting can be changed	I/E	I/E	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

## B7: Internal data memory write control

0: Write stopped

1: Write

The data set in CR8 and CR9 (D15 to D0) is written into the internal data memory at the address set in CR6 and CR7 (A15 to A0). When this writing is completed, this bit is automatically cleared to “0”. When writing data successively, make the settings after confirming that this bit is “0”.

For details of the method of controlling the internal memory, see the section on the method of accessing and controlling the internal data memory later in this booklet.

## B6: Internal data memory read control

0: Read stopped

1: Read

The data in the internal data memory at the address set in CR6 and CR7 (A15 to A0) can be read out from CR8 and CR9 (D15 to D0).

When this reading is completed, this bit is cleared to “0” automatically. When reading out data successively, read the data after confirming that this bit has become “0”.

For details of the method of controlling the internal memory, see the section on the method of accessing and controlling the internal data memory later in this booklet.

Notice: It is not possible to carry out simultaneously the above internal memory read and write controls. The setting of CR1-B7 and CR1-B6 = “11” is prohibited and should never be made.

B5 to B0: Reserved bits. Prohibited to change the initial settings.

## (3) CR2

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR2	SC_EN	FGEN_EN	DEC_OUTON	TDET1_EN	TDET0_EN	DTMF_EN	EC_EN	#	R/W
Mode in which the setting can be changed	I/E	I/E	/E	I/E	I/E	I/E	I/E	—	
Initial value	0	0	0	0	0	0	0	0	

## B7: Speech CODEC control register

0: Speech CODEC stopped

The encoder stops and the storing of data in the transmit buffer is stopped. The decoder stops and no-tone data is output continuously. It is possible to change the speech data compression coding method when the speech CODEC has stopped.

1: Speech CODEC operated

The speech CODEC starts operating when this bit is set to "1".

The speech CODEC starts after carrying out its own initialization.

## Note:

When stopping the speech CODEC by setting SC\_EN to "0", set DEC\_OUTON to "0" at the same time. In addition, when starting the speech CODEC by setting SC\_EN to "1", make sure that DEC\_OUTON has been set to "0".

## B6: FSK\_GEN control register

0: FSK\_GEN stopped

1: FSK\_GEN operated

The operation is started by setting this bit to "1". For more information about the control method, see the FSK Generator subsection in the Method of Accessing and Controlling Internal Data Memory section described later.

## B5: Decoder output control register

This bit controls the first decoder output timing after the speech CODEC is started.

After the speech CODEC is started, if the first receive data has been written and the tWAIT wait time has elapsed, this bit can be set to "1". When this bit is set to "1", the decoder output starts depending on the coding format of the selected speech CODEC, as shown below.

When G.711 ( $\mu$ -law/A-law) is selected:

If the PLC function is enabled, no-tone data about 3.75 ms long is output after this bit is set to "1".

Then, decoder output starts.

If the PLC function is disabled, the decoder output starts after this bit is set to "1".

When G.729.A is selected:

The decoder output starts about 15 ms after this bit is set to "1".

In addition, when stopping the speech CODEC by setting SC\_EN to "0", set this bit also to "0" at the same time. For more information about the control method, see Figures 15 through 18 in the Transmit and Receive Buffer Control Method section.

Note: At least 1 ms of the tWAIT wait time is required after the speech CODEC has been started.

## B4: TONE\_DET1 detector control register

0: TONE\_DET1 Stopped

1: TONE\_DET1 Operated

The operation is started by setting this bit to "1". A "1" is set to TONE\_DET1 (CR3-B4) during the period when a 2100 Hz\* tone is being detected.

B3: TONE\_DET0 detector control register

0: TONE\_DET0 Stopped

1: TONE\_DET0 Operation

The operation is started by setting this bit to "1". A "1" is set to TONE\_DET0 (CR3-B3) during the period when a 1650 Hz\* tone is being detected.

Remarks:

\* It is possible to change the detect frequencies. Contact ROHM's responsible sales person if you wish to change these frequencies.

B2: DTMF detector control register

0: DTMF detect function stopped

1: DTMF detect function operated

B1: Echo canceller control register

0: Echo canceller function stopped (The echo canceller is put in the through mode)

1: Echo canceller function active

Remarks:

The operation is started after the echo canceller internal coefficients cleared.

B0: Reserved bit. Prohibited to change the initial setting.

## (4) CR3

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR3	DSP _ERR	#	#	TONE1 _DET	TONE0 _DET	#	TX _ERR	RX _ERR	R/
Mode in which the setting can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

## B7: DSP status register

0: Normal operation state

1: Abnormal operation state

This LSI has a built-in watchdog timer, and when the program of the DSP section goes into uncontrollable execution state due to external disturbances around this LSI or due to power supply abnormalities, etc., the DSP\_ERR status will be set to “1” and an interrupt will be generated. When this bit becomes “1”, carry out a power down reset using either PDNB or SPDN of CR0-B7. This bit gets cleared by a power down reset operation.

## Notice:

The DSP\_ERR status cannot detect all abnormal operation conditions. The abnormality will not be detected even when the DSP goes into uncontrolled program execution if the watchdog timer gets cleared during that program execution.

B6, B5: Reserved bit. Prohibited to change the initial setting.

## B4: TONE1 detector detect status register

0: Not detected

1: Detected

## B3: TONE0 detector detect status register

0: Not detected

1: Detected

B2: Reserved bit. Prohibited to change the initial setting.

## B1: Transmit buffer status register

0: Transmit buffer in normal operation state

1: Transmit buffer in error state

This bit becomes “1” when an overrun error occurs in the transmit buffer, and will be “0” otherwise.

## B0: Receive buffer status register

0: Receive buffer in normal operation state

1: Receive buffer in error state

This bit becomes “1” when an underflow error occurs in the receive buffer, and will be “0” otherwise.

An interrupt is generated whenever there is a change in the state of any of the above bits (“0” → “1” or “1” → “0”).

## (5) CR4

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR4	INT	DP_DET	#	DTMF_DET	DTMF_CODE3	DTMF_CODE2	DTMF_CODE1	DTMF_CODE0	R/
Mode in which the setting can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

## B7: Interrupt generation status register

This is a directly coupled register with the logic of INTB inverted. A “1” will be read out from this bit when INTB is “L” and will be “0” otherwise.

0: During the period INTB is “H”

1: During the period INTB is “L”

Notice: The statuses of the INT bit and INTB may not be the same when a DSP\_ERR is generated.

## B6: Dial pulse detector detect status register

This bit indicates the detect status of the dial pulse detector. This bit becomes “1” during the period when a dial pulse is being detected and will be “0” otherwise.

0: Dial pulse not detected

1: Dial pulse detected

## B5: Reserved bit. Prohibited to change the initial value.

## B4: DTMF detector detect status register

This bit indicates the detect status of the DTMF detector.

This bit becomes “1” during the period when a DTMF signal is being detected and will be “0” otherwise.

0: No DTMF signal detected

1: DTMF signal detected

## B3 to B0: DTMF code indication registers

When DTMF\_EN (CR2-B2) has been set to “1”, a valid DTMF code is stored in these bits during the period a DTMF signal is being detected (CR4-B4 DTMF\_DET = “1”). These bits output the data “0000” when no DTMF signal is detected (DTMF\_DET = “0”). The codes are listed in Table 5.

**Table 5 DTMF detect code table**

DTMF_3	DTMF_2	DTMF_1	DTMF_0	Low frequency [Hz]	High frequency [Hz]	Dial number
0	0	0	0	697	1209	1
0	0	0	1	770	1209	4
0	0	1	0	852	1209	7
0	0	1	1	941	1209	*
0	1	0	0	697	1336	2
0	1	0	1	770	1336	5
0	1	1	0	852	1336	8
0	1	1	1	941	1336	0
1	0	0	0	697	1477	3
1	0	0	1	770	1477	6
1	0	1	0	852	1477	9
1	0	1	1	941	1477	#
1	1	0	0	697	1633	A
1	1	0	1	770	1633	B
1	1	1	0	852	1633	C
1	1	1	1	941	1633	D

An interrupt is generated whenever there is a change in the statuses of the bits B6, B4 to B0 above (“0” → “1” or “1” → “0”).

## (6) CR5

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR5	READY	#	#	#	#	#	#	FGEN _FLAG	R/W
Mode in which the setting can be changed.	—	—	—	—	—	—	—	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7: Initialization mode indication register

0: Other than the initialization mode

1: Initialization in progress

After the power down reset state is released, this LSI enters the initialization mode. This bit will be set to “1” in the initialization mode.

B6 to B1: Reserved bits. Prohibited to change the initial settings.

B0: FSK output data setup completion flag

After writing data into the FSK output data setup register (CR18), set this bit to “1”. Once the written data is read into the internal buffer of the FSK signal generation block, this bit is automatically cleared to “0”, and an interrupt is generated at the same time. Do not write to CR5 when this bit is “0”.

An interrupt is generated when there is a change in bit B0 (“1” → “0”).

## (7) CR6

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR6	A15	A14	A13	A12	A11	A10	A9	A8	/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Higher order address of the internal data memory

These bits are the registers for setting the higher order byte of the address in the internal data memory. For details on the method of writing, see the section on the method of accessing and controlling the internal data memory

## (8) CR7

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR7	A7	A6	A5	A4	A3	A2	A1	A0	/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Lower order address of the internal data memory

These bits are the registers for setting the lower order byte of the address in the internal data memory. For details on the method of writing, see the section on the method of accessing and controlling the internal data memory.

## (9) CR8

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR8	D15	D14	D13	D12	D11	D10	D9	D8	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Higher order data of the internal data memory

These bits are the registers for setting the higher order byte of the data in the internal data memory. For details on the method of writing and reading, see the section on the method of accessing and controlling the internal data memory.

## (10) CR9

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR9	D7	D6	D5	D4	D3	D2	D1	D0	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Lower order data of the internal data memory

These bits are the registers for setting the lower order byte of the data in the internal memory. For details on the method of writing and reading, see the section on the method of accessing and controlling the internal data memory.

## (11) CR10

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR10	#	DPDET_ EN	#	TDET1_ SEL	TDET0_ SEL	VFRO1_ SEL	VFRO0_ SEL	AIN_ SEL	R/W
Mode in which the value can be changed	—	I/E	—	I/	I/	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bit. Prohibited to change the initial setting.

B6: Dial pulse detector control register  
 0: Dial pulse detector stopped  
 1: Dial pulse detector active

B5: Reserved bit. Prohibited to change the initial setting.

B4: TDET1 detect path select register  
 0: Transmitting section  
 1: Receiving section

B3: TDET0 detect path select register  
 0: Transmitting section  
 1: Receiving section

B2: VFRO1 selection  
 0: AVREF (Output of about 1.4 V)  
 1: Receiver side speech output

B1: VFRO0 selection  
 0: AVREF (Output of about 1.4 V)  
 1: Receiver side speech output

B0: Input amplifier selection  
 0: Selection of AMP0  
 1: Selection of AMP1

## (12) CR11

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR11	FRAME/ DMA	10ms /20ms	16B /8B	#	#	SC _SEL1	SC _SEL0	G711_ PLCDIS	R/W
Mode in which the value can be changed	I/	I/	I/	—	—	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

## B7: FRAME/DMA select register

- 0: FRAME access
- 1: DMA slave interface access

This bit selects the method of accessing the transmit and receive buffers. The initial value is frame access.

## B6: 10 ms/20 ms select register

- 0: 10 ms
- 1: 20 ms

This bit selects the buffering time of the transmit and receive buffers. The initial value is 10 ms.

## B5: MCU interface data width select register

- 0: 16-bit data width interface
- 1: 8-bit data width interface

This bit selects the width of the data bus connected to the transmit and receive buffers. The initial value is 16 bits.

When the 8-bit bus width is used, tie D15 to D8 to either “1” or “0”.

B4, B3: Reserved bits. Prohibited to change the initial values.

## B2, B1: Speech CODEC select registers

- When using the analog I/F mode,
- (0, 0): G.729.A
- (0, 1): G.711 ( $\mu$ -law)
- (1, 0): Prohibited
- (1, 1): G.711 (A-law)

The speech CODEC can be selected when CR2-B7 (SC\_EN) is in the “0” state. Prohibited to change the speech CODEC when it is operating.

- When using the PCM I/F mode (CR12-B0 = “1”),

These bits select the PCM I/F coding method.

Further, the speech CODEC select bits will be CR12-B2 and CR12-B1.

- (0, 0): 16-bit linear (2's complement format)
- (0, 1): G.711 ( $\mu$ -law)
- (1, 0): Prohibited
- (1, 1): G.711 (A-law)

The coding method can be selected when CR2-B7 (SC\_EN) is in the “0” state. Prohibited to change the coding method during operation.

## B0: G.711 PLC function disable control register

Setting this bit to “1” disables the G.711 PLC function.

If the G.711 PLC function is disabled, no-tone data is output when a receive error occurs.

- 0: Enable
- 1: Disable

This bit can be enabled or disabled when CR2-B7 (SC\_EN) is “0”. Change of setting during operation is prohibited.

## (13) CR12

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR12	#	#	#	#	#	PSC_SEL1	PSC_SEL0	PCMIF_EN	/W
Mode in which the value can be changed	—	—	—	—	—	I/E	I/E	I/	
Initial value	0	0	0	0	0	0	0	0	

B7 to B3: Reserved bits. Prohibited to change the initial settings.

B2, B1: Speech CODEC select registers in the PCM I/F mode

(0, 0): G.729.A

(0, 1): G.711 ( $\mu$ -law)

(1, 0): Prohibited

(1, 1): G.711 (A-law)

The speech CODEC type can be selected when CR2-B7 (SC\_EN) is in the “0” state. Prohibited to change the speech CODEC type during operation.

B0: PCM I/F mode control register

0: Analog I/F mode

Set the speech CODEC type selection in CR11-B2 and CR11-B1.

1: PCM I/F mode

Set the PCM/IF coding method in CR11-B2 and CR11-B1, and set the speech CODEC type selection in B2 and B1 of this register.

## (14) CR13

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR13	\$	\$	\$	\$	\$	\$	\$	\$	/
Mode in which the value can be changed	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7 to B0: Reserved bits. Prohibited to change the initial settings.

## (15) CR14

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR14	\$	\$	\$	\$	\$	\$	\$	\$	/
Mode in which the value can be changed	—	—	—	—	—	—	—	—	
Initial value	—	—	—	—	—	—	—	—	

B7 to B0: Reserved bits. Prohibited to change the initial settings.

## (16) CR15

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR15	TA2	TA1	TA0	\$	\$	\$	\$	\$	R/W
Mode in which the value can be changed	I/	I/	I/	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7 to B5: Registers for adjustment

Set to “010” at the beginning of the initialization mode.

(0, 1, 0): Fixed

B4 to B0: Reserved bits. Prohibited to change the initial settings.

## (17) CR16

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR16	#	#	#	#	#	#	GPI1	GPI0	R/
Mode in which the value can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	—	—	

B7 to B2: Reserved bits. Prohibited to change the initial settings.

B1: GPI1 level read out register

0: GPI1 level is “0”.

1: GPI1 level is “1”.

B0: GPIO level read out register

0: GPIO level is “0”.

1: GPIO level is “1”.

Note:

GPIO is used as the input of the dial pulse detector in the secondary functions. It is possible to read out GPIO even when the dial pulse detector is operating.

## (18) CR17

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR17	#	#	#	#	#	#	GPO1	GPO0	R/W
Mode in which the value can be changed	—	—	—	—	—	—	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 to B2: Reserved bits. Prohibited to change the initial settings.

B1: GPO1 output level register

0: "L" level is output at GPO1.

1: "H" level is output at GPO1.

B0: GPO0 output level register

0: "L" level is output at GPO0.

1: "H" level is output at GPO0.

Notice:

GPO0 is used in the secondary functions as the output of the dial pulse transmitter.

Note that it is prohibited to change the content of the GPO0 bit when the dial pulse detector is operating.

## (19) CR18

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR18	FGEN _D7	FGEN _D6	FGEN _D5	FGEN _D4	FGEN _D3	FGEN _D2	FGEN _D1	FGEN _D0	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: FSK transmit data setting registers

## (20) CR19

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR19	TGEN0 _RX	TGEN0 _TX	TGEN0 _CNT5	TGEN0 _CNT4	TGEN0 _CNT3	TGEN0 _CNT2	TGEN0 _CNT1	TGEN0 _CNT0	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7: TGEN0 RX section output control register

0: Output stopped.

1: Tone output at the RX section

B6: TGEN0 TX section output control register

0: Output stopped.

1: Tone output at the TX section

B5: Register for controlling addition or multiplication of TONE A/B

0: Addition (The TONE A and TONE B outputs are added.)

1: Multiplication (The TONE A and TONE B outputs are multiplied.)

B4: TONE A/B output control register

0: Onetime tone output

The signal is output for a duration equal to the sum of TIM\_M0 and TIM\_M1 and then stopped.

After stopping, CR19 will be cleared automatically within the LSI.

1: Repetitive tone output

The signal is output repeatedly as controlled by the time duration equal to the sum of TIM\_M0 and TIM\_M1.

Write 00h in this register CR19 in order to stop the signal output.

Notice:

It is prohibited to write any value in this register other than 00h when repetitive output is being made.

In the case of onetime tone output operation, make the next setting only after making sure that the content of this register has become 00h. When tone output is intended to resume after repetitive tone output is once ceased, the register setting must be made only after Fade-out time plus 250μs.

B3, B2: TONE A output control registers

00: No tone is output.

01: The tone is stopped during the M0 period and is output during the M1 period.

10: The tone is output during the M0 period and stopped during the M1 period.

11: The tone is output during both the M0 and M1 periods.

B1, B0: TONE B output control registers

00: No tone is output.

01: The tone is stopped during the M0 period and is output during the M1 period.

10: The tone is output during the M0 period and is stopped during the M1 period.

11: The tone is output during both the M0 and M1 periods.

Note:

Although it is possible to output TONE A and TONE B alternately when the output controls of TONE A and TONE B are set in a mutually exclusive manner and their outputs are summed, the waveform after addition will be discontinuous since the phases of the two signals will be independent of each other.

## (21) CR20

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR20	TGEN1 _RX	TGEN1 _TX	TGEN1 _CNT5	TGEN1 _CNT4	TGEN1 _CNT3	TGEN1 _CNT2	TGEN1 _CNT1	TGEN1 _CNT0	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7: TGEN1 PCM section output control register

0: Output stopped.

1: Tone output at the RX section

B6: TGEN1 TX section output control register

0: Output stopped.

1: Tone output at the TX section

B5: Register for controlling addition or multiplication of TONE C/D

0: Addition (The TONE C and TONE D outputs are added.)

1: Multiplication (The TONE C and TONE D outputs are multiplied.)

B4: TONE C/D output control register

0: Onetime tone output

The signal is output for a duration equal to the sum of TIM\_M0 and TIM\_M1 and then stopped.

After stopping, CR20 will be cleared automatically within the LSI.

1: Repetitive tone output

The signal is output repeatedly as controlled by the time duration equal to the sum of TIM\_M0 and TIM\_M1.

Write 00h in this register CR20 in order to stop the signal output.

Notice:

It is prohibited to write any value in this register other than 00h when repetitive output is being made.

In the case of onetime tone output operation, make the next setting only after making sure that the content of this register has become 00h. When tone output is intended to resume after repetitive tone output is once ceased, the register setting must be made only after Fade-out time plus 250μs.

B3, B2: TONE C output control registers

00: No tone is output.

01: The tone is stopped during the M0 period and is output during the M1 period.

10: The tone is output during the M0 period and stopped during the M1 period.

11: The tone is output during both the M0 and M1 periods.

B1, B0: TONE D output control registers

00: No tone is output.

01: The tone is stopped during the M0 period and is output during the M1 period.

10: The tone is output during the M0 period and is stopped during the M1 period.

11: The tone is output during both the M0 and M1 periods.

Note:

Although it is possible to output TONE C and TONE D alternately when the output controls of TONE C and TONE D are set in a mutually exclusive manner and their outputs are summed, the waveform after addition will be discontinuous since the phases of the two signals will be independent of each other.

Figure 25 shows block diagrams of the tone generation blocks (TONE\_GEN0, TONE\_GEN1).

There is no difference in the tone generation method between TONE\_GEN0 and TONE\_GEN1. So, using TONE\_GEN0 as an example, Figure 26 shows the tone output control method, and Figures 27 and 28 show the tone output control parameters.

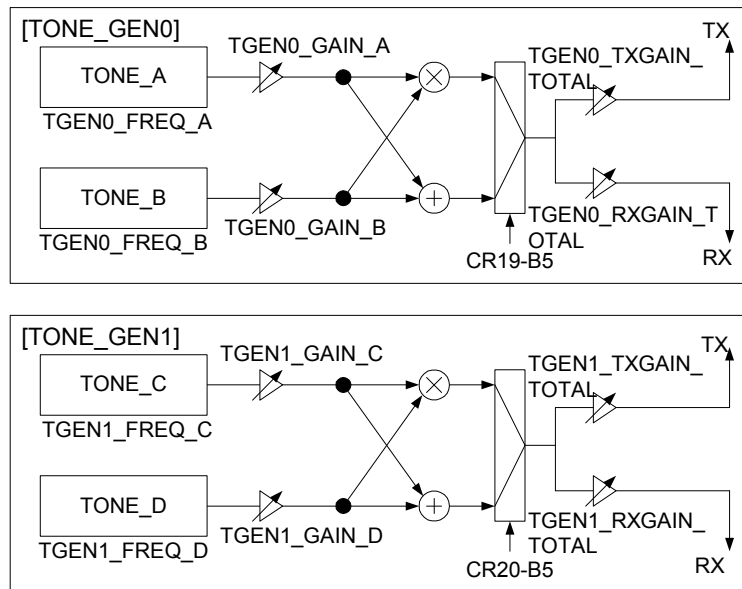
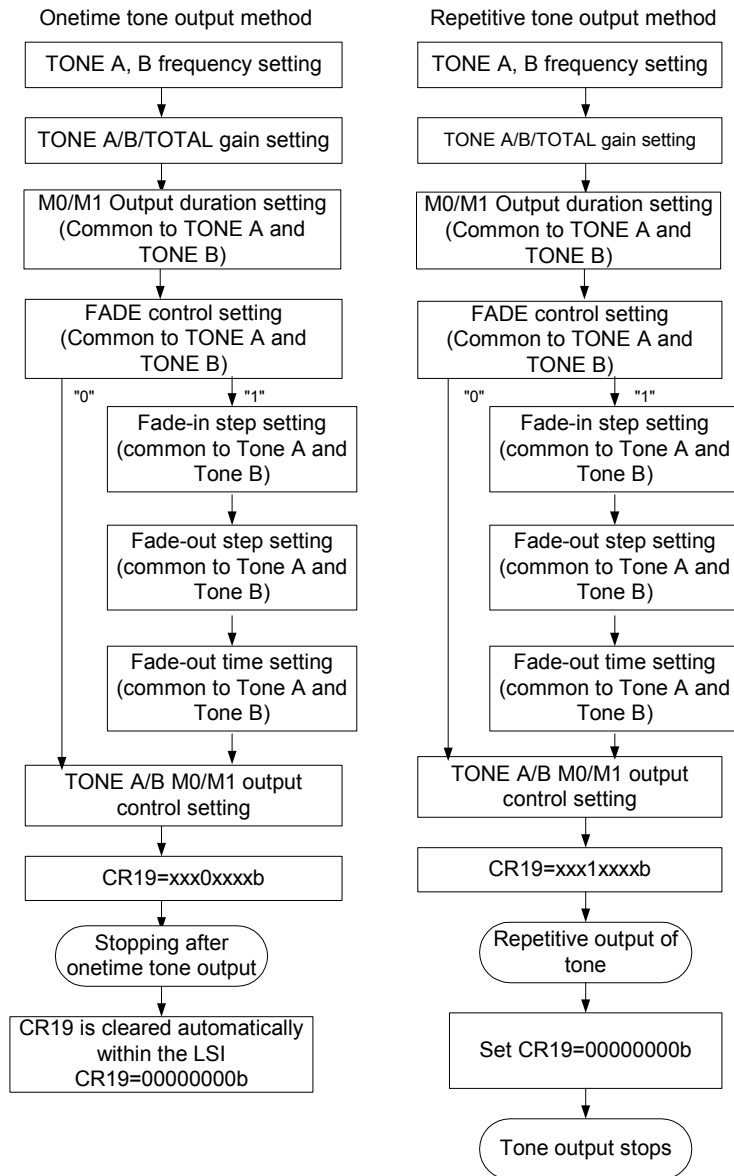


Fig. 25 Tone generator section block diagram



\* When tone output is intended to resume after repetitive tone output is once ceased, the register setting must be made only after Fade-out time plus 250µs.

Fig. 26 Tone output control method (in the case of TONE\_GEN0)

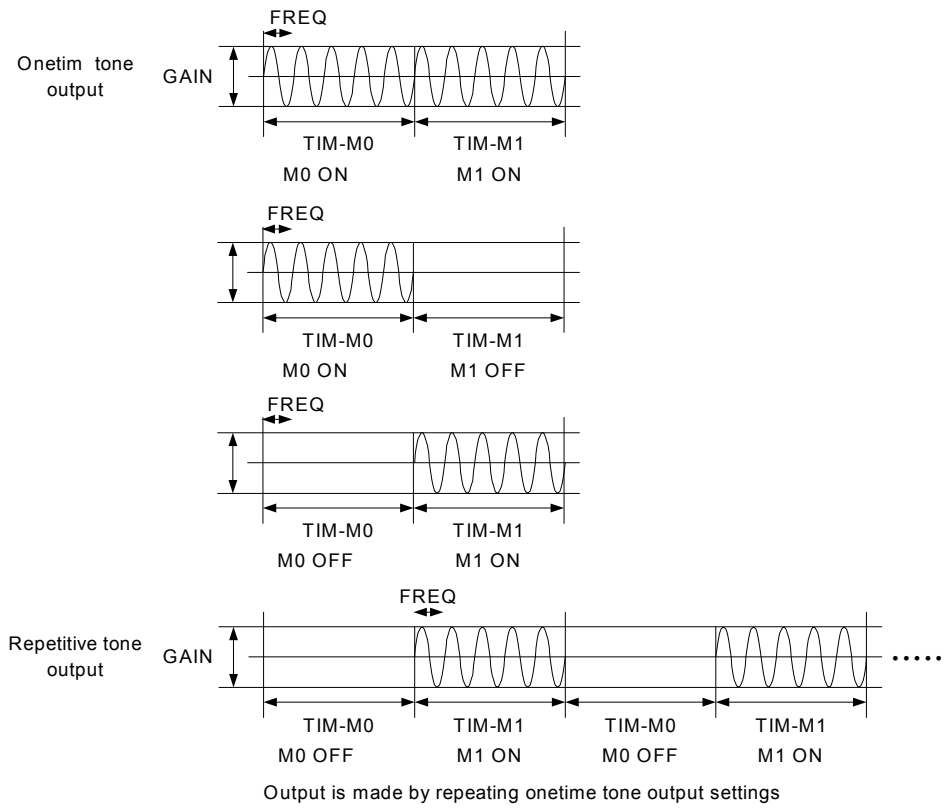


Fig. 27 Tone output control parameters (in the case of TONE\_GENO/TGEN0\_FADE\_CONT OFF)

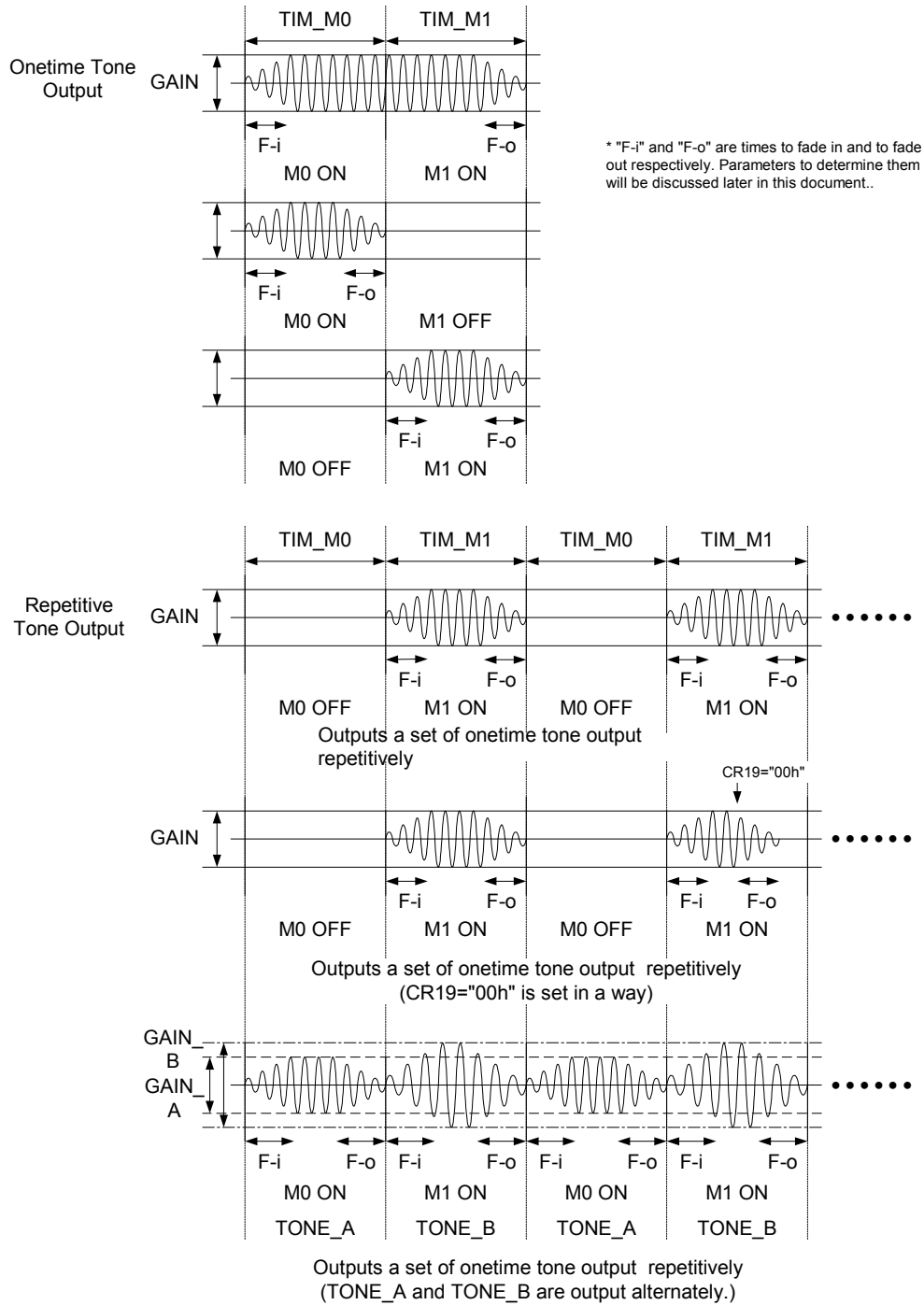


Fig. 28 Tone output control parameters (in the case of TONE\_GEN0/TGEN0\_FADE\_CONT "ON")

## METHOD OF ACCESSING AND CONTROLLING INTERNAL DATA MEMORY

### Writing Method

The four 8-bit registers CR6 to CR9 mapped within the set of control registers are allocated to the following:  
 16-bit address of the internal data memory (A15 to A0)  
 16-bit data to be written (D15 to D0)

The initialization mode is entered and a "1" is set in CR5-B7 (READY) about 1.0 s after release from a power down reset due to PDNB or after a release from a software power down reset due to CR0-B7.

In this writable state, after setting in CR6 to CR9 the internal data memory address and the data to be written, if a "1" is set in CR1-B7 (XDMWR), the writing of one word of data in the internal data memory will be completed. After completion of writing the data, CR1-B7 will be cleared to "0" automatically. The method of setting data in the internal data memory is shown in Fig. 29.

Repeat the above operations for writing to several memory locations. When all the writing operations have been completed, the normal operations can be started by setting a "1" in CR0-B0 (OPE\_STAT).

It is possible to re-write even in modes other than the initialization mode the internal data memory locations related to gain control, TONE transmission, EC, DPGEN, and TIMER. Even in such cases, carry out the updating of the internal data memory using the same method as described above.

Table 6 to Table 9 list the internal data memory and related control registers.

Note:

When data is set in the internal data memory during operation, since the reading is done in synchronization with the SYNC signal (8 kHz), maintain the state for 250  $\mu$ s or more.

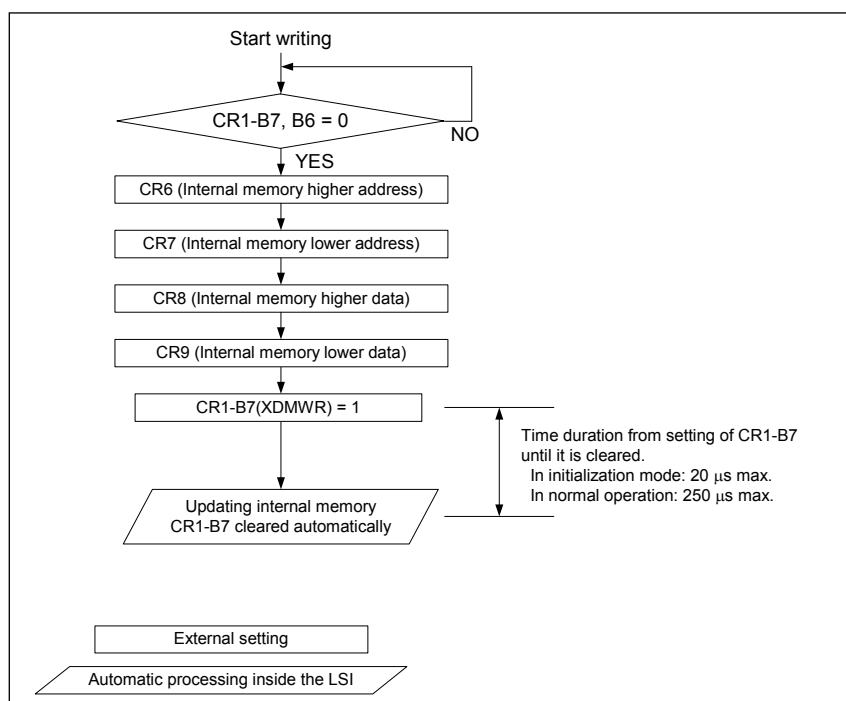


Fig. 29 Method of setting data in the internal data memory

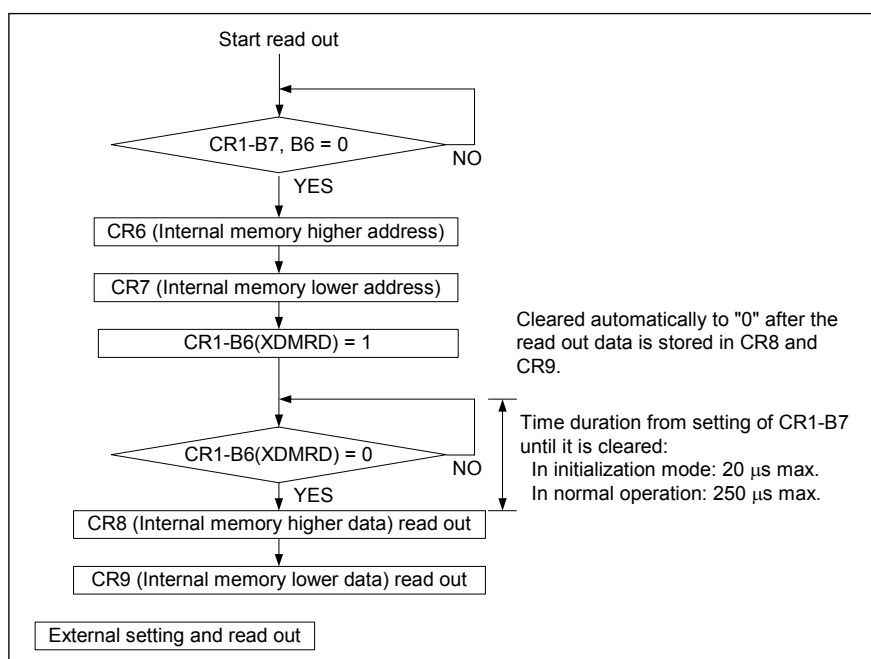
### Reading Method

After setting the internal data memory address in CR6 and CR7, one word of data from the internal data memory is stored in CR8 and CR9 when a "1" is written in CR1-B6 (XDMRD). After reading the data, CR1-B6 will be cleared to "0" automatically. The method of reading the internal data memory is shown in Fig. 30.

Further, the internal data memory read out can only be made for the internal data memory and the read only data memory within the related registers listed in Table 6 to Table 9.

Notice:

When the internal data memory is read out during operation, since the reading out is done in synchronization with the SYNC signal (8 kHz), maintain the set address in the same state for 250  $\mu$ s or more.



**Fig. 30 Method of reading out internal data memory**

Table 6 Internal data memory and related control registers (1/4)

Function name	Internal data memory name	Address	Initial value		Modes in which updating and read are possible		
			Data	Data value	In initialization mode	During idle state	During operation
Gain control	Transmit gain (TXGAIN)	02ACh	0080h	0 dB	Y	Y	Y
	Receive gain (RXGAIN)	02ADh	0080h	0 dB	Y	Y	Y
	Side tone gain (STGAIN)	02AEh	0000h	MUTE	Y	Y	Y
	Gain fade control (GAIN_FADE_CONT)	02AFh	0000h	disabled	Y	Y	N
	Gain fade-in step (GAIN_FADE_IN_ST)	02B0h	4C10h	+1.5dB	Y	Y <sup>*1</sup>	N
	Gain fade-out step (GAIN_FADE_OUT_ST)	02B1h	35D9h	-1.5dB	Y	Y <sup>*1</sup>	N
Tone generation 0 TONE_GENO	TGEN0 transmit control	CR19	00h	Transmission stopped	Y	Y	Y
	TGEN0 in-execution flag (TGEN0_EXE_FLAG) (Read-only memory)	1141h	0000h	Not in execution	Y	Y	Y
	TONE A frequency control (TGEN0_FREQ_A)	1143h	0CCCCh	400 Hz	Y	Y	N
	TONE B frequency control (TGEN0_FREQ_B)	1145h	007Ah	15 Hz	Y	Y	N
	TONE A gain control (TGEN0_GAIN_A)	1147h	0080h	-13.3 dBm0	Y	Y	Y
	TONE B gain control (TGEN0_GAIN_B)	1148h	0080h	-13.3 dBm0	Y	Y	Y
	TGEN0 time control 0 (TGEN0_TIM_M0)	1149h	0FA0h	500 ms	Y	Y	N
	TGEN0 time control 1 (TGEN0_TIM_M1)	114Ch	0FA0h	500 ms	Y	Y	N
	TGEN0 RX section tone total gain (TGEN0_RXGAIN_TOTAL)	1150h	0080h	0 dB	Y	Y	Y
	TGEN0 TX section tone total gain (TGEN0_TXGAIN_TOTAL)	1151h	0080h	0 dB	Y	Y	Y
	TGEN0 fade control (TGEN0_FADE_CONT)	113Bh	0000h	disabled	Y	Y	N
	TGEN0 fade-in step (TGEN0_FADE_IN_ST)	113Ch	47CFh	+1dB	Y	Y	N
	TGEN0 fade-out step (TGEN0_FADE_OUT_ST)	113Dh	390Ah	-1dB	Y	Y	N
	TGEN0 fade-out time (TGEN0_FADE_OUT_TIM)	113Eh	002Bh	43 Sync	Y	Y	N
	TGEN0 total gain fade control (TGEN0_GAIN_TOTAL_FADE_CONT)	114Dh	0000h	disabled	Y	Y	N
	TGEN0 total gain fade-in step (TGEN0_GAIN_TOTAL_FADE_IN_ST)	114Eh	4C10h	+1.5dB	Y	Y	N
TGEN0 total gain fade-out step (TGEN0_GAIN_TOTAL_FADE_OUT_ST)	114Fh	35D9h	-1.5dB	Y	Y	N	

\*1 when gain fade is disabled

Table 7 Internal data memory and related control registers (2/4)

Function name	Internal data memory name	Address	Initial value		Modes in which updating and read are possible		
			Data	Data value	In initialization mode	During idle state	During operation
Tone generation 1 TONE_GEN1	TGEN1 transmit control	CR20	00h	Transmission stopped	Y	Y	Y
	TGEN1 in-execution flag (TGEN1_EXE_FLAG) (Read-only memory)	1158h	0000h	Not in execution	Y	Y	Y
	TONE C frequency control (TGEN1_FREQ_C)	115Ah	0CCCCh	400 Hz	Y	Y	N
	TONE D frequency control (TGEN1_FREQ_D)	115Ch	007Ah	15 Hz	Y	Y	N
	TONE C gain control (TGEN1_GAIN_C)	115Eh	0080h	-13.3 dBm0	Y	Y	Y
	TONE D gain control (TGEN1_GAIN_D)	115Fh	0080h	-13.3 dBm0	Y	Y	Y
	TGEN1 time control 0 (TGEN1_TIM_M0)	1160h	0FA0h	500 ms	Y	Y	N
	TGEN1 time control 1 (TGEN1_TIM_M1)	1163h	0FA0h	500 ms	Y	Y	N
	TGEN1 RX section tone total gain (TGEN1_RXGAIN_TOTAL)	1167h	0080h	0 dB	Y	Y	Y
	TGEN1 TX section tone total gain (TGEN1_TXGAIN_TOTAL)	1168h	0080h	0 dB	Y	Y	Y
	TGEN1 fade control (TGEN1_FADE_CONT)	1152h	0000h	Stopped	Y	Y	N
	TGEN1 fade-in step (TGEN1_FADE_IN_ST)	1153h	47CFh	+1dB	Y	Y	N
	TGEN1 fade-out step (TGEN1_FADE_OUT_ST)	1154h	390Ah	-1dB	Y	Y	N
	TGEN1 fade-out time (TONE1_FADE_OUT_TIM)	1155h	002Bh	43 Sync	Y	Y	N
	TGEN1 total gain fade control (TGEN1_GAIN_TOTAL_FADE_CONT)	1164h	0000h	Stopped	Y	Y	N
	TGEN1 total gain fade-in step (TGEN1_GAIN_TOTAL_FADE_IN_ST)	1165h	4C10h	+1.5dB	Y	Y	N
TGEN1 total gain fade-out step (TGEN1_GAIN_TOTAL_FADE_OUT_ST)	1166h	35D9h	-1.5dB	Y	Y	N	
FSK generator FSK_GEN	FSK output control (FGEN_EN)	CR2-B6	0b	Stopped	Y	Y	Y
	FSK output data setting complete flag (FGEN_FLAG)	CR5-B0	0b	Writable	Y	Y	Y
	FSK output data setting register (FGEN_D[7:0])	CR18	00h	00h	Y	Y	Y
	FSK gain control (FGEN_GAIN)	02C4h	0080h	-13.3 dBm0	Y	Y	N

Table 8 Internal data memory and related control registers (3/4)

Function name	Internal data memory name	Address	Initial value		Modes in which updating and read are possible		
			Data	Data value	In initialization mode	During idle state	During operation
TONE 0 detector TONE_DET0	TONE 0 control (TDET0_EN)	CR2-B3	0b	Stopped	Y	Y	Y
	Main signal detect level control (TDET0_S_TH)	1356h	1EBBh	-5.3 dBm0	Y	Y	N
	Noise detect level control (TDET0_N_TH)	136Bh	1EBBh	-5.3 dBm0	Y	Y	N
	Detect ON guard timer control (TDET0_ON_TM)	136Ch	0028h	5 ms	Y	Y	N
	Detect OFF guard timer control (TDET0_OFF_TM)	136Dh	0028h	5 ms	Y	Y	N
	Detect frequency (TDET0_FREQ)	---- h	-	1650 Hz	Y	N	N
TONE 1 detector TONE_DET1	TONE 1 control (TDET1_EN)	CR2-B4	0b	Stopped	Y	Y	Y
	Main signal detect level control (TDET1_S_TH)	1382h	1EBBh	-5.3 dBm0	Y	Y	N
	Noise detect level control (TDET1_N_TH)	1397h	1EBBh	-5.3 dBm0	Y	Y	N
	Detect ON guard timer control (TDET1_ON_TM)	1398h	0028h	5 ms	Y	Y	N
	Detect OFF guard timer control (TDET1_OFF_TM)	1399h	0028h	5 ms	Y	Y	N
	Detect frequency (TDET1_FREQ)	---- h	-	2100 Hz	Y	N	N
DTMF detector DTMF_REC	DTMF control (DTMF_EN)	CR2-B2	0b	Stopped	Y	Y	Y
	Detect level control (DTMF_TH)	0170h	1000h	-37.0 dBm0	Y	Y	N
	Detect ON guard timer control (DTMF_ON_TM)	01D5h	00A0h	20 ms	Y	Y	N
	Detect OFF guard timer control (DTMF_OFF_TM)	01D7h	00A0h	20 ms	Y	Y	N
	Noise detect function control (DTMF_NDET_CONT)	01D8h	0002h	Enabled	Y	Y	N
Echo canceller	EC control (EC_EN)	CR2-B1	0b	Stopped	Y	Y	Y
	EC control (EC_CR)	002Ch	0012h	HD ATT OFF	Y	Y	Y
	GLPAD control (GLPAD_CR)	002Dh	000Fh	+6/-6 dB	Y	Y	N
Dial pulse detector DPDET	Dial pulse detect control (DPDET_EN)	CR10-B6	0b	Stopped	Y	Y	Y
	Detect ON guard timer control (DPDET_ON_TIM)	0FCBh	0028h	5 ms	Y	Y	N
	Detect OFF guard timer control (DPDET_OFF_TIM)	0FCCh	0028h	5 ms	Y	Y	N
	Detect polarity control (DPDET_POL)	0FCAh	0000h	Positive logic	Y	Y	N
	End of detect timer control (DPDET_DETOFF_TIM)	0FD1h	03E8h	125 ms	Y	Y	N
	Detect code (DPDET_CODE) (Read only data memory)	0FD3h	0000h	Not detected	Y	Y	Y
Dial Pulse generator DPGEN	Dial pulse output control (DPGEN_EN) (Can be read out)	0FBDh	0000h	Stopped	Y	Y	Y
	Pulse count setting (DPGEN_DATA)	0FBEh	0000h	Stopped	Y	Y	N
	Dial pulse speed control (DPGEN_PPS)	0FBFh	0000h	10 pps	Y	Y	N
	Dial pulse make ratio control (DPGEN_DUTY)	0FC0h	0108h	33 ms	Y	Y	N
	End of output control (DPGEN_OFF_TIM)	0FC2h	03E8h	125 ms	Y	Y	N
Output polarity control (DPGEN_POL)	0FC3h	0000h	Positive logic	Y	Y	N	

**Table 9 Internal data memory and related control registers (4/4)**

Function name	Internal data memory name	Address	Initial value		Modes in which updating and read are possible		
			Data	Data value	In initialization mode	During idle state	During operation
TIMER	Timer control (TIM_EN)	0FB7h	0000h	Stopped	Y	Y	Y
	Timer counter value display (TIM_COUNT) (read only data memory)	0FB8h	0000h	Count value 0000h	Y	Y	Y
	Timer data setting (TIM_DATA)	0FB9h	FFFFh	MAX FFFFh	Y	Y	N
Outband control	Outband control (OUTBAND_CONTROL)	0FDAh	0000h	Stopped	Y	N	N
Outband G.729.A data	Outband G.729.A data (OUTBAND_G729_DAT)	00A6h 00A7h 00A8h 00A9h 00AAh	7852h 80A0h 00FAh C200h 07D6h	—	Y	N	N
Version	LSI code display (ML7074_VERSION) (read only data memory)	0152h	0003h	ML7074-004	Y	Y	Y

**Note:**

**Initialization mode:** The state after release from a power down reset, and in which the initial values of control registers and internal data memory can be altered.

**During idle state:** The state in which the function given in the function name column has stopped.

**During operation:** The state in which the function given in the function name column is operating.

### Gain Control (TXGAIN, RXGAIN, STGAIN)

It is possible to change the values of the transmit gain (TXGAIN), receive gain (RXGAIN), and side tone gain (STGAIN). The positions of the respective gain controllers are the following.

- Transmit gain (TXGAIN): Immediately before the speech CODEC input.
- Receive gain (RXGAIN): Immediately after the speech CODEC output.
- Side tone gain (STGAIN): Added to the input of the receiver section LPF from the output of the transmitter section BPF of the linear PCM CODEC.

#### A. Internal data memory for adjusting transmit gain (TXGAIN)

Initial value: 0080h (0.0 dB)

When changing the gain value, compute it using the following equation:

Equation:  $0080h \times GAIN$

Example: Making the gain +6 dB ( $\times 2$ ):

$0080h \times 2 = 0100h$

- Upper limit : About 40 dB higher (data: 3200h)
- : 0 dB (data: 0080h)
- Lower limit : About -42 dB (data: 0001h)
- : MUTE (data: 0000h)

#### B. Internal data memory for adjusting receive gain (RXGAIN)

Initial value: 0080h (0.0 dB)

When changing the gain value, compute it using the following equation:

Equation:  $0080h \times GAIN$

Example: Making the gain +6 dB ( $\times 2$ ):

$0080h \times 2 = 0100h$

- Upper limit : About 40 dB higher (data: 3200h)
- : 0 dB (data: 0080h)
- Lower limit : About -42 dB (data: 0001h)
- : MUTE (data: 0000h)

#### C. Internal data memory for adjusting side tone gain (STGAIN)

Initial value: 0000h (MUTE)

When changing the side tone gain value, compute it using the following equation:

Equation:  $1000h \times GAIN$

Example: Making the gain -20 dB ( $\times 0.1$ ):

$1000h \times 0.1 = 019Ah$

- Upper limit : 0 dB (data: 1000h)
- Lower limit : About -72 dB (data: 0001h)
- : MUTE (data: 0000h)

## D. Internal data memory for gain fade (GAIN\_FADE\_CONT)

“1” in B0 enables fade-in/-out in Tx gain alternation; “1” in B1 enables the function in Rx gain alternation; and “1” in B2 enables the function at muting in outband control.

	B7	B6	B5	B4	B3	B2	B1	B0
	—	—	—	—	—	OUTBAND _FADE_ _CONT	RX_FADE _CONT	TX_FADE _CONT
Initial value	0	0	0	0	0	0	0	0

Initial value : 0000h (Outband : disabled, Rx : disabled, Tx : disabled)

B7, 6, 5, 4, 3 : Reserved bits (Prohibited to change the initial settings)

B2 : OUTBAND\_FADE\_CONT

1 : ON (Fading-in/-out at muting and at un-muting)

0 : OFF

B1 : RX\_FADE\_CONT

1 : ON (Fading-in/-out at Rx gain alternation)

0 : OFF

B0 : TX\_FADE\_CONT

1 : ON (Fading-in/-out at Tx gain alternation)

0 : OFF

## E. Internal data memory for gain fade-in step (GAIN\_FADE\_IN\_ST)

Initial value: 4C10h (+1.5dB)

When changing the step value, X, compute it using the following equation:

Equation:  $10^{(X/20)} * 16384$

Example: Making the step value +3 dB:

$10^{(3/20)} * 16384 = 23143d = 5A67h$

Upper limit : About +6.0 dB (data: 7FFFh)

Lower limit : About +0.1 dB (data: 40BDh)

## F. Internal data memory for gain fade-out step (GAIN\_FADE\_OUT\_ST)

Initial value: 35D9h (-1.5dB)

When changing the step value, X, compute it using the following equation:

Equation:  $10^{(X/20)} * 16384$

Example: Making the step value -3 dB:

$10^{(-3/20)} * 16384 = 11598d = 2D4Eh$

Upper limit : About -6.0 dB (data: 2000h)

Lower limit : About -0.1 dB (data: 3F44h)

(Note) Step values for fade-in and fade-out can be determined independently; whereas the step values determined for fade-in and fade-out are common to Tx gain, Rx gain and OUTBAND\_FADE\_CONT.

**Tone Generator0 (TONE\_GEN0)**

It is possible to set the various types of parameters of the tone generator block.

**A. Internal data memory for tone frequency control**

TONE\_A (TGEN0\_FREQ\_A)  
Initial value: 0CCCh (400 Hz)  
TONE\_B (TGEN0\_FREQ\_B)  
Initial value: 007Ah (15 Hz)

At the initial setting values a TONE A of 400 Hz and a TONE B of 15 Hz are output. Use the following equation to compute the value of the setting when changing the frequency.

Equation:  $A \times 8.192$  (A is the frequency to be set)

Example: To set a frequency of 2100 Hz:

$$2100 \times 8.192 \cong 4333h$$

Upper limit : 3 kHz (data: 6000h)  
Lower limit : 15 Hz (data: 007Ah)

**B. Internal data memory for tone gain control**

TONE\_A (TGEN0\_GAIN\_A)  
Initial value: 0080h  
TONE\_B (TGEN0\_GAIN\_B)  
Initial value: 0080h

The output level with the initial setting will be -13.3 dBm0. Use the following equation to compute the value of the setting when changing the gain.

Equation:  $0080h \times \text{GAIN}$

Example: For reducing the gain by 6 dB ( $\times 0.5$ ):

$$0080h \times 0.5 = 0040h$$

Upper limit : 12 dB more (data: 01FDh)  
Lower limit : -12 dB less (data: 0020h)

**Notice:**

Make sure that the maximum amplitude does not exceed 3.17 dBm0 when the tones are multiplied or added.

## C. Internal data memory for tone output time control (TGEN0\_TIM\_M0/TGEN0\_TIM\_M1)

TGEN0\_TIM\_M0

(Output time duration)

Initial value: 0FA0h (500 ms)

TGEN0\_TIM\_M1

(Output time duration)

Initial value: 0FA0h (500 ms)

Compute the value using the following equation when changing the time durations:

Equation:  $T/0.125$  (T is the time duration in ms)

Example: When setting a time duration of 200 ms:

 $200/0.125 = 1600d = 0640h$ 

Upper limit : 4095.875 ms (data: 7FFFh)

Lower limit : 0.125 ms (data: 0001h)

Notice:

It is prohibited to set a time duration of 0000h (0 ms) and hence be sure never to make such a setting.

The tone output times set here are commonly valid for TONE\_A and TONE\_B, and cannot be determined differently.

## D. Internal data memory for tone total gain control (TGEN0\_RXGAIN\_TOTAL, TGEN0\_TXGAIN\_TOTAL)

TGEN0\_RXGAIN\_TOTAL

Initial value: 0080h

TGEN0\_TXGAIN\_TOTAL

Initial value: 0080h

The initial values will be 0 dB. Compute using the following equation when changing the output level.

Equation:  $0080h \times \text{GAIN}$ 

Example: Decreasing the output level by 6 dB:

 $0080h \times 0.5 = 0040h$ 

Upper limit : 40 dB higher (data: 3200h)

Lower limit : -40 dB lower (data: 0001h)

: MUTE (data: 0000h)

Notice:

The maximum amplitude should never exceed 1.3 Vp-p.

## E. Internal data memory for TGEN0 fade control (TGEN0\_FADE\_CONT)

Initial value: 0000h (disabled)

“0000h” in this data memory enables fade-in/-out with tone gain control.

0000h: Fade-in/-out disabled

0001h: Fade-in/-out enabled

Notice:

When this fade-in/-out function is enabled, be sure that a corresponding fade-out step value and fade-out time are also set correctly.

## F. Internal data memory for TGEN0 fade-in step value control (TGEN0\_FADE\_IN\_ST)

Initial value: 47CFh (+1.0dB)

Compute using the following equation when changing the step value, X.

Equation:  $10^{(X/20)} \times 16384$

Example: Sets a fade-in step to +3dB:

$10^{(3/20)} \times 16384 = 23143d = 5A67h$

Upper limit : about +6.0dB (data: 7FFFh)

Lower limit : about +0.1dB (data: 40BDh)

Notice:

The value set here are commonly valid for TONE\_A and TONE\_B, and cannot be determined differently.

## G. Internal data memory for TGEN0 fade-out step value control (TGEN0\_FADE\_OUT\_ST)

Initial value: 390Ah (-1.0dB)

Compute using the following equation when changing the step value, X.

Equation:  $10^{(X/20)} \times 16384$

Example: Sets a fade-out step to -3dB:

$10^{(-3/20)} \times 16384 = 11598d = 2D4Eh$

Upper limit : about -6.0dB (data: 2000h)

Lower limit : about -0.1dB (data: 3F44h)

Notice:

The value set here are commonly valid for TONE\_A and TONE\_B, and cannot be determined differently.

## H. Internal data memory for TGEN0 fade-out time control (TGEN0\_FADE\_OUT\_TIM)

Initial value: 002Bh (43 Sync)

Compute using the following equation when changing the fade-out time.

Equation:  $43dB / \text{fade-out step value} [dB]$

Example: in a case with a fade-out step value 2dB:

$43/2 = 21d = 15h$

Upper limit : 422 sync (data: 01A6h)

Lower limit : 8 sync (data: 0008h)

Notice:

“0000h” is prohibited to set.

Set a fade-out time < TIM\_M0, TIM\_M1

The value set here are commonly valid for TONE\_A and TONE\_B, and cannot be determined differently.

## I. Internal data memory for TGEN0 total gain fade-out control (TGEN0\_GAIN\_TOTAL\_FADE\_CONT)

Initial value: 0000h (disabled)

“0000h” in this data memory enables a function of total gain fade-in/-out for Tx and Rx.

0000h: disabled

0001h: enabled

Notice:

The control of this function is commonly valid for Tx and Rx, and cannot be determined differently.

J. Internal data memory for fade-in step value control of TGEN0 total gain (TGEN0\_GAIN\_TOTAL\_FADE\_IN\_ST)

Initial value: 4C10h (+1.5dB)

Compute using the following equation when changing the step value, X.

Equation:  $10^{(X/20)} * 16384$

Example: Sets a fade-in step to +3dB:

$10^{(3/20)} * 16384 = 23143d = 5A67h$

Upper limit : about +6.0dB (data: 7FFFh)

Lower limit : about +0.1dB (data: 40BDh)

Notice:

The value set here are commonly valid for Tx and Rx, and cannot be determined differently.

K. Internal data memory for fade-out step value control of TGEN0 total gain (TGEN0\_GAIN\_TOTAL\_FADE\_OUT\_ST)

Initial value: 35D9h (-1.5dB)

Compute using the following equation when changing the step value, X.

Equation:  $10^{(X/20)} * 16384$

Example: Sets a fade-out step to -3dB:

$10^{(-3/20)} * 16384 = 11598d = 2D4Eh$

Upper limit : about -6.0dB (data: 2000h)

Lower limit : about -0.1dB (data: 3F44h)

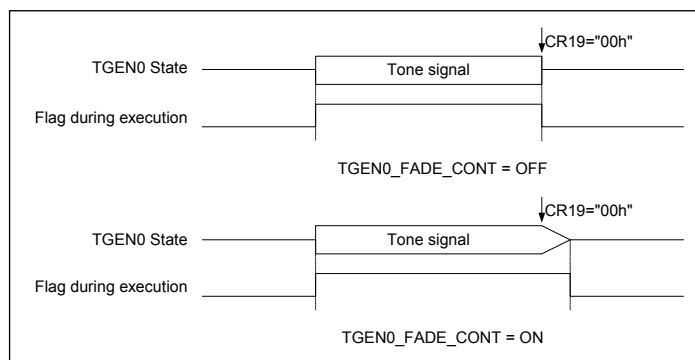
Notice:

Step values can be set differently and parameters set are common to TGEN0\_TXGAIN\_TOTAL and TGEN0\_RXGAIN\_TOTAL.

L. Internal data memory for TGEN0 in-execution flag (TGEN0\_EXE\_FLAG)

This address becomes "0001h" when a tone generator is under operation.

Initial value: 0000h



**Tone Generator1 (TONE\_GEN1)**

It is possible to set the various types of parameters of the tone generator block.

**A. Internal data memory for tone frequency control**

TONE\_C (TGEN1\_FREQ\_C)  
Initial value: 0CCC<sub>h</sub> (400 Hz)  
TONE\_D (TGEN1\_FREQ\_D)  
Initial value: 007A<sub>h</sub> (15 Hz)

At the initial setting values a TONE C of 400 Hz and a TONE D of 15 Hz are output. Use the following equation to compute the value of the setting when changing the frequency.

Equation:  $A \times 8.192$  (A is the frequency to be set)

Example: To set a frequency of 2100 Hz:

$$2100 \times 8.192 \cong 4333\text{h}$$

Upper limit : 3 kHz (data: 6000<sub>h</sub>)  
Lower limit : 15 Hz (data: 007A<sub>h</sub>)

**B. Internal data memory for tone gain control**

TONE\_C (TGEN1\_GAIN\_C)  
Initial value: 0080<sub>h</sub>  
TONE\_D (TGEN1\_GAIN\_D)  
Initial value: 0080<sub>h</sub>

The output level with the initial setting will be -13.3 dBm<sub>0</sub>. Use the following equation to compute the value of the setting when changing the gain.

Equation:  $0080\text{h} \times \text{GAIN}$

Example: For reducing the gain by 6 dB ( $\times 0.5$ ):

$$0080\text{h} \times 0.5 = 0040\text{h}$$

Upper limit : 12 dB more (data: 01FD<sub>h</sub>)  
Lower limit : -12 dB less (data: 0020<sub>h</sub>)

Notice:

Make sure that the maximum amplitude does not exceed 3.17 dBm<sub>0</sub> when the tones are multiplied or added.

## C. Internal data memory for tone output time control (TGEN1\_TIM\_M0/TGEN1\_TIM\_M1)

TGEN1\_TIM\_M0

(Output time duration)

Initial value: 0FA0h (500 ms)

TGEN1\_TIM\_M1

(Output time duration)

Initial value: 0FA0h (500 ms)

Compute the value using the following equation when changing the time durations:

Equation:  $T/0.125$  (T is the time duration in ms)

Example: When setting a time duration of 200 ms:

 $200/0.125 = 1600d = 0640h$ 

Upper limit : 4095.875 ms (data: 7FFFh)

Lower limit : 0.125 ms (data: 0001h)

Notice:

It is prohibited to set a time duration of 0000h (0 ms) and hence be sure never to make such a setting.

The tone output times set here are commonly valid for TONE\_A and TONE\_B, and cannot be determined differently.

## D. Internal data memory for tone total gain control (TGEN1\_RXGAIN\_TOTAL, TGEN1\_TXGAIN\_TOTAL)

TGEN1\_RXGAIN\_TOTAL

Initial value: 0080h

TGEN1\_TXGAIN\_TOTAL

Initial value: 0080h

The initial values will be 0 dB. Compute using the following equation when changing the output level.

Equation:  $0080h \times \text{GAIN}$ 

Example: Decreasing the output level by 6 dB:

 $0080h \times 0.5 = 0040h$ 

Upper limit : 40 dB higher (data: 3200h)

Lower limit : -40 dB lower (data: 0001h)

: MUTE (data: 0000h)

Notice:

The maximum amplitude should never exceed 1.3 Vp-p.

## E. Internal data memory for TGEN1 fade control (TGEN1\_FADE\_CONT)

Initial value: 0000h (disabled)

“0000h” in this data memory enables fade-in/-out with tone gain control.

0000h: Fade-in/-out disabled

0001h: Fade-in/-out enabled

Notice:

When this fade-in/-out function is enabled, be sure that a corresponding fade-out step value and fade-out time are also set correctly, otherwise a pop noise might be generated at a tail.

## F. Internal data memory for TGEN1 fade-in step value control (TGEN1\_FADE\_IN\_ST)

Initial value: 47CFh (+1.0dB)

Compute using the following equation when changing the step value, X.

Equation:  $10^{(X/20)} \times 16384$

Example: Sets a fade-in step to +3dB:

$10^{(3/20)} \times 16384 = 23143d = 5A67h$

Upper limit : about +6.0dB (data: 7FFFh)

Lower limit : about +0.1dB (data: 40BDh)

Notice:

The value set here are commonly valid for TONE\_A and TONE\_B, and cannot be determined differently.

## G. Internal data memory for TGEN1 fade-out step value control (TGEN1\_FADE\_OUT\_ST)

Initial value: 390Ah (-1.0dB)

Compute using the following equation when changing the step value, X.

Equation:  $10^{(X/20)} \times 16384$

Example: Sets a fade-out step to -3dB:

$10^{(-3/20)} \times 16384 = 11598d = 2D4Eh$

Upper limit : about -6.0dB (data: 2000h)

Lower limit : about -0.1dB (data: 3F44h)

Notice:

The value set here are commonly valid for TONE\_A and TONE\_B, and cannot be determined differently.

## H. Internal data memory for TGEN1 fade-out time control (TGEN1\_FADE\_OUT\_TIM)

Initial value: 002Bh (43 Sync)

Compute using the following equation when changing the fade-out time.

Equation:  $43dB / \text{fade-out step value} [dB]$

Example: in a case with a fade-out step value 2dB:

$43/2 = 21d = 15h$

Upper limit : 422 sync (data: 01A6h)

Lower limit : 8 sync (data: 0008h)

Notice:

“0000h” is prohibited to set.

Set a fade-out time less than TIM\_M0

The value set here are commonly valid for TONE\_C and TONE\_D, and cannot be determined differently.

## I. Internal data memory for TGEN1 total gain fade-out control (TGEN1\_GAIN\_TOTAL\_FADE\_CONT)

Initial value: 0000h (disabled)

“0000h” in this data memory enables a function of total gain fade-in/-out for Tx and Rx.

0000h: disabled

0001h: enabled

Notice:

The control of this function is commonly valid for Tx and Rx, and cannot be determined differently.

J. Internal data memory for fade-in step value control of TGEN1 total gain (TGEN1\_GAIN\_TOTAL\_FADE\_IN\_ST)

Initial value: 4C10h (+1.5dB)

Compute using the following equation when changing the step value, X.

Equation:  $10^{(X/20)} * 16384$

Example: Sets a fade-in step to +3dB:

$10^{(3/20)} * 16384 = 23143d = 5A67h$

Upper limit : about +6.0dB (data: 7FFFh)

Lower limit : about +0.1dB (data: 40BDh)

Notice:

The value set here are commonly valid for Tx and Rx, and cannot be determined differently.

K. Internal data memory for fade-out step value control of TGEN1 total gain (TGEN1\_GAIN\_TOTAL\_FADE\_OUT\_ST)

Initial value: 35D9h (-1.5dB)

Compute using the following equation when changing the step value, X.

Equation:  $10^{(X/20)} * 16384$

Example: Sets a fade-out step to -3dB:

$10^{(-3/20)} * 16384 = 11598d = 2D4Eh$

Upper limit : about -6.0dB (data: 2000h)

Lower limit : about -0.1dB (data: 3F44h)

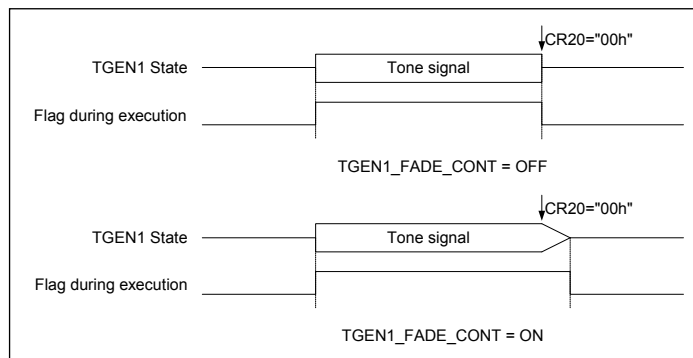
Notice:

Step values can be set differently and parameters set are common to TGEN1\_TXGAIN\_TOTAL and TGEN1\_RXGAIN\_TOTAL.

L. Internal data memory for TGEN1 in-execution flag (TGEN1\_EXE\_FLAG)

This address becomes "0001h" when a tone generator is under operation.

Initial value: 0000h



### FSK Generator (FSK\_GEN)

The FSK generator (FSK\_GEN) frequency modulates the data set in the control register, and outputs it to VFRO0 and VFRO1. Table 10 lists the specifications of the FSK generator, and Figure 31 shows its block diagram. The FSK generator is made up of an FSK signal generation block that allows buffering of up to three words, a register for setting data, and a gain adjustment block.

By setting FGEN\_EN (CR2-B6) to “1”, the FSK generator starts operating, and outputs a mark bit (“1”) successively. To start data transmission, set the first transmit data in FGEN\_D[7:0](CR18), and set FGEN\_FLAG (CR5-B0) to “1”. When FGEN\_FLGA is set to “1”, the FSK generator transfers the transmit data in FGEN\_D[7:0] to the internal buffer if it has a free space, and clears FGEN\_FLAG to “0”.

The data that has been transferred to the internal buffer is then output with ST (Start Bit “0”) and SP (Stop Bit “1”) appended to in the transmit sequence shown in Figure 32. When setting the next transmit data, do so when FGEN\_FLAG is “0”. If there is no data waiting to be transmitted in the internal buffer of the FGEN signal generation block, a mark bit (“1”) is successively transmitted. The internal buffer of the FSK signal generation block has a 3-stage structure; it can buffer data of up to 4 words including the FSK output data setup register FGEN\_D[7:0].

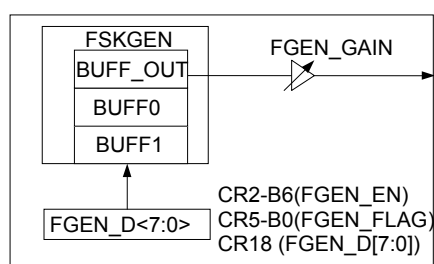
To end transmission, set FGEN\_EN to “0” while FGEN\_FLAG is “0”. If the transmission of the data that is set in FGEN\_D[7:0] is completed before FGEN\_EN is set to “0”, the FSK generator stops. If FGEN\_EN is set to “0” while the FSK generator transmits a mark bit (“1”) successively, and if there is no data waiting to be transmitted, the FSK generator stops after outputting a mark bit (“1”) for a maximum of 1-bit period.

Figure 33 shows the transmit and stop timings, and Figure 34 shows an example of control.

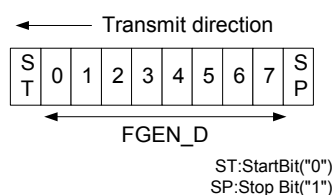
In addition, the output level of the FSK generator can be changed by FGEN\_GAIN (internal data memory).

**Table 10 Specifications of FSK generator**

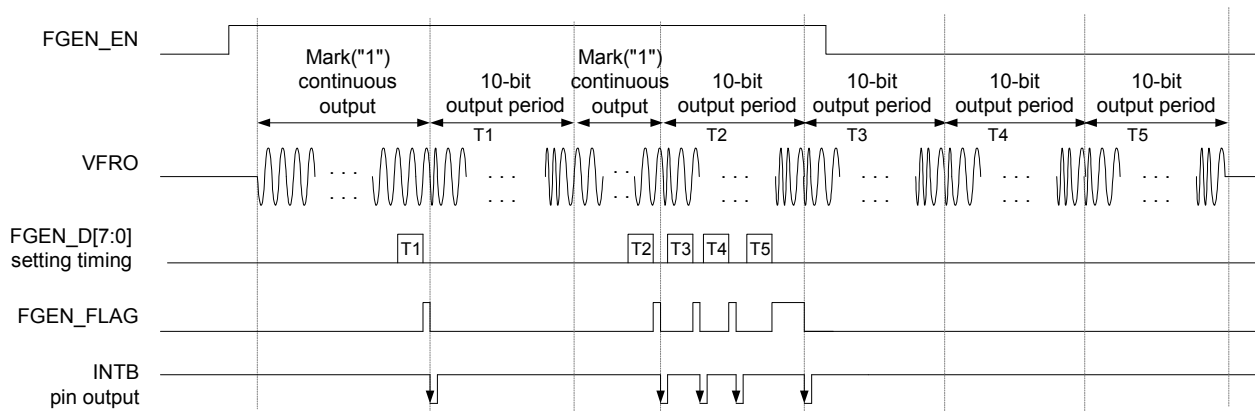
Modulation method	Frequency modulation
Synchronization	Start-stop
Transfer speed	1200 bps
Output frequencies	1300 Hz (Data “1” Mark)
	2100 Hz (Data “0” Space)
Output data setting register	8 bits (CR18-B[7:0])
Output level	-13.3 dBm0 (Initial value, gain adjustment possible)



**Fig. 31 FSK generator block diagram**



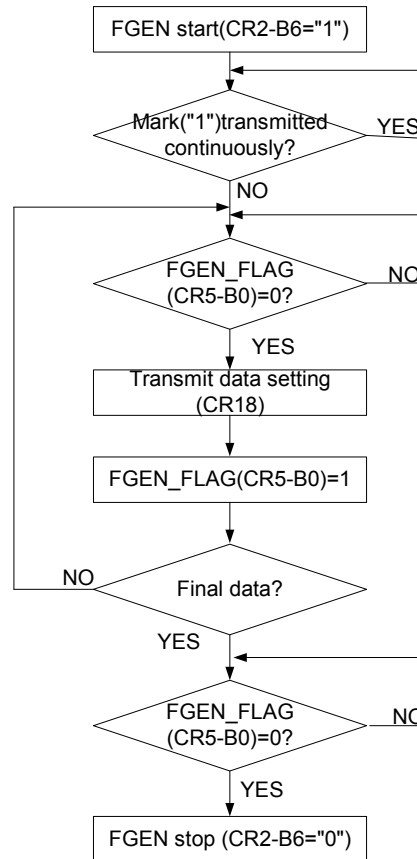
**Fig. 32 Data transmit sequence**



**Fig. 33 FSK data transmit and stop timings (when transmitting 50 bits)**

Note:

When the FSK generator is operating, it is recommended to keep the other detector sections deactive so that they do not cause to generate an interrupt.



**Fig. 34 FSK output control method**

A. Internal data memory for FSK gain adjustment (FGEN\_GAIN)

Initial value: 0080h

The output level of the initial value will be  $-13.3$  dBm0. Compute the setting value using the following equation when changing the output level.

Equation:  $0080h \times \text{GAIN}$

Example: For decreasing the output level by 6 dB.

$0080h \times 0.5 = 0040h$

Upper limit: 40 dB higher (data: 3200h)

Lower limit: 40 dB lower (data: 0001h)

Notice:

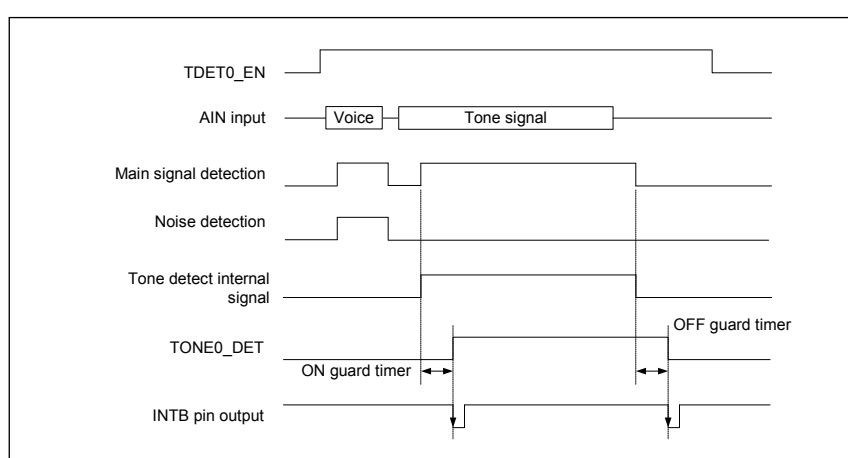
The maximum amplitude should not exceed 1.3Vp-p.

### TONE0 Detector (TONE\_DET0)

The TONE\_DET0 detector is composed of a main signal detector that detects the signal of the corresponding frequency, noise detector that detects the signals other than the corresponding frequency, and ON/OFF guard timers.

The detector detects a 1650 Hz single tone signal input from AIN0 and AIN1. This detector becomes effective when the control register TDET0\_EN (CR2-B3) is "1". When the tone is detected (main signal detected and noise not detected), the control register TONE0\_DET (CR3-B3) will be set to "1". TONE0\_DET will become "0" when the tone is not detected or when TDET0\_EN is "0".

The tone detector can adjust detect time using ON/OFF guard timers and adjust detect level for noise detection. The initial values of both ON and OFF guard timers are 5 ms. The initial values for both main signal detect level and noise detect level are -5.3 dBm0. The tone detect timing is shown in Fig. 35.



**Fig. 35 Tone detect timing**

#### A. Internal data memory for control of the main signal detect level (TDET0\_S\_TH)

Initial value: 1EBBh (-5.3 dBm0)

Compute the setting value using the following equation when changing the detect level X.

$$\text{Equation: } 10^{((X-3.17)/20)} \times 2/\pi \times 32768$$

Example: Detect level of -5.3 dBm0.

$$10^{((-5.3-3.17)/20)} \times 2/\pi \times 32768 = 7857d = 1EBBh$$

Upper limit	: 3.17 dBm0	(data: 517Ch)
	: -5.3 dBm0	(data: 1EBBh)
Lower limit	: -35 dBm0	(data: 0102h)

#### B. Internal data memory for control of the noise detect level (TDET0\_N\_TH)

Initial value: 1EBBh (-5.3 dBm0)

Compute the setting value using the following equation when changing the detect level X.

$$\text{Equation: } 10^{((X-3.17)/20)} \times 2/\pi \times 32768$$

Example: Detect level of -5.3 dBm0.

$$10^{((-5.3-3.17)/20)} \times 2/\pi \times 32768 = 7857d = 1EBBh$$

Upper limit	: 3.17 dBm0	(data: 517Ch)
	: -5.3 dBm0	(data: 1EBBh)
Lower limit	: -30 dBm0	(data: 0102h)

Write 7FFFh to the above-mentioned internal data memory (TDET0\_N\_TH) when stopping the noise detect function.

C. Internal data memory for the detect ON guard timer (TDET0\_ON\_TM)

Initial value: 0028h (5 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 5 ms

$$5/0.125 = 40d = 0028h$$

Upper limit : 4095.875 ms (data: 7FFFh)

: 5 ms (data: 0028h)

Lower limit : 0.125 ms (data: 0001h)

D. Internal data memory for the detect OFF guard timer (TDET0\_OFF\_TM)

Initial value: 0028h (5 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 5 ms

$$5/0.125 = 40d = 0028h$$

Upper limit : 4095.875 ms (data: 7FFFh)

: 5 ms (data: 0028h)

Lower limit : 0.125 ms (data: 0001h)

E. Internal data memory for controlling the detect frequency (TDET0\_FREQ)

Initial value: —

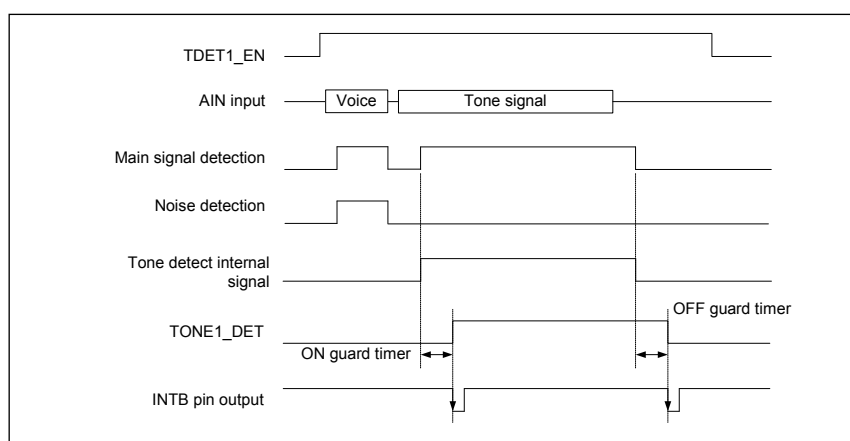
The detect frequency can be changed. Contact ROHM's responsible sales person when you wish to change the detect frequency.

### TONE1 Detector (TONE\_DET1)

The TONE\_DET1 detector is composed of a main signal detector that detects the signal of the corresponding frequency, noise detector that detects the signals other than the corresponding frequency, and ON/OFF guard timers.

The detector detects a 2100 Hz single tone signal input from AIN0 and AIN1. This detector becomes effective when the control register TDET1\_EN (CR2-B4) is "1". When the tone is detected (main signal detected and noise not detected), the control register TONE1\_DET (CR3-B4) will be set to "1". TONE1\_DET will become "0" when the tone is not detected or when TDET1\_EN is "0".

The tone detector can adjust detect time using ON/OFF guard timers and adjust detect level for noise detection. The initial values of both ON and OFF guard timers are 5 ms. The initial values for both main signal detect level and noise detect level are -5.3 dBm0. The tone detect timing is shown in Fig. 36.



**Fig. 36 Tone detect timing**

#### A. Internal data memory for control of the main signal detect level (TDET1\_S\_TH)

Initial value: 1EBBh (-5.3 dBm0)

Compute the setting value using the following equation when changing the detect level X.

$$\text{Equation: } 10^{((X-3.17)/20)} \times 2/\pi \times 32768$$

Example: Detect level of -5.3 dBm0.

$$10^{((-5.3-3.17)/20)} \times 2/\pi \times 32768 = 7857d = 1EBBh$$

Upper limit	: 3.17 dBm0	(data: 517Ch)
	: -5.3 dBm0	(data: 1EBBh)
Lower limit	: -35 dBm0	(data: 0102h)

#### B. Internal data memory for control of the noise detect level (TDET0\_N\_TH)

Initial value: 1EBBh (-5.3 dBm0)

Compute the setting value using the following equation when changing the detect level X.

$$\text{Equation: } 10^{((X-3.17)/20)} \times 2/\pi \times 32768$$

Example: Detect level of -5.3 dBm0.

$$10^{((-5.3-3.17)/20)} \times 2/\pi \times 32768 = 7857d = 1EBBh$$

Upper limit	: 3.17 dBm0	(data: 517Ch)
	: -5.3 dBm0	(data: 1EBBh)
Lower limit	: -30 dBm0	(data: 0102h)

Write 7FFFh to the above-mentioned internal data memory (TDET1\_N\_TH) when stopping the noise detect function.

C. Internal data memory for the detect ON guard timer (TDET1\_ON\_TM)

Initial value: 0028h (5 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 5 ms

$5/0.125 = 40d = 0028h$

Upper limit : 4095.875 ms (data: 7FFFh)

: 5 ms (data: 0028h)

Lower limit : 0.125 ms (data: 0001h)

D. Internal data memory for the detect OFF guard timer (TDET1\_OFF\_TM)

Initial value: 0028h (5 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 5 ms

$5/0.125 = 40d = 0028h$

Upper limit : 4095.875 ms (data: 7FFFh)

: 5 ms (data: 0028h)

Lower limit : 0.125 ms (data: 0001h)

E. Internal data memory for controlling the detect frequency (TDET1\_FREQ)

Initial value: —

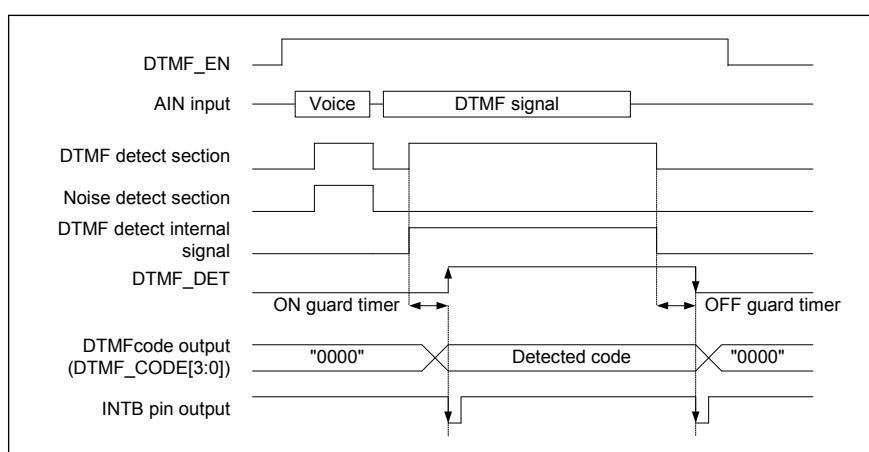
The detect frequency can be changed. Contact ROHM's responsible sales person when you wish to change the detect frequency.

### DTMF Detector (DTMF\_REC)

This section detects the DTMF signal input from AIN. The DTMF detector is made up of a DTMF detection block that detects the DTMF signal, a noise detection block that detects signals other than the DTMF signal, an ON guard timer, and an OFF guard timer. The DTMF detector becomes effective when the control register DTMF\_EN (CR2-B2) is "1", and when a valid DTMF signal is detected, DTMF\_DET (CR4-B4) becomes "1" and the received code is stored in DTMF\_0 to DTMF\_3 (CR4-B3, 2, 1, 0).

When no DTMF signal is detected or when DTMF\_EN is "0", DTMF\_DET will be "0" and also DTMF\_0 to DTMF\_3 will be "0000". The DTMF detect timing is shown in Fig. 38.

The DTMF detector is composed of a detector section, an ON guard timer, and an OFF guard timer. The detect time and the detect level can be adjusted. The initial values of both ON and OFF guard timers are 20 ms. The initial value of the detect level is -37.0 dBm0.



**Fig. 37 DTMF detect timing**

#### A. Internal data memory for gain adjustment (DTMF\_TH)

Initial value: 1000h (-37.0 dBm0)

Compute the setting value using the following equation when changing the detect level.

Equation:  $1000h \times 1 / \text{GAIN}$

Example: Increasing the detect level by 6 dB.

$1000h \times 0.5 = 0800h$

Upper limit : 12 dB higher (data: 0400h)

Lower limit : 12 dB lower (data: 4000h)

Note:

The detection level set in the above data memory (DTMF\_TH) is the common detection level of the DTMF detection block and the noise detection block.

#### B. Internal data memory for the ON guard timer (DTMF\_ON\_TM)

Initial value: 00A0h (20 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 5 ms

$5/0.125 = 40d = 0028h$

Upper limit : 4095.875 ms (data: 7FFFh)

: 5 ms (data: 0028h)

Lower limit : 0.125 ms (data: 0001h)

C. Internal data memory for the OFF guard timer (DTMF\_OFF\_TM)

Initial value: 00A0h (20 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 5 ms

$5/0.125 = 40d = 0028h$

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

D. Internal data memory for noise detection function control (DTMF\_NDET\_CONT)

Initial value: 0002h (noise detection function enabled)

By writing 0000h into this internal data memory, the noise detection function of the DTMF detector is disabled.

Notice:

During DTMF signal detection, if the DTMF signal changes to another code successively, the received code changes and an interrupt can be generated with DTMF\_DET in the "1" state.

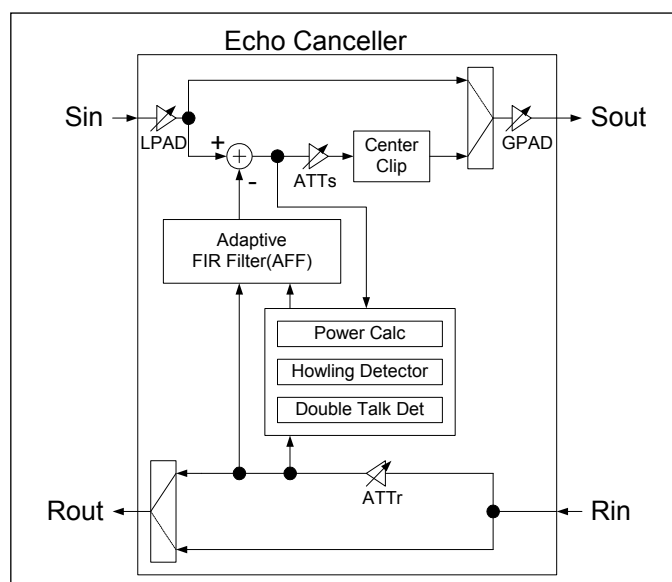
Note:

To use this internal data memory by inputting signals in G.711 coding format from the PCM interface, set the input level of the DTMF signal (per wave) at -10 dBmO or lower. If the DTMF signal is input at a level greater than -10 dBmO, the DTMF signal may not be detected normally.

### Echo Canceller

The block diagram of the echo canceller is shown in Fig. 38.

The echo canceller has a delay time of 32 ms and is activated by setting a "1" in EC\_EN (CR2-B1). The operation setting of the echo canceller is done mainly using the internal data memory locations EC\_CR and GLPAD\_CR.



**Fig. 38 Echo canceller block diagram**

#### A. Echo canceller control (EC\_CR)

Initial value: 0012h

Write "0" in the higher order 8 bits (B15 to B8)

	B7	B6	B5	B4	B3	B2	B1	B0
	THR	—	HLD	HDB	CLP	—	ATTB	—
Initial value	0	0	0	1	0	0	1	0

B7: Through mode control

1: Through mode

0: Normal mode (echo cancel operation)

When this through mode control bit of the echo canceller is set, the data of Rin and Sin are output directly to Rout and Sout while retaining their respective echo coefficients. Further, during the through mode, the HLD, HDB, ATTB and CLP functions are disabled.

B6: Reserved bit. Prohibited to change the initial value.

B5: Coefficient update control

1: Coefficient fixed

0: Coefficient updated

This bit selects the presence or absence of updating of the adaptive FIR filter (AFF) coefficient of the echo canceller. This function becomes valid when THR is in the normal mode.

B4: Howling detector control

1: OFF

0: ON

This bit controls the function of detecting and removing howling which is generated in a hands-free acoustic system, etc. This function becomes valid when THR is in the normal mode.

B3: Center clip control

1: ON

0: OFF

This bit controls the center clip function in which the Sout output is forcibly fixed to the minimum positive value when the Sout output of the echo canceller is  $-57$  dBm0 or less. This function becomes valid when THR is in the normal mode.

B2: Reserved bit. Prohibited to change the initial value.

B1: Attenuator control

1: ATT OFF

0: ATT ON

This bit selects the switching ON/OFF of the ATT function which prevents howling using the attenuators ATTs and ATTr provided at the Rin input and Sout output of the echo canceller. When only the Rin input is present, the attenuator (ATTs) of Sout will be inserted. When only the Sin input is present or when both the Sin and Rin inputs are present, the attenuator (ATTr) of Rin will be inserted. The respective attenuation values are 6 dB. This function becomes valid when THR is in the normal mode.

B0: Reserved bit. Prohibited to change the initial value.

B. GLPAD control (GLPAD\_CR)

Initial value: 000Fh

This data memory controls the GLPAD within the echo canceller. Write "0" in the higher order 8 bits (B15 to B8).

	B7	B6	B5	B4	B3	B2	B1	B0
	—	—	—	—	GPAD2	GPAD1	LPAD2	LPAD1
Initial value	0	0	0	0	1	1	1	1

B7, 6, 5, 4: Reserved bits.

B3, 2: Output level control

These bits control the GPAD level for the echo canceller output gain.

(0, 1): +18 dB

(0, 0): +12 dB

(1, 1): +6 dB

(1, 0): 0 dB

B1, 0: Input level control

These bits control the LPAD level for the echo canceller input loss.

(0, 1):  $-18$  dB

(0, 0):  $-12$  dB

(1, 1):  $-6$  dB

(1, 0): 0 dB

### C. Precautions in using the Echo Canceller

#### C-1

In the echo path, make sure that the echo signal does not cause saturation, waveform distortion, etc., in the external amplifier, etc. The echo attenuation becomes poor if any saturation or waveform distortion occur.

#### C-2

Make the settings so that the echo return loss (E.R.L.) is attenuating. Further, it is recommended to use the GLPAD function if the E.R.L. is set to be amplified. The echo attenuation gets deteriorated seriously if the E.R.L. is set to be amplified.

The E.R.L. is the attenuation (loss) of echo amount from the echo canceller output (Rout) to the echo canceller input (Sin).

#### C-3

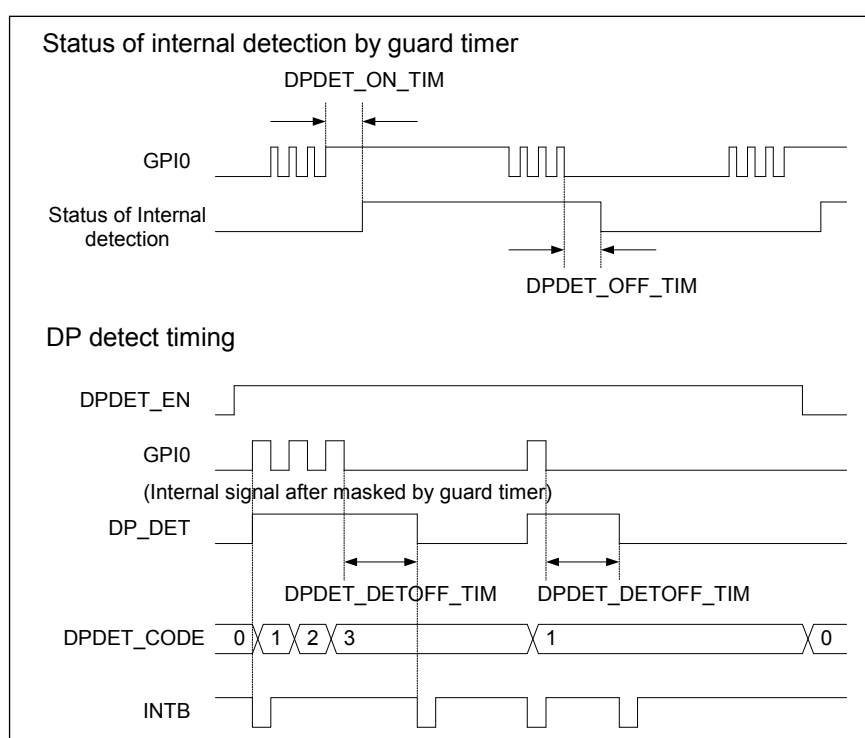
When the echo path can change (such as during a reconnected call), it is recommended to carry out a reset using EC\_EN (CR2-B1), PDNB, or SPDN (CR0-B7).

### Dial Pulse Detector (DPDET)

Dial pulse signals input at the general-purpose input pin GPIO are detected by this DPDET. The dial pulse detector becomes effective when the control register bit DPDET\_EN (CR10-B6) is "1". DP\_DET (CR4-B6) becomes "1" when a dial pulse signal is detected and the detected number of dial pulses is stored in DPDET\_CODE. The number of dial pulses detected should be read out from DPDET\_CODE at the time when DP\_DET goes from "1" to "0".

When a dial pulse signal is not detected, or when DPDET\_EN is "0", DP\_DET will remain "0".

The dial pulse detect timing is shown in Fig. 39. The dial pulse detector samples the dial pulse signal input at GPIO at 8 kHz sampling rate, and detects the dial pulses based on the settings of the ON guard timer (DPDET\_ON\_TIM) and OFF guard timer (DPDET\_OFF\_TIM). Further, it is possible to adjust the detect end time by setting the detect end timer (DPDET\_DETOFF\_TIM).



**Fig. 39 Dial pulse detect timing**

A. Dial pulse detect control register (DPDET\_EN CR10-B6)

0: Dial pulse detection stopped

1: Dial pulse detection active

B. Dial pulse detector detect status register (DP\_DET CR4-B6)

0: Dial pulses not detected

1: Dial pulses detected

This bit is set to "1" after DPDET\_EN has been set when an edge at GPIO is detected. Further, if no edge is detected for a period set in DPDET\_DETOFF\_TIM after an edge detection, this bit will be cleared automatically to "0".

## C. Internal data memory for ON guard timer (DPDET\_ON\_TIM)

Initial value: 0028h (5 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 5 ms

$5/0.125 = 40d = 0028h$

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

## D. Internal data memory for OFF guard timer (DPDET\_OFF\_TIM)

Initial value: 0028h (5 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 5 ms

$5/0.125 = 40d = 0028h$

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

## E. Internal data memory for detect polarity control (DPDET\_POL)

Initial value: 0000h (no polarity reversal)

Controls the polarity of the input from GPIO.

0000h: No polarity reversal

0001h: Polarity reversal present

## F. Internal data memory for detect end control (DPDET\_DETOFF\_TIM)

Initial value: 03E8h (125 ms)

Use the following equation when changing the timer value.

Equation: Guard timer value in ms/0.125 ms

Example: 125 ms

$125/0.125 = 1000d = 03E8h$

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 125 ms	(data: 03E8h)
Lower limit	: 0.125 ms	(data: 0001h)

## G. Internal data memory for indicating number of detected pulses (DPDET\_CODE)

Initial value: 0000h (not-detected state)

Indicates the number of detected pulses.

This internal data memory for indication is updated when an edge is detected.

## Notice:

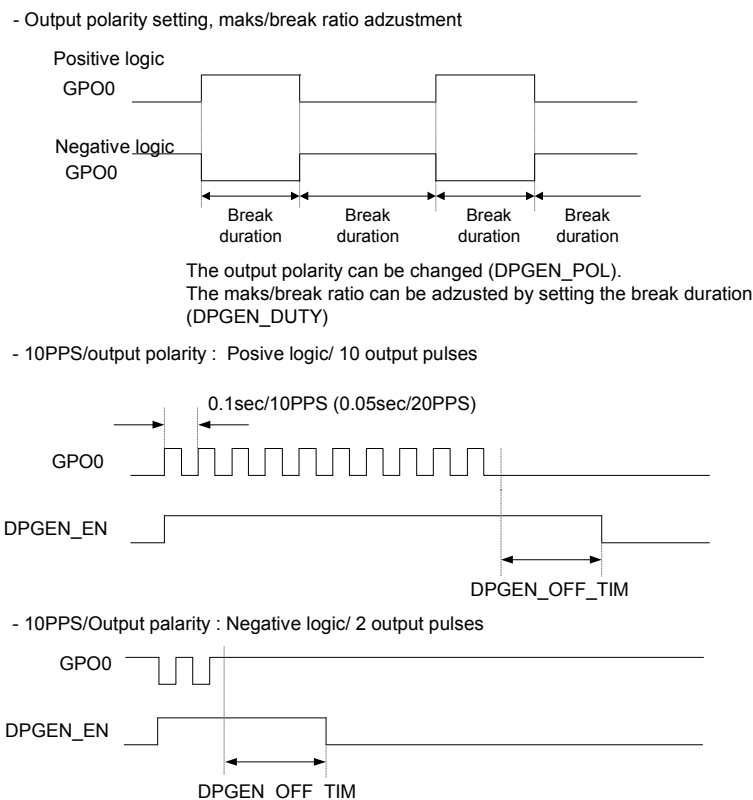
Ignore the interrupt occurred after the time set by the ON guard timer if the DPDET is activated under the following conditions:

- DPDET\_POL = "0", GPIO = "1"
- DPDET\_POL = "1", GPIO = "0"

### Dial Pulse Transmitter (DPGEN)

The dial pulse transmitter outputs a dial pulse signal at the general-purpose output pin GPO0. The dial pulse generation will be effective when the control memory bit DPGEN\_EN is “1”, and a dial pulse signal is output with the number of pulses set in DPGEN\_DATA.

The dial pulse output timing is shown in Fig. 40. The speed (rate) of dial pulses can be selected to be 10PPS or 20PPS by setting DPGEN\_PPS accordingly. Further, it is possible to adjust the make/break ratio by setting the break duration using DPGEN\_DUTY. Also, the output polarity of the dial pulse signal can be changed by DPGEN\_POL.



**Fig. 40 Dial pulse output timing**

#### A. Internal data memory for dial pulse transmit control (DPGEN\_EN)

Initial value: 0000h

The dial pulses are transmitted when a “0001h” is written in this data memory.

This data memory will be cleared automatically after a period of time set in DPGEN\_OFF\_TIM.

0000h: Dial pulse output stopped

0001h: Dial pulse output active

#### Notice:

Activate DPGEN with CR17-B0 (GPO0) being in the “0” state, according to the setting of internal of data memory for output polarity control (DPGEN\_POL).

DPGEN\_POL =0000h (positive logic) : CR17-B0 (GPO0) = “0”

DPGEN\_POL =0001h (negative logic) : CR17-B0 (GPO0) = “1”

## B. Internal data memory for setting the number of pulses (DPGEN\_DATA)

Initial value: 0000h

Upper limit: 10 (data: 000Ah)

Lower limit: 1 (data: 0001h)

## C. Internal data memory for dial pulse rate control (DPGEN\_PPS)

Initial value: 0000h

0000h: 10 PPS

0001h: 20 PPS

## D. Internal data memory for controlling make/break ratio (DPGEN\_DUTY)

Initial value: 0108h (33 ms/10 PPS, 16.5 ms/20 PPS)

Use the following equation when setting the “break” duration.

The value will be half this set value in the case of 20 PPS.

Equation: “break” output time duration in ms/0.125 ms

Example: 33 ms

 $33/0.125 = 264d = 0108h$ 

Upper limit : 100 ms (data: 0320h)

: 33 ms (data: 0108h)

Lower limit : 0.125 ms (data: 0001h)

## E. Internal data memory for end of output control (DPGEN\_OFF\_TIM)

Initial value: 03E8h (125 ms)

Use the following equation when setting the end of output control.

Equation: End of output time duration in ms/0.125 ms

Example: 125 ms

 $125/0.125 = 1000d = 03E8h$ 

Upper limit : 4095.875 ms (data: 7FFFh)

: 125 ms (data: 03E8h)

Lower limit : 0 ms (data: 0000h)

## F. Internal data memory for output polarity control (DPGEN\_POL)

Initial value: 0000h

Controls the polarity of output from GPO0.

Setup value: 0000h •••• Positive logic (Low: make segment, High: break segment)

Setup value: 0001h •••• Negative logic (Low: break segment, High: make segment)

**Timer (TIMER)**

This is a 16-bit up-counter timer. When a “0001h” is set in the internal memory for timer control (TIM\_EN), the timer starts counting up the timer count (TIM\_COUNT) at every 125  $\mu$ s. When the timer count value becomes equal to the timer data value, the timer counter value will be reset to “0000h” and the timer starts counting up again.

**A. Internal data memory for timer control (TIM\_EN)**

Initial value: 0000h

The timer starts counting up when “0001h” is written in this data memory location.

When a “0000h” is set here, the counting up will be stopped and the counter value will be cleared.

0000h: Stops counting

0001h: Starts counting

**B. Internal data memory for timer count indication (TIM\_COUNT)**

Initial value: 0000h

**C. Internal data memory for timer data (TIM\_DATA)**

Initial value: FFFFh

Upper limit : 8192 ms (data: FFFFh)

Lower limit : 0.250 ms (data: 0001h)

**Outband Control (OUTBAND\_CONTROL)**

This is a function is automatically to mute or to write silence data in Tx buffer when corresponding detection bit (\*\*\*\_DET) gets "1". Either to mute or to write silence data in Tx buffer differs among speech codec's as shown below;

G.711 ( $\mu$ -/A-law)	Mutes speech data given to codec
G.729.A	Writes silence data (80 bits) in Tx buffer The 80 bits meaning silence in G.729.A to write in Tx buffer as default could be altered any 80 bits you like in the initial mode.

Initial value : 0000h

	B7	B6	B5	B4	B3	B2	B1	B0
	—	—	—	—	—	TDET1 _OB_EN	TDET0 _OB_EN	DTMFDET _OB_EN
Initial Value	0	0	0	0	0	0	0	0

B7, 6, 5, 4, 3 : Reserved bits

B2 : TDET1\_OUTBAND\_EN control

1 : ON (Mutes speech data given to codec when TDET1\_DET is "1")

0 : OFF

B1 : TDET0\_OUTBAND\_EN control

1 : ON (Mutes speech data given to codec when TDET0\_DET is "1")

0 : OFF

B0 : DTMFDET\_OUTBAND\_EN control

1 : ON (Writes data specified by OUTBAND\_G729\_DAT which is silence as default when DTMF\_DET is "1")

0 : OFF

- Leak time of tones to Tx buffer

A referential equation for leak time of tones to Tx buffer with each speech codec is shown below;

G.711	$0\text{ms} + A + B$
G.729.A	$-10\text{ms to } -20\text{ms} + A + B$ * $-10\text{ms to } -20\text{ms}$ by prediction and framing process

A : detection delay time of a given detector (ms)

Depends upon input level, frequency, etc..

B : ON-guard timer time of a given detector

< Example >

If the detect delay time of a detector is about 30 ms and the ON-guard timer time of a detector is 20 ms, the leak time to the Tx buffer is shown below.

G.711  $30\text{ms} (A) + 20\text{ms} (B) = \text{approx. } 50\text{ms}$

G.729.A  $(-10\text{ms to } -20\text{ms}) + 20\text{ms} (A) + 20\text{ms} (B) = \text{approx. } 30\text{ms to } 40\text{ms}$

**Outband G.729.A data (OUTBAND\_G729\_DAT)**

When outband control is made in G.729.A mode, the data in the addresses below are written into Tx buffer when corresponding detection bit (\*\*\*\_DET) gets "1". The data to write into Tx buffer could be altered in the initial mode.

Address: 00A6h 00A7h 00A8h 00A9h 00AAh  
Initial value: 7852h 80A0h 00FAh C200h 07D6h

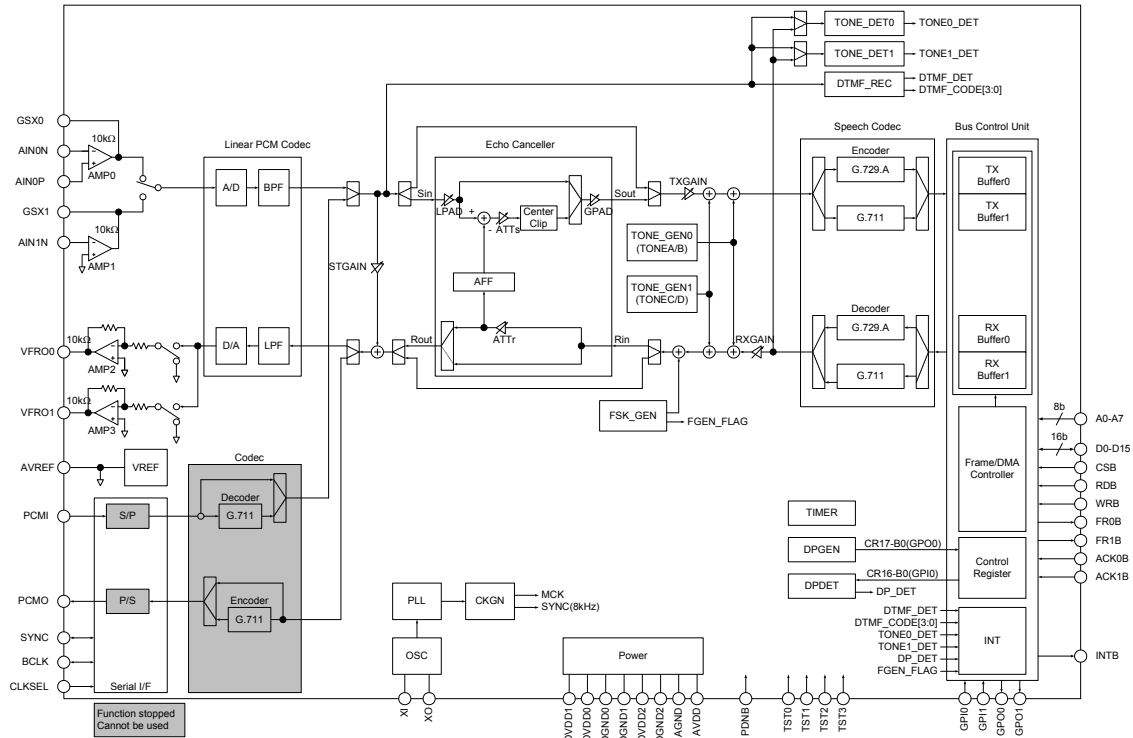
**LSI Code Indication (ML7074\_VERSION)**

The code ML7074-004 is indicated here.

Value: 0003h

**EXAMPLE OF CONFIGURATION**

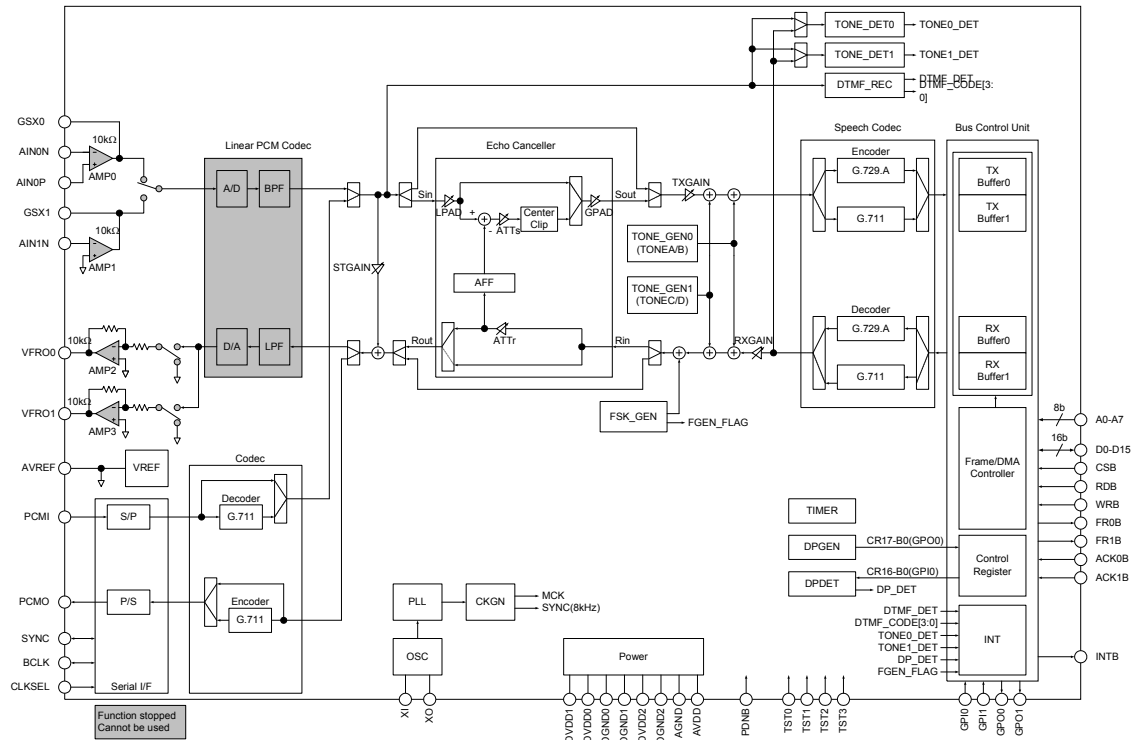
**Analog I/F mode**



**Example of settings in the initialization mode**

- CR15 = 40h \* This is mandatory.
- CR6=0Fh,CR7=FFh,CR8=00h,CR9=01h,CR1=80h (Address : 0FFh, Data : 0001h)
- \* This is mandatory. As for how to set them, refer to Method of Accessing and Controlling Internal Data Memory.
- CR11 = 00h (Frame/10 ms/16B/Speech CODEC = G.729.A)
- Various settings
- CR0 = 09h (OPE\_STAT = "1")

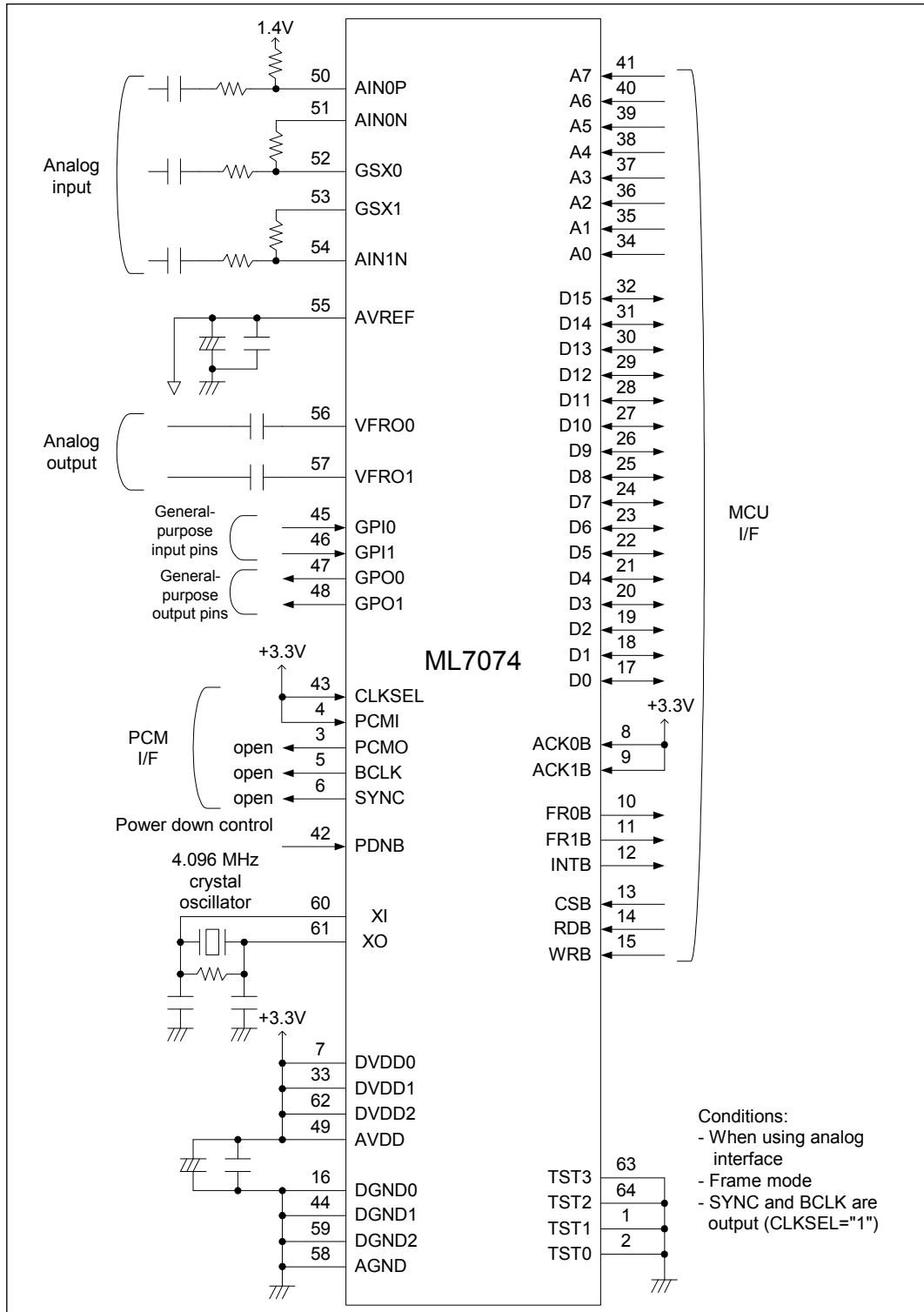
PCM I/F Mode



Examples of settings in the initialization mode

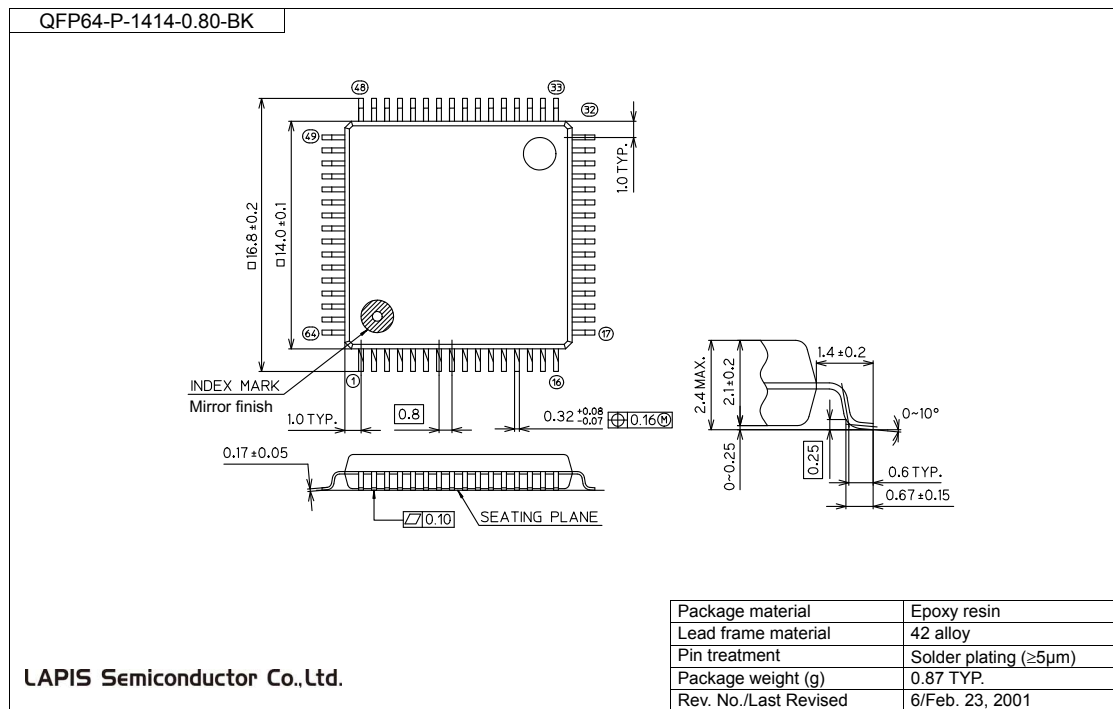
- CR15 = 40h \* This is mandatory.
- CR6=0Fh,CR7=FFh,CR8=00h,CR9=01h,CR1=80h (Address : 0FFFh, Data : 0001h)
- \* This is mandatory. As for how to set them, refer to Method of Accessing and Controlling Internal Data Memory.
- CR10 = 00h (VFRO1 = AVREF/VFRO0 = AVREF)
- CR11 = 00h (Frame/10 ms/16B/PCMIF = 16-bit linear)
- CR12 = 01h (Speech CODEC = G.729.A/PCMIF\_EN = "1")
- Various settings
- CR0 = 29h (AFE\_EN = Power down/LONG/OPE\_STAT = "1")

EXAMPLE OF APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7074-004-01	Nov. 12, 2003	–	–	Final edition 1

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