ML7074-003

VoIP CODEC

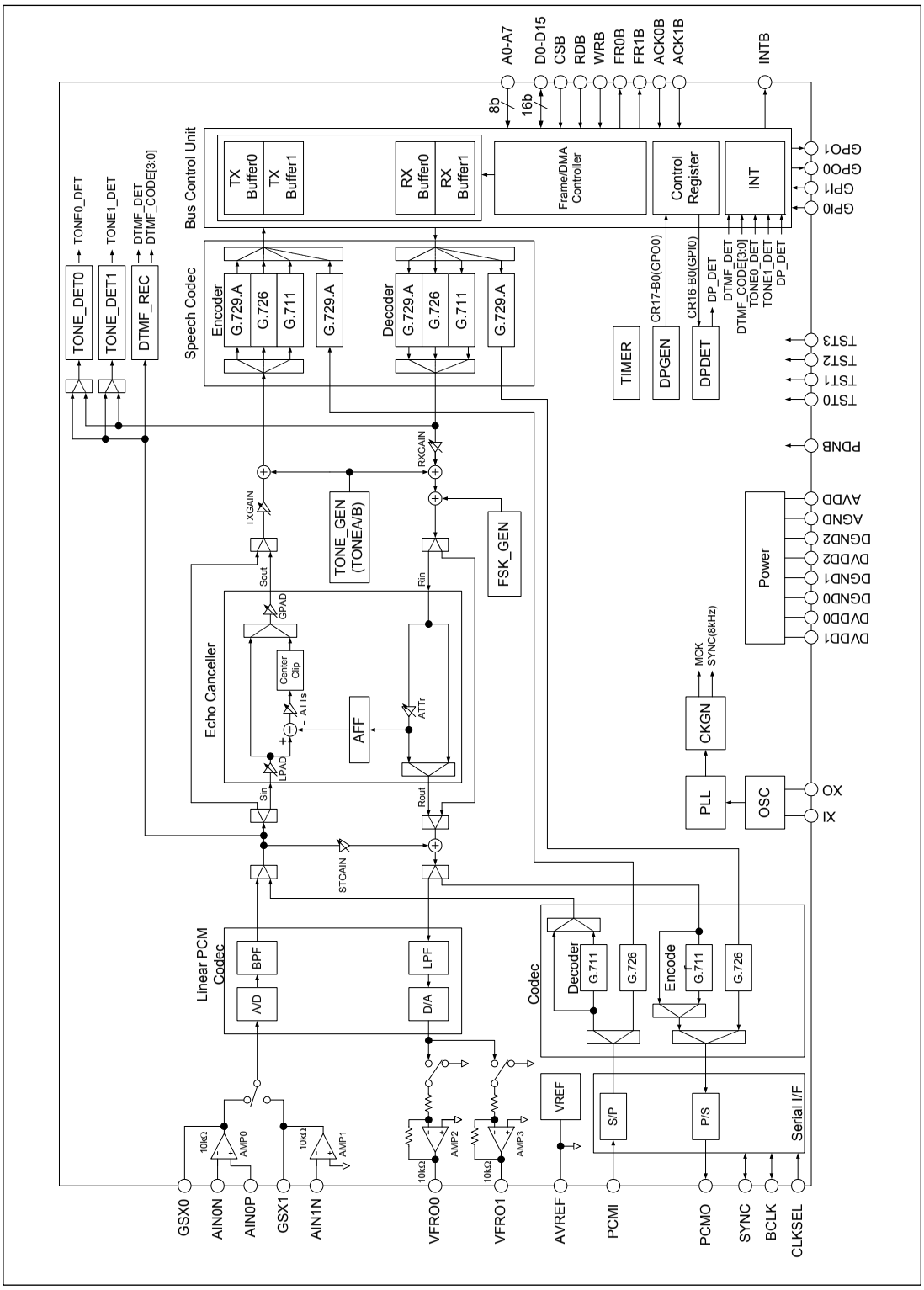
GENERAL DESCRIPTION

The ML7074-003 is a speech CODEC for VoIP. This LSI allows selection of G.729.A, G.726, or G.711 standard as a speech CODEC. The LSI is optimum for adding VoIP functions to TAs, routers, etc., since it has the functions of an echo canceller for 32 msec delay, DTMF detection, tone detection, tone generation, etc.

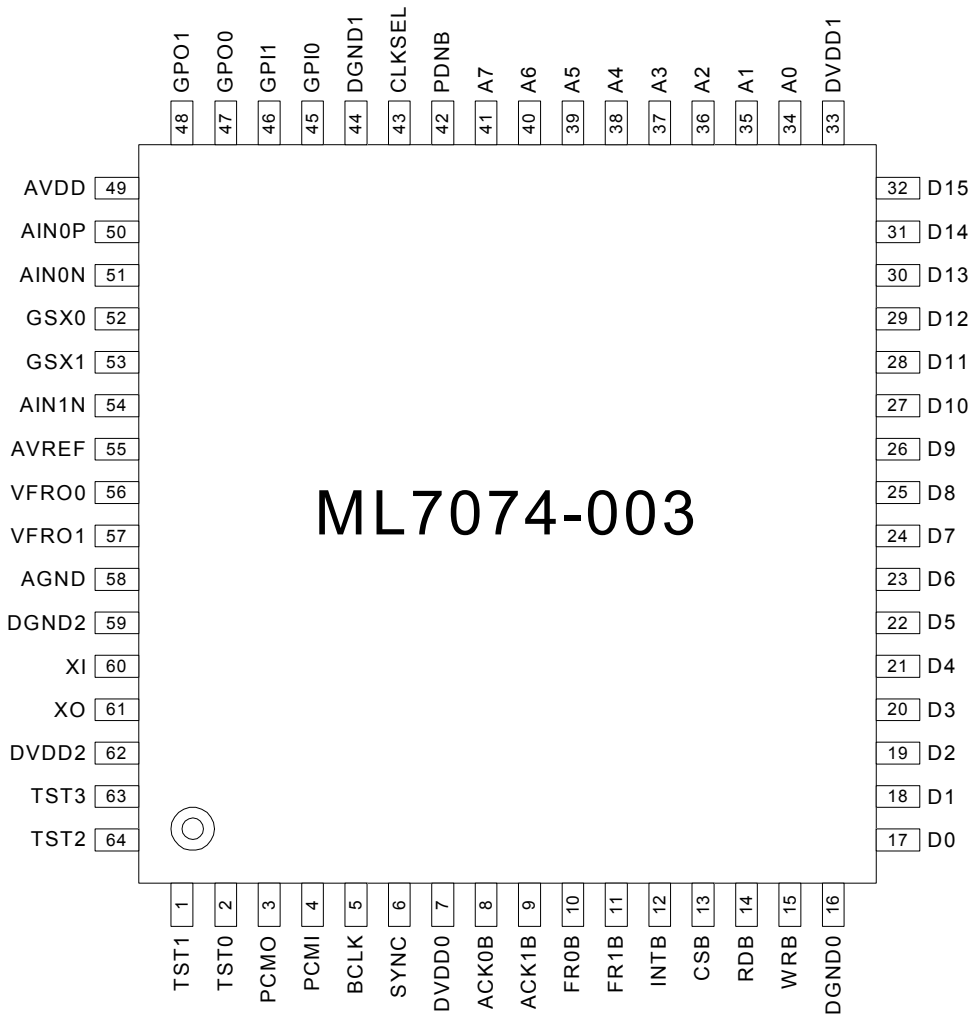
FEATURES

- Single 3.3 V power supply operation (DV_{DD}0, 1, 2, AV_{DD}: 3.0 to 3.6 V)
- Speech CODEC:
  Selectable among G.729.A (8 kbps), G726 (32 kbps), G.711 (64 kbps) μ-law, and A-law
  Mutual conversion function between G.729.A (8 kbps) and G.726 (32 kbps).
- Echo canceller for 32 ms delay
- DTMF detect function
- Tone detect function: 2 systems (1650 Hz, 2100 Hz: Detect frequency can be changed.)
- Tone generate function
- FSK generate function
- Dial pulse detect function
- Dial pulse transmit function
- Internal 1-channel 16-bit timer
- Built-in FIFO buffers (640 bytes) for transferring transmit and receive data
  Frame/DMA (slave) interface selectable.
- Master clock frequency: 4.096 MHz (crystal oscillation or external input)
- Hardware or software power down operation possible.
- Analog input/output type:
  Two built-in input amplifiers, 10 MΩ driving
  Two built-in output amplifiers, 10 kΩ driving
- Package:
  64-pin plastic QFP (QFP64-P-1414-0.80-BK)
- Ordering part number:
  ML7074-003GA

BLOCK DIAGRAM



PIN ASSIGNMENT (TOP VIEW)



64-pin plastic QFP

PIN DESCRIPTIONS

Pin No.	Symbol	I/O	PDNB = "0"	Description
1	TST1	I	"0"	Test control input 1: Normally input "0".
2	TST0	I	"0"	Test control input 0: Normally input "0".
3	PCMO	O	"Hi-z"	PCM data output
4	PCMI	I	I	PCM data input
5	BCLK	I/O	I	CLKSEL = "0" PCM shift clock input
			"L"	CLKSEL = "1" PCM shift clock output
6	SYNC	I/O	I	CLKSEL = "0" PCM sync signal 8 kHz input
			"L"	CLKSEL = "1" PCM sync signal 8 kHz output
7	$DV_{DD}0$	—	—	Digital power supply
8	ACK0B	I	I	Transmit buffer DMA access acknowledge signal input
9	ACK1B	I	I	Receive buffer DMA access acknowledge signal input
10	FR0B (DMARQ0B)	O	"H"	FR0B: (CR11-B7 = "0") Transmit buffer frame signal output DMARQ0B: (CR11-B7 = "1") Transmit buffer DMA access request signal output
11	FR1B (DMARQ1B)	O	"H"	FR1B: (CR11-B7 = "0") Receive buffer frame signal output DMARQ1B: (CR11-B7 = "1") Receive buffer DMA access request signal output
12	INTB	O	"H"	Interrupt request output "L" level is output for about 1.0 μsec when an interrupt is generated.
13	CSB	I	I	Chip select control input
14	RDB	I	I	Read control input
15	WRB	I	I	Write control input
16	DGND0	—	I	Digital ground (0.0 V)
17	D0	I/O	I	Data input/output
18	D1	I/O	I	Data input/output
19	D2	I/O	I	Data input/output
20	D3	I/O	I	Data input/output
21	D4	I/O	I	Data input/output
22	D5	I/O	I	Data input/output
23	D6	I/O	I	Data input/output
24	D7	I/O	I	Data input/output
25	D8	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = "1").

26	D9	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = “1”).
27	D10	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = “1”).
28	D11	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = “1”).
29	D12	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = “1”).
30	D13	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = “1”).
31	D14	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = “1”).
32	D15	I/O	I	Data input/output Fix to input state when using in 8-bit bus access (CR11-B5 = “1”).
33	$DV_{DD}1$	—	—	Digital power supply
34	A0	I	I	Address input
35	A1	I	I	Address input
36	A2	I	I	Address input
37	A3	I	I	Address input
38	A4	I	I	Address input
39	A5	I	I	Address input
40	A6	I	I	Address input
41	A7	I	I	Address input
42	PDNB	I	“0”	Power down input “0”: Power down reset “1”: Normal operation
43	CLKSEL	I	I	SYNC and BCLK I/O control input “0”: SYNC and BCLK become inputs “1”: SYNC and BCLK become outputs
44	DGND1	—	—	Digital ground (0.0 V)
45	GPI0	I	I	General-purpose input pin 0 (5 V tolerant input) /Secondary function: Dial pulse detect input pin
46	GPI1	I	I	General-purpose input pin 1 (5 V tolerant input)
47	GPO0	O	“L”	General-purpose output pin 0 (5 V tolerant output, can be pulled up externally) /Secondary function: Dial pulse transmit pin
48	GPO1	O	“L”	General-purpose output pin 1 (5 V tolerant output, can be pulled up externally)
49	AV_{DD}	—	—	Analog power supply
50	AIN0P	I	I	AMP0 non-inverted input
51	AIN0N	I	I	AMP0 inverted input
52	GSX0	O	“Hi-z”	AMP0 output (10 kΩ driving)
53	GSX1	O	“Hi-z”	AMP1 output (10 kΩ driving)
54	AIN1N	I	I	AMP1 inverted input
55	AVREF	O	“L”	Analog signal ground (1.4 V)

56	VFRO0	O	“Hi-z”	AMP2 Output (10 kΩ driving)
57	VFRO1	O	“Hi-z”	AMP3 Output (10 kΩ driving)
58	AGND	—		Analog ground (0.0 V)
59	DGND2	—		Digital ground (0.0 V)
60	XI	I	I	4.096 MHz crystal oscillator I/F, 4.096 MHz clock input
61	XO	O	“H”	4.096 MHz crystal oscillator I/F
62	$DV_{DD}2$	—		Digital power supply
63	TST3	I	“0”	Test control input 3: Normally input “0”.
64	TST2	I	“0”	Test control input 2: Normally input “0”.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Analog power supply voltage	VDA	—	−0.3 to 5.0	V
Digital power supply voltage	V_{DD}	—	−0.3 to 5.0	V
Analog input voltage	VAIN	Analog pins	−0.3 to V_{DD} + 0.3	V
Digital input voltage	VDIN1	Normal digital pins	−0.3 to V_{DD} + 0.3	V
	VDIN2	5 V tolerant pins	−0.3 to 6.0	V
Storage temperature range	Tstg	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Analog power supply voltage	VDA	—	3.0	3.3	3.6	V
Digital power supply voltage	V_{DD}	—	3.0	3.3	3.6	V
Operating temperature range	Ta	—	−20	—	60	°C
Digital high level input voltage	VIH1	Digital input pins	2.0	—	V_{DD}+ 0.3	V
	VIH2	GPI0 and GPI1 pins	2.0	—	5.5	V
Digital low level input voltage	VIL	Digital pins	−0.3	—	0.8	V
Digital input rise time	tIR	Digital pins	—	2	20	ns
Digital input fall time	tIF	Digital pins	—	2	20	ns
Digital output load capacitance	CDL	Digital pins	—	—	50	pF
Capacitance of bypass capacitor for AVREF	Cvref	Between AVREF and AGND	2.2+0.1	—	4.7+0.1	μF
Master clock frequency	Fmck	MCK	−0.01%	4.096	+0.01%	MHz
PCM shift clock frequency	Fbclk	BCLK (at input)	64	—	2048	kHz
PCM sync signal frequency	Fsync	SYNC (at input)	—	8.0	—	kHz
Clock duty ratio	DRCLK	MCK, BCLK (at input)	40	50	60	%
PCM sync timing	tBS	BCLK to SYNC (at input)	100	—	—	ns
	tSB	SYNC to BCLK (at input)	100	—	—	ns
PCM sync signal width	tWS	SYNC (at input)	1BCLK	—	100	μs

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply current	ISS	Standby state (PDNB = ”0”, V_{DD} = 3.3 V, Ta = 25°C)	—	5.0	20.0	μA
	$I_{DD}1$	Operating state 1 In the PCM/IF mode (SC_EN = “1”, PCMIF_EN = “1”, AFE_EN = “1”, TRANS_EN = “1”) Connect a 4.096 MHz crystal oscillator between XI and XO.	—	45.0	55.0	mA
	$I_{DD}2$	Operating state 2 When operating the whole system (SC_EN = “1”, PCMIF_EN = “0”, TRANS_EN = “0”, AFE_EN = “0”) Connect a 4.096 MHz crystal oscillator between XI and XO.	—	50.0	65.0	mA
Digital input pin input leakage current	IIH	Vin = DV_{DD}	—	0.01	1.0	μA
	IIL	Vin = DGND	−1.0	−0.01	—	μA
Digital I/O pin output leakage current	IOZH	Vout = DV_{DD}	—	0.01	1.0	μA
	IOZL	Vout = DGND	−1.0	−0.01	—	μA
High level output voltage	VOH	Digital output pins, I/O pins IOH = 4.0 mA IOH = 1.0 mA (XO pin)	2.2	—	—	V
Low level output voltage	VOL	Digital output pins, I/O pins IOL = −4.0 mA IOL = −1.0 mA (XO pin)	—	—	0.4	V
Input capacitance *1	CIN	Input pins	—	8	12	pF

Note: *1 Guaranteed design value

Analog Interface

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input resistance *1	RIN	AIN0N, AIN0P, AIN1N	10	—	—	MΩ
Output load resistance	RL	GSX0, GSX1, VFRO0, VFRO1	10	—	—	kΩ
Output load capacitance	CL	Analog output pins	—	—	50	pF
Offset voltage	VOF	VFRO0, VFRO1	−40	—	40	mV
Output voltage level *2	VO	GSX0, GSX1, VFRO0, VFRO1 RL = 10 kΩ	—	—	1.3	Vpp

Notes:

*1 Guaranteed design value

*2 −7.7 dBm (600Ω) = 0 dBm0, +3.17 dBm0 = 1.3 Vpp

AC Characteristics

CODEC (Speech CODEC in G.711 (μ-law) Mode)

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)				
Transmit frequency characteristics	LT1	0 to 60	0	25	—	—	dB
	LT2	300 to 3000		−0.15	—	0.20	dB
	LT3	1020		Reference value			—
	LT4	3300		−0.15	—	0.80	dB
	LT5	3400		0	—	0.80	dB
	LT6	3968.75		13	—	—	dB
Receive frequency characteristics	LR2	0 to 3000	0	−0.15	—	0.20	dB
	LR3	1020		Reference value			—
	LR4	3300		−0.15	—	0.80	dB
	LR5	3400		0	—	0.80	dB
	LR6	3968.75		13	—	—	dB
Transmit signal to noise ratio [*1]	SDT1	1020	3	35	—	—	dBp
	SDT2		0	35	—	—	dBp
	SDT3		−30	35	—	—	dBp
	SDT4		−40	28	—	—	dBp
	SDT5		−45	23	—	—	dBp
Receive signal to noise ratio [*1]	SDR1	1020	3	35	—	—	dBp
	SDR2		0	35	—	—	dBp
	SDR3		−30	35	—	—	dBp
	SDR4		−40	28	—	—	dBp
	SDR5		−45	23	—	—	dBp
Transmit inter-level loss error	GTT1	1020	3	−0.2	—	0.2	dB
	GTT2		−10	Reference value			—
	GTT3		−40	−0.2	—	0.2	dB
	GTT4		−50	−0.6	—	0.6	dB
	GTT5		−55	−1.2	—	1.2	dB
Receive inter-level loss error	GTR1	1020	3	−0.2	—	0.2	dB
	GTR2		−10	Reference value			—
	GTR3		−40	−0.2	—	0.2	dB
	GTR4		−50	−0.6	—	0.6	dB
	GTR5		−55	−1.2	—	1.2	dB
Idle channel noise [*1]	NIDLT	—	Analog input = AVREF	—	—	−68	dBm0p
	NIDLR	—	PCMI = ”1”	—	—	−72	dBm0p
Transmit absolute level [*2]	AVT	1020	0	0.285	0.320	0.359	Vrms
Receive absolute level [*2]	AVR	1020	0	0.285	0.320	0.359	Vrms
Power supply noise reject ratio	PSRRT	Noise frequency range: 0 to 50 kHz Noise level: 50mVpp	—	30	—	—	dB
	PSRRR		—	30	—	—	dB

Notes: *1 Using P-message filter

*2 0.320 Vrms = 0 dBm0 = −7.7 dBm (600Ω)

Gain Setting (Speech CODEC in G.711 (μ-law) Mode)

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transmit and receive gain setting accuracy	GAC	—	–1.0	—	1.0	dB

Tone Output (Speech CODEC in G.711 (μ-law) Mode)

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency deviation	fDFT	Relative to set frequency	–1.5	—	1.5	%
Output level	oLEV	Relative to set gain	–2.0	—	2.0	dB

DTMF Detector, Other Detectors (Speech CODEC in G.711 (μ-law) Mode)

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

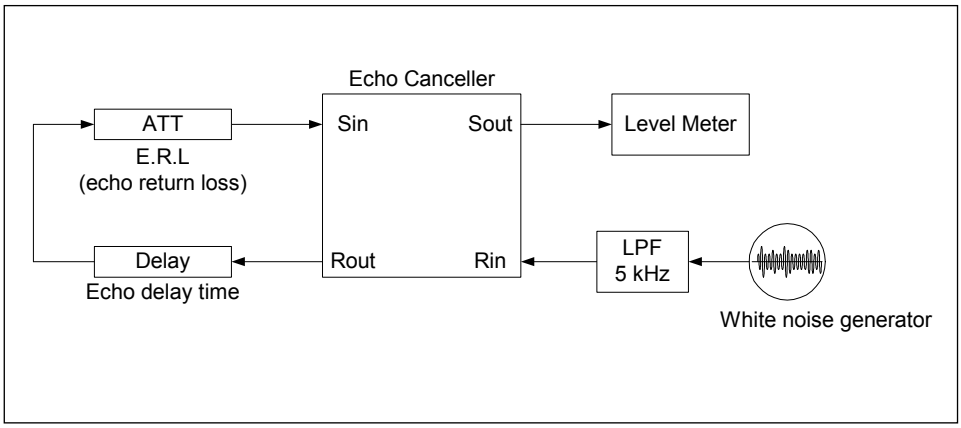
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detect level accuracy	dLAC	Relative to set detect level	–2.5	—	2.5	dB

Echo Canceller

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Echo attenuation	eRES	In the analog I/F mode In the PCM I/F (16-bit linear) mode	—	35	—	dB
		In the PCM I/F (G.711) mode		30		
Erasable echo delay time	tECT	—	—	—	32	ms

Measurement method



PDNB, XO, AVREF Timings

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power down signal pulse width	tPDNB	PDNB pin	1	—	—	μs
Oscillation start-up time	txtal	—	—	2+α	100	ms
AVREF rise time	tAVREF	AVREF = 1.4 (90%) C5 = 4.7 μF, C6 = 0.1 μF (See Fig. 9.)	—	—	600	ms
Initialization mode start-up time	tINIT	—	—	1	—	s

* α is a value that depends on the oscillation stabilizing time when using a crystal oscillator.

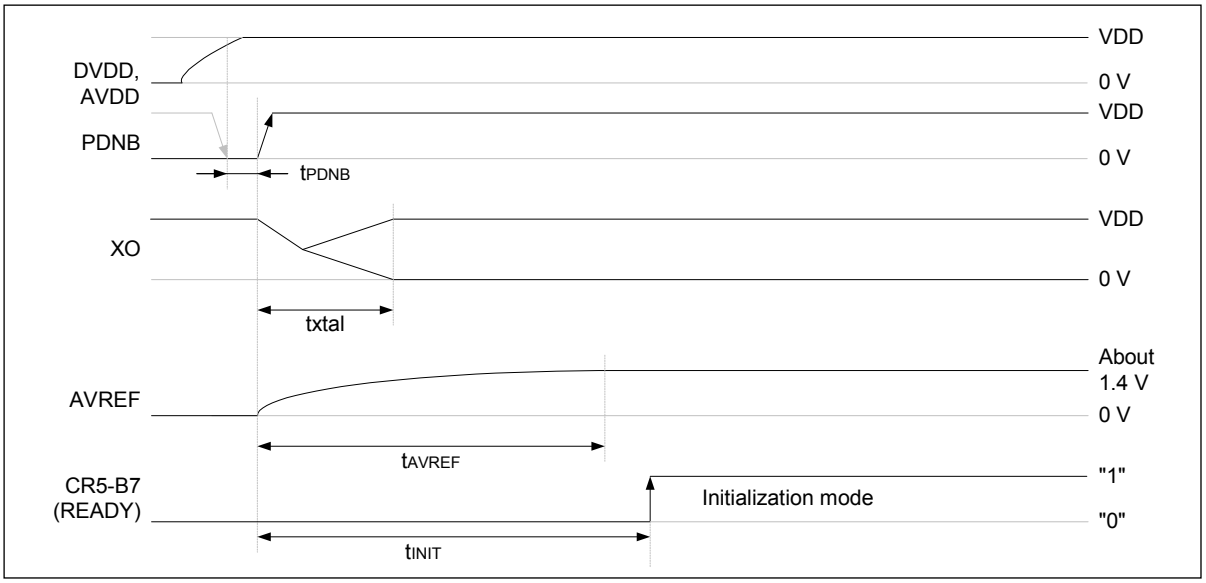


Fig. 1 PDNB, XO, and AVREF timings

PCM I/F Mode

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bit clock frequency	fBCLK	CDL = 20pF(at output)	−0.1%	64	+0.1%	kHz
Bit clock duty ratio	dBCLK	CDL = 20pF(at output)	45	50	55	%
Sync signal frequency	fSYNC	CDL = 20pF(at output)	−0.1%	8	+0.1%	kHz
Sync signal duty ratio	dSYNC1	CDL = 20pF(at output) At 64 kHz output	12.4	12.5	12.6	%
	dSYNC2	CDL = 20pF(at output) At 128 kHz output	6.24	6.25	6.26	%
Transmit/receive signal sync timing	tBS	BCLK to SYNC (at output)	100	—	—	ns
	tSB	SYNC to BCLK (at output)	100	—	—	ns
Input setup time	tDS	—	100	—	—	ns
Input hold time	tDH	—	100	—	—	ns
Digital output delay time	tSDX	PCMO pin Pull-up, pull-down resistors RDL = 1 kΩ, CDL = 50 pF	—	—	100	ns
	tXD1		—	—	100	ns
Digital output hold time	tXD2		—	—	100	ns
	tXD3		—	—	100	ns

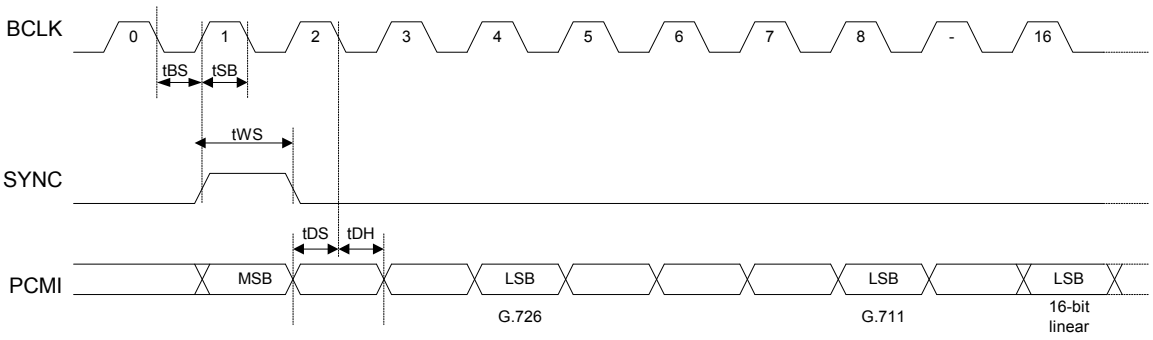


Fig. 2 PCM I/F mode input timing (long frame)

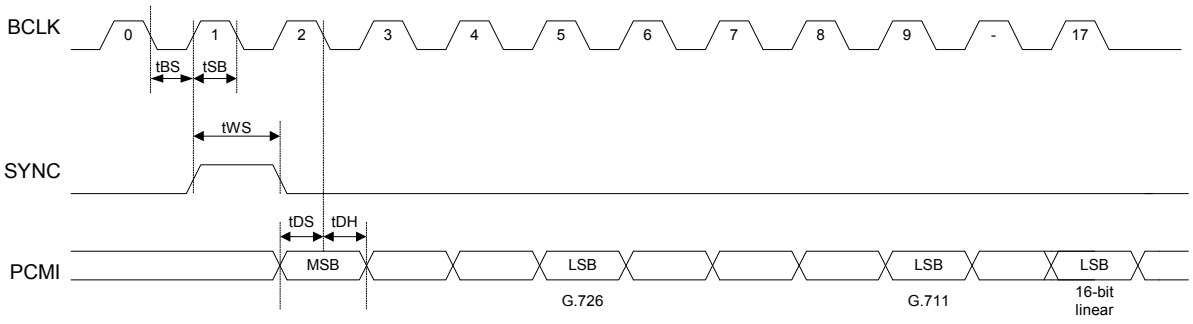


Fig. 3 PCM I/F mode input timing (short frame)

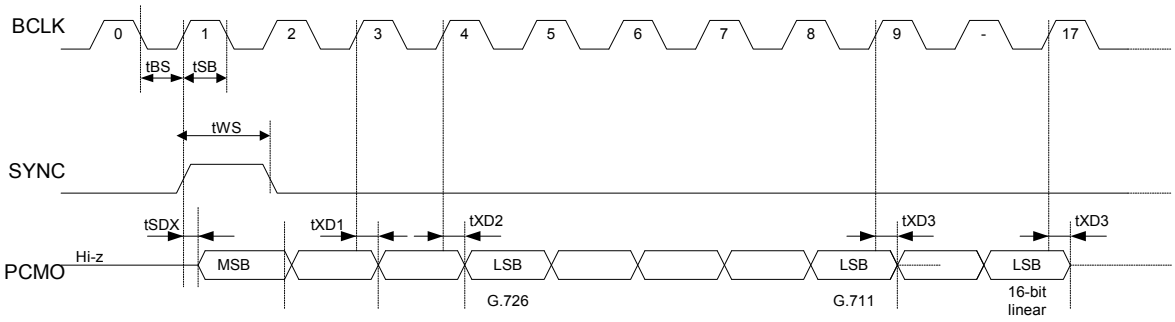


Fig. 4 PCM I/F mode output timing (long frame)

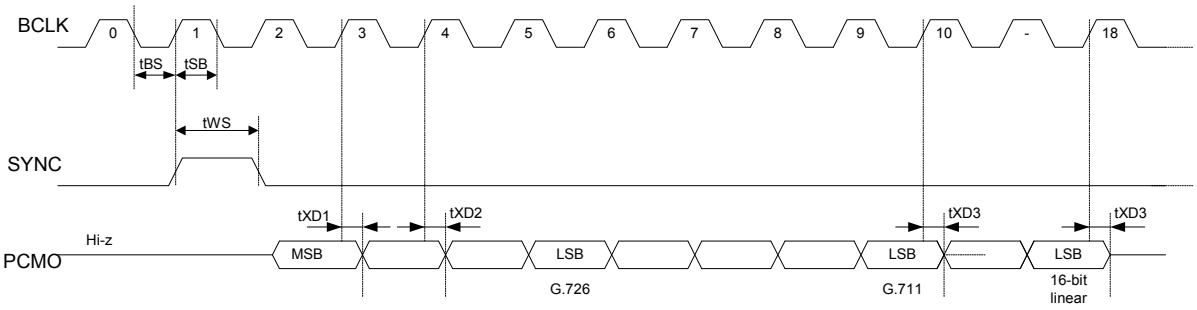


Fig. 5 PCM I/F mode output timing (short frame)

Control Register Interface

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address setup time	tAS	CL = 50 pF	10	—	—	ns
Address hold time	tAH		10	—	—	ns
Write data setup time	tWDS		10	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time	tCS		10	—	—	ns
CSB hold time	tCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
Read data output delay time	tRDD		—	—	20	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		25	—	—	ns
CSB disable time	tCD		10	—	—	ns

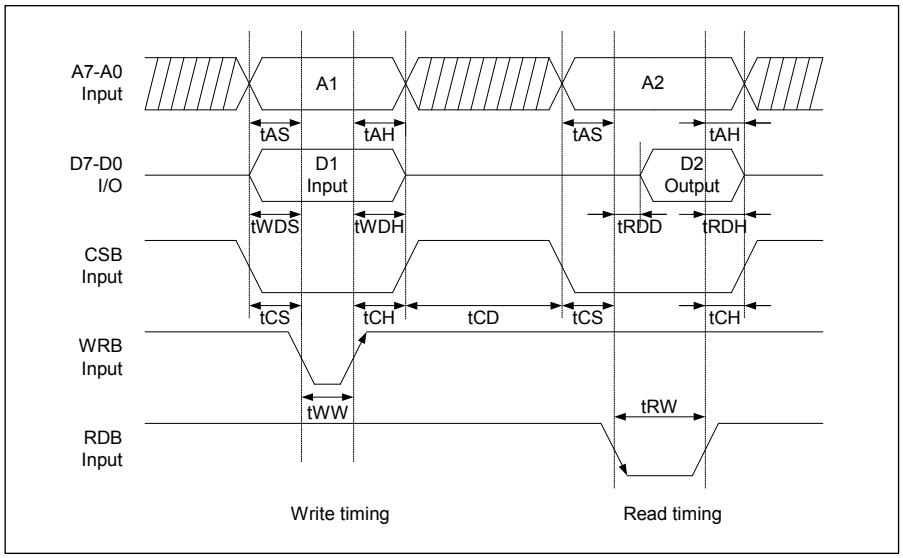


Fig. 6 Control register interface

Transmit and Receive Buffer Interface (in Frame Mode)

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
FR1B setup time	tF1S	CL = 50 pF	3	—	—	ns
FR1B output delay time	tF1D		—	—	20	ns
Address setup time	tAS		10	—	—	ns
Address hold time	tAH		10	—	—	ns
Write data setup time	tWDS		10	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time	tCS		10	—	—	ns
CSB hold time	tCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
FR0B setup time	tF0S		3	—	—	ns
FR0B output delay time	tF0D		—	—	20	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
CSB disable time	tCD		10	—	—	ns

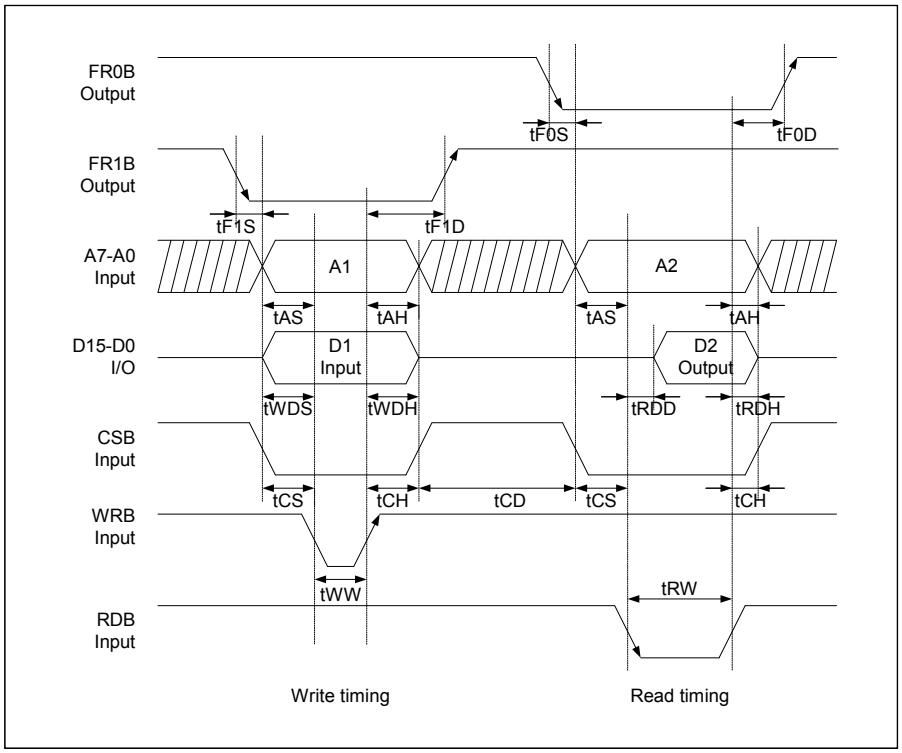


Fig. 7 Transmit and receive buffer interface (in frame mode)

Transmit and Receive Buffer Interface (in DMA Mode)

(Unless otherwise specified, AV_{DD} = 3.0 to 3.6 V, DV_{DD}0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = −20 to +60°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DMARQ1B setup time	tDR1S	CL = 50 pF	3	—	—	ns
DMARQ1B output delay time	tDR1RD		—	—	25	ns
	tDR1FD		—	—	25	ns
Address setup time	tAS		10	—	—	ns
Address hold time	tAH		10	—	—	ns
Write data setup time	tWDS		10	—	—	ns
Write data hold time	tWDH		10	—	—	ns
ACK setup time	tAKS		10	—	—	ns
ACK hold time	tAKH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
DMARQ0B setup time	tDR0S		3	—	—	ns
DMARQ0B output delay time	tDR0RD		—	—	20	ns
	tDR0FD		—	—	25	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
ACKB disable time	tAD		10	—	—	ns

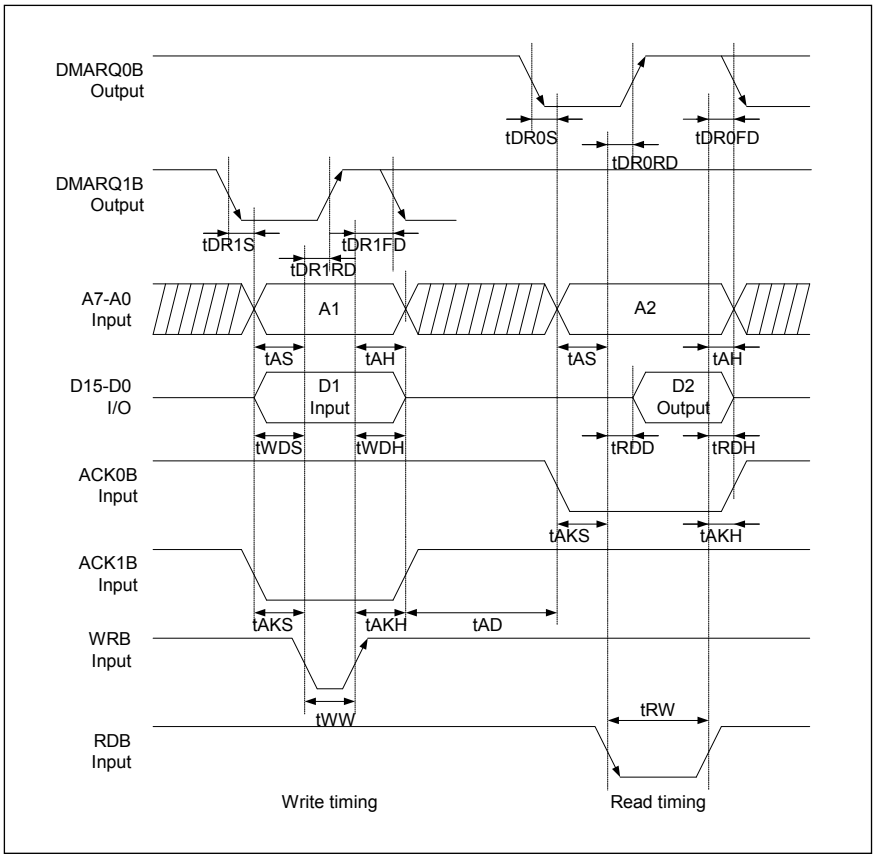


Fig. 8 Transmit and receive buffer interface (in DMA mode)

PIN FUNCTION DESCRIPTIONS

AIN0N, AIN0P, GSX0, AIN1N, GSX1

These are the analog transmit input and transmit level adjust pins. Each of AIN0N and AIN1N is connected to each of the inverting input pins of the built-in transmit amplifiers AMP0 and AMP1, and AIN0P is connected to the non-inverting input pin of AMP0. In addition, GSX0 and GSX1 are connected to the output pins of AMP0 and AMP1, respectively. The selection between AMP0 and AMP1 is made by CR10-B0. See Fig. 9 for the method of making level adjustment. During the power down mode (when PDNB = "0" or CR0-B7 = "1"), the outputs of GSX0 and GSX1 go to the high impedance state. If AMP0 is not used in the specific application of this LSI, short GSX0 with AIN0N and connect AIN0P with AVREF. When AMP1 is not used, short GSX1 with AIN1N.

Notice:
It is recommended to select the amplifier to be used before the conversation starts, since a small amount of noise will be generated if the amplifier selection is changed while conversation is in progress.

VFRO0, VFRO1

These are analog receive output pins and are connected to the output pins of the built-in receive amplifiers AMP2 and AMP3, respectively. The output signals of VFRO0 and VFRO1 can be selected using CR10-B1 and CR10-B2, respectively. When selected ("1"), the received signal will be output, and when deselected ("0"), the AVREF signal (about 1.4 V) will be output. In the power down mode, these pins will be in the high impedance state. It is recommended to use these output signals via DC coupling capacitors.

Notice:
It is recommended to select the amplifier to be used before the conversation starts, since a small amount of noise is generated if the output selection is changed while the conversation is in progress.
At the time of resetting or releasing from the reset state, it is recommended to select the AVREF as outputs of VFRO0 and VFRO1.

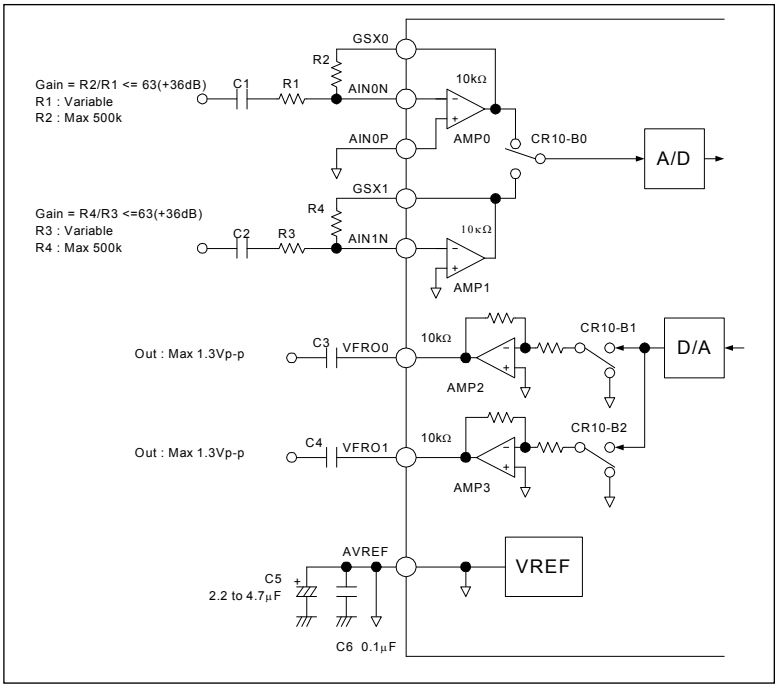
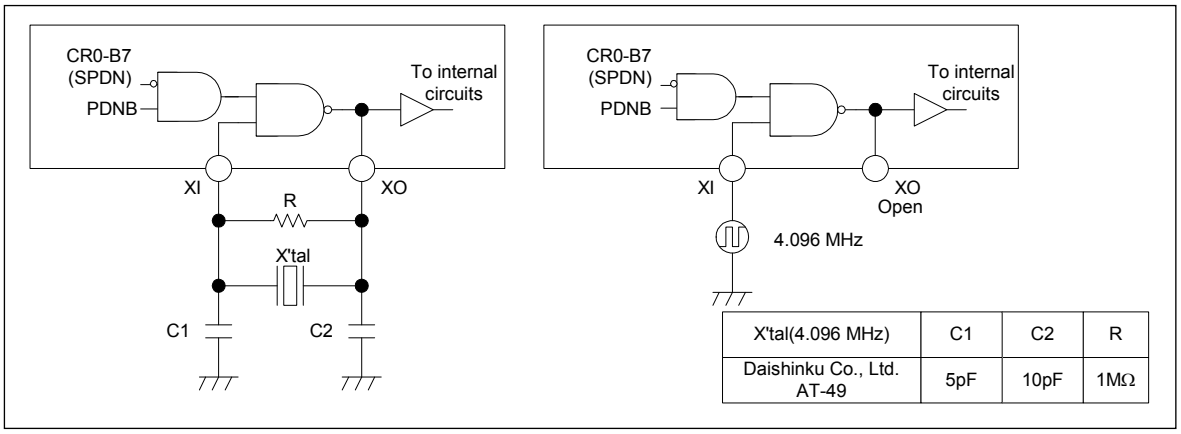


Fig. 9 Analog interface

AVREF
This is the output pin for the analog signal ground potential. The output potential at this pin will be about 1.4 V. Connect a 2.2 to 4.7 μF (aluminum electrolytic type) capacitor and a 0.1 μF (ceramic type) capacitor in parallel between this pin and the GND pin as bypass capacitors. The output at the AVREF pin goes to 0.0 V in the power down mode. The voltage starts rising after the power down mode is released (PDNB = "1" and also CR0-B7 = "0"). The rise time is about 0.6 sec.

XI, XO
These are the pins for either connecting the crystal oscillator for the master clock or for inputting an external master clock signal.
The oscillations of the master clock oscillator will be stopped during a power down due to the PDNB signal or during a software power down due to CR0-B7 (SPDN). The oscillations start when the power down condition is released, and the internal clock supply of the LSI will be started after counting up the oscillation stabilization period (of about 16 ms). Examples of crystal oscillator connection and external master clock input are shown in Fig. 10.



X'tal(4.096 MHz)	C1	C2	R
Daishinku Co., Ltd. AT-49	5pF	10pF	1MΩ

Fig. 10 Examples of oscillator circuit and clock input

PDNB
This is the power down control input pin. The power down mode is entered when this pin goes to "0". In addition, this pin also has the function of resetting the LSI. In order to prevent wrong operation of the LSI, carry out the initial power-down reset after switching on the power using this PDNB pin. Also, keep the PDNB pin at "0" level for 1 μs or more to initiate the power down state.
Further, it is possible to carry out a power down reset of the LSI when the power is being supplied by performing control of CR0-B7 (SPDN) in the sequence "0" → "1" → "0".
The READY signal (CR5-B7) goes to "1" about 1.0 second after the power down mode is released thereby entering the mode of setting various functions (initialization mode). See Fig. 1 for the timings of PDNB and AVREF, XO, and the initialization mode.

Notice: At the time of switching on the power, start from the power down mode using PDNB.

$DV_{DD}0$, $DV_{DD}1$, $DV_{DD}2$, AV_{DD}
These are power supply pins. $DV_{DD}0$, 1, 2 are the power supply pins for the digital circuits while AV_{DD} is the power supply pin for the analog circuits of the LSI. Connect these pins together in the neighborhood of the LSI and connect as bypass capacitors a 10 μF electrolytic capacitor and a 0.1 μF ceramic capacitor in parallel between the DGND and AGND pins.

DGND0, DGND1, DGND2, AGND
These are ground pins. GDND0, 1, 2 are the ground pins for the digital circuits and AGND is the ground pin for the analog circuits of the LSI. Connect these pins together in the neighborhood of the LSI.

TST0, TST1, TST2, TST3
These are input pins for testing purposes only. Keep the inputs to these pins at the "0" level during normal use conditions.

INTB
This is the interrupt request output pin. An "L" level is output for a duration of about 1.0 μsec at this pin when there is a change in state of an interrupt cause.
This output will be maintained at the "H" level when there is no change in state of any of the interrupt causes. The actual interrupt cause generating the interrupt can be verified by reading CR3 and CR4. The different interrupt causes are described below.

- Underflow error (CR3-B0)
  An interrupt is generated when an internal read from the receive buffer occurs before the writing into the receive buffer from the MCU has been completed.
  An interrupt is generated when a normal writing is made in the receive buffer by the MCU and the underflow error is released.

- Overrun error (CR3-B1)
  An interrupt is generated when an internal write of the next data into the transmit buffer occurs before the transmit buffer data read out from the MCU has been completed.
  An interrupt is generated when a normal read out is made from the transmit buffer by the MCU and the overrun error is released.

- When a dial pulse is detected (CR4-B6).

- When a DTMF signal is detected (CR4-B4).

- When DTMF_CODEC0, 1, 2, 3 are detected (CR4-B0, B1, B2, B3).
  An interrupt is generated when a DTMF signal is detected.
  An interrupt is generated when there is a change from the DTMF signal detected state to the no-detected state.
  An interrupt is generated when there is a change in the detected code (CR4-B0, B1, B2, B3) in the condition in which a DTMF signal is being detected.

- When TONE0 is detected (CR3-B3).
  An interrupt is generated when a 1650 Hz tone signal is detected.
  An interrupt is generated when there is a change to the non-detection condition in the tone signal detection condition.

- When TONE1 is detected (CR3-B4).
  An interrupt is generated when a 2100 Hz tone signal is detected.
  An interrupt is generated when there is a change to the non-detection condition in the tone signal detection condition.

- When FGEN_RQ is generated (CR3-B6).
  An interrupt is generated when the FSK generator makes a request for the next data to be transmitted.
  An interrupt is generated when there is a change from the condition in which the FSK generator is requesting for transmission data to the condition in which there is no request for internal fetch of the data to be transmitted next.

- When DSP_ERR is detected (CR3-B7).
  An interrupt is generated when any error occurs in the DSP inside the LSI.

A0 to A7
These are the address input pins for use during an access of the frame, DMA, or control registers. The different addresses will be the following.
Transmit buffer (TX Buffer)
A7 to A0 = 10xxxxxxb (the lower 6 bits are not valid)
Receive buffer (RX Buffer)
A7 to A0 = 01xxxxxxb (the lower 6 bits are not valid)
Control register (CR)
A7 to A0 = 00xxxxxxb

D0 to D15
These are the data input/output pins for use during an access of the frame, DMA, or control registers. Connect pull-up resistors to these pins since they are I/O pins. When the 8-bit bus access method is selected by CR11-B5, only D0 to D7 become valid. Since the higher 8 bits D8 to D15 will always be in the input state when the 8-bit bus access method is selected (CR11-B5 = "1"), tie them to "0" or "1" inputs.

CSB
This is the chip select input pin for use during a frame or control register access.

RDB
This is the read enable input pin for use during a frame, DMA, or control register access.

WRB
This is the write enable input pin for use during a frame, DMA, or control register access.

FR0B (DMARQ0B)

- FR0B (In frame mode, CR11-B7 = "0")
  This is the transmit frame output pin which outputs the signal when the transmit buffer is full during frame access. This pin outputs an "L" level when the transmit buffer becomes full, and maintains that "L" level output until a specific number of words are read out from the MCU.
- DMARQ0B (In DMA mode, CR11-B7 = "1")
  This is the DMA request output pin which outputs the signal when the transmit buffer is full during DMA access. This output becomes "L" when the transmit buffer becomes full, and returns to the "H" level automatically on the falling edge of the read enable signal (RDB = "1" → "0") when there is an acknowledgement signal (ACK0B = "0") from the MCU. This relationship is repeated until a specific number of words are read out from the MCU.

FR1B (DMARQ1B)

- FR1B (In frame mode, CR11-B7 = "0")
  This is the receive frame output pin which outputs the signal when the receive buffer is empty during frame access. This pin outputs an "L" level when the receive buffer becomes empty, and maintains that "L" level output until a specific number of words are written from the MCU.
- DMARQ1B (In DMA mode, CR11-B7 = "1")
  This is the DMA request output pin which outputs the signal when the receive buffer is empty during DMA access. This output becomes "L" when the receive buffer becomes empty, and returns to the "H" level automatically on the falling edge of the write enable signal (WRB = "1" → "0") when there is an acknowledgement signal (ACK1B = "0") from the MCU. This relationship is repeated until a specific number of words are written from the MCU.

ACK0B

This is the DMA acknowledgement input pin for the DMARQ0B signal during DMA access of the transmit buffer and becomes valid in the DMA mode (CR11-B7 = "1").
Tie this pin to "1" when using this LSI in the frame access mode (CR11-B7 = "0").

ACK1B

This is the DMA acknowledgement input pin for the DMARQ1B signal during DMA access of the receive buffer and becomes valid in the DMA mode (CR11-B7 = "1").
Tie this pin to "1" when using this LSI in the frame access mode (CR11-B7 = "0").

GPI0, GPI1

These are general-purpose input pins. The state ("1" or "0") of each of these GPI0 and GPI1 pins can be read out respectively from CR16-B0 and CR16-B1. Further, GPI0 becomes the input pin for the dial pulse detector (DPDET) in the secondary functions.

GPO0, GPO1

These are general-purpose output pins. The values set in CR17-B0 and CR17-B1 are output at these pins GPO0 and GPO1, respectively. Further, GPO0 becomes the output pin for the dial pulse generator (DPGEN) in the secondary functions.

CLKSEL
This is the input/output control input pin of SYNC and BCLK. The pin becomes input at "0" level and output at "1" level.

SYNC
This is the 8 kHz sync signal input/output pin of PCM signals. When CLKSEL is "0", input continuously an 8 kHz clock synchronous with BCLK. Further, when CLKSEL is "1", this pin outputs an 8 kHz clock synchronous with BCLK. Long frame synchronization is used when CR0-B1 (LONG/SHORT) is "0" and short frame synchronization is used when it is "1".

BCLK
This is the shift clock input/output pin for the PCM signal. When CLKSEL is "0", it is necessary to input to this pin a clock signal that is synchronous with SYNC. Input a 64 to 2048 kHz clock when the G.711 mode or the G.726 mode has been selected, and input a 128 to 2048 kHz clock when the 16-bit linear mode has been selected. When CLKSEL is "1", this pin outputs a clock that is synchronous with SYNC. This pin outputs a 64 kHz clock when the G.711 mode or the G.726 mode has been selected, and outputs an 128 kHz clock when the 16-bit linear mode or G.729.A mode has been selected.

Note: The input/output control and frequencies of the above SYNC and BLCK signals will be as shown in Table 1 below.

Table 1 Input/output control of SYNC and BCLK

CLKSEL	SYNC	BCLK	Remarks
"0"	Input (8 kHz)	Input (64 kHz to 2048 kHz)	Input a continuous clock after starting the power supply. Input a 64 to 2048 kHz clock when G.711 or G.726 is selected. Input a 128 to 2048 kHz clock when 16-bit linear mode is selected.
"1"	Output (8 kHz)	Output (64 kHz or 128 kHz)	An "L" level is output during the power down mode. A 64 kHz clock is output when G.711 or G.726 is selected. A 128 kHz clock is output when G.729.A or 16-bit linear mode is selected.

PCMO
This is the PCM signal output pin for the transmitting section. The PCM signal is output in synchronization with the rising edges of SYNC and BCLK. The PCMO outputs the data only during the valid data segment in the selected coding format and goes to the high impedance state during all other segments. The basic timing chart of the PCM I/F mode is shown in Fig. 11. The PCMO output will be in the high impedance state when the mutual conversion function is not used (CR11-B0 = "0") or when the PCM I/F mode is not used (CR12-B0 = "0").

PCMI
This is the PCM signal input pin for the receiving section. The data is entered starting from the MSB by shift on the falling edge of BCLK.
The basic timing chart of the PCM I/F mode is shown in Fig. 11.
Fix input with "0" or "1" when the mutual conversion function is not used (CR11-B0 = "0") or when the PCM I/F mode (CR12-B0 = "0") is not used.

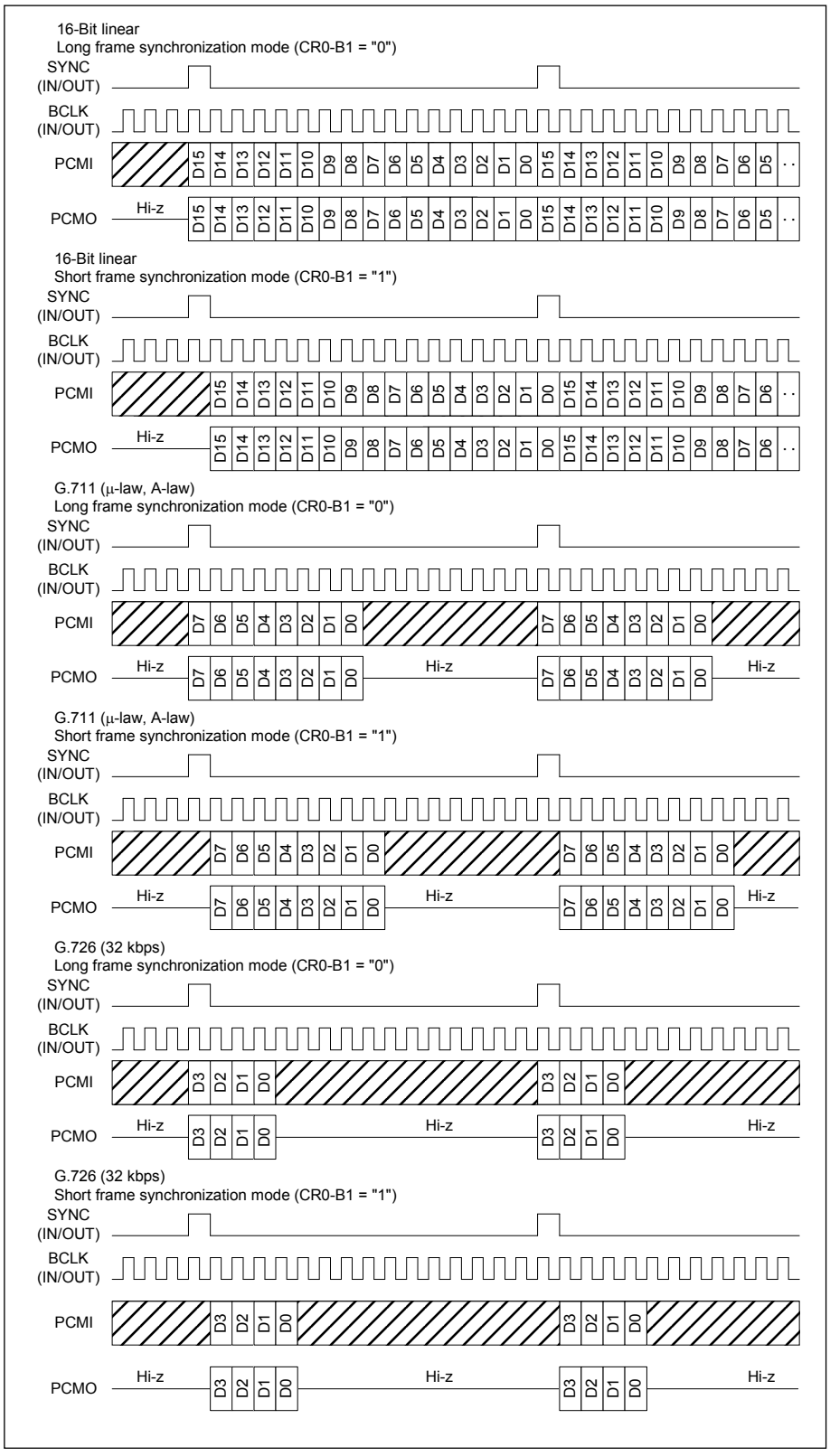


Fig. 11 PCM I/F mode timing diagram

FUNCTION DESCRIPTION

On the Transmit and Receive Buffers

The controllable parameters of the transmit and receive buffers are shown in Table 2 below.

Table 2 Controllable parameters of transmit and receive buffers

Content	Changeable parameter	Initial value	Remarks
Speech CODEC	G.729.A/G.726(32kbps) /G.711(μ-law, A-law)	G.729.A	The buffering size of the FIFO is changed automatically depending on the speech CODEC type.
Buffering time	10 ms/20 ms	10 ms	The number of words is changed automatically depending on the buffering time.
Accessing method	Frame or DMA	Frame	—
FIFO data width	16-bit/8-bit	16-bit	The number of words is changed automatically depending on the data width.

Transmit and Receive Buffer Sizes

The transmit and receive buffers have a double buffer configuration of the FIFO (First In First Out) type, and one buffer can buffer data of 10 msec or 20 msec.

The timing of generation of the frame signals (FR0B, FR1B) requested to the MCU when the transmit buffer is full or the receive buffer is empty, and the timing of generation of the DMA request signals (DMARQ0B, DMARQ1B) depend on the buffering time. Further, the number of words of FIFO is changed automatically depending on the selected speech CODEC type and the FIFO data width. The buffer size and the number of words for the different speech CODEC types and data widths are shown in Table 3.

Table 3 Buffer size and number of words of transmit and receive buffers

Speech CODEC	10 ms mode			20 ms mode		
	Buffer size	16-bit	8-bit	Buffer size	16-bit	8-bit
G.729.A (8 kbps)	10 bytes	5 words	10 words	20 bytes	10 words	20 words
G.726 (32 kbps)	40 bytes	20 words	40 words	80 bytes	40 words	80 words
G.711 (64 kbps)	80 bytes	40 words	80 words	160 bytes	80 words	160 words

Transmit and Receive Buffers Configuration

The timings of accessing the transmit and receive buffers are shown in Fig. 12. Although both transmit and receive buffers have a double buffer configuration, they can be accessed as a single buffer from the MCU.

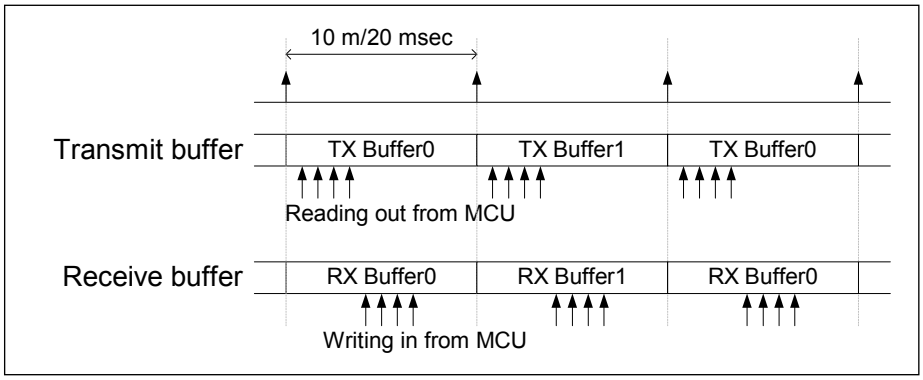


Fig. 12 Timings of accessing the transmit and receive buffers

Data Width Selection (16-Bit Mode, 8-Bit Mode)

In the method of accessing the transmit and receive buffers, it is possible to select data width of 16 bits or 8 bits using the control register bit CR11-B5.

During the 16-bit mode, the access is made with a data width of 16 bits and the data bits D15 to D0 are accessed. In the 8-bit mode, the transmit and receive data are input or output to D7 to D0. During the 8-bit access mode, the bits D15 to D8 will always be in the input state.

Data Storage Format

The data storage formats during transmission and reception depending on the settings of the different parameters are shown in Fig. 13, Fig. 14, and Fig. 15.

A. G.729.A

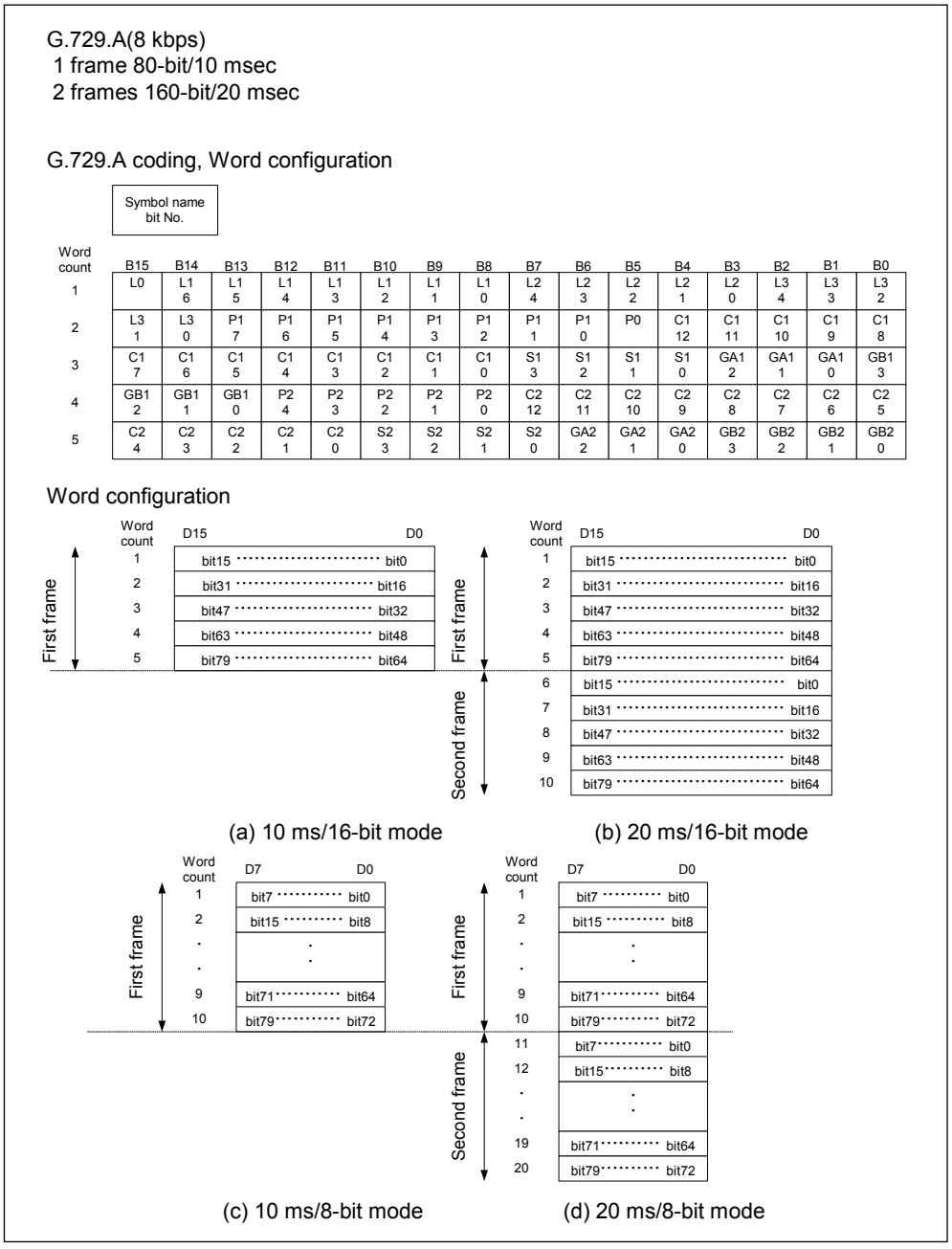


Fig. 13 G.729.A data format

B. G.726 (32 kbps)

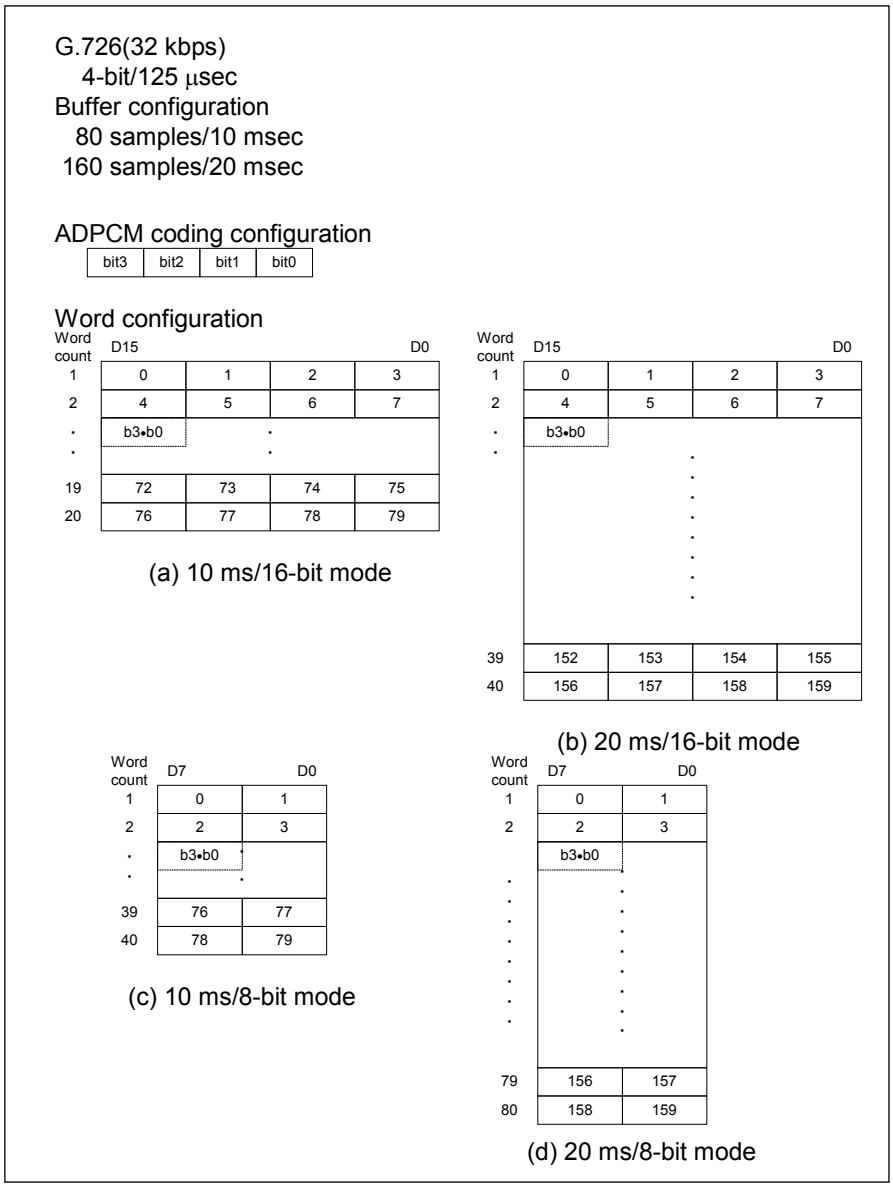


Fig. 14 G.726 (32 kbps) data format

C. G.711 (64 kbps)

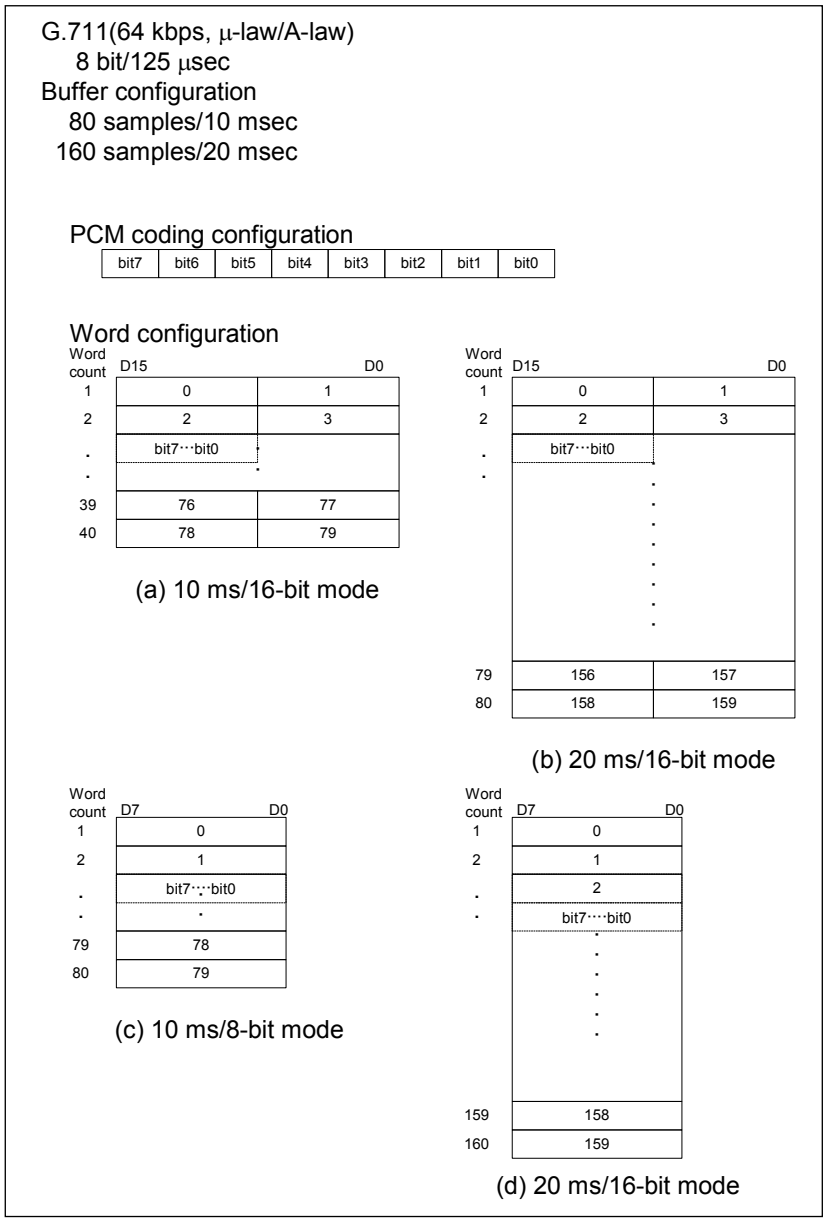
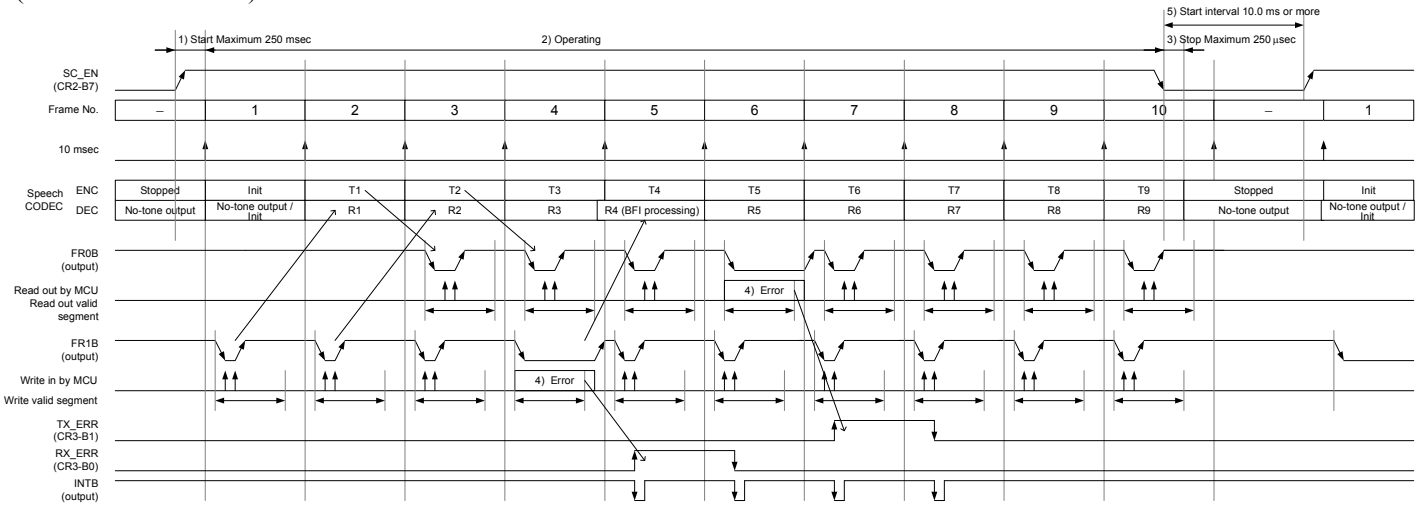


Fig. 15 G.711 data format

Transmit and Receive Buffer Control Method

The methods of controlling the transmit and receive buffers depending on the different parameters are shown in Figs. 16 to 19.

A. G.729.A (10 msec/frame mode)



1) Start SC_EN "0" → "1"

The speech CODEC starts within about 250 µsec after SC_EN has been set to "1". During the first 10 ms (Frame No. 1), initialization and no-tone data output are made, and encoding and decoding are started from Frame No. 2. Request for received data is made after the speech CODEC has been started.

2) Operating

The data written at Frame No. 1 is decoded (R1) at the next Frame No. 2. This operation is repeated until stopping.
The data encoded (T1) at Frame No. 2 is read out at the next Frame No. 3. This operation is repeated until stopping.

3) Stop SC_EN "1" → "0"

The data of the frame (Frame No. 10) in which the stop is set becomes invalid.
Within a maximum of 250 µsec after SC_EN has been set to "0", the encoder stops writing the data, and no-tone data is output after the encoder has stopped.

4) Error processing

Receive error:
Frame No. 4 is an example of receive error occurrence.
When the writing of data does not get completed within the write valid segment, RX_ERR becomes "1" and an interrupt is generated.
The state of RX_ERR will be maintained during and after the next frame until the end of a frame in which the receive buffer has been written normally.
When an error has occurred in Frame No. 4, the decoding processing in Frame No. 5 is carried out according to the frame loss compensation processing (BFI: Bad Frame Indicator) stipulated in the G.729.A standard.

Transmit error:
Frame No. 6 is an example of transmit error occurrence.
When the reading of data does not get completed within the read valid segment, TX_ERR becomes "1" and an interrupt is generated.
The state of TX_ERR is maintained during and after the next frame until the end of a frame in which the transmit buffer has been read normally.
Even when the data read out does not end, the data in the transmit buffer will continue to be updated normally.

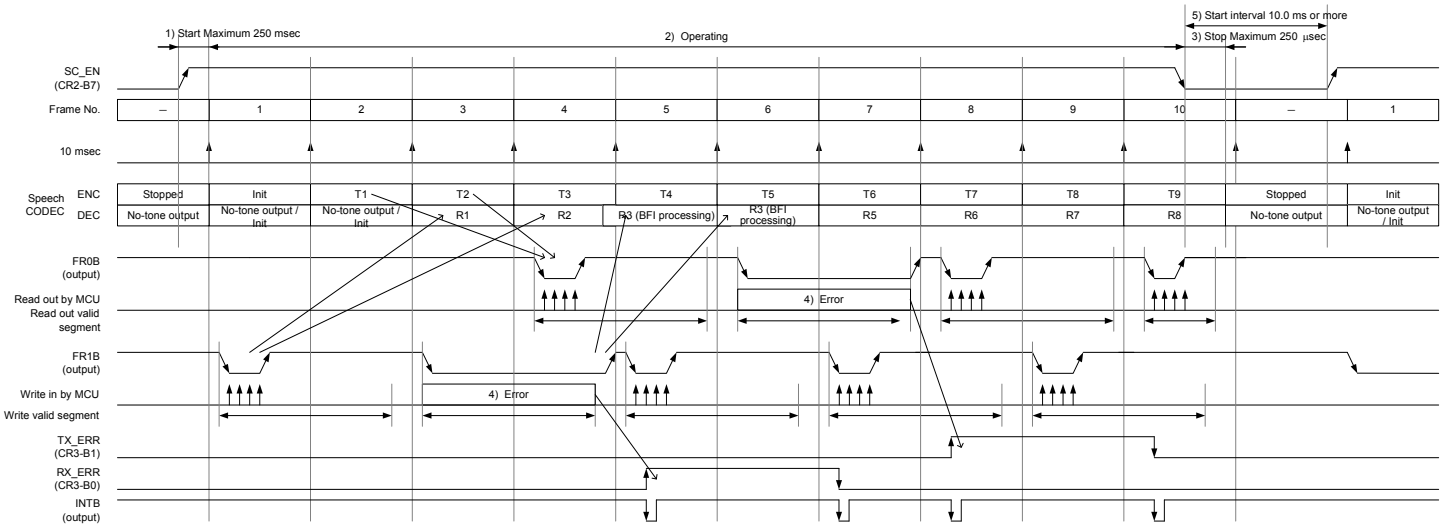
5) Start interval

An interval of 10.0 msec or more is necessary after the speech CODEC has stopped before it is started again. During this interval, it is possible to change the speech CODEC.

Write valid segment: Complete the writing of data to the RX buffer within 9.0 msec from the falling edge of FR1B.
Read valid segment: Complete the data read out from the TX buffer within 9.0 msec from the falling edge of FR0B.

Fig. 16 G.729.A control timing (10 msec/frame mode)

B. G.729.A (20 msec/frame mode)



1) Start SC_EN "0" → "1"
The speech CODEC starts within about 250 µsec after SC_EN has been set to "1". The encoder carries out initialization during the first 10 msec (Frame No. 1), and starts encoding from Frame No. 2.
The decoder carries out initialization during the first 20 msec (Frame No. 1 and Frame No.2), outputs no-tone data, and starts decoding from Frame No. 3. Request for received data is made after the speech CODEC has been started.

2) Operating
The data written at frames No. 1 and No. 2 is decoded (R1, R2) at the subsequent frames No. 3 and No. 4. This operation is repeated until stopping.
The data encoded (T1, T2) at frames No. 2 and No. 3 is read out at the subsequent frames No. 4 and No.5. This operation is repeated until stopping.

3) Stop SC_EN "1" → "0"
The data of the frame (Frame No. 10) in which the stop is set becomes invalid.
Within about 250 µsec after SC_EN has been set to "0", the encoder stops writing the data, and after the decoder has stopped, no-tone data is output.

4) Error processing
Receive error:
Frames No. 3 and No. 4 are examples of receive error occurrence.
When the writing of data does not get completed within the write valid segment, RX_ERR becomes "1" and an interrupt is generated.
The state of RX_ERR will be maintained during and after the next frame until the end of a frame in which the receive buffer has been written normally.
When an error has occurred in frames No. 3 and No. 4, the decoding processing in frames No. 5 and No. 6 is carried out according to the frame loss compensation processing (BFI:Bad Frame Indicator) stipulated in the G.729.A standard.

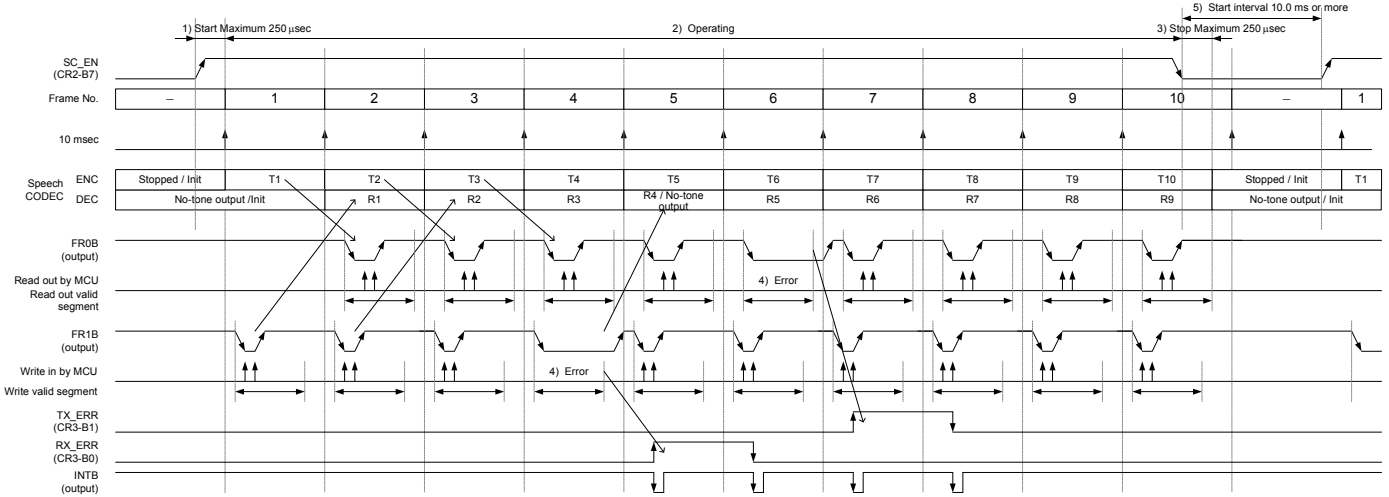
Transmit error:
Frames No. 6 and No. 7 are examples of transmit error occurrence.
When the reading of data does not get completed within the read valid segment, TX_ERR becomes "1" and an interrupt is generated.
The state of TX_ERR is maintained during and after the next frame until the end of a frame in which the transmit buffer has been read normally.
Even when the data read out does not end, the data in the transmit buffer will continue to be updated normally.

5) Start interval
An interval of 10.0 msec or more is necessary after the speech CODEC has stopped before it is started again. During this interval, it is possible to change the speech CODEC.

Write valid segment: Complete the writing of data to the RX buffer within 18.0 msec from the falling edge of FR1B.
Read valid segment: Complete the data read out from the TX buffer within 18.0 msec from the falling edge of FR0B.

Fig. 17 G.729.A control timing (20 msec/frame mode)

C. G.711 (μ-law, A-law), G.726 (10 msec/frame mode)



1) Start SC_EN "0" → "1"
The speech CODEC starts within about 250 μsec after SC_EN has been set to "1". The encoder starts in the already initialized condition and starts encoding from Frame No. 1.
The decoder carries out initialization during the first 10 msec (Frame No. 1), outputs no-tone data, and starts decoding from Frame No. 2. Request for received data is made after the speech CODEC has been started.

2) Operating
The data written at Frame No. 1 is decoded (R1) at the next Frame No. 2. This operation is repeated until stopping.
The data encoded (T1) at Frame No. 1 is read out at the next Frame No. 2. This operation is repeated until stopping.

3) Stop SC_EN "1" → "0"
The data of the frame (Frame No. 10) in which the stop is set becomes invalid.
Within about 250 μsec after SC_EN has been set to "0", the encoder stops writing the data, and no-tone data is output after the decoder has stopped.

4) Error processing
Receive error:
Frame No. 4 is an example of receive error occurrence.
When the writing of data does not get completed within the write valid segment, RX_ERR becomes "1" and an interrupt is generated.
The state of RX_ERR will be maintained during and after the next frame until the end of a frame in which the reception buffer has been written normally.
When an error has occurred in Frame No. 4, the decoding processing in Frame No. 5 is not carried out and no-tone data is output. In addition, the decoder of G.726 willalso be initialized at the same time.

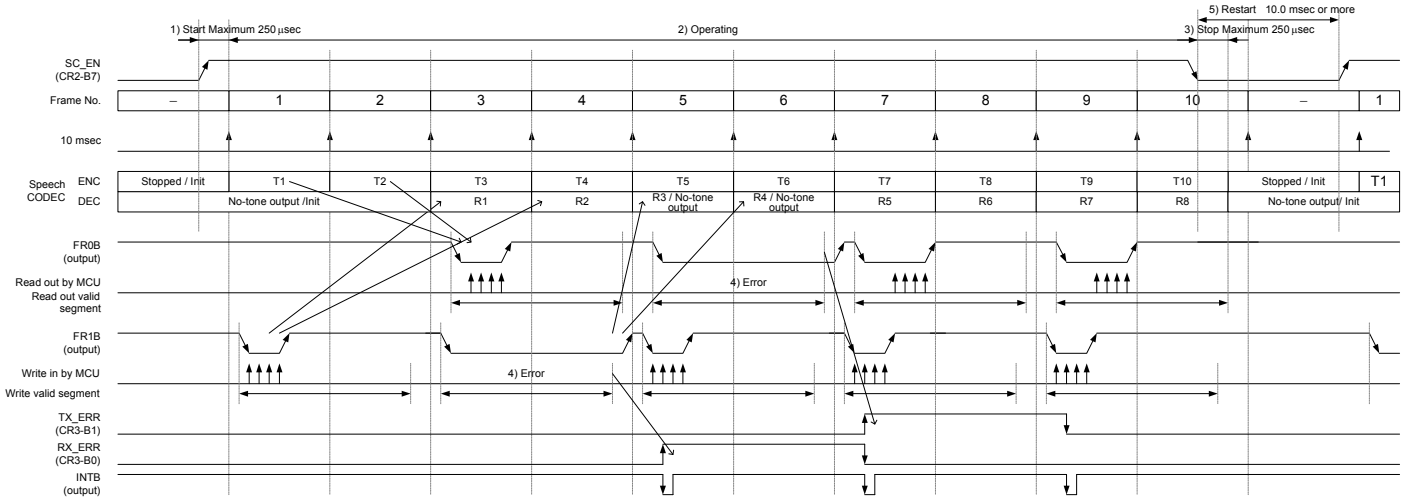
Transmit error:
Frame No. 6 is an example of transmit error occurrence. When the reading of data does not get completed within the read valid segment, TX_ERR becomes "1" and an interrupt is generated.
The state of TX_ERR is maintained during and after the next frame until the end of a frame in which the transmit buffer has been read normally.
Even when the data read out does not end, the data in the transmit buffer will continue to be updated normally.

5) Start interval
An interval of 10.0 msec or more is necessary after the speech CODEC has stopped before it is started again. During this interval, it is possible to change the speech CODEC.

Write valid segment: Complete the writing of data to the RX buffer within 9.0 msec from the falling edge of FR1B.
Read valid segment: Complete the data read out from the TX buffer within 9.0 msec from the falling edge of FR0B.

Fig. 18 G.711 (μ-law, A-law) and G.726 control timing (10 msec/frame mode)

D. G.711 (μ-law, A-law), G.726 (10 msec/frame mode)



1) Start SC_EN "0" → "1"
The speech CODEC starts within about 250 μsec after SC_EN has been set to "1". The encoder starts in the already initialized condition and starts encoding (T1) from Frame No. 1.
The decoder carries out initialization during the first 10 msec (Frame No. 1), outputs no-tone data, and starts decoding (R1) from Frame No. 2. Request for received data is made after the speech CODEC has been started.

2) Operating
The data written at Frame No. 1 and Frame No. 2 is decoded (R1, R2) at the next frames No. 3 and No. 4. This operation is repeated until stopping.
The data encoded (T1, T2) at the Frames No. 1 and No. 2 is read out at the Frames No. 3 and No. 4. This operation is repeated until stopping.

3) Stop SC_EN "1" → "0"
The data of the frame (Frame No. 10) in which the stop is set becomes invalid.
Within about 250 μsec after SC_EN has been set to "0", the encoder stops writing the data, and no-tone data is output after the decoder has stopped.

4) Error processing
Receive error:
Frame No. 3 and Frame No. 4 are examples of receive error occurrence.
When the writing of data does not get completed within the write valid segment, RX_ERR becomes "1" and an interrupt is generated.
The state of RX_ERR will be maintained during and after the next frame until the end of a frame in which the receive buffer has been written normally.
When an error has occurred in Frame No. 3 and Frame No. 4, no decoding processing will be done in Frame No. 5 and Frame No. 6 but no-tone data is output.
In addition, the decoder of G.726 will also be initialized at the same time.

Transmit error:
Frame No. 5 and Frame No. 6 are examples of transmit error occurrence.
When the reading of data does not get completed within the read valid segment, TX_ERR becomes "1" and an interrupt is generated.
The state of TX_ERR is maintained during and after the next frame until the end of a frame in which the transmit buffer has been read normally.
Even when the data read out does not end, the data in the transmit buffer will continue to be updated normally.

5) Start interval
An interval of 10.0 msec or more is necessary after the speech CODEC has stopped before it is started again. During this interval, it is possible to change the speech CODEC.

Write valid segment: Complete the writing of data to the RX buffer within 18.0 msec from the falling edge of FR1B.
Read valid segment: Complete the data read out from the TX buffer within 18.0 msec from the falling edge of FR0B

Fig. 19 G.711 (μ-law, A-law) and G.726 control timing (20 msec/frame mode)

Method of Controlling Control Registers

The method of controlling the control registers is shown in Fig. 20.

This LSI contains 20 control registers CR0 to CR20 for carrying out various controls. Further, the control bit (CR1-B7) assigned within such a control register, the address (CR6, CR7), and the data (CR8, CR9) are used to modify and control the data memory inside the DSP in this LSI.

See the section on "Method of Accessing and Controlling the Internal Data Memory" for details on how to access the data memory inside the DSP of this LSI.

The higher two bits of the address of a control register will be "0". Irrespective of the 16-bit or 8-bit data width selected in CR11-B5 (16b/8b), all control operations of control registers are made with an 8-bit data width using only data bits D7 to D0. When the data bus is being accessed in the 16-bit access mode, data bits D15 to D8 are configured as inputs while the data is written to the control register, and are configured as outputs while the data is read from the control register. When a control register write is being made, "1" or "0" is input to D15 to D8, and "1" is read out during a control register read.

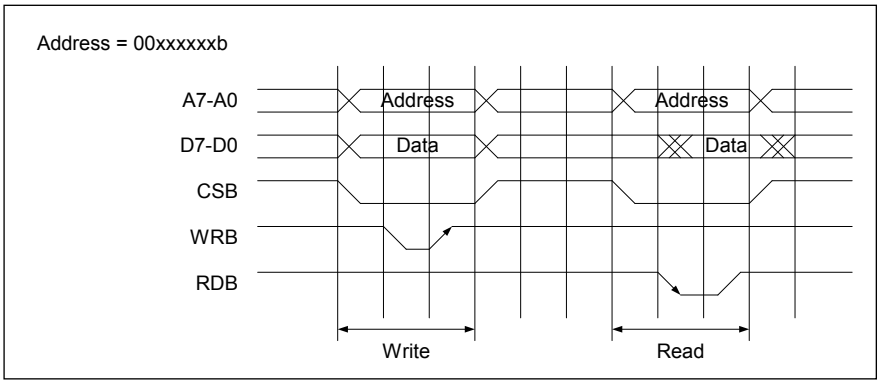


Fig. 20 Method of controlling the control registers

Method of Accessing Transmit and Receive Buffers

A. In the Frame Mode (CR11-B7 = "0")

The control timing and the method of accessing the transmit buffer (TX Buffer) during the frame mode are shown in Fig. 21. When the transmit buffer, which stores the compressed speech data of the transmit side (the speech compressing side), becomes full, a read request is made to the MPU by taking FR0B from the "H" state to the "L" state. Read the data in the transmit buffer during the following timing. The read address of the transmit buffer during the following timing. The read address of the transmit buffer is "10xxxxxxb" in which the lower 6 bits are ignored. Further, FR0B will be maintained in the "L" state until all the data bytes in the transmit buffer are read out.

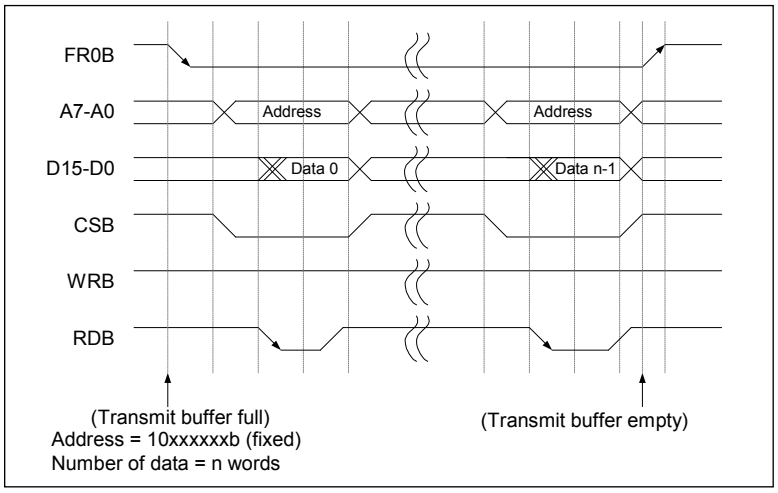


Fig. 21 Transmit buffer control timing

The control timing of the receive buffer (RX buffer) in the frame mode is shown in Fig. 22. A write request is made to the MPU by taking FR1B from the "H" state to the "L" state indicating that the receive buffer for storing the speech compression data of the receive side (the speech decompression side) has become empty. Write data into the receive buffer at the following timing. The write address of the receive buffer is "01xxxxxxb" in which the lower 6 bits are ignored. Further, FR1B will be maintained in the "L" state until the receive buffer is written to become full.

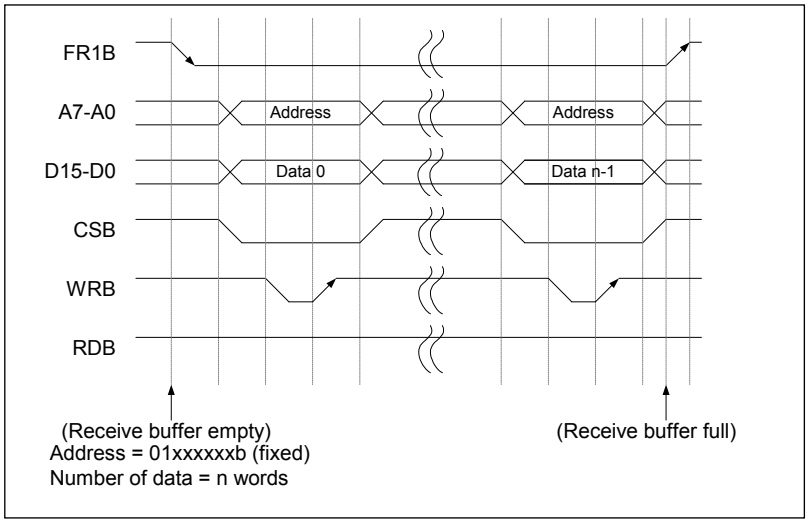


Fig. 22 Receive buffer control timing

B. In the DMA mode (CR11-B7 = "1")

The control timing of the transmit buffer in the DMA mode is shown in Fig. 23. A DMA request is made to the MPU by taking DMARQ0B from the "H" state to the "L" state when the transmit buffer storing the compressed speech data of the transmit side (the speech compressing side) becomes full. After the DMA request is made, an acknowledgement is input by changing the acknowledgement signal DMAACK0B to "0" from "1", and also, this DMARQ0B will be cleared automatically ("L" → "H") when a falling edge of the read enable signal is accepted (RDB = "1" → "0"). Read the data in the transmit buffer at the following timing simultaneously with the acknowledgement input. DMARQ0B repeats the DMA request until all the data in the transmit buffer has been read out.

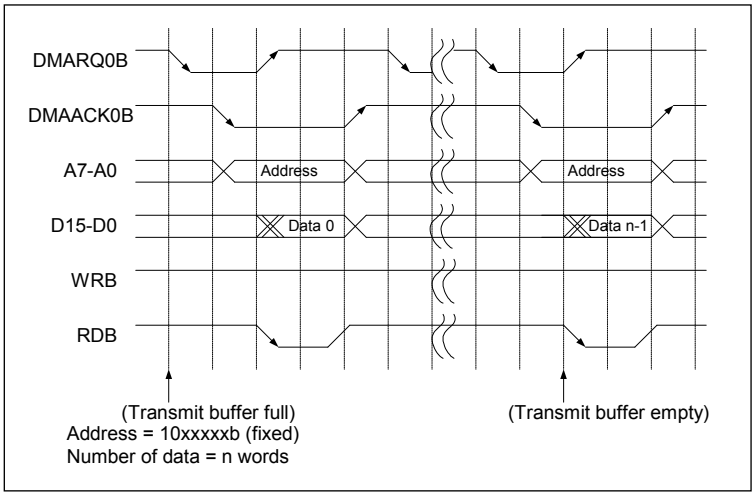


Fig. 23 Transmit buffer control timing in the DMA mode

The control timing of the receive buffer during the DMA transfer mode is shown in Fig. 24. A DMA transfer request is made to the MPU by taking DMARQ1B from the "H" state to the "L" state when the receive buffer for storing the speech compression data of the receive side (the speech decompression side) has become empty. After the DMA transfer request is made, an acknowledgement is input by changing the acknowledgement signal DMAACK1B from "1" to "0", and also, this acknowledgement signal DMAACK1B will be cleared automatically ("L" → "H") when a falling edge of the read enable signal is accepted (RDB = "1" → "0"). Write data into the receive buffer at the following timing simultaneously with the acknowledgement input. DMARQ1B repeats the DMA transfer request until data has been written into the receive buffer to make it full.

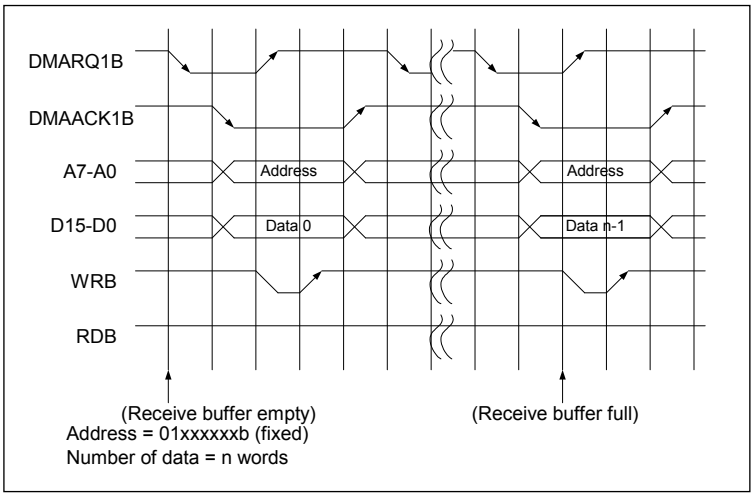


Fig. 24 Receive buffer control timing in the DMA mode

Control Registers

Table 4 shows a map of the control registers. CR6 to CR9 are used for accessing the data memory inside the DSP. In addition, the changeable mode of operation is shown below the name of the register assigned to each bit.

Table 4 Map of control registers

Reg Name	Address	Contents								R/W
	A7 to A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	00h	SPDN	#	AFE_EN	#	#	#	LONG/ SHORT	OPE _STAT	R/W
		/E	—	I/	—	—	—	I/	I/	
CR1	01h	XDMWR	XDMRD	#	#	#	#	#	#	R/W
		I/E	I/E	—	—	—	—	—	—	
CR2	02h	SC_EN	FGEN _EN	#	TDET1 _EN	TDET0 _EN	DTMF _EN	EC_EN	#	R/W
		I/E	I/E	—	I/E	I/E	I/E	I/E	—	
CR3	03h	DSP _ERR	FGEN _RQ	#	TONE1 _DET	TONE0 _DET	#	TX _ERR	RX _ERR	R/
		—	—	—	—	—	—	—	—	
CR4	04h	INT	DP_DET	#	DTMF _DET	DTMF_ CODE3	DTMF_ CODE2	DTMF_ CODE1	DTMF_ CODE0	R/
		—	—	—	—	—	—	—	—	
CR5	05h	READY	#	#	#	#	#	#	#	R/
		—	—	—	—	—	—	—	—	
CR6	06h	Internal data memory access (higher address)								/W
		A15	A14	A13	A12	A11	A10	A9	A8	
		I/E								
CR7	07h	Internal data memory access (lower address)								/W
		A7	A6	A5	A4	A3	A2	A1	A0	
		I/E								
CR8	08h	Internal data memory access (higher data))								R/W
		D15	D14	D13	D12	D11	D10	D9	D8	
		I/E								
CR9	09h	Internal data memory access (lower data))								R/W
		D7	D6	D5	D4	D3	D2	D1	D0	
		I/E								
CR10	0Ah	#	DPDET _EN	#	TDET1 _SEL	TDET0 _SEL	VFRO1 _SEL	VFRO0 _SEL	AIN _SEL	R/W
		—	I/E	—	I/	I/	I/E	I/E	I/E	
CR11	0Bh	FRAME/ DMA	10ms /20ms	16B /8B	#	#	SC _SEL1	SC _SEL0	TRANS _EN	R/W
		I/	I/	I/	—	—	I/E	I/E	I/	

CR12	0Ch	#	#	#	#	#	PSC _SEL1	PSC _SEL0	PCMIF _EN	/W
		—	—	—	—	—	I/E	I/E	I/	
CR13	0Dh	$	$	$	$	$	$	$	$	/
CR14	0Eh	$	$	$	$	$	$	$	$	/
CR15	0Fh	TA	TA	TA	$	$	$	$	$	R/W
		I	I	I	—	—	—	—	—	
CR16	10h	#	#	#	#	#	#	GPI1	GPI0	R/
		—	—	—	—	—	—	—	—	
CR17	11h	#	#	#	#	#	#	GPO1	GPO0	R/W
		—	—	—	—	—	—	I/E	I/E	
CR18	12h	FSK _D7	FSK _D6	FSK _D5	FSK _D4	FSK _D3	FSK _D2	FSK _D1	FSK _D0	R/W
		I/E								
CR19	13h	#	#	#	#	#	#	FSK _D9	FSK _D8	R/W
		—						I/E		
CR20	14h	TGEN _RX	TGEN _TX	TGEN _CNT5	TGEN _CNT4	TGEN _CNT3	TGEN _CNT2	TGEN _CNT1	TGEN _CNT0	R/W
		I/E								
—	15h-3Fh	$	$	$	$	$	$	$	$	/

Notes:
Register names
#: Reserved bit. Do not change the initial value of “0”.
$: Access-prohibited bit. Do not read or write this bit.
Changeable operating mode:
I/E: Can be changed in either the initialization mode or the operating mode.
I/: Can be changed only in the initialization mode.
/E: Can be changed only in the operating mode.
R/W
R/W: Both read and write are possible.
/W: Write only
R/: Read only
/: Access prohibited

Notice:
Since the reading is made in synchronization with the SYNC signal (8 kHz) when the following control registers are set in the operating mode, maintain the condition for 250 μs or more.
CR1, CR2, CR10, CR11, CR12, CR20

See the method of accessing and controlling the internal data memory for the method of setting the following control registers.
CR6, CR7, CR8, CR9

(1) CR0

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR0	SPDN	#	AFE _EN	#	#	#	LONG/ SHORT	OPE _STAT	R/W
Mode in which the setting can be changed	/E	—	I/	—	—	—	I/	I/	
Initial value	0	0	0	0	1*	0	0	0	

B7: Software power down reset control
0: Normal operation mode
1: Power down reset
The power down reset state can be initiated by setting this bit to "1" for 200 nsec or longer. During the power down reset, all the contents of the control registers and of the internal data memory will be cleared automatically. The power down reset state is released by setting this bit to "1" first and then resetting it to "0".

B6: Reserved bit. Do not change the initial value.

B5: Analog front-end power down control
0: Normal operation mode
1: Power down state (excluding AVREF)
When using the G.729.A (8 kbps) ↔ G.726 (32 kbps) mutual conversion mode or the PCM I/F mode, it is recommended to set this bit to "1" since the analog front-end function is not used in these modes. In addition, when setting this bit to "1", simultaneously set the VFRO0 and VFRO1 outputs to the AVREF side (CR10-B2, B1 = "0").

B4-2: Reserved bits. Do not change the initial values.

B1: SYNC frame control
0: Long frame synchronization signal
1: Short frame synchronization signal

B0: Operation start control
0: Operation hold
1: Operation start
The initialization mode is entered after releasing the power down reset state. In the initialization mode, it becomes possible to modify the contents of the control registers and the internal data memory. Read out the READY bit (CR5-B7) repeatedly and start modifying the contents of the control registers and the internal data memory after detecting a "1" in this bit.
When this bit is set to "1" after completing the writing of data in the control registers and the internal data memory, the LSI goes into the READY state (CR5-B7 = "0") and the normal operation mode is initiated.
Carry out modifications of the control registers and the internal data memory after changing to the normal operation mode.
The method of changing the contents of the internal data memory is described later.
The flowchart of the initialization mode is shown in Fig. 25.

Note: *
Although the initial value of this bit is "0", it will be set to "1" automatically before starting the initialization mode. Further, a "0" will be set in this bit automatically after the initialization mode if TRANS_EN (CR11-B0) and PCMIF_EN (CR12-B0) are "1".
When setting this register, make sure that the above value is not changed.

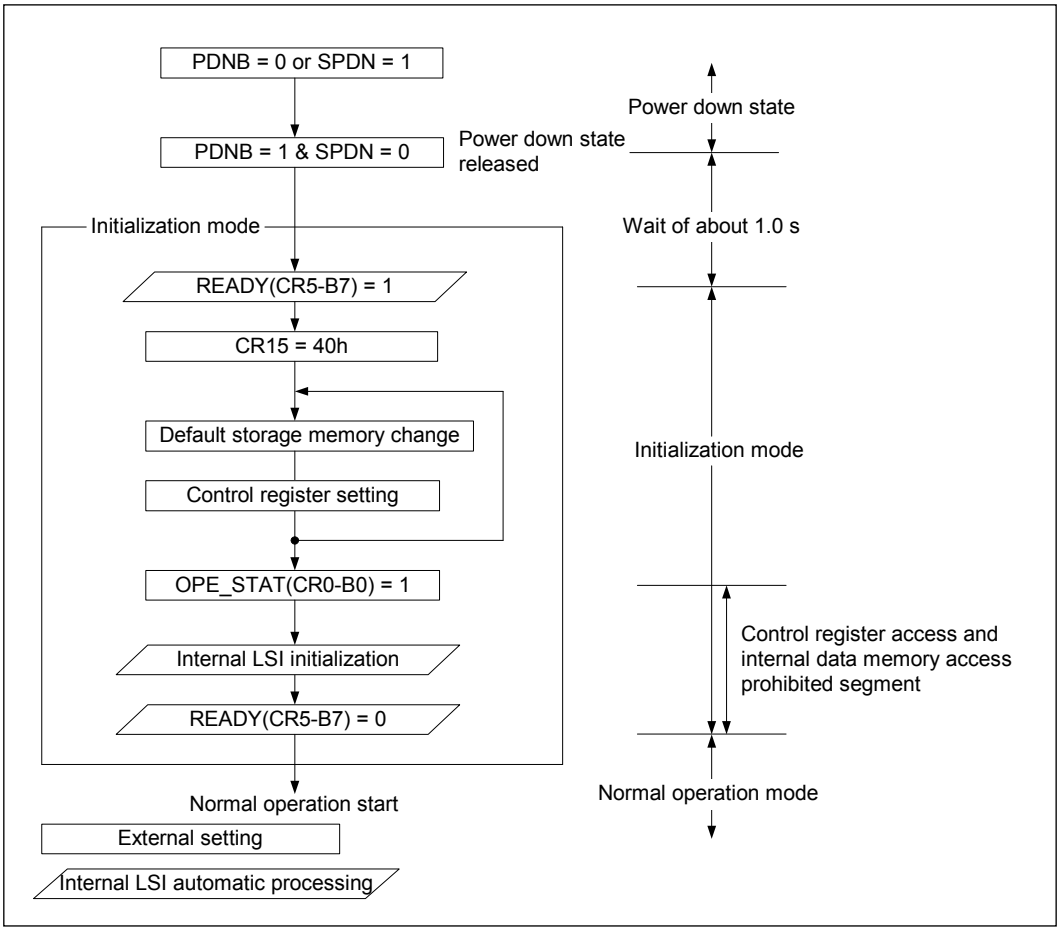


Fig. 25 Initialization mode flowchart

(2) CR1

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR1	XDMWR	XDMRD	#	#	#	#	#	#	R/W
Mode in which the setting can be changed	I/E	I/E	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Internal data memory write control

0: Write stopped

1: Write

The data set in CR8 and CR9 (D15 to D0) is written into the internal data memory at the address set in CR6 and CR7 (A15 to A0). When this writing is completed, this bit is automatically cleared to "0". When writing data successively, make the settings after confirming that this bit is "0".

For details of the method of controlling the internal memory, see the section on the method of accessing and controlling the internal data memory later in this booklet.

B6: Internal data memory read control

0: Read stopped

1: Read

The data in the internal data memory at the address set in CR6 and CR7 (A15 to A0) can be read out from CR8 and CR9 (D15 to D0).

When this reading is completed, this bit is cleared to "0" automatically. When reading out data successively, read the data after confirming that this bit has become "0".

For details of the method of controlling the internal memory, see the section on the method of accessing and controlling the internal data memory later in this booklet.

Notice: It is not possible to carry out simultaneously the above internal memory read and write controls. The setting of CR1-B7 and CR1-B6 = "11" is prohibited and should never be made.

B5 to B0: Reserved bits. Prohibited to change the initial settings.

(3) CR2

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR2	SC_EN	FGEN _EN	#	TDET1 _EN	TDET0 _EN	DTMF _EN	EC_EN	#	R/W
Mode in which the setting can be changed	I/E	I/E	—	I/E	I/E	I/E	I/E	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Speech CODEC control register

0: Speech CODEC stopped

The encoder stops and the storing of data in the transmit buffer is stopped. The decoder stops and no-tone data is output continuously. It is possible to change the speech data compression coding method when the speech CODEC has stopped.

1: Speech CODEC operated

The speech CODEC starts operating when this bit is set to "1".

The speech CODEC starts after carrying out its own initialization.

B6: FSK_GEN control register

0: FSK_GEN stopped

1: FSK_GEN operated

The operation is started by setting this bit to "1". Set this bit to "1" after storing the transmit data in CR18 and CR19. To stop the FSK data transmission, if this bit is reset to "0" during the period when FGEN_RQ (CR3-B5) is "1", the FSK_GEN stops after transmitting the final data.

B5: Reserved bit. Prohibited to change the initial setting.

B4: TONE_DET1 detector control register

0: TONE_DET1 Stopped

1: TONE_DET1 Operated

The operation is started by setting this bit to "1". A "1" is set to TONE_DET1 (CR3-B4) during the period when a 2100 Hz* tone is being detected.

B3: TONE_DET0 detector control register

0: TONE_DET1 Stopped

1: TONE_DET1 Operation

The operation is started by setting this bit to "1". A "1" is set to TONE_DET0 (CR3-B3) during the period when a 1650 Hz* tone is being detected.

Remarks:

* It is possible to change the detect frequencies. Contact ROHM's responsible sales person if you wish to change these frequencies.

B2: DTMF detector control register

0: DTMF detect function stopped

1: DTMF detect function operated

B1: Echo canceller control register

0: Echo canceller function stopped (The echo canceller is put in the through mode)

1: Echo canceller function active

Remarks:

The operation is started after the echo canceller internal coefficients cleared.

B0: Reserved bit. Prohibited to change the initial setting.

(4) CR3

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR3	DSP _ERR	FGEN _RQ	#	TONE1 _DET	TONE0 _DET	#	TX _ERR	RX _ERR	R/
Mode in which the setting can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: DSP status register
0: Normal operation state
1: Abnormal operation state
This LSI has a built-in watchdog timer, and when the program of the DSP section goes into uncontrollable execution state due to external disturbances around this LSI or due to power supply abnormalities, etc., the DSP_ERR status will be set to "1" and an interrupt will be generated. When this bit becomes "1", carry out a power down reset using either PDNB or SPDN of CR0-B7. This bit gets cleared by a power down reset operation.

Notice:
The DSP_ERR status cannot detect all abnormal operation conditions. The abnormality will not be detected even when the DSP goes into uncontrolled program execution if the watchdog timer gets cleared during that program execution.

B6: FSK generator transmit data request status register
0: No request present
1: Request present
When FGEN_EN (CR2-B6) is in the "1" state, this bit is set to "1" after the DSP takes in the FSK transmit data thereby requesting for the next FSK transmit data.

B5: Reserved bit. Prohibited to change the initial setting.

B4: TONE1 detector detect status register
0: Not detected
1: Detected

B3: TONE0 detector detect status register
0: Not detected
1: Detected

B2: Reserved bit. Prohibited to change the initial setting.

B1: Transmit buffer status register
0: Transmit buffer in normal operation state
1: Transmit buffer in error state
This bit becomes "1" when an overrun error occurs in the transmit buffer, and will be "0" otherwise.

B0: Receive buffer status register
0: Receive buffer in normal operation state
1: Receive buffer in error state
This bit becomes "1" when an underflow error occurs in the receive buffer, and will be "0" otherwise.

An interrupt is generated whenever there is a change in the state of any of the above bits ("0" → "1" or "1" → "0").

(5) CR4

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR4	INT	DP_DET	#	DTMF _DET	DTMF_ CODE3	DTMF_ CODE2	DTMF_ CODE1	DTMF_ CODE0	
Mode in which the setting can be changed	—	—	—	—	—	—	—	—	R/
Initial value	0	0	0	0	0	0	0	0	

B7: Interrupt generation status register
This is a directly coupled register with the logic of INTB inverted. A "1" will be read out from this bit when INTB is "L" and will be "0" otherwise.
0: During the period INTB is "H"
1: During the period INTB is "L"

Notice: The statuses of the INT bit and INTB may not be the same when a DSP_ERR is generated.

B6: Dial pulse detector detect status register
This bit indicates the detect status of the dial pulse detector. This bit becomes "1" during the period when a dial pulse is being detected and will be "0" otherwise.
0: Dial pulse not detected
1: Dial pulse detected

B5: Reserved bit. Prohibited to change the initial value.

B4: DTMF detector detect status register
This bit indicates the detect status of the DTMF detector.
This bit becomes "1" during the period when a DTMF signal is being detected and will be "0" otherwise.
0: No DTMF signal detected
1: DTMF signal detected

B3 to B0: DTMF code indication registers
When DTMF_EN (CR2-B2) has been set to "1", a valid DTMF code is stored in these bits during the period a DTMF signal is being detected (CR4-B4 DTMF_DET = "1"). These bits output the data "0000" when no DTMF signal is detected (DTMF_DET = "0"). The codes are listed in Table 5.

Table 5 DTMF detect code table

DTMF_3	DTMF_2	DTMF_1	DTMF_0	Low frequency [Hz]	High frequency [Hz]	Dial number
0	0	0	0	697	1209	1
0	0	0	1	770	1209	4
0	0	1	0	852	1209	7
0	0	1	1	941	1209	*
0	1	0	0	697	1336	2
0	1	0	1	770	1336	5
0	1	1	0	852	1336	8
0	1	1	1	941	1336	0
1	0	0	0	697	1477	3
1	0	0	1	770	1477	6
1	0	1	0	852	1477	9
1	0	1	1	941	1477	#
1	1	0	0	697	1633	A
1	1	0	1	770	1633	B
1	1	1	0	852	1633	C
1	1	1	1	941	1633	D

An interrupt is generated whenever there is a change in the statuses of the bits B6, B4 to B0 above ("0" → "1" or "1" → "0").

(6) CR5

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR5	READY	#	#	#	#	#	#	#	R/
Mode in which the setting can be changed.	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7: Initialization mode indication register

0: Other than the initialization mode

1: Initialization in progress

After the power down reset state is released, this LSI enters the initialization mode. This bit will be set to "1" in the initialization mode.

B6 to B0: Reserved bits. Prohibited to change the initial settings.

(7) CR6

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR6	A15	A14	A13	A12	A11	A10	A9	A8	/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Higher order address of the internal data memory

These bits are the registers for setting the higher order byte of the address in the internal data memory. For details on the method of writing, see the section on the method of accessing and controlling the internal data memory

(8) CR7

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR7	A7	A6	A5	A4	A3	A2	A1	A0	/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Lower order address of the internal data memory

These bits are the registers for setting the lower order byte of the address in the internal data memory. For details on the method of writing, see the section on the method of accessing and controlling the internal data memory.

(9) CR8

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR8	D15	D14	D13	D12	D11	D10	D9	D8	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Higher order data of the internal data memory

These bits are the registers for setting the higher order byte of the data in the internal data memory. For details on the method of writing and reading, see the section on the method of accessing and controlling the internal data memory.

(10) CR9

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR9	D7	D6	D5	D4	D3	D2	D1	D0	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Lower order data of the internal data memory

These bits are the registers for setting the lower order byte of the data in the internal memory. For details on the method of writing and reading, see the section on the method of accessing and controlling the internal data memory.

(11) CR10

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR10	#	DPDET_EN	#	TDET1_SEL	TDET0_SEL	VFRO1_SEL	VFRO0_SEL	AIN_SEL	R/W
Mode in which the value can be changed	—	I/E	—	I/	I/	I/E	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7: Reserved bit. Prohibited to change the initial setting.

B6: Dial pulse detector control register
0: Dial pulse detector stopped
1: Dial pulse detector active

B5: Reserved bit. Prohibited to change the initial setting.

B4: TDET1 detect path select register
0: Transmitting section
1: Receiving section

B3: TDET0 detect path select register
0: Transmitting section
1: Receiving section

B2: VFRO1 selection
0: AVREF (Output of about 1.4 V)
1: Receiver side speech output

B1: VFRO0 selection
0: AVREF (Output of about 1.4 V)
1: Receiver side speech output

B0: Input amplifier selection
0: Selection of AMP0
1: Selection of AMP1

(12) CR11

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR11	FRAME/ DMA	10ms /20ms	16B /8B	#	#	SC _SEL1	SC _SEL0	TRANS _EN	R/W
Mode in which the value can be changed	I/	I/	I/	—	—	I/E	I/E	I/	
Initial value	0	0	0	0	0	0	0	0	

B7: FRAME/DMA select register
0: FRAME access
1: DMA slave interface access
This bit selects the method of accessing the transmit and receive buffers. The initial value is frame access.

B6: 10 ms/20 ms select register
0: 10 ms
1: 20 ms
This bit selects the buffering time of the transmit and receive buffers. The initial value is 10 ms.

B5: MCU interface data width select register
0: 16-bit data width interface
1: 8-bit data width interface
This bit selects the width of the data bus connected to the transmit and receive buffers. The initial value is 16 bits.
When the 8-bit bus width is used, tie D15 to D8 to either "1" or "0".

B4, B3: Reserved bits. Prohibited to change the initial values.

B2, B1: Speech CODEC select registers
- When using the analog I/F mode,
(0, 0): G.729.A
(0, 1): G.711 (μ-law)
(1, 0): G.726 (32 kbps)
(1, 1): G.711 (A-law)
The speech CODEC can be selected when CR2-B7 (SC_EN) is in the "0" state. Prohibited to change the speech CODEC when it is operating.
- When using the PCM I/F mode (CR12-B0 = "1"),
These bits select the PCM I/F coding method.
Further, the speech CODEC select bits will be CR12-B2 and CR12-B1.
(0, 0): 16-bit linear (2's complement format)
(0, 1): G.711 (μ-law)
(1, 0): Prohibited
(1, 1): G.711 (A-law)
The coding method can be selected when CR2-B7 (SC_EN) is in the "0" state. Prohibited to change the coding method during operation.

B0: G.726 ↔ G.729.A Mutual conversion control
This bit controls the G.726 (32 kbps) ↔ G.729.A (8 kbps) mutual conversion mode.
0: Mutual conversion stopped
1: Mutual conversion active
When this bit is set to "1", the PCM I/F is used and the operation becomes a G.726 ↔ G.729.A mutual conversion operation.
When using this function, the operation is started after setting the coding method in B2 and B1 to "10" and making CR2-B7 (SC_EN) "1".

(13) CR12

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR12	#	#	#	#	#	PSC _SEL1	PSC _SEL0	PCMIF _EN	
Mode in which the value can be changed	—	—	—	—	—	I/E	I/E	I/	/W
Initial value	0	0	0	0	0	0	0	0	

B7 to B3: Reserved bits. Prohibited to change the initial settings.

B2, B1: Speech CODEC select registers in the PCM I/F mode
(0, 0): G.729.A
(0, 1): G.711 (μ-law)
(1, 0): G.726 (32 kbps)
(1, 1): G.711 (A-law)
The speech CODEC type can be selected when CR2-B7 (SC_EN) is in the "0" state. Prohibited to change the speech CODEC type during operation.

B0: PCM I/F mode control register
0: Analog I/F mode
Set the speech CODEC type selection in CR11-B2 and CR11-B1.
1: PCM I/F mode
Set the PCM/IF coding method in CR11-B2 and CR11-B1, and set the speech CODEC type selection in B2 and B1 of this register.

(14) CR13

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR13	$	$	$	$	$	$	$	$	
Mode in which the value can be changed	—	—	—	—	—	—	—	—	/
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Reserved bits. Prohibited to change the initial settings.

(15) CR14

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR14	$	$	$	$	$	$	$	$	
Mode in which the value can be changed	—	—	—	—	—	—	—	—	/
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: Reserved bits. Prohibited to change the initial settings.

(16) CR15

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR15	TA	TA	TA	$	$	$	$	$	R/W
Mode in which the value can be changed	I	I	I	—	—	—	—	—	
Initial value	0	0	0	0	0	0	0	0	

B7 to B5: Registers for adjustment
Set to "010" at the beginning of the initialization mode.
(0, 1, 0): Fixed

B4 to B0: Reserved bits. Prohibited to change the initial settings.

(17) CR16

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR16	#	#	#	#	#	#	GPI1	GPI0	R/
Mode in which the value can be changed	—	—	—	—	—	—	—	—	
Initial value	0	0	0	0	0	0	—	—	

B7 to B2: Reserved bits. Prohibited to change the initial settings.

B1: GPI1 level read out register
0: GPI1 level is "0".
1: GPI1 level is "1".

B0: GPI0 level read out register
0: GPI0 level is "0".
1: GPI0 level is "1".
Note:
GPI0 is used as the input of the dial pulse detector in the secondary functions. It is possible to read out GPI0 even when the dial pulse detector is operating.

(18) CR17

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR17	#	#	#	#	#	#	GPO1	GPO0	R/W
Mode in which the value can be changed	—	—	—	—	—	—	I/E	I/E	
Initial value	0	0	0	0	0	0	0	0	

B7 to B2: Reserved bits. Prohibited to change the initial settings.

B1: GPO1 output level register
0: "L" level is output at GPO1.
1: "H" level is output at GPO1.

B0: GPO0 output level register
0: "L" level is output at GPO0.
1: "H" level is output at GPO0.
Notice:
GPO0 is used in the secondary functions as the output of the dial pulse transmitter.
Note that it is prohibited to change the content of the GPO0 bit when the dial pulse detector is operating.

(19) CR18

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR18	FSK_D7	FSK_D6	FSK_D5	FSK_D4	FSK_D3	FSK_D2	FSK_D1	FSK_D0	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7 to B0: FSK transmit data setting registers

(20) CR19

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR19	#	#	#	#	#	#	FSK_D9	FSK_D8	R/W
Mode in which the value can be changed	—						I/E		
Initial value	0	0	0	0	0	0	0	0	

B7 to B2: Reserved bits. Prohibited to change the initial settings.

B1, B0: FSK transmit data setting registers.

(21) CR20

	B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR20	TGEN _RX	TGEN _TX	TGEN _CNT5	TGEN _CNT4	TGEN _CNT3	TGEN _CNT2	TGEN _CNT1	TGEN _CNT0	R/W
Mode in which the value can be changed	I/E								
Initial value	0	0	0	0	0	0	0	0	

B7: TONE RX section output control register
0: Output stopped.
1: Tone output at the RX section

B6: TONE TX section output control register
0: Output stopped.
1: Tone output at the TX section

B5: Register for controlling addition or multiplication of TONE A/B
0: Addition (The TONE A and TONE B outputs are added.)
1: Multiplication (The TONE A and TONE B outputs are multiplied.)

B4: TONE A/B output control register
0: Onetime tone output
The signal is output for a duration equal to the sum of TIM_M0 and TIM_M1 and then stopped.
After stopping, CR20 will be cleared automatically within the LSI.
1: Repetitive tone output
The signal is output repeatedly as controlled by the time duration equal to the sum of TIM_M0 and TIM_M1.
Write 00h in this register CR20 in order to stop the signal output.
Notice:
It is prohibited to write any value in this register other than 00h when repetitive output is being made.
In the case of onetime tone output operation, make the next setting only after making sure that the content of this register has become 00h. When tone output is intended to resume after repetitive tone output is once ceased, the register setting must be made only after Fade-out time plus 250μs.

B3, B2: TONE A output control registers
00: No tone is output.
01: The tone is stopped during the M0 period and is output during the M1 period.
10: The tone is output during the M0 period and stopped during the M1 period.
11: The tone is output during both the M0 and M1 periods.

B1, B0: TONE B output control registers
00: No tone is output.
01: The tone is stopped during the M0 period and is output during the M1 period.
10: The tone is output during the M0 period and is stopped during the M1 period.
11: The tone is output during both the M0 and M1 periods.

Note:
Although it is possible to output TONE A and TONE B alternately when the output controls of TONE A and TONE B are set in a mutually exclusive manner and their outputs are summed, the waveform after addition will be discontinuous since the phases of the two signals will be independent of each other.

The tone generator section block diagram is shown in Fig. 26, the tone output control method is shown in Fig. 27, and the tone output control parameters are shown in Fig. 28.

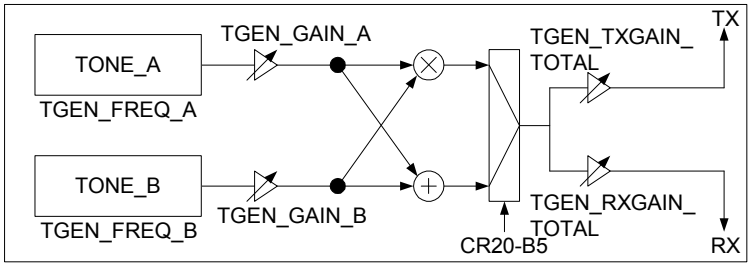


Fig. 26 Tone generator section block diagram

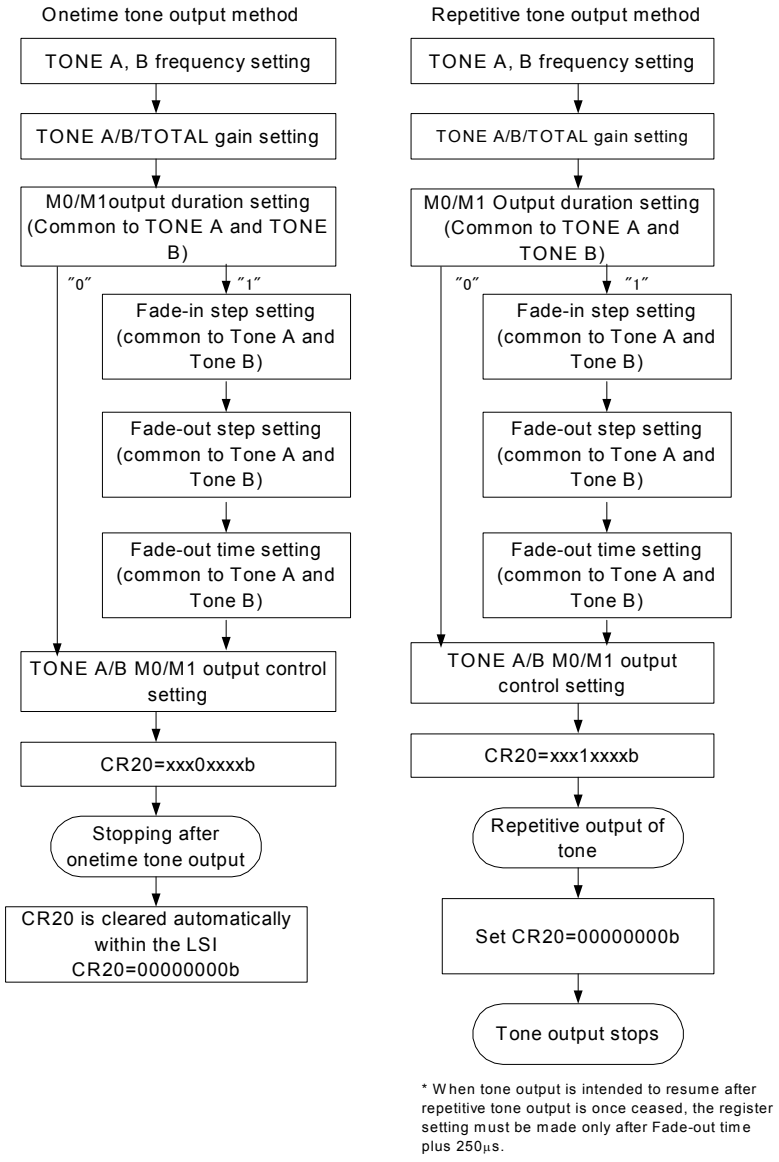


Fig. 27 Tone output control method

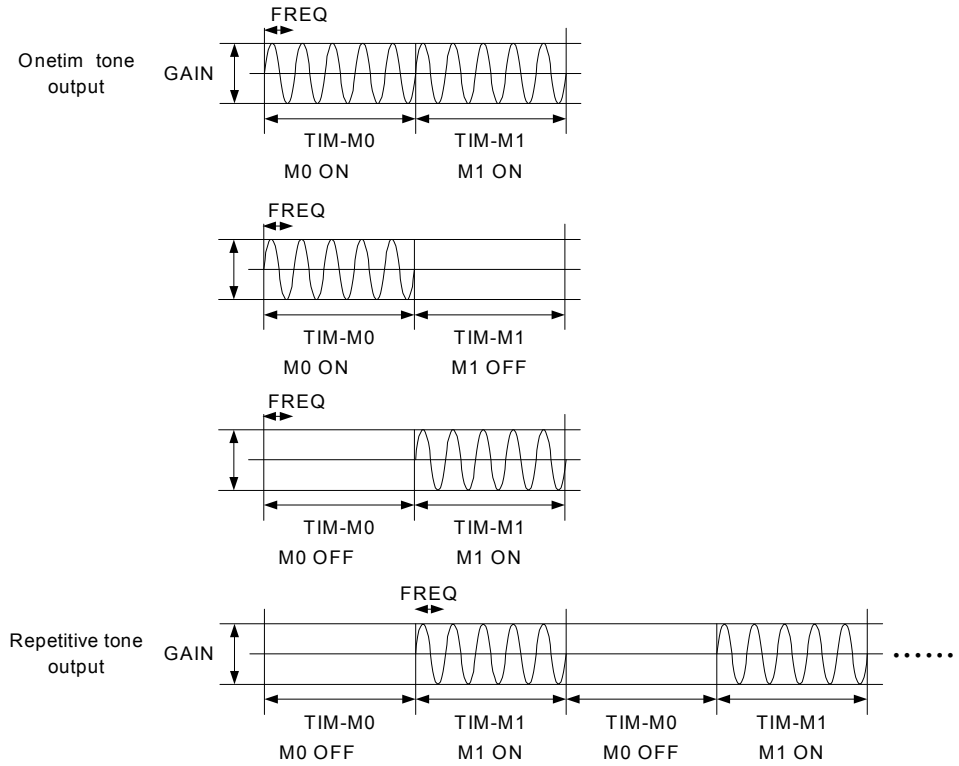


Fig. 28 Tone output control parameters

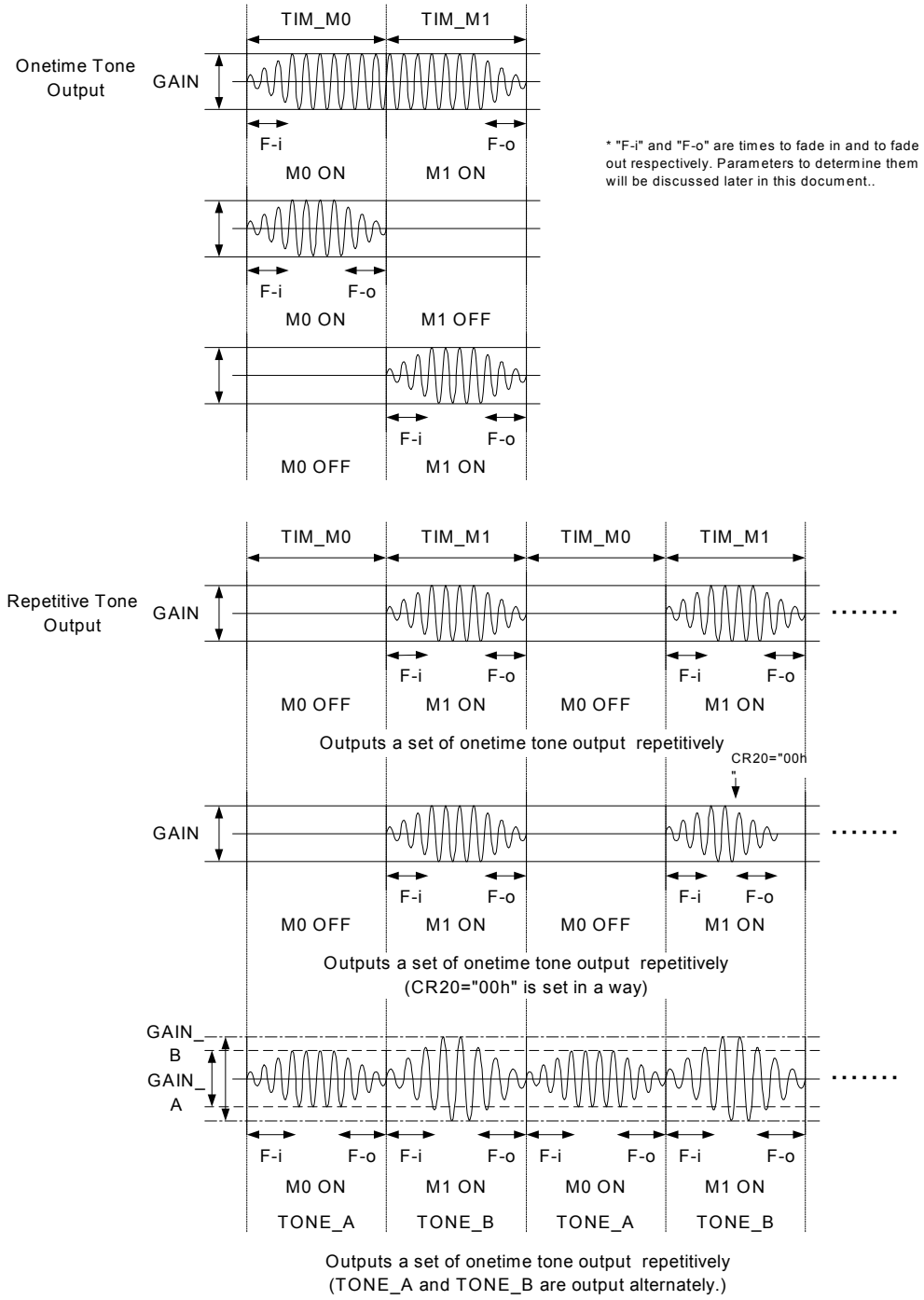


Fig. 29 Tone output control parameters (in a case with TGEN_FADE_CONT "ON")

METHOD OF ACCESSING AND CONTROLLING INTERNAL DATA MEMORY

Writing Method

The four 8-bit registers CR6 to CR9 mapped within the set of control registers are allocated to the following:
16-bit address of the internal data memory (A15 to A0)
16-bit data to be written (D15 to D0)

The initialization mode is entered and a "1" is set in CR5-B7 (READY) about 1.0 s after release from a power down reset due to PDNB or after a release from a software power down reset due to CR0-B7.
In this writable state, after setting in CR6 to CR9 the internal data memory address and the data to be written, if a "1" is set in CR1-B7 (XDMWR), the writing of one word of data in the internal data memory will be completed. After completion of writing the data, CR1-B7 will be cleared to "0" automatically. The method of setting data in the internal data memory is shown in Fig. 30.
Repeat the above operations for writing to several memory locations. When all the writing operations have been completed, the normal operations can be started by setting a "1" in CR0-B0 (OPE_STAT).

It is possible to re-write even in modes other than the initialization mode the internal data memory locations related to gain control, TONE transmission, EC, DPGEN, and TIMER. Even in such cases, carry out the updating of the internal data memory using the same method as described above.
Table 6 and Table 7 list the internal data memory and related control registers.

Note:
When data is set in the internal data memory during operation, since the reading is done in synchronization with the SYNC signal (8 kHz), maintain the state for 250 μs or more.

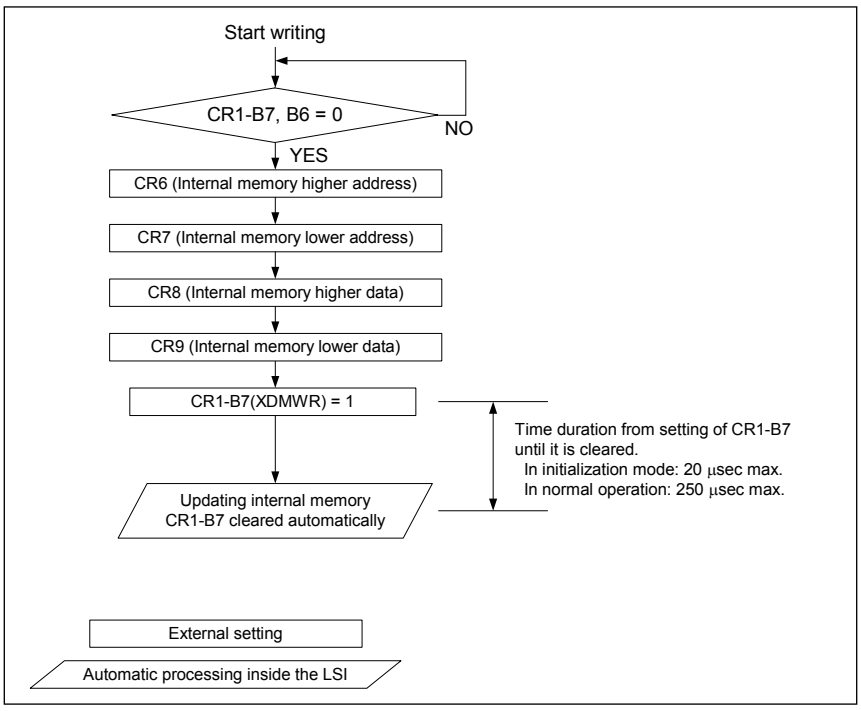


Fig. 30 Method of setting data in the internal data memory

Reading Method

After setting the internal data memory address in CR6 and CR7, one word of data from the internal data memory is stored in CR8 and CR9 when a "1" is written in CR1-B6 (XDMRD). After reading the data, CR1-B6 will be cleared to "0" automatically. The method of reading the internal data memory is shown in Fig. 31.

Further, the internal data memory read out can only be made for the internal data memory and the read only data memory within the related registers listed in Table 6 and Table 7.

Notice:

When the internal data memory is read out during operation, since the reading out is done in synchronization with the SYNC signal (8 kHz), maintain the set address in the same state for 250 μs or more.

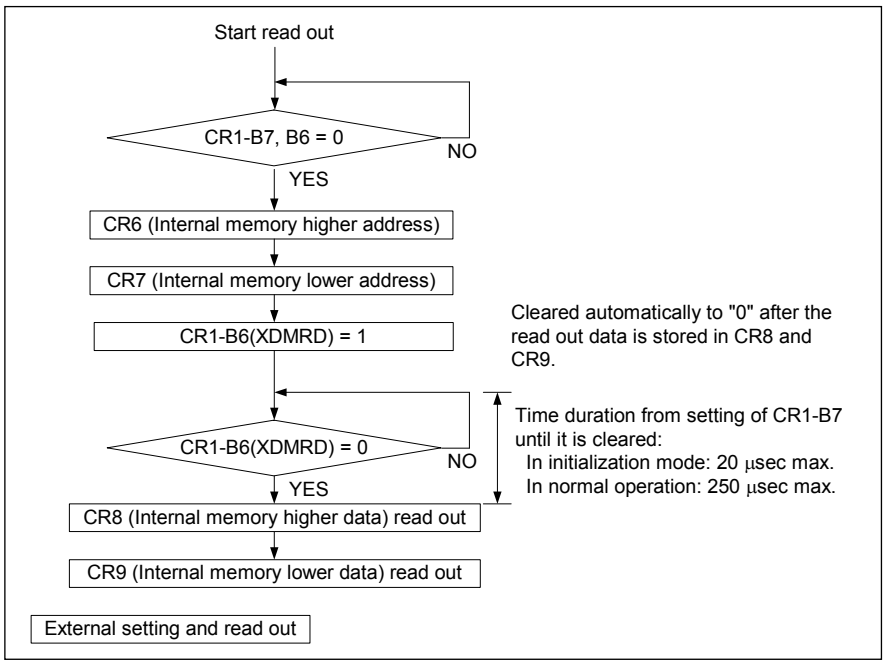


Fig. 31 Method of reading out internal data memory

Table 6 Internal data memory and related control registers (1/3)

Function name	Internal data memory name	Address	Initial value		Modes in which updating and read are possible		
			Data	Data value	In initializa-tion mode	During idle state	During operation
Gain control	Transmit gain (TXGAIN)	00ECh	0080h	0 dB	Y	Y	Y
	Receive gain (RXGAIN)	00EDh	0080h	0 dB	Y	Y	Y
	Side tone gain (STGAIN)	00EEh	0000h	MUTE	Y	Y	Y
	Gain fade control (GAIN_FADE_CONT)	00EFh	0000h	disabled	Y	Y	N
	Gain fade-in step (GAIN_FADE_IN_ST)	00F0h	4C10h	+1.5dB	Y	Y*1	N
	Gain fade-out step (GAIN_FADE_OUT_ST)	00F1h	35D9h	-1.5dB	Y	Y*1	N
Tone genera-tion TONE_ GEN	TONE transmit control	CR20	00h	Transmission stopped	Y	Y	Y
	In-execution flag (TGEN_EXE_FLAG) (Read-only memory)	00C3h	0000h	Not in execution	Y	Y	Y
	TONE A frequency control (TGEN_FREQ_A)	00C8h	0CCCh	400 Hz	Y	Y	N
	TONE B frequency control (TGEN_ FREQ_B)	00CAh	007Ah	15 Hz	Y	Y	N
	TONE A gain control (TGEN_GAIN_A)	00CCh	0080h	–13.3 dBm0	Y	Y	Y
	TONE B gain control (TGEN_GAIN_B)	00CDh	0080h	–13.3 dBm0	Y	Y	Y
	TONE time control 0 (TGEN_TIM_M0)	00CEh	0FA0h	500 ms	Y	Y	N
	TONE time control 1 (TGEN_TIM_M1)	00D1h	0FA0h	500 ms	Y	Y	N
	RX section transmit gain (TGEN_RXGAIN_TOTAL)	00D2h	0080h	0 dB	Y	Y	Y
	TX section transmit gain (TGEN_TXGAIN_TOTAL)	00D3h	0080h	0 dB	Y	Y	Y
	TONE fade control (TGEN_FADE_CONT)	00D4h	0000h	disabled	Y	Y	N
	TONE fade-in step (TGEN_FADE_IN_ST)	00D5h	47CFh	+1dB	Y	Y	N
	TONE fade-out step (TGEN_FADE_OUT_ST)	00D6h	390Ah	-1dB	Y	Y	N
	TONE fade-out time (TONE_FADE_OUT_TIM)	00D7h	002Bh	43 Sync	Y	Y	N
	TONE total gain fade control (TGEN_GAIN_TOTAL_FADE_CONT)	00C4h	0000h	disabled	Y	Y	N
	TONE total gain fade-in step (TGEN_GAIN_TOTAL_FADE_IN_ST)	00C5h	4C10h	+1.5dB	Y	Y	N
	TONE total gain fade-out step (TGEN_GAIN_TOTAL_FADE_OUT_ST)	00C6h	35D9h	-1.5dB	Y	Y	N

*1 when gain fade is disabled

Table 7 Internal data memory and related control registers (2/3)

Function name	Internal data memory name	Address	Initial value		Modes in which updating and read are possible		
			Data	Data value	In initializa-tion mode	During idle state	During operation
FSK generat-or FSK_ GEN	FSK output control	CR2-B6	0b	Stopped	Y	Y	Y
	FSK transmit data 0	CR18	00h	00h	Y	Y	Y
	FSK transmit data 1	CR19-B1 ,B0	00b	00b	Y	Y	Y
	FSK gain control (FGEN_GAIN)	00E4h	0080h	–13.3 dBm0	Y	Y	N
TONE 0 detector TONE_ DET0	TONE 0 control	CR2-B3	0b	Stopped	Y	Y	Y
	Detect level control (TDET0_TH)	0040h	1EBBh	–5.3 dBm0	Y	Y	N
	ON guard timer control (TDET0_ON_TM)	0041h	0028h	5 ms	Y	Y	N
	OFF guard timer control(TDET0_OFF_TM)	0042h	0028h	5 ms	Y	Y	N
	Detect frequency (TDET0_FREQ)	- - - - h	-	1650 Hz	Y	N	N
TONE 1 detector TONE_ DET1	TONE 1 control	CR2-B4	0b	Stopped	Y	Y	Y
	Detect level control (TDET1_TH)	0052h	1EBBh	–5.3 dBm0	Y	Y	N
	Detect ON guard timer control(TDET1_ON_TM)	0053h	0028h	5 ms	Y	Y	N
	Detect OFF guard timer control (TDET1_OFF_TM)	0054h	0028h	5 ms	Y	Y	N
	Detect frequency (TDET1_FREQ)	- - - - h	-	2100 Hz	Y	N	N
DTMF detector DTMF_ REC	DTMF control	CR2-B2	0b	Stopped	Y	Y	Y
	Detect level (DTMF_TH)	005Ah	1000h	–37.0 dBm0	Y	Y	N
	Detect ON guard timer(DTMF _ON_TM)	00BFh	00A0h	20 ms	Y	Y	N
	Detect OFF guard timer(DTMF _OFF_TM)	00C1h	00A0h	20 ms	Y	Y	N
Echo Cancel-ler	EC control	CR2-B1	0b	Stopped	Y	Y	Y
	EC control (EC_CR)	0171h	0012h	HD ATT OFF	Y	Y	Y
	GLPAD control (GLPAD_CR)	0172h	000Fh	+6/–6 dB	Y	Y	N

Table 8 Internal data memory and related control registers (3/3)

Function name	Internal data memory name	Address	Initial value		Modes in which updating and read are possible		
			Data	Data value	In initializa-tion mode	During idle state	During operation
Dial pulse Detector DPDET	ON guard timer control (DPDET_ON_TIM)	011Bh	0028h	5 ms	Y	Y	N
	OFF guard timer control (DPDET_OFF_TIM)	011Ch	0028h	5 ms	Y	Y	N
	Polarity control (DPDET_POL)	122Eh	0000h	Positive logic	Y	Y	N
	End of detect timer control (DPDET_DETOFF_TIM)	122Fh	03E8h	125 ms	Y	Y	N
	Detect code (DPDET_CODE) (Read only data memory)	1231h	0000h	Not detected	Y	Y	Y
Dial Pulse Generat-or DPGEN	Output control (DPGEN_EN) (Can be read out)	1220h	0000h	Stopped	Y	Y	Y
	Output data (DPGEN_DATA)	1221h	0000h	Stopped	Y	Y	N
	PPS control (DPGEN_PPS)	1222h	0000h	10 pps	Y	Y	N
	High period setting (DPGEN_DUTY)	1223h	0108h	33 ms	Y	Y	N
	End of output control (DPGEN_OFF_TIM)	1225h	03E8h	125 ms	Y	Y	N
TIMER	Timer control (TIM_EN)	1218h	0000h	Stopped	Y	Y	Y
	Timer counter value display (TIM_COUNT) (read only data memory)	1219h	0000h	Count value	Y	Y	Y
	Timer data setting (TIM_DATA)	121Ah	FFFFh	MAX FFFFh	Y	Y	N
Outband control	Outband control (OUTBAND_CONTROL)	1307h	0000h	disabled	Y	N	N
Outband G.729.A data	Outband G.729.A data (OUTBAND_G729_DAT)	016Ch 016Dh 016Eh 016Fh 0170h	7852h 80A0h 00FAh C200h 07D6h	-	Y	N	N
Version	LSI code display (ML7074_VERSION) (read only data memory)	0152h	0000h	ML7074-003	Y	Y	Y

Note:
Initialization mode: The state after release from a power down reset, and in which the initial values of control registers and internal data memory can be altered.
During idle state: The state in which the function given in the function name column has stopped.
During operation: The state in which the function given in the function name column is operating.

Gain Control (TXGAIN, RXGAIN, STGAIN)

It is possible to change the values of the transmit gain (TXGAIN), receive gain (RXGAIN), and side tone gain (STGAIN). The positions of the respective gain controllers are the following.

Transmit gain (TXGAIN):	Immediately before the speech CODEC input.
Receive gain (RXGAIN):	Immediately after the speech CODEC output.
Side tone gain (STGAIN):	Added to the input of the receiver section LPF from the output of the transmitter section BPF of the linear PCM CODEC.

A. Internal data memory for adjusting transmit gain (TXGAIN)
Address: 00Ech, initial value: 0080h (0.0 dB)
When changing the gain value, compute it using the following equation:
Equation: 0080h × GAIN
Example: Making the gain +6 dB (×2):
0080h × 2 = 0100h

Upper limit	: About 40 dB higher	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit	: About –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

B. Internal data memory for adjusting receive gain (RXGAIN)
Address: 00EDh, initial value: 0080h (0.0 dB)
When changing the gain value, compute it using the following equation:
Equation: 0080h × GAIN
Example: Making the gain +6 dB (×2):
0080h × 2 = 0100h

Upper limit	: About 40 dB higher	(data: 3200h)
	: 0 dB	(data: 0080h)
Lower limit	: About –42 dB	(data: 0001h)
	: MUTE	(data: 0000h)

C. Internal data memory for adjusting side tone gain (STGAIN)
Address: 00EEh, initial value: 0000h (MUTE)
When changing the side tone gain value, compute it using the following equation:
Equation: 1000h × GAIN
Example: Making the gain –20 dB (×0.1):
1000h × 0.1 = 019Ah

Upper limit	: 0 dB	(data: 1000h)
Lower limit	: About –72 dB	(data: 0001h)
	: MUTE	(data: 0000h)

D. Internal data memory for gain fade (GAIN_FADE_CONT)
"1" in B0 enables fade-in/-out in Tx gain alternation; "1" in B1 enables the function in Rx gain alternation; and "1" in B2 enables the function at muting in outband control.

	B7	B6	B5	B4	B3	B2	B1	B0
	-	-	-	-	-	OUTBAND_FADE_CONT	RX_FADE_CONT	TX_FADE_CONT
Initial value	0	0	0	0	0	0	0	0

Address : 00EFh, initial value : 0000h (Outband : disabled, Rx : disabled, Tx : disabled)
B7, 6, 5, 4, 3 : Reserved bits (Prohibited to change the initial settings)
B2 : OUTBAND_FADE_CONT
1 : ON (Fading-in/-out at muting and at un-muting)
0 : OFF
B1 : RX_FADE_CONT
1 : ON (Fading-in/-out at Rx gain alternation)
0 : OFF
B0 : TX_FADE_CONT
1 : ON (Fading-in/-out at Tx gain alternation)
0 : OFF

E. Internal data memory for gain fade-in step (GAIN_FADE_IN_ST)
Address: 00F0h, initial value: 4C10h (+1.5dB)
When changing the step value, X, compute it using the following equation:
Equation: 10^(X/20)*16384
Example: Making the step value +3 dB:
10^(3/20)*16384 = 23143d = 5A67h
Upper limit : About +6.0 dB (data: 7FFFh)
Lower limit : About +0.1 dB (data: 40BDh)

F. Internal data memory forgain fade-out step (GAIN_FADE_OUT_ST)
Address: 00F1h, initial value: 35D9h (-1.5dB)
When changing the step value, X, compute it using the following equation:
Equation: 10^(X/20)*16384
Example: Making the step value -3 dB:
10^(-3/20)*16384 = 11598d = 2D4Eh
Upper limit : About -6.0 dB (data: 2000h)
Lower limit : About -0.1 dB (data: 3F44h)
(Note) Step values for fade-in and fade-out can be determined independently; whereas the step values determined for fade-in and fade-out are common to Tx gain, Rx gain and OUTBAND_FADE_CONT.

Tone Generator (TONE_GEN)

It is possible to set the various types of parameters of the tone generator block.

A. Internal data memory for tone frequency control
TONE_A (TGEN_FREQ_A)
Address: 00C8h
Initial value: 0CCCh (400 Hz)
TONE_B (TGEN_FREQ_B)
Address: 00CAh
Initial value: 007Ah (15 Hz)

At the initial setting values a TONE A of 400 Hz and a TONE B of 15 Hz are output. Use the following equation to compute the value of the setting when changing the frequency.
Equation: A × 8.192 (A is the frequency to be set)
Example: To set a frequency of 2100 Hz:
2100 × 8.192 ≅ 4333h
Upper limit : 3 kHz (data: 6000h)
Lower limit : 15 Hz (data: 007Ah)

B. Internal data memory for tone gain control
TONE_A (TGEN_GAIN_A)
Address: 00CCh
Initial value: 0080h
TONE_B (TGEN_GAIN_B)
Address: 00CDh
Initial value: 0080h

The output level with the initial setting will be –13.3 dBm0. Use the following equation to compute the value of the setting when changing the gain.
Equation: 0080h × GAIN
Example: For reducing the gain by 6 dB (×0.5):
008Dh × 0.5 = 0040h
Upper limit : 12 dB more (data: 01FDh)
Lower limit : –12 dB less (data: 0020h)

Notice:
Make sure that the maximum amplitude does not exceed 3.17 dBm0 when the tones are multiplied or added.

C. Internal data memory for tone output time control (TGEN_TIM_M0/TGEN_TIM_M1)

TGEN_TIM_M0
(Output time duration)
Address: 00CEh
Initial value: 0FA0h (500 ms)

TGEN_TIM_M1
(Output time duration)
Address: 00D1h
Initial value: 0FA0h (500 ms)

Compute the value using the following equation when changing the time durations:
Equation: T/0.125 (T is the time duration in ms)
Example: When setting a time duration of 200 ms:
200/0.125 = 1600d = 0640h
Upper limit : 4095.875 msec (data: 7FFFh)
Lower limit : 0.125 msec (data: 0001h)

Notice:
It is prohibited to set a time duration of 0000h (0 msec) and hence be sure never to make such a setting.
The tone output times set here are commonly valid for TONE_A and TONE_B, and cannot be determined differently.

D. Internal data memory for tone total gain adjustment (TGEN_RXGAIN_TOTAL, TGEN_TXGAIN_TOTAL)

TGEN_RXGAIN_TOTAL
Address: 00D2h
Initial value: 0080h
TGEN_TXGAIN_TOTAL
Address: 00D3h
Initial value: 0080h

The initial values will be 0 dB. Compute using the following equation when changing the output level.
Equation: 0080h × GAIN
Example: Decreasing the output level by 6 dB:
0080h × 0.5 = 0040h
Upper limit : 40 dB higher (data: 3200h)
Lower limit : –40 dB lower (data: 0001h)
: MUTE (data: 0000h)

Notice:
The maximum amplitude should never exceed 1.3 Vp-p.

E. Internal data memory for tone fade control (TGEN_FADE_CONT)
Address: 00D4h
Initial value: 0000h (disabled)
"0000h" in this data memory enables fade-in/-out with tone gain control.
0000h: Fade-in/-out disabled
0001h: Fade-in/-out enabled

Notice:
When this fade-in/-out function is enabled, be sure that a corresponding fade-out step value and fade-out time are also set correctly, otherwise a pop noise might be generated at a tail.

F. Internal data memory for fade-in step value (TGEN_FADE_IN_ST)
Address: 00D5h
Initial value: 47CFh (+1.0dB)
Compute using the following equation when changing the step value, X.
Equation: 10^(X/20)*16384
Example: Sets a fade-in step to +3dB:
10^(3/20)*16384 = 23143d = 5A67h
Upper limit : about +6.0dB (data: 7FFFh)
Lower limit : about +0.1dB (data: 40BDh)

Notice:
The value set here are commonly valid for TONE_A and TONE_B, and cannot be determined differently.

G. Internal data memory for fade-out step value (TGEN_FADE_OUT_ST)
Address: 00D6h
Initial value: 390Ah (-1.0dB)
Compute using the following equation when changing the step value, X.
Equation: 10^(X/20)*16384
Example: Sets a fade-out step to -3dB:
10^(-3/20)*16384 = 11598d = 2D4Eh
Upper limit : about -6.0dB (data: 2000h)
Lower limit : about -0.1dB (data: 3F44h)

Notice:
The value set here are commonly valid for TONE_A and TONE_B, and cannot be determined differently.

H. Internal data memory for fade-out time (TGEN_FADE_OUT_TIM)
Address: 00D7h
Initial value: 002Bh (43 Sync)
Compute using the following equation when changing the fade-out time.
Equation: 43dB/"fade-out step value"[dB]
Example: in a case with a fade-out step value 2dB:
43/2 = 21d = 15h
Upper limit : 422 sync (data: 01A6h)
Lower limit : 8 sync (data: 0008h)

Notice:
"0000h" is prohibited to set.
Set a fade-out time less than TIM_M0
The value set here are commonly valid for TONE_A and TONE_B, and cannot be determined differently.

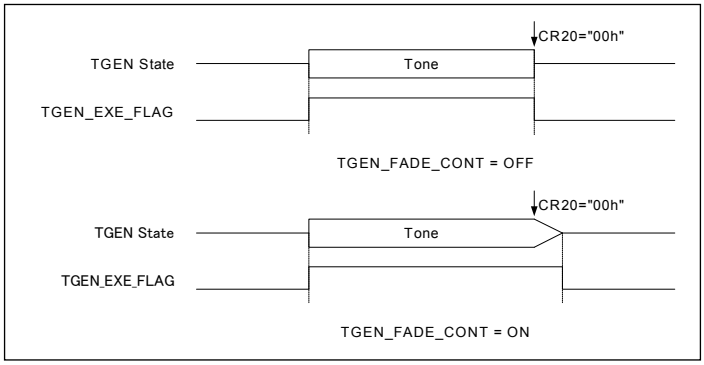
I. Internal data memory for total gain fade-out (TGEN_GAIN_TOTAL_FADE_CONT)
Address: 00C4h
Initial value: 0000h (disabled)
"0000h" in this data memory enables a function of total gain fade-in/-out for Tx and Rx.
0000h: disabled
0001h: enabled

Notice:
The control of this function is commonly valid for Tx and Rx, and cannot be determined differently.

J. Internal data memory for a fade-in step value of total gain (TGEN_GAIN_TOTAL_FADE_IN_ST)
Address: 00C5h
Initial value: 4C10h (+1.5dB)
Compute using the following equation when changing the step value, X.
Equation: 10^(X/20)*16384
Example: Sets a fade-in step to +3dB:
10^(3/20)*16384 = 23143d = 5A67h
Upper limit : about +6.0dB (data: 7FFFh)
Lower limit : about +0.1dB (data: 40BDh)
Notice:
The value set here are commonly valid for Tx and Rx, and cannot be determined differently.

K. Internal data memory for a fade-out step value of total gain (TGEN_GAIN_TOTAL_FADE_OUT_ST)
Address: 00D6h
Initial value: 35D9h (-1.5dB)
Compute using the following equation when changing the step value, X.
Equation: 10^(X/20)*16384
Example: Sets a fade-out step to -3dB:
10^(-3/20)*16384 = 11598d = 2D4Eh
Upper limit : about -6.0dB (data: 2000h)
Lower limit : about -0.1dB (data: 3F44h)
Notice:
The value set here are commonly valid for Tx and Rx, and cannot be determined differently.

L. Internal data memory for in-execution flag (TGEN_EXE_FLAG)
This address becomes “0001h” when a tone generator is under operation.
Address: 00C3h
Initial value: 0000h



FSK Generator (FSK_GEN)

The FSK generator (FSK_GEN) frequency-modulates the data set in the control register and outputs at VFRO0 and VFRO1. The specifications of the FSK generator are listed in Table 9 and its block diagram is shown in Fig. 32. The FSK generator is made up of an FSK signal generator, register for setting data, and gain adjustment section. After the data to be transmitted is set in the control registers FSK_D0 (CR18) or FSK_D1 (CR19), the data transmission is started when a "1" is set in FGEN_EN (CR2-B6). The buffer for data transmission consists of 10 bits and the data is output successively from the LSB side of FSK_D0 to the MSB (B1) of FSK_D1. The data transmit sequence is shown in Fig. 33. Further, the output level can be changed using the internal data memory (FGEN_GAIN). Once the data transmission is started, FGEN_RQ (CR3-B6) becomes "1" automatically thereby requesting the MCU to set the next transmission data. When transmitting data successively, set the 10 bits of data to be transmitted next in FSK_D0 and FSK_D1 within the period when FGEN_RQ is "1" (the period when data setting is valid). In order to end the transmission of data, set a "0" in FGEN_EN within the period in which FGEN_RQ is "1". The FSK generator will then stop after outputting the 10 bits of data currently being transmitted within the setting valid period. The transmit and stop timings are shown in Fig. 34 and an example of control is shown in Fig. 35.

Table 9 Specifications of FSK generator

Modulation method	Frequency modulation
Transfer speed	1200 bps
Output frequencies	1300 Hz (Data "1" Mark)
	2100 Hz (Data "0" Space)
Buffer for data output	10 bits (CR18-B7 to CR18-B0, CR19-B1, CR19-B0)
Output level	–13.3 dBm0 (Initial value, gain adjustment possible)

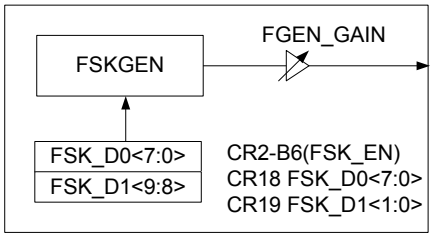


Fig. 32 FSK generator block diagram

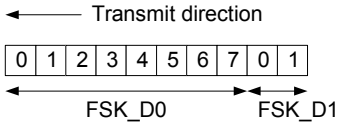


Fig. 33 Data transmit sequence

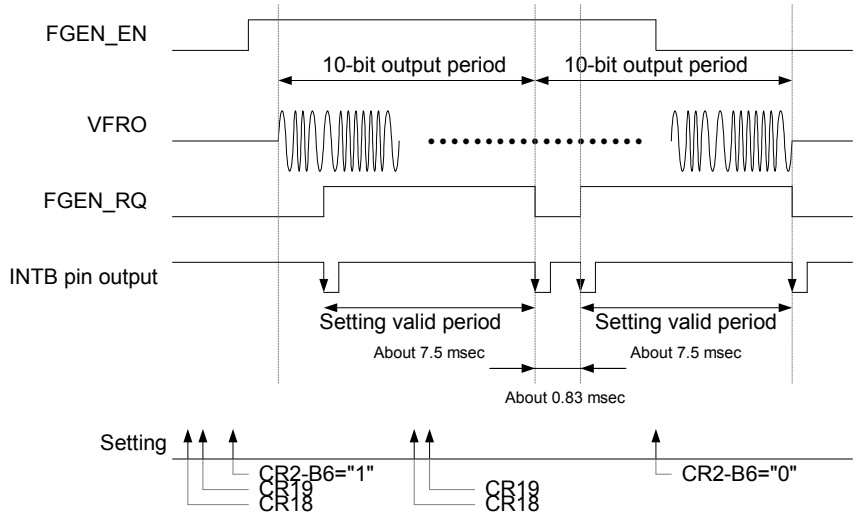


Fig. 34 FSK data transmit and stop timings (when transmitting 20 bits)

Note:
When the FSK generator is operating, it is recommended to keep the other detector sections deactive so that they do not cause to generate an interrupt.

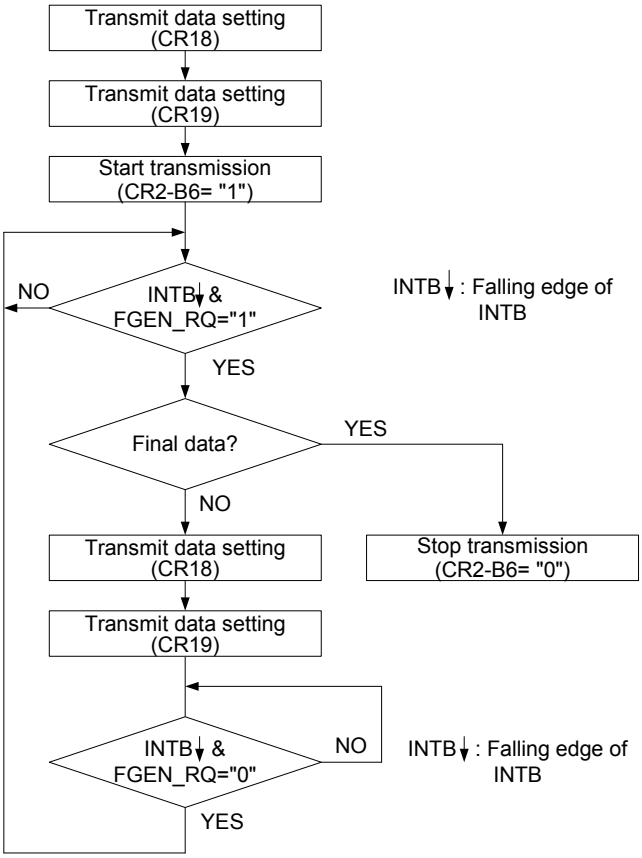


Fig. 35 FSK output control method

A. Internal data memory for FSK gain adjustment (FGEN_GAIN)
Address: 00E4h
Initial value: 0080h
The output level of the initial value will be –13.3 dBm0. Compute the setting value using the following equation when changing the output level.
Equation: 0080h × GAIN
Example: For decreasing the output level by 6 dB.
0080h × 0.5 = 0040h
Upper limit: 40 dB higher (data: 3200h)
Lower limit: 40 dB lower (data: 0001h)

Notice:
The maximum amplitude should not exceed 1.3Vp-p.

TONE_DET0 Detector

The TONE_DET0 detector detects a 1650 Hz single tone signal input from AIN0 and AIN1. This detector becomes effective when the control register TDET0_EN (CR3-B3) is "1". When the tone is detected, the control register TONE0_DET (CR3-B3) will be set to "1". TONE0_DET will become "0" when the tone is not detected or when TDET0_EN is "0". The tone detect timing is shown in Fig. 36.
The tone detector is composed of a detector section, an ON guard timer, and an OFF guard timer. The detect time and the detect level can be adjusted. The initial values of both ON and OFF guard timers are 5 ms. The initial value of the detect level is –5.3 dBm0.

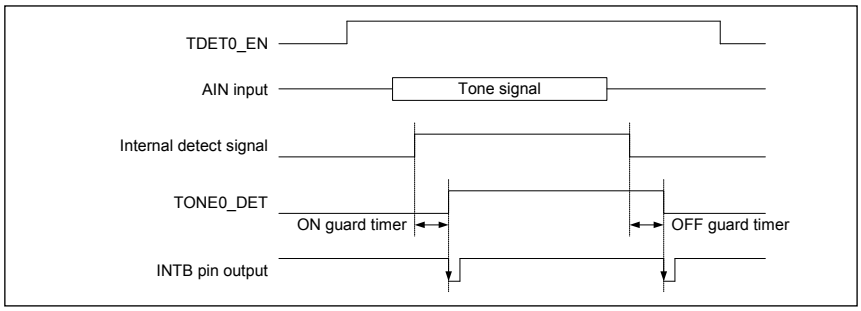


Fig. 36 Tone detect timing

A. Internal data memory for control of the detect level (TDET0_TH)
Address: 0040h
Initial value: 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detect level X.
Equation: $10^{((X-3.17)/20)} \times 2/\pi \times 32768$
Example: Detect level of –5.3 dBm0.
$10^{((-5.3-3.17)/20)} \times 2/\pi \times 32768 = 7857d = 1EBBh$

Upper limit	:3.17 dBm0	(data: 517Ch)
	: –5.3 dBm0	(data: 1EBBh)
Lower limit	: –83.22 dBm0	(data: 0001h)

B. Internal data memory for the ON guard timer (TDET0_ON_TM)
Address: 0041h
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

C. Internal data memory for the OFF guard timer (TDET0_OFF_TM)
Address: 0042h
Initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

D. Internal data memory for controlling the detect frequency (TDET0_FREQ)
Address: ----h, initial value: —
The detect frequency can be changed. Contact ROHM's responsible sales person when you wish to change the detect frequency.

TONE_DET1 Detector

The TONE_DET1 detector detects a 2100 Hz single tone signal input from AIN. This detector becomes effective when the control register TDET1_EN (CR2-B4) is "1". When the tone is detected, the control register TONE1_DET (CR3-B4) will be set to "1". TONE1_DET will become "0" when the tone is not detected or when TDET1_EN is "0". The tone detect timing is shown in Fig. 37.
The tone detector is composed of a detector section, an ON guard timer, and an OFF guard timer. The detect time and the detect level can be adjusted. The initial values of both ON and OFF guard timers are 5 ms. The initial value of the detect level is –5.3 dBm0.

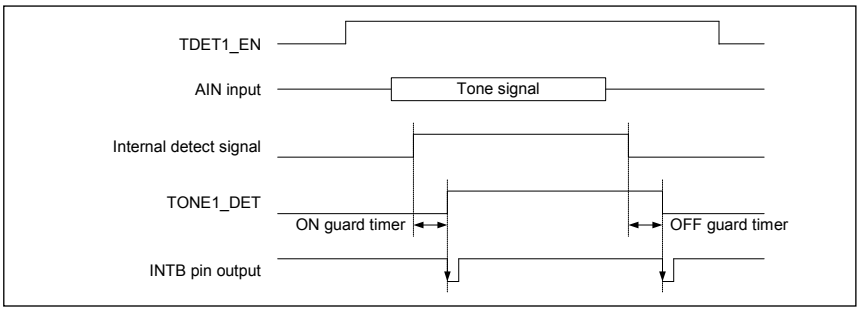


Fig. 37 Tone detect timing

A. Internal data memory for control of the detect level (TDET1_TH)
Address: 0052h, initial value: 1EBBh (–5.3 dBm0)
Compute the setting value using the following equation when changing the detect level X.
Equation: $10^{((X-3.17)/20)} \times 2/\pi \times 32768$
Example: Detect level of -5.3 dBm0.
$10^{((-5.3-3.17)/20)} \times 2/\pi \times 32768 = 7857d = 1EBBh$

Upper limit	: 3.17 dBm0	(data: 517Ch)
	: –5.3 dBm0	(data: 1EBBh)
Lower limit	: –83.22 dBm0	(data: 0001h)

B. Internal data memory for the ON guard timer (TDET1_ON_TM)
Address: 0053h, initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

C. Internal data memory for the OFF guard timer (TDET1_OFF_TM)
Address: 0054h, initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

D. Internal data memory for controlling the detect frequency
Address: ----h, initial value: —
The detect frequency can be changed. Contact ROHM's responsible sales person when you wish to change the detect frequency.

DTMF Detector

This section detects the DTMF signal input from AIN. The DTMF detector becomes effective when the control register DTMF_EN (CR2-B2) is "1", and when a valid DTMF signal is detected, DTMF_DET (CR4-B4) becomes "1" and the received code is stored in DTMF_0 to DTMF_3 (CR4-B3, 2, 1, 0).
When no DTMF signal is detected or when DTMF_EN is "0", DTMF_DET will be "0" and also DTMF_0 to DTMF_3 will be "0000". The DTMF detect timing is shown in Fig. 38.

The DTMF detector is composed of a detector section, an ON guard timer, and an OFF guard timer. The detect time and the detect level can be adjusted. The initial values of both ON and OFF guard timers are 20 ms. The initial value of the detect level is –37.0 dBm0.

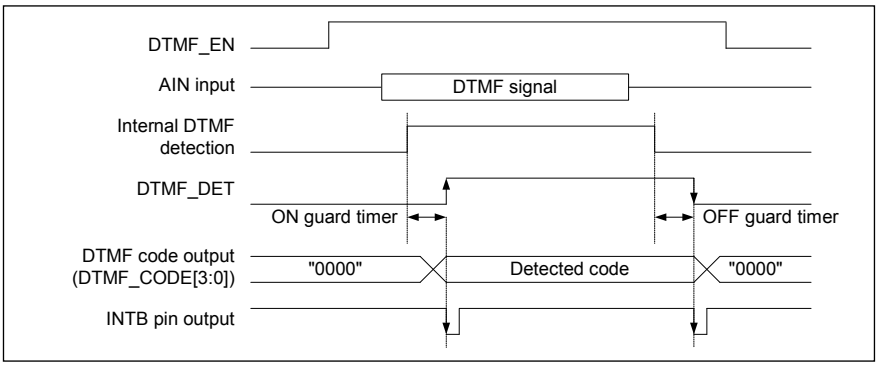


Fig. 38 DTMF detect timing

A. Internal data memory for gain adjustment (DTMF_TH)
Address: 005Ah, initial value: 1000h (–37.0 dBm0)
Compute the setting value using the following equation when changing the detect level.
Equation: 1000h × 1 / GAIN
Example: Increasing the detect level by 6 dB.
1000h × 0.5 = 0800h
Upper limit : 12 dB higher (data: 0400h)
Lower limit : 12 dB lower (data: 4000h)

B. Internal data memory for the ON guard timer (DTMF_ON_TM)
Address: 00BFh, initial value: 00A0h (20 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h
Upper limit : 4095.875 ms (data: 7FFFh)
: 5 ms (data: 0028h)
Lower limit : 0.125 ms (data: 0001h)

C. Internal data memory for the OFF guard timer (DTMF_OFF_TM)
Address: 00C1h, initial value: 00A0h (20 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

Notice:
During DTMF signal detection, if the DTMF signal changes to another code successively, the received code changes and an interrupt can be generated with DTMF_DET in the “1” state.

Echo Canceller

The block diagram of the echo canceller is shown in Fig. 39.
The echo canceller has a delay time of 32 ms and is activated by setting a "1" in EC_EN (CR2-B1). The operation setting of the echo canceller is done mainly using the internal data memory locations EC_CR and GLPAD_CR.

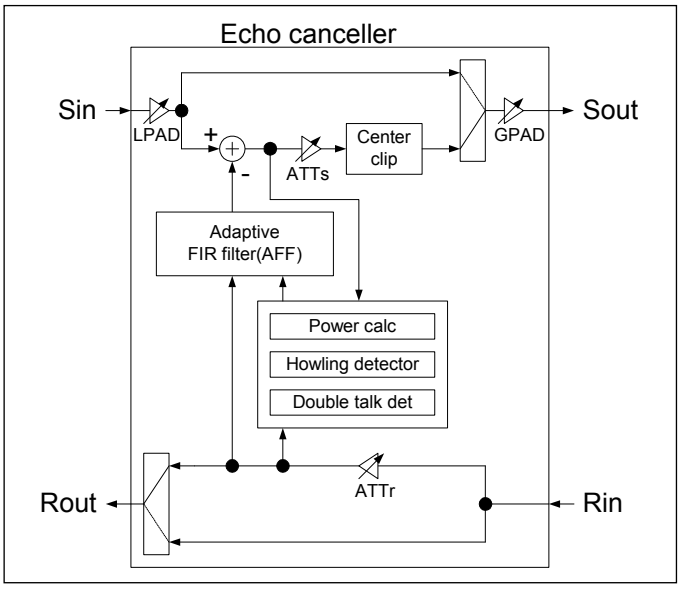


Fig. 39 Echo canceller block diagram

A. Echo canceller control (EC_CR)
Address: 0171h, initial value: 0012h
Write "0" in the higher order 8 bits (B15 to B8)

	B7	B6	B5	B4	B3	B2	B1	B0
	THR	—	HLD	HDB	CLP	—	ATTB	—
Initial value	0	0	0	1	0	0	1	0

B7: Through mode control
1: Through mode
0: Normal mode (echo cancel operation)
When this through mode control bit of the echo canceller is set, the data of Rin and Sin are output directly to Rout and Sout while retaining their respective echo coefficients. Further, during the through mode, the HLD, HDB, ATTB and CLP functions are disabled.

B6: Reserved bit. Prohibited to change the initial value.

B5: Coefficient update control
1: Coefficient fixed
0: Coefficient updated
This bit selects the presence or absence of updating of the adaptive FIR filter (AFF) coefficient of the echo canceller. This function becomes valid when THR is in the normal mode.

B4: Howling detector control
1: OFF
0: ON
This bit controls the function of detecting and removing howling which is generated in a hands-free acoustic system, etc. This function becomes valid when THR is in the normal mode.

B3: Center clip control
1: ON
0: OFF
This bit controls the center clip function in which the Sout output is forcibly fixed to the minimum positive value when the Sout output of the echo canceller is –57 dBm0 or less. This function becomes valid when THR is in the normal mode.

B2: Reserved bit. Prohibited to change the initial value.

B1: Attenuator control
1: ATT OFF
0: ATT ON
This bit selects the switching ON/OFF of the ATT function which prevents howling using the attenuators ATTs and ATTr provided at the Rin input and Sout output of the echo canceller. When only the Rin input is present, the attenuator (ATTs) of Sout will be inserted. When only the Sin input is present or when both the Sin and Rin inputs are present, the attenuator (ATTr) of Rin will be inserted. The respective attenuation values are 6 dB. This function becomes valid when THR is in the normal mode.

B0: Reserved bit. Prohibited to change the initial value.

B. GLPAD control (GLPAD_CR)
Address: 0172h, initial value: 000Fh
This data memory controls the GLPAD within the echo canceller. Write "0" in the higher order 8 bits (B15 to B8).

	B7	B6	B5	B4	B3	B2	B1	B0
	—	—	—	—	GPAD2	GPAD1	LPAD2	LPAD1
Initial value	0	0	0	0	1	1	1	1

B7, 6, 5, 4: Reserved bits. Prohibited to change the initial values.

B3, 2: Output level control
These bits control the GPAD level for the echo canceller output gain.
(0, 1): +18 dB
(0, 0): +12 dB
(1, 1): +6 dB
(1, 0): 0 dB

B1, 0: Input level control
These bits control the LPAD level for the echo canceller input loss.
(0, 1): –18 dB
(0, 0): –12 dB
(1, 1): –6 dB
(1, 0): 0 dB

C. Precautions in using the Echo Canceller

C-1
In the echo path, make sure that the echo signal does not cause saturation, waveform distortion, etc., in the external amplifier, etc. The echo attenuation becomes poor if any saturation or waveform distortion occur.

C-2
Make the settings so that the echo return loss (E.R.L.) is attenuating. Further, it is recommended to use the GLPAD function if the E.R.L. is set to be amplified. The echo attenuation gets deteriorated seriously if the E.R.L. is set to be amplified.
The E.R.L. is the attenuation (loss) of echo amount from the echo canceller output (Rout) to the echo canceller input (Sin).

C-3
When the echo path can change (such as during a reconnected call), it is recommended to carry out a reset using EC_EN (CR2-B1), PDNB, or SPDN (CR0-B7).

Dial Pulse Detector (DPDET)

Dial pulse signals input at the general-purpose input pin GPI0 are detected by this DPDET. The dial pulse detector becomes effective when the control register bit DPDET_EN (CR10-B6) is "1". DP_DET (CR4-B6) becomes "1" when a dial pulse signal is detected and the detected number of dial pulses is stored in DPDET_CODE. The number of dial pulses detected should be read out from DPDET_CODE at the time when DP_DET goes from "1" to "0".

When a dial pulse signal is not detected, or when DPDET_EN is "0", DP_DET will remain "0".

The dial pulse detect timing is shown in Fig. 40. The dial pulse detector samples the dial pulse signal input at GPI0 at 8 kHz sampling rate, and detects the dial pulses based on the settings of the ON guard timer (DPDET_ON_TIM) and OFF guard timer (DPDET_OFF_TIM). Further, it is possible to adjust the detect end time by setting the detect end timer (DPDET_DETOFF_TIM).

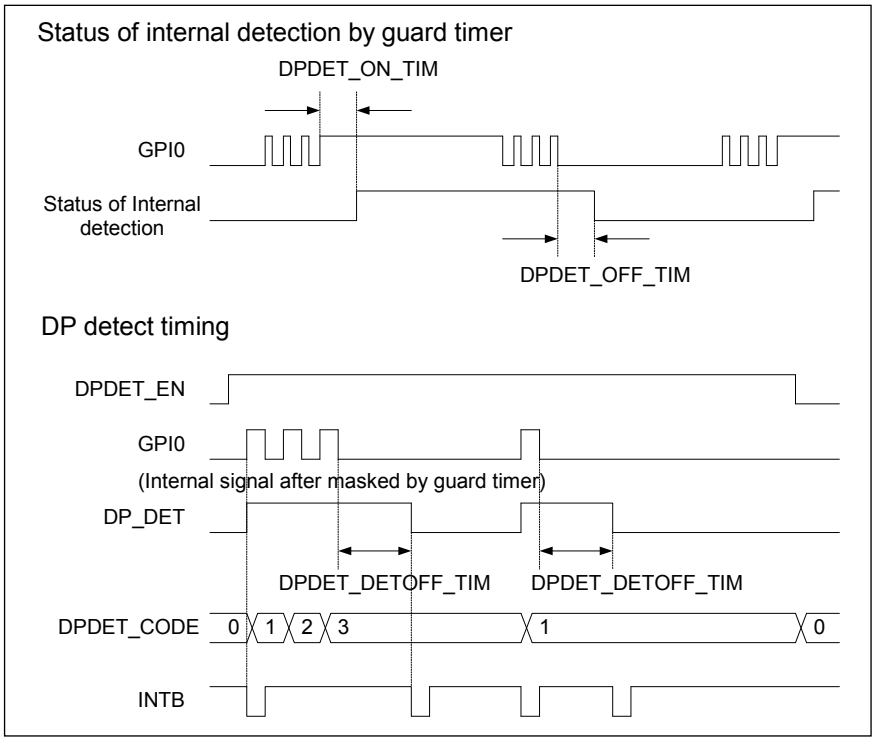


Fig. 40 Dial pulse detect timing

A. Dial pulse detect control register (DPDET_EN CR10-B6)
   0: Dial pulse detection stopped
   1: Dial pulse detection active

B. Dial pulse detector detect status register (DP_DET CR4-B6)
   0: Dial pulses not detected
   1: Dial pulses detected

   This bit is set to "1" after DPDET_EN has been set when an edge at GPI0 is detected. Further, if no edge is detected for a period set in DPDET_DETOFF_TIM after an edge detection, this bit will be cleared automatically to "0".

C. Internal data memory for ON guard timer (DPDET_ON_TIM)
Address: 011Bh, initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

D. Internal data memory for OFF guard timer (DPDET_OFF_TIM)
Address: 011Ch, initial value: 0028h (5 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 5 ms
5/0.125 = 40d = 0028h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 5 ms	(data: 0028h)
Lower limit	: 0.125 ms	(data: 0001h)

E. Internal data memory for polarity control (DPDET_POL)
Address: 122Eh, initial value: 0000h (no polarity reversal)
Controls the polarity of the input from GPI0.
0000h: No polarity reversal
0001h: Polarity reversal present

F. Internal data memory for detect end control (DPDET_DETOFF_TIM)
Address: 122Fh, initial value: 03E8h (125 ms)
Use the following equation when changing the timer value.
Equation: Guard timer value in ms/0.125 ms
Example: 125 ms
125/0.125 = 1000d = 03E8h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 125 ms	(data: 03E8h)
Lower limit	: 0.125 ms	(data: 0001h)

G. Internal data memory for indicating number of detected pulses (DPDET_CODE)
Address: 1231h, initial value: 0000h (not-detected state)
Indicates the number of detected pulses.
This internal data memory for indication is updated when an edge is detected.

Notice:
Ignore the interrupt occurred after the time set by the ON guard timer if the DPDET is activated under the following conditions:

- DPDET_POL = “0”, GPI0 = “1”
- DPDET_POL = “1”, GPI0 = “1” or “0”

Dial Pulse Transmitter (DPGEN)

The dial pulse transmitter outputs a dial pulse signal at the general-purpose output pin GPO0. The dial pulse generation will be effective when the control memory bit DPGEN_EN is "1", and a dial pulse signal is output with the number of pulses set in DPGEN_DATA.

The dial pulse output timing is shown in Fig. 41. The speed (rate) of dial pulses can be selected to be 10PPS or 20PPS by setting DPGEN_PPS accordingly. Further, it is possible to adjust the make ratio by setting the HIGH duration of the output pulses using DPGEN_DUTY.

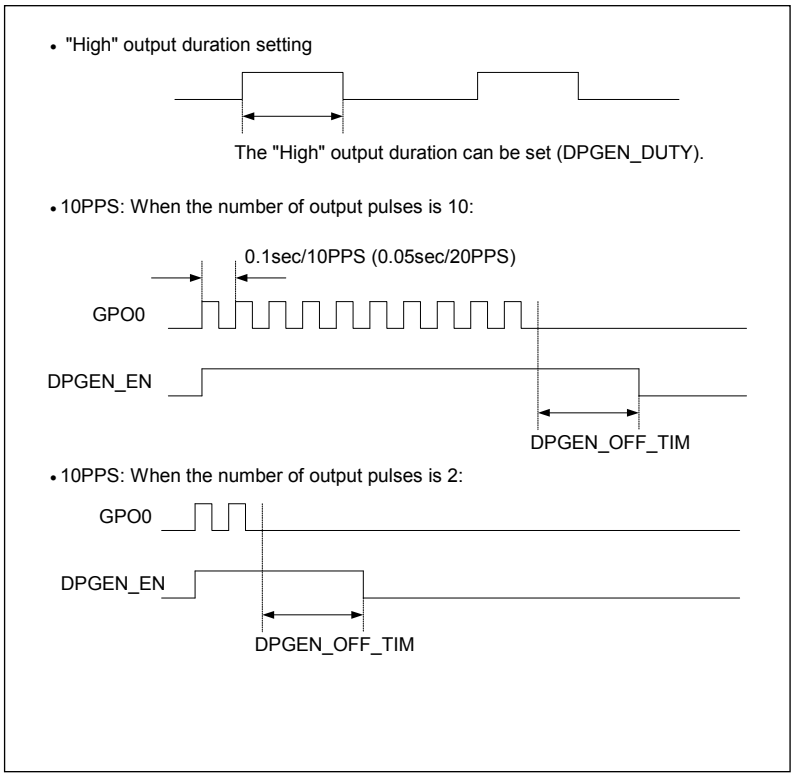


Fig. 41 Dial pulse output timing

A. Internal data memory for dial pulse transmit control (DPGEN_EN)
Address: 1220h, initial value: 0000h
The dial pulses are transmitted when a "0001h" is written in this data memory.
This data memory will be cleared automatically after a period of time set in DPGEN_OFF_TIM.
0000h: Dial pulse output stopped
0001h: Dial pulse output active

Notice:
Start DPGEN only when CR17-B0 (GPO0) is in the "0" state.

B. Internal data memory for setting the number of pulses (DPGEN_DATA)
Address: 1221h, initial value: 0000h
Upper limit: 10 (data: 000Ah)
Lower limit: 1 (data: 0001h)

C. Internal data memory for dial pulse rate control (DPGEN_PPS)
Address: 1222h, initial value: 0000h
0000h: 10 PPS
0001h: 20 PPS

D. Internal data memory for setting "High" output duration (DPGEN_DUTY)
Address: 1223h, initial value: 0108h (33 ms/10 PPS, 16.5 ms/20 PPS)
Use the following equation when setting the "High" duration.
The value will be half this set value in the case of 20 PPS.
Equation: "High" output time duration in ms/0.125 ms
Example: 33 ms
33/0.125 = 264d = 0108h

Upper limit	: 100 ms	(data: 0320h)
	: 33 ms	(data: 0108h)
Lower limit	: 0.125 ms	(data: 0001h)

E. Internal data memory for end of output control (DPGEN_OFF_TIM)
Address: 1225h, initial value: 03E8h (125 ms)
Use the following equation when setting the end of output control.
Equation: End of output time duration in ms/0.125 ms
Example: 125 ms
125/0.125 = 1000d = 03E8h

Upper limit	: 4095.875 ms	(data: 7FFFh)
	: 125 ms	(data: 03E8h)
Lower limit	: 0 ms	(data: 0000h)

Timer (TIMER)

This is a 16-bit up-counter timer. When a "0001h" is set in the internal memory for timer control (TIM_EN), the timer starts counting up the timer count (TIM_COUNT) at every 125 μsec. When the timer count value becomes equal to the timer data value, the timer counter value will be reset to "0000h" and the timer starts counting up again.

A. Internal data memory for timer control (TIM_EN)
Address: 1218h, initial value: 0000h
The timer starts counting up when "0001h" is written in this data memory location.
When a "0000h" is set here, the counting up will be stopped and the counter value will be cleared.
0000h: Stops counting
0001h: Starts counting

B. Internal data memory for timer count indication (TIM_COUNT)
Address: 1219h, initial value: 0000h

C. Internal data memory for timer data (TIM_DATA)
Address: 121Ah, initial value: FFFFh
Upper limit : 8192 ms (data: FFFFh)
Lower limit : 0.250 ms (data: 0001h)

Outband Control (OUTBAND_CONTROL)
This is a function is automatically to mute or to write silence data in Tx buffer when corresponding detection bit (***_DET) gets "1". Either to mute or to write silence data in Tx buffer differs among speech codec's as shown below;

G.711 (μ-/A-law)	Mutes speech data given to codec
G.726	Mutes speech data given to codec
G.729.A	Writes silence data (80 bits) in Tx buffer The 80 bits meaning silence in G.729.A to write in Tx buffer as default could be altered any 80 bits you like in the initial mode.

Address : 1307h, Initial value : 0000h

	B7	B6	B5	B4	B3	B2	B1	B0
	-	-	-	-	-	TDET1_OB_EN	TDET0_OB_EN	DTMFDET_OB_EN
Initial Value	0	0	0	0	0	0	0	0

B7, 6, 5, 4, 3 : Reserved bits
B2 : TDET1_OUTBAND_EN control
1 : ON (Mutes speech data given to codec when TDET1_DET is "1")
0 : OFF
B1 : TDET0_OUTBAND_EN control
1 : ON (Mutes speech data given to codec when TDET0_DET is "1")
0 : OFF
B0 : DTMFDET_OUTBAND_EN control
1 : ON (Writes data specified by OUTBAND_G729_DAT which is silence as default when DTMF_DET is "1")
0 : OFF

- Leak time of tones to Tx buffer
  A referential equation for leak time of tones to Tx buffer with each speech codec is shown below;

G.711/G.726	0ms + A + B
G.729.A	-10ms to -20ms + A + B * -10ms to -20ms by prediction and framing process

A : detection delay time of a given detector (ms)
Depends upon input level, frequency, etc..
B : ON-guard timer time of a given detector

< Example>

G.711 / G.726	30ms (A) + 20m s (B) = approx. 50ms
G.729	(-10ms to -20ms) + 20ms (A) + 20ms (B) = approx. 30ms to 40ms

Outband G.729.A data (OUTBAND_G729_DAT)
When outband control is made in G.729.A mode, the data in the addresses below are written into Tx buffer when corresponding detection bit (***_DET) gets "1". The data to write into Tx buffer could be altered in the initial mode.

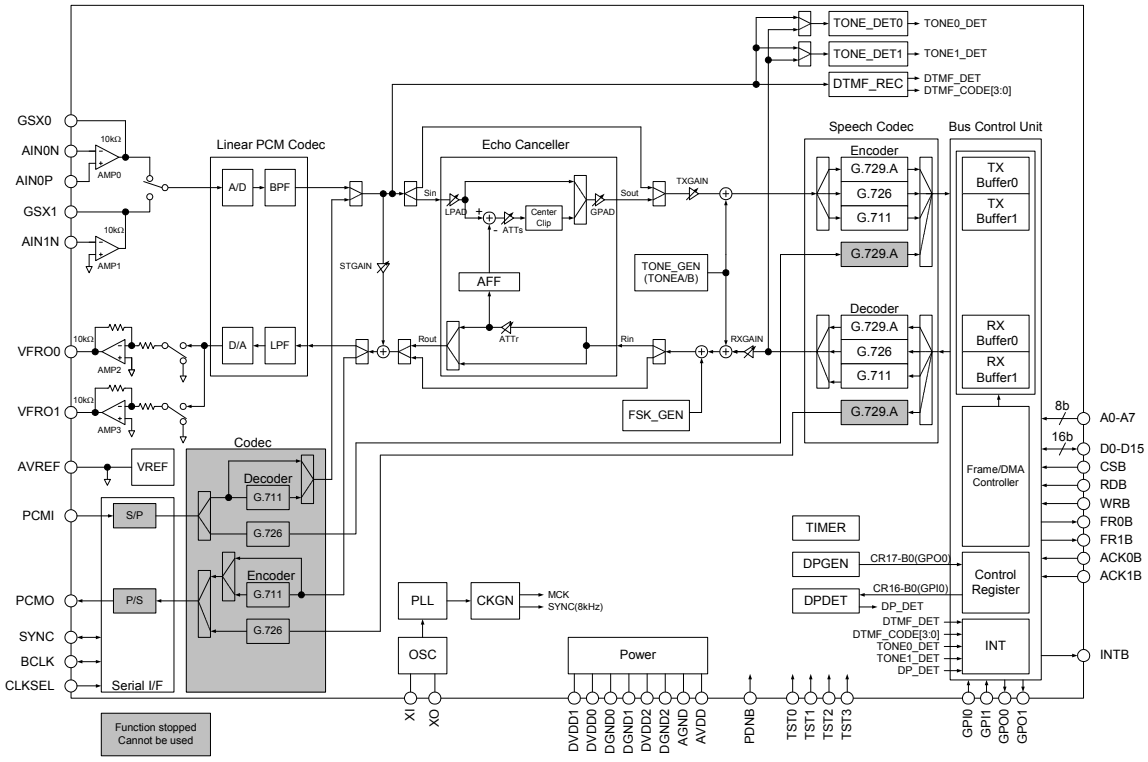
Address	: 016Ch	016Dh	016Eh	016Fh	0170h
Initial value	: 7852h	80A0h	00FAh	C200h	07D6h

LSI Code Indication (ML7074_VERSION)
The code ML7074-003 is indicated here.

Address: 0152h, initial value: 0002h

EXAMPLE OF CONFIGURATION

Analog I/F mode



Example of settings in the initialization mode

· CR15 = 40h * This is mandatory.

· CR6=01h,CR7=16h,CR8=00h,CR9=01h,CR1=80h (Address : 0116h, Data : 0001h)

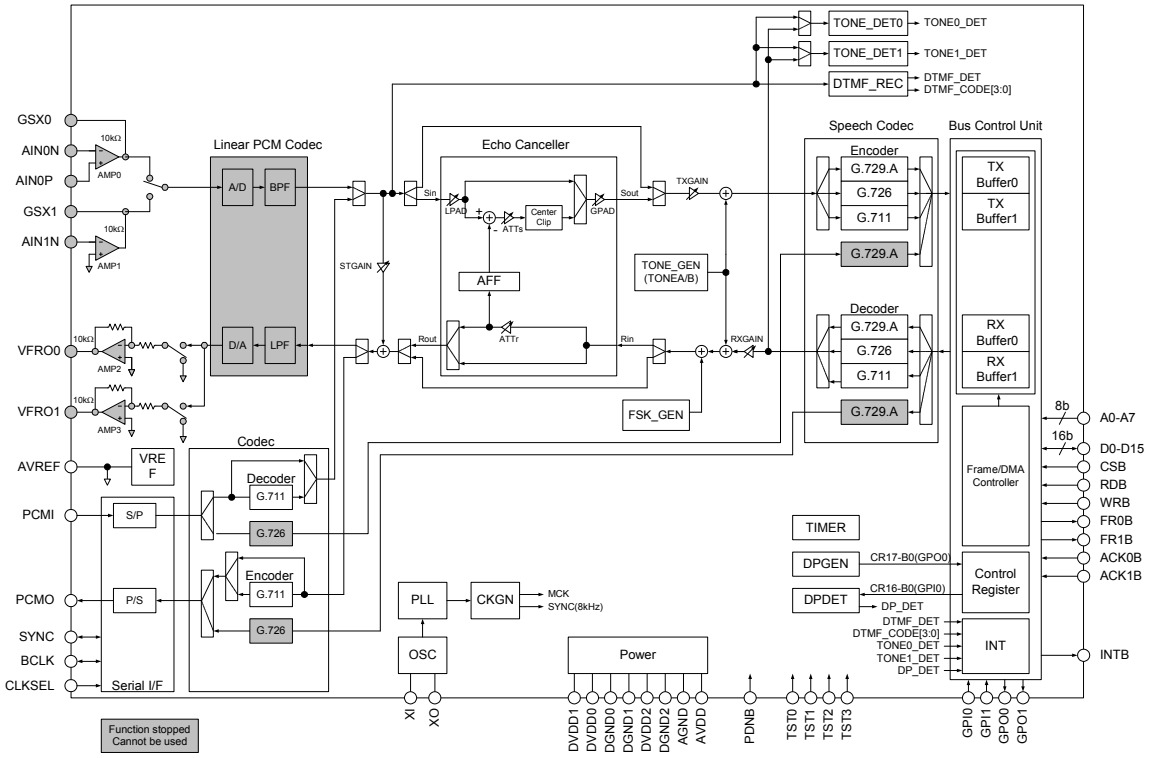
* This is mandatory. As for how to set them, refer to Method of Accessing and Controlling Internal Data Memory.

· CR11 = 00h (Frame/10 ms/16B/Speech CODEC = G.729.A)

· Various settings

· CR0 = 09h (OPE_STAT = “1”)

PCM I/F Mode



Examples of settings in the initialization mode

· CR15 = 40h * This is mandatory.

· CR6=01h,CR7=16h,CR8=00h,CR9=01h,CR1=80h (Address : 0116h, Data : 0001h)

* This is mandatory. As for how to set them, refer to Method of Accessing and Controlling Internal Data Memory.·

· CR10 = 00h (VFRO1 = AVREF/VFRO0 = AVREF)

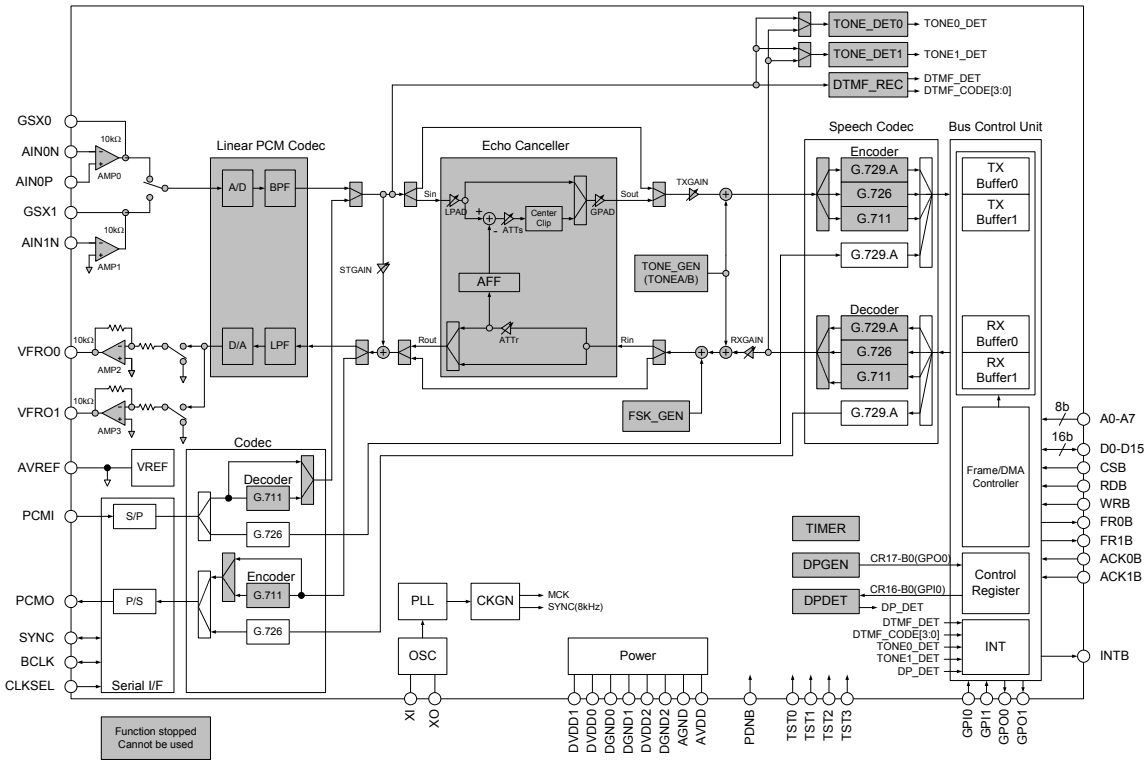
· CR11 = 00h (Frame/10 ms/16B/PCMIF = 16-bit linear)

· CR12 = 01h (Speech CODEC = G.729.A/PCMIF_EN = “1”)

· Various settings

· CR0 = 29h (AFE_EN = Power down/LONG/OPE_STAT = “1”)

G.729.A ↔ G.726 Mutual Conversion



Examples of settings in the initialization mode

· CR15 = 40h * This is mandatory.

· CR6=01h,CR7=16h,CR8=00h,CR9=01h,CR1=80h (Address : 0116h, Data : 0001h)

* This is mandatory. As for how to set them, refer to Method of Accessing and Controlling Internal Data Memory.

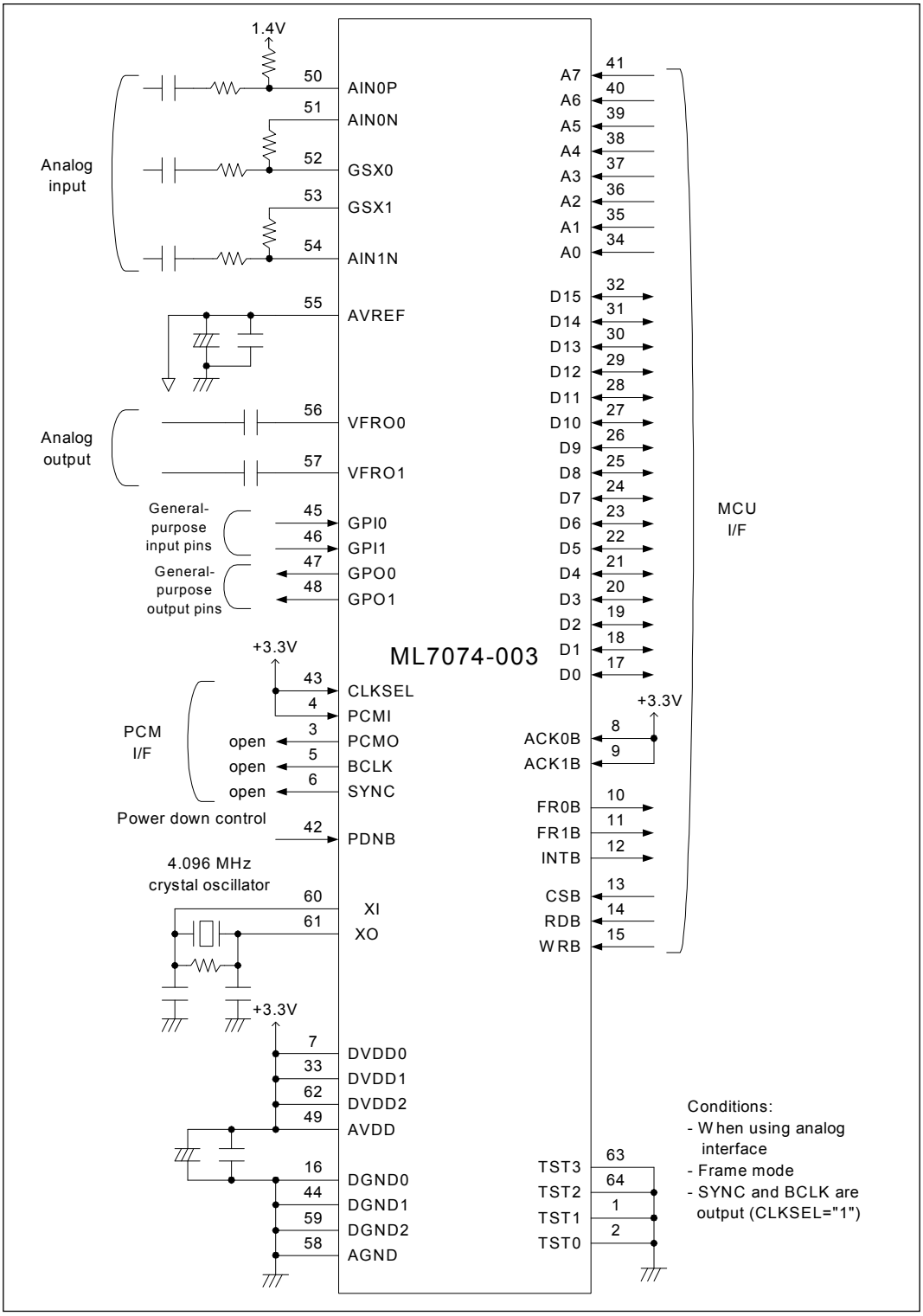
· CR11 = 05h (Frame/10 ms/16B/G.726/TRANS_EN= “1”)

· CR10 = 00h (VFRO1 = AVREF/VFRO0 = AVREF)

· Various settings

· CR0 = 29h (AFE_EN = Power down/LONG/OPE_STAT = “1”)

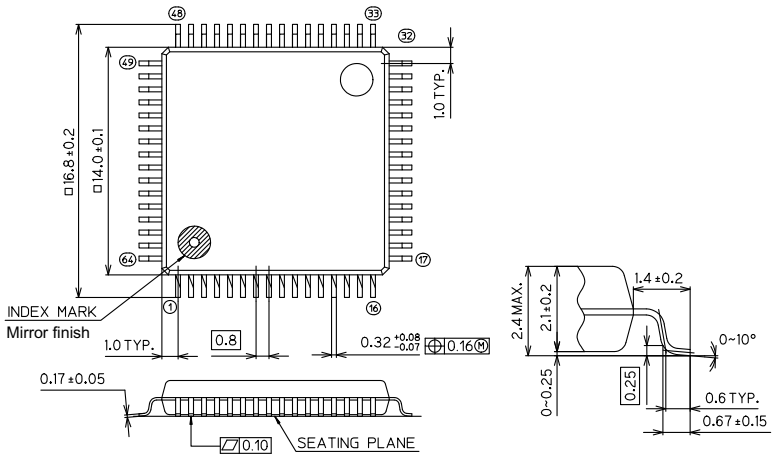
EXAMPLE OF APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit: mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	6/Feb. 23, 2001

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7074-003-01	Mar. 2, 2003	–	–	Final edition 1

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