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# ML610Q407/ML610Q408/ML61Q0409

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8-bit Microcontroller with a Built-in LCD driver

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## GENERAL DESCRIPTION

ML610Q407/ML610Q408/ML610Q409 is a high-performance 8-bit CMOS microcontroller into which peripheral circuits, such as synchronous serial port, UART, melody driver, RC oscillation type A/D converter, and LCD driver, are incorporated around LAPIS Semiconductor-original 8-bit CPU nX-U8/100. ML610Q407/ML610Q408/ML610Q409 operates in both high/low-speed mode and power-saving mode, it is most suitable for battery operated products.

The short TAT are entertained by offering MTP version ML610Q407(P)/ML610Q408(P)/ML610Q409(P). ML610Q407P/ML610Q408P/ML610Q409P support industrial temperature -40°C to +85°C, are added to the product lineup.

## FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function (MTP version only)
  - Minimum instruction execution time
    - 30.5  $\mu$ s (@32.768 kHz system clock)
    - 2 $\mu$ s (@500kHz system clock)
    - 0.5 $\mu$ s(@2MHz system clock)
- Internal memory
  - Internal 16KByte Flash ROM (8K $\times$ 16 bits) (including unusable 1K Byte TEST area)
  - Internal 1KByte Data RAM (1024 $\times$ 8 bits)
- Interrupt controller
  - 1 non-maskable interrupt sources
    - Internal source: 1 (Watch dog timer)
  - 27 maskable interrupt sources
    - Internal sources: 14 (SSIO0, SSIO1, Timer0, Timer1, Timer2, Timer3, UART0, Melody0, RC-A/D converter, PWM0, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    - External sources: 13 (P00, P01, P02, P03, P04, P50, P51, P52, P53, P54, P55, P56, P57)
    - (One interrupt request is generated from P50 to P57 interrupt sources.)
- Time base counter
  - Low-speed time base counter  $\times$ 1 channel
    - Frequency compensation (Compensation range: Approx. -488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter  $\times$ 1 channel
- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)
- Timers
  - 8 bits  $\times$  4 channels (Timer0-3: 16-bit  $\times$  2 configuration available by using Timer0-1 or Timer2-3)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- Capture
  - Time base capture × 2 channels (4096 Hz to 32 Hz)
- PWM
  - Resolution 16 bits × 1 channel
- Synchronous serial port
  - Master/slave selectable × 2 channel
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable
- UART
  - Half-Duplex Communication
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator
- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)
- RC oscillation type A/D converter
  - 16-bit counter
  - Time division × 2 channels
- General-purpose ports
  - Input-only port × 5 channels (including secondary functions)
  - Output-only port
    - ML610Q407: × 12 channels (including secondary functions)
    - ML610Q408: × 8 channels (including secondary functions)
    - ML610Q409: × 4 channels (including secondary functions)
  - Input/output port × 22 channels (including secondary functions)
- LCD driver
  - The number of segments
    - ML610Q407: 145 dots max. (29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable)
    - ML610Q408: 165 dots max. (33seg×5com, 34seg×4com, 35seg×3com, and 36seg×2com selectable)
    - ML610Q409: 185 dots max. (37seg×5com, 38seg×4com, 39seg×3com, and 40seg×2com selectable)
  - 1/1 to 1/5 duty
  - 1/2, 1/3 bias (built-in bias generation circuit)
  - Frame frequency selectable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function
- Reset
  - Reset through the RESET\_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow
- Clock
  - Low-speed clock: Crystal oscillation (32.768 kHz)  
(This LSI can not guarantee the operation without low-speed crystal oscillation clock)

- High-speed clock: Built-in RC oscillation (500 kHz, 2MHz)
  - Power management
    - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
    - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
    - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
    - Block Control Function: Resets and completely turns circuits of unused peripherals off.
  - Shipment
    - Chip
      - ML610Q407-xxxWA
      - ML610Q408-xxxWA
      - ML610Q409-xxxWA
      - ML610Q407D-xxxWA
      - ML610Q408D-xxxWA
      - ML610Q409D-xxxWA
      - ML610Q407P-xxxWA
      - ML610Q408P-xxxWA
      - ML610Q409P-xxxWA
      - ML610Q407PD-xxxWA
      - ML610Q408PD-xxxWA
      - ML610Q409PD-xxxWA
    - 100-pin plastic TQFP
      - ML610Q407-xxxTBZ03A
      - ML610Q408-xxxTBZ03A
      - ML610Q409-xxxTBZ03A
      - ML610Q407D-xxxTBZ03A
      - ML610Q408D-xxxTBZ03A
      - ML610Q409D-xxxTBZ03A
      - ML610Q407P-xxxTBZ03A
      - ML610Q408P-xxxTBZ03A
      - ML610Q409P-xxxTBZ03A
      - ML610Q407PD-xxxTBZ03A
      - ML610Q408PD-xxxTBZ03A
      - ML610Q409PD-xxxTBZ03A
- xxx: ROM code number (xxx is NNN for blank product)  
 Q: MTP version  
 P: Wide range temperature version  
 D: LCD 1/2 bias waveform alternative version (D version, See the LCD driver section of the user's manual in detail)  
 WA: Chip  
 TBZ03A: TQFP
- Guaranteed operating range
    - Operating temperature:  $-20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  (P version:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
    - Operating voltage:  $V_{\text{DD}} = 1.25\text{V}$  to  $3.6\text{V}$

**BLOCK DIAGRAM**

**ML610Q407/ML610Q408/ML610Q409 Block Diagram**

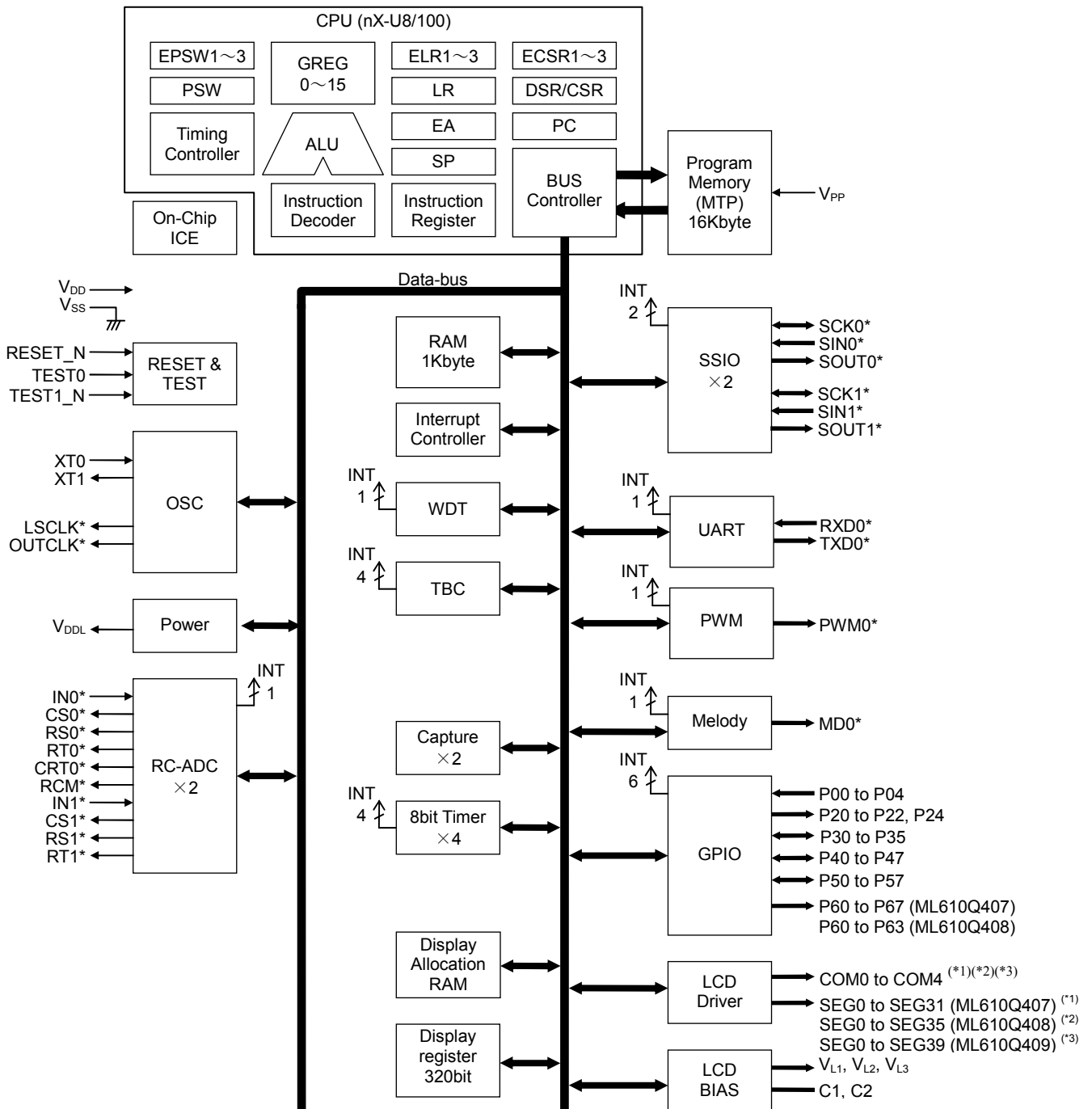
Figure 1 show the block diagram of the ML610Q407/ML610Q408/ML610Q409.

“\*” indicates the secondary function of each port.

“(1)”: 29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable

“(2)”: 33seg×5com, 34seg×4com, 35seg×3com, and 36seg×2com selectable

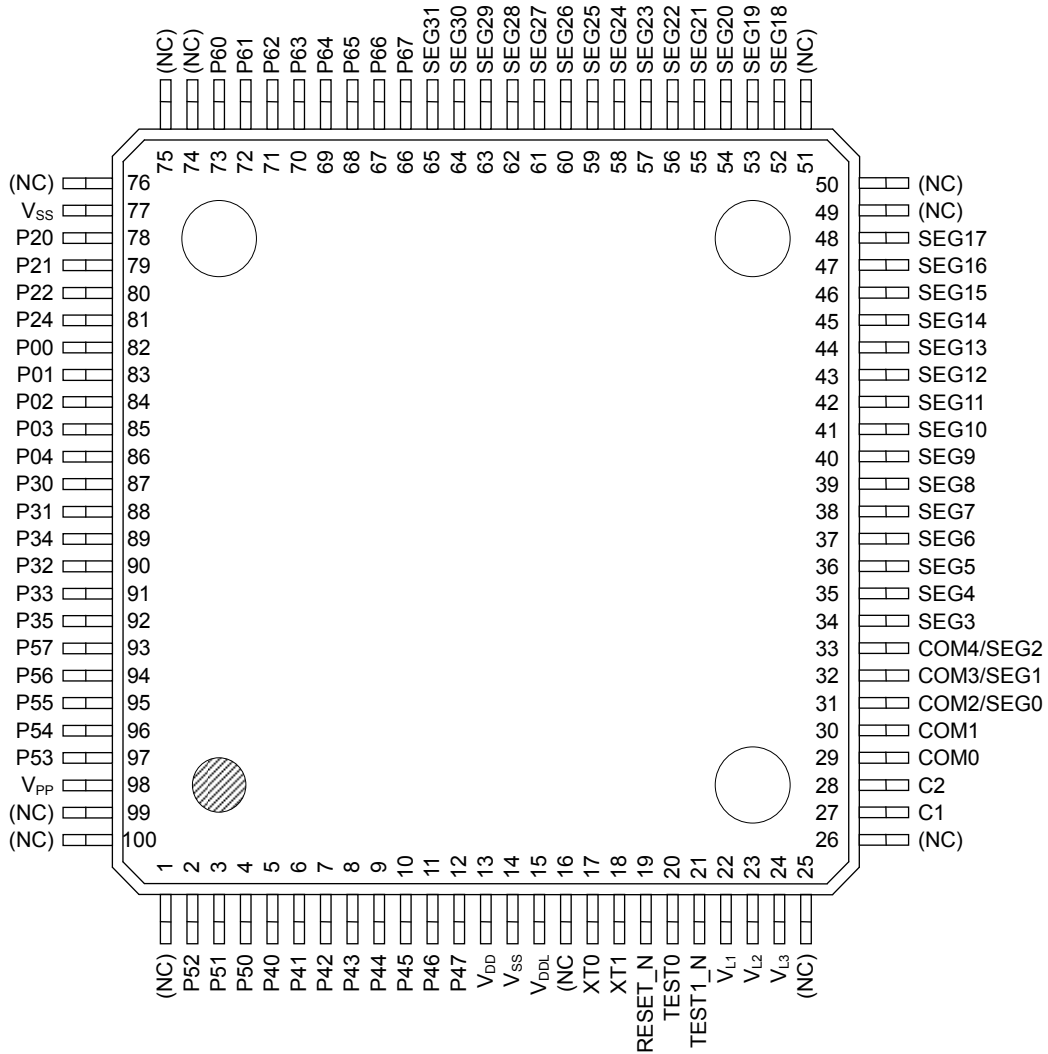
“(3)”: 37seg×5com, 38seg×4com, 39seg×3com, and 40seg×2com selectable



**Figure 1 ML610Q407/ML610Q408/ML610Q409 Block Diagram**

PIN CONFIGURATION

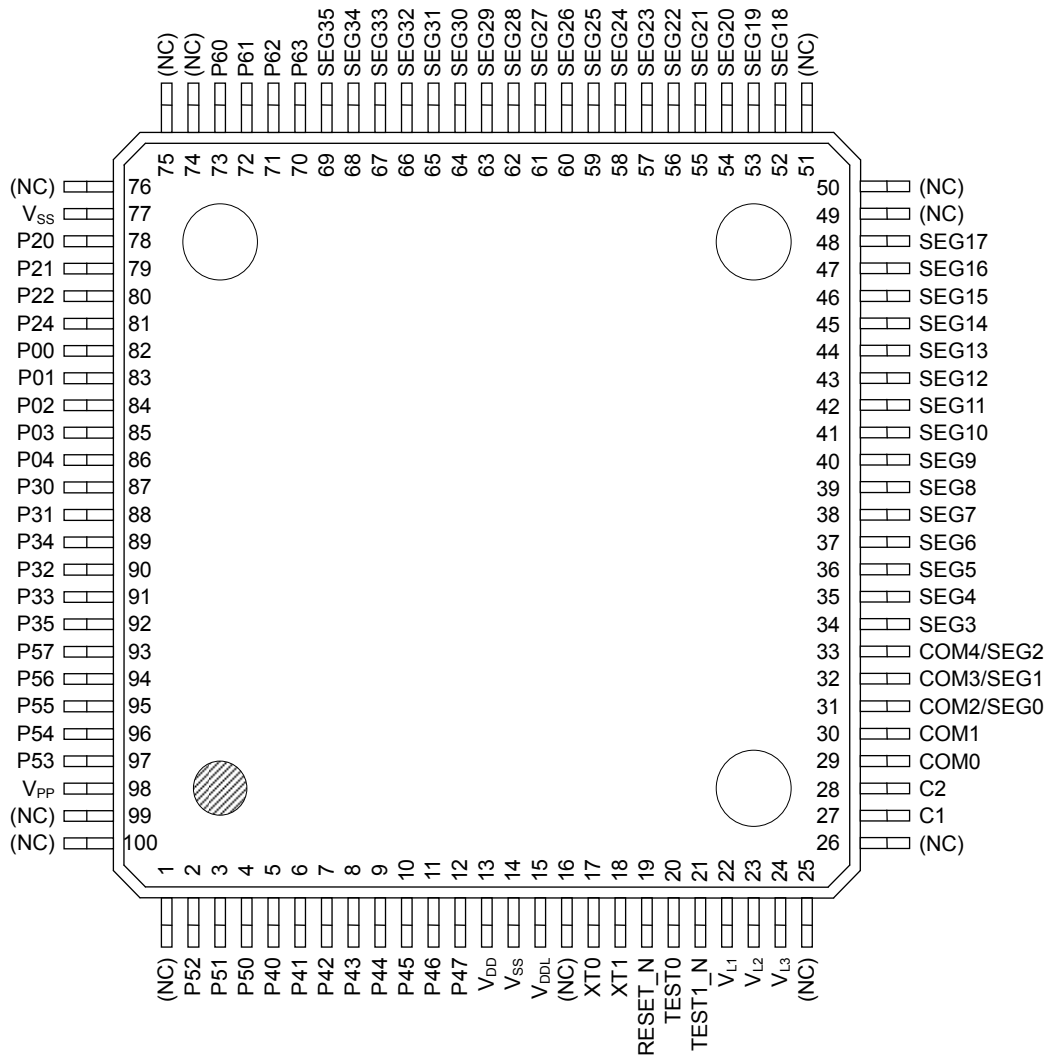
ML610Q407 TQFP100 Pin Layout



Note:  
The assignment of the P30 to P35 are not in order.

Figure 2 ML610Q407 TQFP100 Pin Configuration

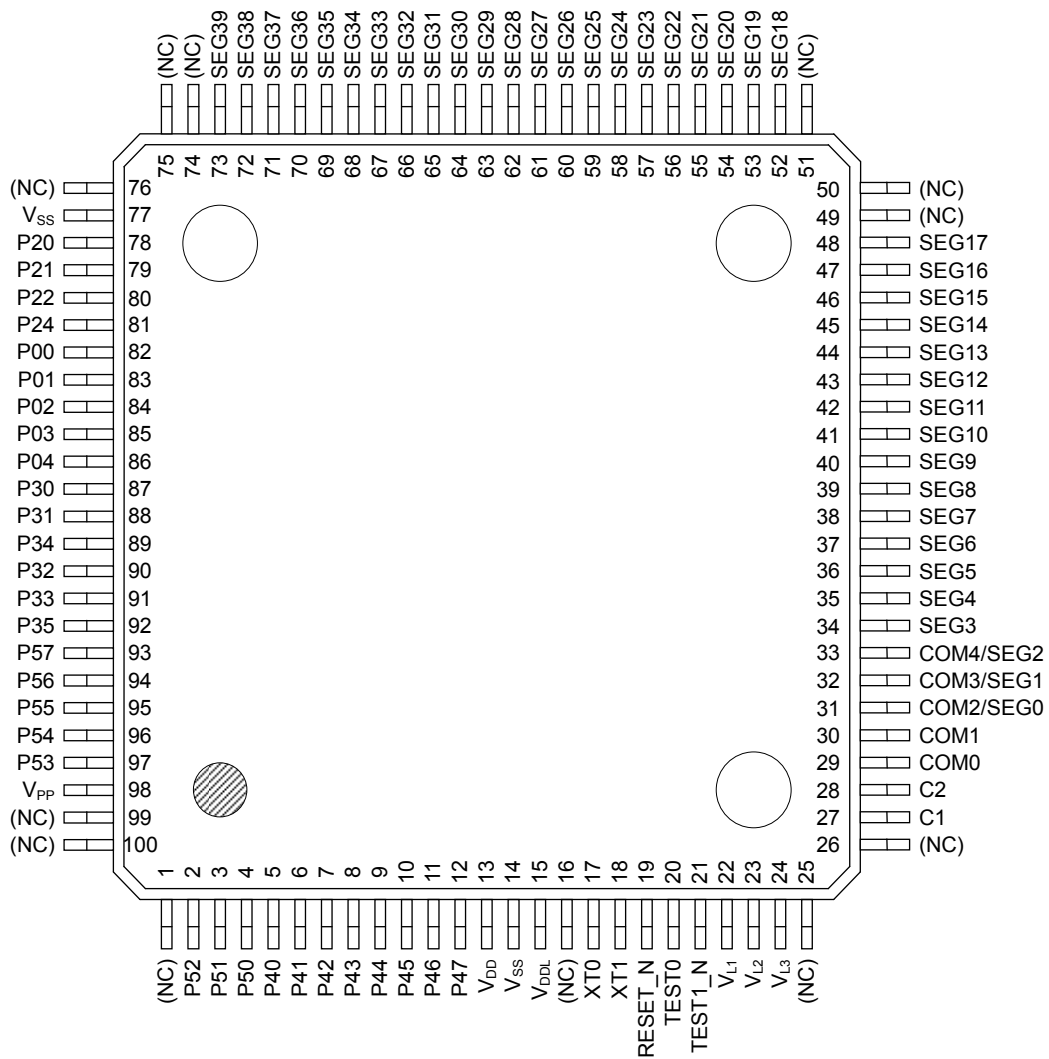
ML610Q408 TQFP100 Pin Layout



Note:  
The assignment of the P30 to P35 are not in order.

Figure 3 ML610Q408 TQFP100 Pin Configuration

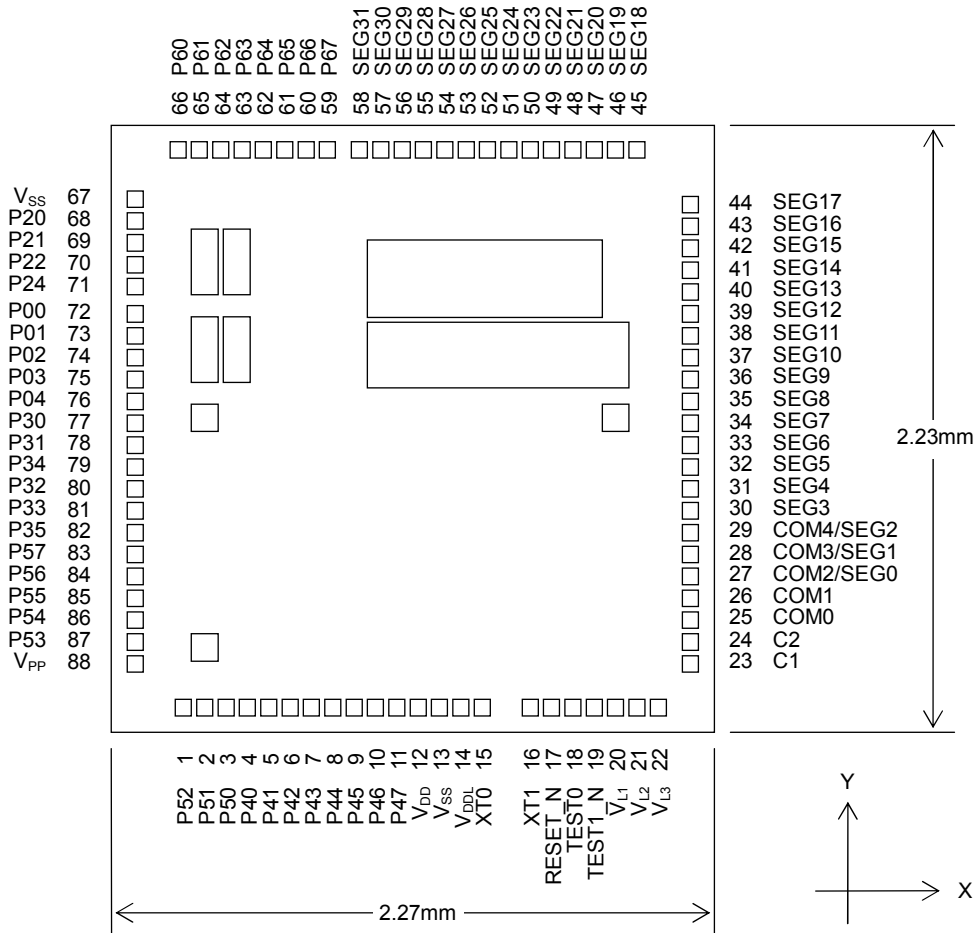
ML610Q409 TQFP100 Pin Layout



Note:  
The assignment of the P30 to P35 are not in order.

Figure 4 ML610Q409 TQFP100 Pin Configuration

**ML610Q407 Chip Pin Layout & Dimension**

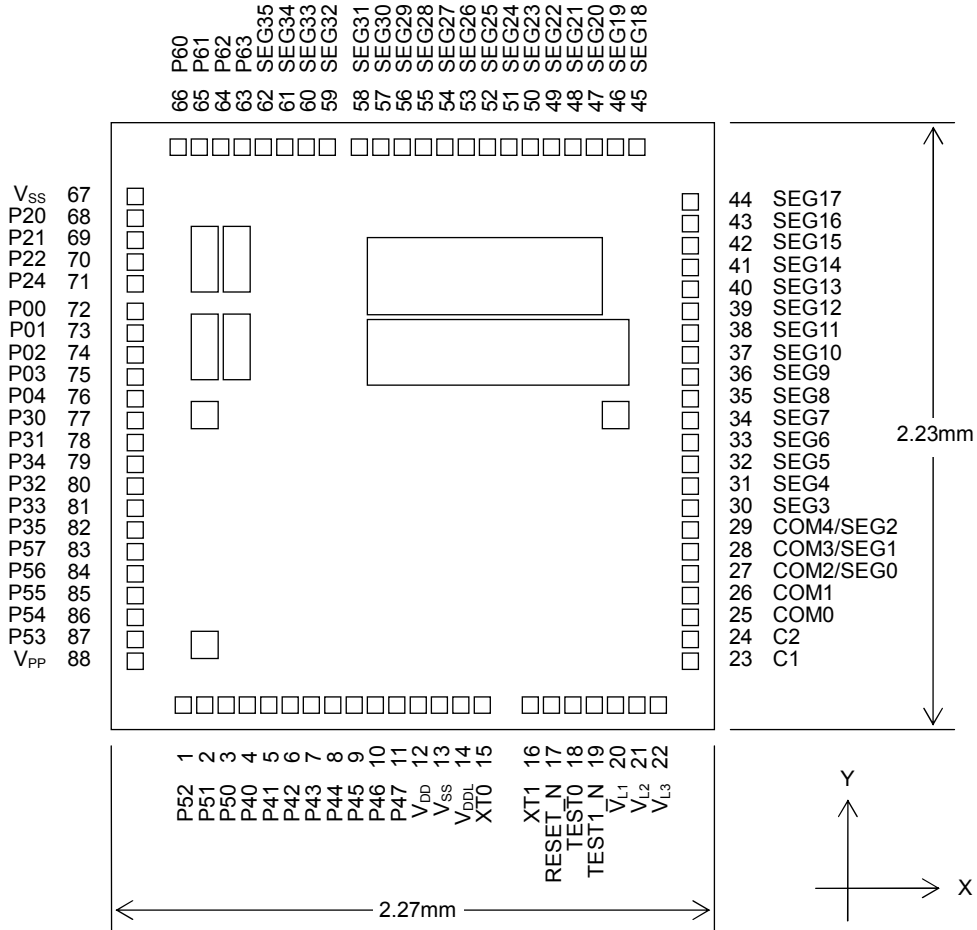


**Note:**  
The assignment of the pads P30 to P35 are not in order.

Chip size: 2.27 mm × 2.23 mm  
 PAD count: 88 pins  
 Minimum PAD pitch: 80µm  
 PAD aperture: 70µm×70µm  
 Chip thickness: 350µm  
 Voltage of the rear side of chip: V<sub>SS</sub> level.

**Figure 5 ML610Q407 Chip Layout & Dimension**

**ML610Q408 Chip Pin Layout & Dimension**

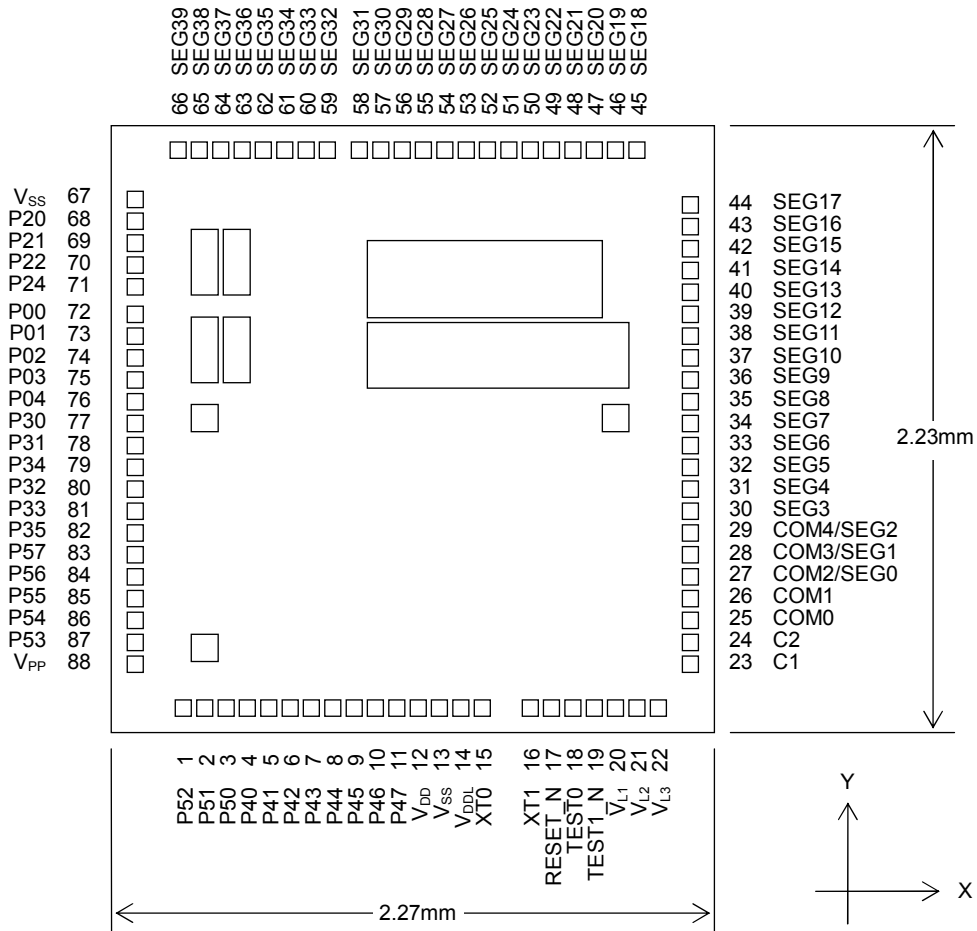


**Note:**  
The assignment of the pads P30 to P35 are not in order.

Chip size: 2.27 mm × 2.23 mm  
 PAD count: 88 pins  
 Minimum PAD pitch: 80µm  
 PAD aperture: 70µm×70µm  
 Chip thickness: 350µm  
 Voltage of the rear side of chip: V<sub>SS</sub> level.

**Figure 6 ML610Q408 Chip Layout & Dimension**

ML610Q409 Chip Pin Layout & Dimension



Note:  
The assignment of the pads P30 to P35 are not in order.

Chip size: 2.27 mm × 2.23 mm  
 PAD count: 88 pins  
 Minimum PAD pitch: 80 μm  
 PAD aperture: 70 μm×70 μm  
 Chip thickness: 350 μm  
 Voltage of the rear side of chip: V<sub>SS</sub> level.

Figure 7 ML610Q409 Chip Layout & Dimension

## ML610Q407/ML610Q408/ML610Q409 Pad Coordinates

Table 1 ML610Q407/ML610Q408/ML610Q409 Pad Coordinates

Chip Center: X=0,Y=0

| PAD No. | Pad Name  | ML610Q407/8/9 |        | PAD No. | Pad Name             | ML610Q407/8/9 |        |
|---------|-----------|---------------|--------|---------|----------------------|---------------|--------|
|         |           | X (μm)        | Y (μm) |         |                      | X (μm)        | Y (μm) |
| 1       | P52       | -853          | -1009  | 49      | SEG22                | 535           | 1009   |
| 2       | P51       | -773          | -1009  | 50      | SEG23                | 455           | 1009   |
| 3       | P50       | -693          | -1009  | 51      | SEG24                | 375           | 1009   |
| 4       | P40       | -613          | -1009  | 52      | SEG25                | 295           | 1009   |
| 5       | P41       | -533          | -1009  | 53      | SEG26                | 215           | 1009   |
| 6       | P42       | -453          | -1009  | 54      | SEG27                | 135           | 1009   |
| 7       | P43       | -373          | -1009  | 55      | SEG28                | 55            | 1009   |
| 8       | P44       | -293          | -1009  | 56      | SEG29                | -25           | 1009   |
| 9       | P45       | -213          | -1009  | 57      | SEG30                | -105          | 1009   |
| 10      | P46       | -133          | -1009  | 58      | SEG31                | -185          | 1009   |
| 11      | P47       | -53           | -1009  | 59      | P67 <sup>(*)</sup>   | -295          | 1009   |
| 12      | VDD       | 27            | -1009  |         | SEG32 <sup>(*)</sup> |               |        |
| 13      | VSS       | 107           | -1009  | 60      | P66 <sup>(*)</sup>   | -375          | 1009   |
| 14      | VDDL      | 187           | -1009  |         | SEG33 <sup>(*)</sup> |               |        |
| 15      | XT0       | 267           | -1009  | 61      | P65 <sup>(*)</sup>   | -455          | 1009   |
| 16      | XT1       | 427           | -1009  |         | SEG34 <sup>(*)</sup> |               |        |
| 17      | RESET_N   | 507           | -1009  | 62      | P64 <sup>(*)</sup>   | -535          | 1009   |
| 18      | TEST0     | 587           | -1009  |         | SEG35 <sup>(*)</sup> |               |        |
| 19      | TEST1_N   | 667           | -1009  | 63      | P63 <sup>(*)</sup>   | -615          | 1009   |
| 20      | VL1       | 747           | -1009  |         | SEG36 <sup>(*)</sup> |               |        |
| 21      | VL2       | 827           | -1009  | 64      | P62 <sup>(*)</sup>   | -695          | 1009   |
| 22      | VL3       | 907           | -1009  |         | SEG37 <sup>(*)</sup> |               |        |
| 23      | C0        | 1029          | -840   | 65      | P61 <sup>(*)</sup>   | -775          | 1009   |
| 24      | C1        | 1029          | -760   |         | SEG38 <sup>(*)</sup> |               |        |
| 25      | COM0      | 1029          | -680   | 66      | P60 <sup>(*)</sup>   | -885          | 1009   |
| 26      | COM1      | 1029          | -600   |         | SEG39 <sup>(*)</sup> |               |        |
| 27      | COM2/SEG0 | 1029          | -520   | 67      | VSS                  | -1029         | 850    |
| 28      | COM3/SEG1 | 1029          | -440   | 68      | P20                  | -1029         | 770    |
| 29      | COM4/SEG2 | 1029          | -360   | 69      | P21                  | --1029        | 690    |
| 30      | SEG3      | 1029          | -280   | 70      | P22                  | -1029         | 610    |
| 31      | SEG4      | 1029          | -200   | 71      | P24                  | -1029         | 530    |
| 32      | SEG5      | 1029          | -120   | 72      | P00                  | -1029         | 430    |
| 33      | SEG6      | 1029          | -40    | 73      | P01                  | -1029         | 350    |
| 34      | SEG7      | 1029          | 40     | 74      | P02                  | -1029         | 270    |
| 35      | SEG8      | 1029          | 120    | 75      | P03                  | -1029         | 190    |
| 36      | SEG9      | 1029          | 200    | 76      | P04                  | -1029         | 110    |
| 37      | SEG10     | 1029          | 280    | 77      | P30                  | -1029         | 30     |
| 38      | SEG11     | 1029          | 360    | 78      | P31                  | -1029         | -50    |
| 39      | SEG12     | 1029          | 440    | 79      | P34                  | -1029         | -130   |
| 40      | SEG13     | 1029          | 520    | 80      | P32                  | -1029         | -210   |
| 41      | SEG14     | 1029          | 600    | 81      | P33                  | -1029         | -290   |
| 42      | SEG15     | 1029          | 680    | 82      | P35                  | -1029         | -370   |
| 43      | SEG16     | 1029          | 760    | 83      | P57                  | -1029         | -450   |
| 44      | SEG17     | 1029          | 840    | 84      | P56                  | -1029         | -530   |
| 45      | SEG18     | 855           | 1009   | 85      | P55                  | -1029         | -610   |
| 46      | SEG19     | 775           | 1009   | 86      | P54                  | -1029         | -690   |
| 47      | SEG20     | 695           | 1009   | 87      | P53                  | -1029         | -770   |
| 48      | SEG21     | 615           | 1009   | 88      | VPP                  | -1029         | -850   |

(\*) ML610Q407 pad name, (\*\*) ML610Q408 pad name, (\*\*\*) ML610Q409 pad name

## PIN LIST

| PIN No. | PAD No. | Primary function     |     |   | Secondary function or Tertiary function |          |     |   |
|---------|---------|----------------------|-----|---|---|----------|-----|---|
|         |         | Pin name             | I/O | Function  | Secondary /Tertiary                     | Pin name | I/O | Function  |
| 14,77   | 13,67   | V <sub>SS</sub>      | —   | Negative power supply pin   | —                                       | —        | —   | —   |
| 13      | 12      | V <sub>DD</sub>      | —   | Positive power supply pin   | —                                       | —        | —   | —   |
| 15      | 14      | V <sub>DDL</sub>     | —   | Power supply pin for internal logic (internally generated)  | —                                       | —        | —   | —   |
| 98      | 88      | V <sub>PP</sub>      | —   | Power supply pin for Flash ROM  | —                                       | —        | —   | —   |
| 22      | 20      | V <sub>L1</sub>      | —   | Power supply pin for LCD bias (internally generated or connected to positive power supply pin) <sup>(2)</sup> | —                                       | —        | —   | —   |
| 23      | 21      | V <sub>L2</sub>      | —   | Power supply pin for LCD bias (internally generated or connected to positive power supply pin) <sup>(2)</sup> | —                                       | —        | —   | —   |
| 24      | 22      | V <sub>L3</sub>      | —   | Power supply pin for LCD bias (internally generated)  | —                                       | —        | —   | —   |
| 27      | 23      | C1                   | —   | Capacitor connection pin for LCD bias generation  | —                                       | —        | —   | —   |
| 28      | 24      | C2                   | —   | Capacitor connection pin for LCD bias generation  | —                                       | —        | —   | —   |
| 20      | 18      | TEST0                | I/O | Test pin  | —                                       | —        | —   | —   |
| 21      | 19      | TEST1_N              | I   | Test pin  | —                                       | —        | —   | —   |
| 19      | 17      | RESET_N              | I   | Reset input pin   | —                                       | —        | —   | —   |
| 17      | 15      | XT0                  | I   | Low-speed clock oscillation pin   | —                                       | —        | —   | —   |
| 18      | 16      | XT1                  | O   | Low-speed clock oscillation pin   | —                                       | —        | —   | —   |
| 82      | 72      | P00/EXI0/<br>CAP0    | I   | Input port,<br>External interrupt,<br>Capture 0 input   | —                                       | —        | —   | —   |
| 83      | 73      | P01/EXI1/<br>CAP1    | I   | Input port,<br>External interrupt,<br>Capture 1 input   | —                                       | —        | —   | —   |
| 84      | 74      | P02/EXI2/<br>RXD0    | I   | Input port,<br>External interrupt,<br>UART0 received data   | —                                       | —        | —   | —   |
| 85      | 75      | P03/EXI3             | I   | Input port,<br>External interrupt   | —                                       | —        | —   | —   |
| 86      | 76      | P04/EXI4/<br>T02POCK | I   | Input port,<br>Timer 0/Timer 2/PWM0 external<br>clock input<br>External interrupt                             | —                                       | —        | —   | —   |
| 78      | 68      | P20/LED0             | O   | Output port   | Secondary                               | LSCLK    | O   | Low-speed clock output                                  |
| 79      | 69      | P21/LED1             | O   | Output port   | Secondary                               | OUTCLK   | O   | High-speed clock output                                 |
| 80      | 70      | P22/LED2             | O   | Output port   | Secondary                               | MD0      | O   | Melody 0 output   |
| 81      | 71      | P24/LED4             | O   | Output port   | Secondary                               | PWM0     | O   | PWM0 output   |
| 87      | 77      | P30                  | I/O | Input/output port   | Secondary                               | IN0      | I   | RC type ADC0 oscillation input pin                      |
| 88      | 78      | P31                  | I/O | Input/output port   | Secondary                               | CS0      | O   | RC type ADC0 reference capacitor connection pin         |
| 89      | 79      | P34                  | I/O | Input/output port   | Secondary                               | RCT0     | O   | RC type ADC0 resistor/capacitor sensor connection pin   |
| 90      | 80      | P32                  | I/O | Input/output port   | Secondary                               | RS0      | O   | RC type ADC0 reference resistor connection pin          |
| 91      | 81      | P33                  | I/O | Input/output port   | Secondary                               | RT0      | O   | RC type ADC0 measurement resistor sensor connection pin |
| 92      | 82      | P35                  | I/O | Input/output port   | Secondary                               | RCM      | O   | RC type ADC oscillation monitor                         |

| PIN No. | PAD No. | Primary function |     |  | Secondary function or Tertiary function |          |     |  |
|---------|---------|------------------|-----|--|---|----------|-----|--|
|         |         | Pin name         | I/O | Function   | Secondary /Tertiary                     | Pin name | I/O | Function   |
| 5       | 4       | P40              | I/O | Input/output port  | Secondary                               | —        | —   | —  |
|         |         |                  |     |  | Tertiary                                | SIN0     | I   | SSIO0 data input   |
| 6       | 5       | P41              | I/O | Input/output port  | Secondary                               | —        | —   | —  |
|         |         |                  |     |  | Tertiary                                | SCK0     | I/O | SSIO0 synchronous clock input/output                       |
| 7       | 6       | P42              | I/O | Input/output port  | Secondary                               | RXD0     | I   | UART data input  |
|         |         |                  |     |  | Tertiary                                | SOUT0    | O   | SSIO0 data output  |
| 8       | 7       | P43              | I/O | Input/output port  | Secondary                               | TXD0     | O   | UART data output   |
|         |         |                  |     |  | Tertiary                                | PWM0     | O   | PWM0 output  |
| 9       | 8       | P44/<br>T02P0CK  | I/O | Input/output port,<br>Timer 0/Timer 2/PWM0 external<br>clock input | Secondary                               | IN1      | I   | RC type ADC1 oscillation input<br>pin                      |
|         |         |                  |     |  | Tertiary                                | SIN0     | I   | SSIO0 data input   |
| 10      | 9       | P45/T13CK        | I/O | Input/output port,<br>Timer 1/Timer 3 external clock<br>input      | Secondary                               | CS1      | O   | RC type ADC1 reference<br>capacitor connection pin         |
|         |         |                  |     |  | Tertiary                                | SCK0     | I/O | SSIO0 synchronous clock<br>input/output                    |
| 11      | 10      | P46              | I/O | Input/output port  | Secondary                               | RS1      | O   | RC type ADC1 reference<br>resistor connection pin          |
|         |         |                  |     |  | Tertiary                                | SOUT0    | O   | SSIO0 data output  |
| 12      | 11      | P47              | I/O | Input/output port  | Secondary                               | RT1      | O   | RC type ADC1 measurement<br>resistor sensor connection pin |
| 4       | 3       | P50/EX18         | I/O | Input/output port,<br>External interrupt                           | Secondary                               | MD0      | O   | Melody 0 output  |
|         |         |                  |     |  | Tertiary                                | SIN1     | I   | SSIO1 data input   |
| 3       | 2       | P51/EX18         | I/O | Input/output port,<br>External interrupt                           | Secondary                               | —        | —   | —  |
|         |         |                  |     |  | Tertiary                                | SCK1     | I/O | SSIO1 synchronous clock<br>input/output                    |
| 2       | 1       | P52/EX18         | I/O | Input/output port,<br>External interrupt                           | Secondary                               | —        | —   | —  |
|         |         |                  |     |  | Tertiary                                | SOUT1    | O   | SSIO1 data output  |
| 97      | 87      | P53/EX18         | I/O | Input/output port,<br>External interrupt                           | —                                       | —        | —   | —  |
| 96      | 86      | P54/EX18         | I/O | Input/output port,<br>External interrupt                           | Secondary                               | —        | —   | —  |
|         |         |                  |     |  | Tertiary                                | SIN1     | I   | SSIO1 data input   |
| 95      | 85      | P55/EX18         | I/O | Input/output port,<br>External interrupt                           | Secondary                               | —        | —   | —  |
|         |         |                  |     |  | Tertiary                                | SCK1     | I/O | SSIO1 synchronous clock<br>input/output                    |
| 94      | 84      | P56/EX18         | I/O | Input/output port,<br>External interrupt                           | Secondary                               | —        | —   | —  |
|         |         |                  |     |  | Tertiary                                | SOUT1    | O   | SSIO1 data output  |
| 93      | 83      | P57/EX18         | I/O | Input/output port,<br>External interrupt                           | —                                       | —        | —   | —  |

| PIN No. | PAD No. | Primary function     |     |                        | Secondary function or Tertiary function |          |     |          |
|---------|---------|----------------------|-----|------------------------|---|----------|-----|----------|
|         |         | Pin name             | I/O | Function               | Secondary/Tertiary                      | Pin name | I/O | Function |
| 29      | 25      | COM0                 | O   | LCD common pin         | —                                       | —        | —   | —        |
| 30      | 26      | COM1                 | O   | LCD common pin         | —                                       | —        | —   | —        |
| 31      | 27      | COM2/<br>SEG0        | O   | LCD common/segment pin | —                                       | —        | —   | —        |
| 32      | 28      | COM3/<br>SEG1        | O   | LCD common/segment pin | —                                       | —        | —   | —        |
| 33      | 29      | COM4/<br>SEG2        | O   | LCD common/segment pin | —                                       | —        | —   | —        |
| 34      | 30      | SEG3                 | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 35      | 31      | SEG4                 | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 36      | 32      | SEG5                 | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 37      | 33      | SEG6                 | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 38      | 34      | SEG7                 | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 39      | 35      | SEG8                 | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 40      | 36      | SEG9                 | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 41      | 37      | SEG10                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 42      | 38      | SEG11                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 43      | 39      | SEG12                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 44      | 40      | SEG13                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 45      | 41      | SEG14                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 46      | 42      | SEG15                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 47      | 43      | SEG16                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 48      | 44      | SEG17                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 52      | 45      | SEG18                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 53      | 46      | SEG19                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 54      | 47      | SEG20                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 55      | 48      | SEG21                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 56      | 49      | SEG22                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 57      | 50      | SEG23                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 58      | 51      | SEG24                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 59      | 52      | SEG25                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 60      | 53      | SEG26                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 61      | 54      | SEG27                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 62      | 55      | SEG28                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 63      | 56      | SEG29                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 64      | 57      | SEG30                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 65      | 58      | SEG31                | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 66      | 59      | P67 <sup>(2)</sup>   | O   | Output port            | —                                       | —        | —   | —        |
|         |         | SEG32 <sup>(3)</sup> | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 67      | 60      | P66 <sup>(2)</sup>   | O   | Output port            | —                                       | —        | —   | —        |
|         |         | SEG33 <sup>(3)</sup> | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 68      | 61      | P65 <sup>(2)</sup>   | O   | Output port            | —                                       | —        | —   | —        |
|         |         | SEG34 <sup>(3)</sup> | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 69      | 62      | P64 <sup>(2)</sup>   | O   | Output port            | —                                       | —        | —   | —        |
|         |         | SEG35 <sup>(3)</sup> | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 70      | 63      | P63 <sup>(4)</sup>   | O   | Output port            | —                                       | —        | —   | —        |
|         |         | SEG36 <sup>(5)</sup> | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 71      | 64      | P62 <sup>(4)</sup>   | O   | Output port            | —                                       | —        | —   | —        |
|         |         | SEG37 <sup>(5)</sup> | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 72      | 65      | P61 <sup>(4)</sup>   | O   | Output port            | —                                       | —        | —   | —        |
|         |         | SEG38 <sup>(5)</sup> | O   | LCD segment pin        | —                                       | —        | —   | —        |
| 73      | 66      | P60 <sup>(4)</sup>   | O   | Output port            | —                                       | —        | —   | —        |
|         |         | SEG39 <sup>(5)</sup> | O   | LCD segment pin        | —                                       | —        | —   | —        |

(\*<sup>1</sup>) Internally generated, or connect to either positive power supply pin ( $V_{DD}$ ) or power supply pin for internal logic ( $V_{DDL}$ ). For details, see "Chapter 22 LCD Drivers. In the user's manual"

(\*<sup>2</sup>) Pin for ML610Q407/ML610Q408.

(\*<sup>3</sup>) Pin for ML610Q409.

(\*<sup>4</sup>) Pin for ML610Q407.

(\*<sup>5</sup>) Pin for ML610Q408/ML610Q409.

## PIN DESCRIPTION

| Pin name                          | I/O | Description   | Primary/<br>Secondary/<br>Tertiary | Logic    |
|-----------------------------------|-----|---|------------------------------------|----------|
| System                            |     |   |                                    |          |
| RESET_N                           | I   | Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected. | —                                  | Negative |
| XT0                               | I   | Crystal connection pin for low-speed clock.<br>A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V <sub>SS</sub> .                                   | —                                  | —        |
| XT1                               | O   |   | —                                  | —        |
| LSCLK                             | O   | Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.  | Secondary                          | —        |
| OUTCLK                            | O   | High-speed clock output pin. This pin is used as the secondary function of the P21 pin.   | Secondary                          | —        |
| General-purpose input port        |     |   |                                    |          |
| P00-P04                           | I   | General-purpose input port.<br>Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.  | Primary                            | Positive |
| General-purpose output port       |     |   |                                    |          |
| P20-P22,P24                       | O   | General-purpose output port.<br>Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.   | Primary                            | Positive |
| General-purpose input/output port |     |   |                                    |          |
| P30-P35                           | I/O | General-purpose input/output port.<br>Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.   | Primary                            | Positive |
| P40-P47                           | I/O | General-purpose input/output port.<br>Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.   | Primary                            | Positive |
| P50-P57                           | I/O | General-purpose input/output port.<br>Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.   | Primary                            | Positive |
| P60-P63                           | O   | General-purpose input/output port.<br>These pins are for the ML610Q407/ ML610Q408, but are not provided in the ML610Q409.   | Primary                            | Positive |
| P64-P67                           | O   | General-purpose input/output port.<br>These pins are for the ML610Q407, but are not provided in the ML610Q409.  | Primary                            | Positive |

| Pin name                         | I/O | Description   | Primary/<br>Secondary/<br>Tertiary | Logic                 |
|----------------------------------|-----|---|------------------------------------|-----------------------|
| <b>UART</b>                      |     |   |                                    |                       |
| TXD0                             | O   | UART data output pin. This pin is used as the secondary function of the P43 pin.  | Secondary                          | Positive              |
| RXD0                             | I   | UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.  | Primary/<br>Secondary              | Positive              |
| <b>Synchronous serial (SSIO)</b> |     |   |                                    |                       |
| SCK0                             | I/O | Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.   | Tertiary                           | —                     |
| SIN0                             | I   | Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.   | Tertiary                           | Positive              |
| SOUT0                            | O   | Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.  | Tertiary                           | Positive              |
| SCK1                             | I/O | Synchronous serial clock input/output pin. This pin is used as the secondary function of the P51 or P55 pin.  | Secondary                          | —                     |
| SIN1                             | I   | Synchronous serial data input pin. This pin is used as the secondary function of the P50 or P54.  | Secondary                          | Positive              |
| SOUT1                            | O   | Synchronous serial data output pin. This pin is used as the secondary function of the P52 or P56pin.  | Secondary                          | Positive              |
| <b>PWM</b>                       |     |   |                                    |                       |
| PWM0                             | O   | PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.   | Tertiary                           | Positive              |
| T02P0CK                          | I   | PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.   | Primary                            | —                     |
| <b>External interrupt</b>        |     |   |                                    |                       |
| EXI0-4                           | I   | External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P04 pins.  | Primary                            | Positive/<br>negative |
| EXI8                             | I   | External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P50-P57 pins.  | Primary                            | Positive/<br>negative |
| <b>Capture</b>                   |     |   |                                    |                       |
| CAP0                             | I   | Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1). | Primary                            | Positive/<br>negative |
| CAP1                             | I   |   | Primary                            | Positive/<br>negative |
| <b>Timer</b>                     |     |   |                                    |                       |
| T02P0CK                          | I   | External clock input pin used for Timer 0 and Timer 2. The clock for this timer is selected by software. This pin is used as the primary function of the P44 pin.   | Primary                            | —                     |
| T13CK                            | I   | External clock input pin used both Timer 1 and Timer 3. The clock for this timer is selected by software. This pin is used as the primary function of the P45 pin.  | Primary                            | —                     |
| <b>Melody</b>                    |     |   |                                    |                       |
| MD0                              | O   | Melody/Buzzer signal output pin. This pin is used as the secondary function of the P22 pin and P50 pin.   | Secondary                          | Positive/<br>negative |
| <b>LED drive</b>                 |     |   |                                    |                       |
| LED0-2,4                         | O   | Nch open drain output pins to drive LED.  | Primary                            | Positive/<br>negative |

| Pin name                                 | I/O | Description  | Primary/<br>Secondary/<br>Tertiary | Logic |
|--|-----|--|------------------------------------|-------|
| <b>RC oscillation type A/D converter</b> |     |  |                                    |       |
| IN0                                      | I   | Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.  | Secondary                          | —     |
| CS0                                      | O   | Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.   | Secondary                          | —     |
| RCT0                                     | O   | Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.  | Secondary                          | —     |
| RS0                                      | O   | This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.   | Secondary                          | —     |
| RT0                                      | O   | Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.  | Secondary                          | —     |
| RCM                                      | O   | RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.   | Secondary                          | —     |
| IN1                                      | I   | Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.   | Secondary                          | —     |
| CS1                                      | O   | Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.  | Secondary                          | —     |
| RS1                                      | O   | Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.   | Secondary                          | —     |
| RT1                                      | O   | Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.  | Secondary                          | —     |
| <b>LCD drive signal</b>                  |     |  |                                    |       |
| COM0-4                                   | O   | Common output pins.  | —                                  | —     |
| SEG0-31                                  | O   | Segment output pins.   | —                                  | —     |
| SEG32-35                                 | O   | Segment output pin. These pins are for the ML610Q408/ML610Q409, but are not provided in the ML610Q407.   | —                                  | —     |
| SEG36-39                                 | O   | Segment output pin. These pins are for the ML610Q409, but are not provided in the ML610Q407/ML610Q408.   | —                                  | —     |
| <b>LCD driver power supply</b>           |     |  |                                    |       |
| V <sub>L1</sub>                          | —   | Power supply pins for LCD bias (internally generated or positive power supply pin connected). Depending on LCD Bias setting and V <sub>DD</sub> voltage level, V <sub>DD</sub> or V <sub>DDL</sub> or capacitor is connected. For details of the connection method, see user's manual. | —                                  | —     |
| V <sub>L2</sub>                          | —   |  | —                                  | —     |
| V <sub>L3</sub>                          | —   |  | —                                  | —     |
| C1                                       | —   | Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2.  | —                                  | —     |
| C2                                       | —   |  | —                                  | —     |
| <b>For testing</b>                       |     |  |                                    |       |
| TEST                                     | I/O | Input/output pin for testing. A pull-down resistor is internally connected.  | —                                  | —     |
| <b>Power supply</b>                      |     |  |                                    |       |
| V <sub>SS</sub>                          | —   | Negative power supply pin.   | —                                  | —     |
| V <sub>DD</sub>                          | —   | Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.   | —                                  | —     |
| V <sub>DDL</sub>                         | —   | Positive power supply pin (internally generated) for internal logic. Capacitor CL (see Appendix C measuring circuit 1) is connected between this pin and V <sub>SS</sub> .   | —                                  | —     |
| V <sub>PP</sub>                          | —   | Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.  | —                                  | —     |

## TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

**Table 2 Termination of Unused Pins**

| Pin   | Recommended pin termination        |
|---|------------------------------------|
| V <sub>PP</sub>                                     | Open                               |
| V <sub>L1</sub> , V <sub>L2</sub> , V <sub>L3</sub> | Open                               |
| C1, C2  | Open                               |
| RESET_N   | Open                               |
| TEST0   | Open                               |
| TEST1_N   | Open                               |
| P00 to P04  | V <sub>DD</sub> or V <sub>SS</sub> |
| P20 to P22, P24                                     | Open                               |
| P30 to P35  | Open                               |
| P40 to P47  | Open                               |
| P50 to P57  | Open                               |
| P60 to P67  | Open                               |
| COM0 to 4   | Open                               |
| SEG0 to 39  | Open                               |

**Note:**

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

**ELECTRICAL CHARACTERISTICS****ABSOLUTE MAXIMUM RATINGS**(V<sub>SS</sub> = 0V)

| Parameter              | Symbol            | Condition          | Rating                       | Unit |
|------------------------|-------------------|--------------------|------------------------------|------|
| Power supply voltage 1 | V <sub>DD</sub>   | Ta = 25°C          | -0.3 to +4.6                 | V    |
| Power supply voltage 2 | V <sub>PP</sub>   | Ta = 25°C          | -0.3 to +9.5                 | V    |
| Power supply voltage 3 | V <sub>DDL</sub>  | Ta = 25°C          | -0.3 to +3.6                 | V    |
| Power supply voltage 4 | V <sub>L1</sub>   | Ta = 25°C          | -0.3 to +2.0                 | V    |
| Power supply voltage 5 | V <sub>L2</sub>   | Ta = 25°C          | -0.3 to +4.0                 | V    |
| Power supply voltage 6 | V <sub>L3</sub>   | Ta = 25°C          | -0.3 to +6.0                 | V    |
| Input voltage          | V <sub>IN</sub>   | Ta = 25°C          | -0.3 to V <sub>DD</sub> +0.3 | V    |
| Output voltage         | V <sub>OUT</sub>  | Ta = 25°C          | -0.3 to V <sub>DD</sub> +0.3 | V    |
| Output current 1       | I <sub>OUT1</sub> | Port3-6, Ta = 25°C | -12 to +11                   | mA   |
| Output current 2       | I <sub>OUT2</sub> | Port2, Ta = 25°C   | -12 to +20                   | mA   |
| Power dissipation      | PD                | Ta = 25°C          | 0.9                          | W    |
| Storage temperature    | T <sub>STG</sub>  | —                  | -55 to +150                  | °C   |

**RECOMMENDED OPERATING CONDITIONS**(V<sub>SS</sub> = 0V)

| Parameter   | Symbol               | Condition                       | Range       | Unit |
|---|----------------------|---------------------------------|-------------|------|
| Operating temperature                                       | T <sub>OP</sub>      | non-P version                   | -20 to +70  | °C   |
|   |                      | P version                       | -40 to +85  |      |
| Operating voltage   | V <sub>DD</sub>      | f <sub>OP</sub> = 30k to 625kHz | 1.25 to 3.6 | V    |
|   |                      | f <sub>OP</sub> = 30k to 2.5MHz | 1.8 to 3.6  |      |
| Operating frequency (CPU)                                   | f <sub>OP</sub>      | V <sub>DD</sub> = 1.25 to 3.6V  | 30k to 625k | Hz   |
|   |                      | V <sub>DD</sub> = 1.8 to 3.6V   | 30k to 2.5M |      |
| Low-speed crystal oscillation frequency                     | f <sub>XTL</sub>     | —                               | 32.768k     | Hz   |
| Low-speed crystal oscillation external capacitor            | C <sub>DL</sub>      | —                               | 3 to 18     | pF   |
|   | C <sub>GL</sub>      | —                               | 3 to 18     |      |
| Capacitor externally connected to V <sub>DDL</sub> pin      | C <sub>L</sub>       | —                               | 0.47±30%    | μF   |
| Capacitors externally connected to V <sub>L1,2,3</sub> pins | C <sub>a, b, c</sub> | —                               | 0.1±30%     | μF   |
| Capacitors externally connected across C1 and C2 pins       | C <sub>12</sub>      | —                               | 0.47±30%    | μF   |

## OPERATING CONDITIONS OF FLASH ROM

(V<sub>SS</sub> = 0V)

| Parameter             | Symbol           | Condition                    | Range       | Unit   |
|-----------------------|------------------|------------------------------|-------------|--------|
| Operating temperature | T <sub>OP</sub>  | At write/erase               | 0 to +40    | °C     |
| Operating voltage     | V <sub>DD</sub>  | At write/erase <sup>*1</sup> | 2.75 to 3.6 | V      |
|                       | V <sub>DDL</sub> | At write/erase <sup>*1</sup> | 2.5 to 2.75 |        |
|                       | V <sub>PP</sub>  | At write/erase <sup>*1</sup> | 7.7 to 8.3  |        |
| erase/program cycles  | C <sub>EP</sub>  | —                            | 80          | cycles |
| Data retention        | Y <sub>DR</sub>  | —                            | 10          | years  |

<sup>\*1</sup>: Those voltages must be supplied to V<sub>DDL</sub> pin and V<sub>PP</sub> pin when programming and erasing Flash ROM.  
V<sub>PP</sub> pin has an internal pulldown resistor.

## DC CHARACTERISTICS (1/5)

(V<sub>DD</sub> = 1.25 to 3.6V, V<sub>SS</sub> = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

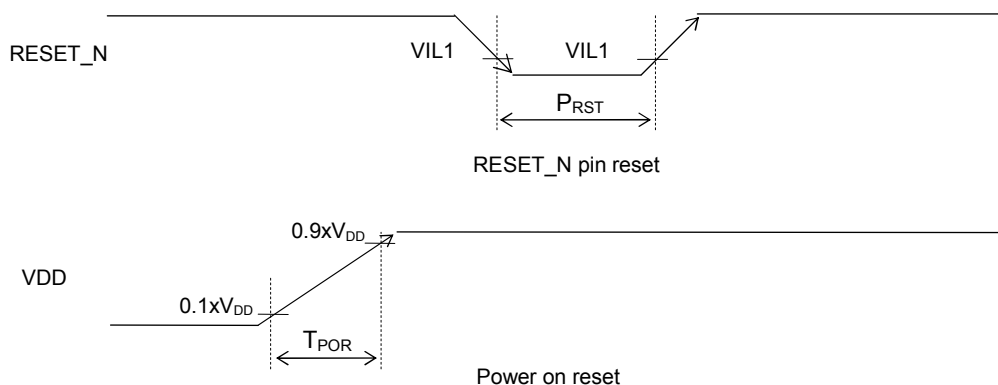
| Parameter  | Symbol            | Condition                      | Rating    |           |      | Unit      | Measuring circuit |
|--|-------------------|--------------------------------|-----------|-----------|------|-----------|-------------------|
|  |                   |                                | Min.      | Typ.      | Max. |           |                   |
| 500kHz/2MHz RC oscillation frequency                   | f <sub>RC</sub>   | V <sub>DD</sub> = 1.25 to 3.6V | Ta = 25°C | Typ. -10% | 500  | Typ. +10% | kHz               |
|  |                   |                                | *3        | Typ. -25% | 500  | Typ. +25% |                   |
|  |                   | V <sub>DD</sub> = 1.80 to 3.6V | Ta = 25°C | Typ. -10% | 2.0  | Typ. +10% | MHz               |
|  |                   |                                | *3        | Typ. -25% | 2.0  | Typ. +25% |                   |
| Low-speed crystal oscillation start time <sup>*2</sup> | T <sub>XTL</sub>  | —                              | —         | 0.6       | 2    | s         | 1                 |
| 500kHz/2MHz RC oscillation start time                  | T <sub>RC</sub>   | —                              | —         | —         | 0.3  | μs        |                   |
| Low-speed oscillation stop detect time <sup>*1</sup>   | T <sub>STOP</sub> | —                              | 12        | 16.4      | 41   | ms        |                   |
| Reset pulse width                                      | P <sub>RST</sub>  | —                              | 200       | —         | —    | μs        |                   |
| Reset noise elimination pulse width                    | P <sub>NRST</sub> | —                              | —         | —         | 0.3  |           |                   |
| Power-on reset activation power rise time              | T <sub>POR</sub>  | —                              | —         | —         | 10   | ms        |                   |

<sup>\*1</sup>: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

<sup>\*2</sup>: Use 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C<sub>GL</sub>=C<sub>DL</sub>=12pF).

<sup>\*3</sup>: Recommended operating temperature (Ta = -20 to +70°C, Ta = -40 to +85°C for P version)

## RESET



**DC CHARACTERISTICS (2/5)**(V<sub>DD</sub> = 1.25 to 3.6V, V<sub>SS</sub> = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

| Parameter                                 | Symbol            | Condition                       | Rating |      |      | Unit  | Measuring circuit |
|---|-------------------|---------------------------------|--------|------|------|-------|-------------------|
|   |                   |                                 | Min.   | Typ. | Max. |       |                   |
| V <sub>DDL</sub> voltage                  | V <sub>DDL</sub>  | f <sub>OP</sub> = 30k to 625kHz | 1.1    | 1.2  | 1.3  |       | 1                 |
|   |                   | f <sub>OP</sub> = 30k to 2.5MHz | 1.35   | 1.5  | 1.65 |       |                   |
| V <sub>DDL</sub> temperature deviation *1 | ΔV <sub>DDL</sub> | V <sub>DD</sub> = 3.0V          | —      | -1   | —    | mV/°C |                   |
| V <sub>DDL</sub> voltage dependency *1    | ΔV <sub>DDL</sub> | —                               | —      | 5    | 20   | mV/V  |                   |

\*1:V<sub>DDL</sub> can not exceed V<sub>DD</sub> level. The maximum V<sub>DDL</sub> becomes V<sub>DD</sub> level when the V<sub>DDL</sub> calculated by the temperature deviation and voltage dependency is going to exceed the V<sub>DD</sub> level.

## DC CHARACTERISTICS (3/5)

(V<sub>DD</sub> = 3.0V, V<sub>SS</sub> = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version)

| Parameter             | Symbol | Condition   | Rating   |      |      | Unit | Measuring circuit |   |
|-----------------------|--------|---|----------|------|------|------|-------------------|---|
|                       |        |   | Min.     | Typ. | Max. |      |                   |   |
| Supply current 1      | IDD1   | CPU: In STOP state.<br>Low-speed/high-speed<br>RC500kHz/2MHz oscillation:<br>stopped.   | Ta= 25°C | —    | 0.4  | 0.8  | μA                | 1 |
|                       |        |   | *5       | —    | —    | 8    |                   |   |
| Supply current 2      | IDD2   | CPU: In HALT state (LTBC and WDT<br>are Operating). <sup>*3*4</sup><br>High-speed 500kHz/2MHz<br>oscillation: Stopped.<br>LCD and BIAS circuits: Operating. <sup>*6</sup> | Ta= 25°C | —    | 0.9  | 1.8  | μA                |   |
|                       |        |   | *5       | —    | —    | 9    |                   |   |
| Supply current 3      | IDD3   | CPU: In 32.768kHz operating<br>state. <sup>*1*3</sup><br>High-speed 500kHz/2MHz<br>oscillation: Stopped.<br>LCD and BIAS circuits: Operating. <sup>*2</sup>               | Ta= 25°C | —    | 5    | 8    | μA                |   |
|                       |        |   | *5       | —    | —    | 15   |                   |   |
| Supply current<br>4-1 | IDD4-1 | CPU: In RC 500kHz operating state.<br>LCD and BIAS circuits: Operating. <sup>*2</sup>   | Ta= 25°C | —    | 70   | 100  | μA                |   |
|                       |        |   | *5       | —    | —    | 120  |                   |   |
| Supply current<br>4-2 | IDD4-2 | CPU: In RC 2MHz operating state.<br>LCD and BIAS circuits: Operating. <sup>*2</sup>   | Ta= 25°C | —    | 280  | 350  | μA                |   |
|                       |        |   | *5       | —    | —    | 400  |                   |   |

\*1: When the CPU operating rate is 100% (No HALT state).

\*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

\*3: Use 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C<sub>GL</sub>=C<sub>DL</sub>=6pF)

\*4: Significant bits of BLKCON0~BLKCON4 registers except DLCD bit on BLKCON4 are all "1".

\*5: Recommended operating temperature (Ta = -20 to +70°C, Ta = -40 to +85°C for P version)

\*6: LCD Stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

**DC CHARACTERISTICS (4/5)**(V<sub>DD</sub> = 1.25 to 3.6V, V<sub>SS</sub> = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

| Parameter   | Symbol | Condition   | Rating                  |      |                         | Unit | Measuring circuit |   |   |
|---|--------|---|-------------------------|------|-------------------------|------|-------------------|---|---|
|   |        |   | Min.                    | Typ. | Max.                    |      |                   |   |   |
| Output voltage 1<br>(P20-P22,P24/<br>2 <sup>nd</sup> function is<br>selected)<br>(P30-P36)<br>(P40-P47)<br>(P50-P57)<br>(P60-P63) <sup>*1 *2</sup><br>(P64-P67) <sup>*1</sup> | VOH1   | IOH1 = -0.5mA, V <sub>DD</sub> = 1.8 to 3.6V                                  | V <sub>DD</sub><br>-0.5 | —    | —                       | V    | 2                 |   |   |
|   |        | IOH1 = -0.03mA, V <sub>DD</sub> = 1.25 to 3.6V                                | V <sub>DD</sub><br>-0.3 | —    | —                       |      |                   |   |   |
|   | VOL1   | IOL1 = +0.5mA, V <sub>DD</sub> = 1.8 to 3.6V                                  | —                       | —    | 0.5                     |      |                   |   |   |
|   |        | IOL1 = +0.1mA, V <sub>DD</sub> = 1.25 to 3.6V                                 | —                       | —    | 0.3                     |      |                   |   |   |
| Output voltage 2<br>(P20-P22,P24/<br>2 <sup>nd</sup> function is Not<br>selected)   | VOL2   | IOL2 = +5mA, V <sub>DD</sub> = 1.8 to 3.6V                                    | —                       | —    | 0.5                     |      |                   | V | 2 |
| Output voltage 3<br>(COM0-4)<br>(SEG0-31) <sup>*1</sup><br>(SEG0-35) <sup>*2</sup><br>(SEG0-39) <sup>*3</sup>   | VOH3   | IOH4 = -0.05mA, VL1=1.2V  | V <sub>L3</sub><br>-0.2 | —    | —                       |      |                   |   |   |
|   | VOML3  | IOMH4 = +0.05mA, VL1=1.2V   | —                       | —    | V <sub>L2</sub><br>+0.2 |      |                   |   |   |
|   | VOML3S | IOM4S = -0.05mA, VL1=1.2V   | V <sub>L2</sub><br>-0.2 | —    | —                       |      |                   |   |   |
|   | VOLM3  | IOML4 = +0.05mA, VL1=1.2V   | —                       | —    | V <sub>L1</sub><br>+0.2 |      |                   |   |   |
|   | VOLM3S | IOML4S = -0.05mA, VL1=1.2V  | V <sub>L1</sub><br>-0.2 | —    | —                       |      |                   |   |   |
|   | VOL3   | IOL4 = +0.05mA, VL1=1.2V  | —                       | —    | 0.2                     |      |                   |   |   |
| Output leakage<br>(P20-P22, P24)<br>(P30-P35)<br>(P40-P47)<br>(P50-P57)<br>(P60-P63) <sup>*1 *2</sup><br>(P64-P67) <sup>*1</sup>  | IOOH   | VOH = V <sub>DD</sub> (in high-impedance state)                               | —                       | —    | 1                       | μA   | 3                 |   |   |
|   | IOOL   | VOL = V <sub>SS</sub> (in high-impedance state)                               | -1                      | —    | —                       |      |                   |   |   |
| Input current 1<br>(RESET_N,<br>TEST1_N)  | IIH1   | VIH1 = V <sub>DD</sub>  | 0                       | —    | 1                       | μA   | 4                 |   |   |
|   | IIL1   | VIL1 = V <sub>SS</sub>  | -600                    | -300 | -2                      |      |                   |   |   |
| Input current 2<br>(TEST0)  | IIH2   | VIH1 = V <sub>DD</sub>  | 2                       | 300  | 600                     |      |                   |   |   |
|   | IIL2   | VIL1 = V <sub>SS</sub>  | -1                      | —    | —                       |      |                   |   |   |
| Input current 3<br>(P00-P04)<br>(P30-P35)<br>(P40-P47)<br>(P50-P57)   | IIH3   | VIH3 = V <sub>DD</sub> , V <sub>DD</sub> = 1.8 to 3.6V<br>(when pulled-down)  | 2                       | 30   | 200                     |      |                   |   |   |
|   |        | VIH3 = V <sub>DD</sub> , V <sub>DD</sub> = 1.25 to 3.6V<br>(when pulled-down) |                         |      |                         |      |                   |   |   |
|   | IIL3   | VIL3 = V <sub>SS</sub> , V <sub>DD</sub> = 1.8 to 3.6V<br>(when pulled-up)    | -200                    | -30  | -2                      |      |                   |   |   |
|   |        | VIL3 = V <sub>SS</sub> , V <sub>DD</sub> = 1.25 to 3.6V<br>(when pulled-up)   | -200                    | -30  | -0.01                   |      |                   |   |   |
|   | IIH3Z  | VIH3 = V <sub>DD</sub> (in high-impedance state)                              | —                       | —    | 1                       |      |                   |   |   |
|   | IIL3Z  | VIL3 = V <sub>SS</sub> (in high-impedance state)                              | -1                      | —    | —                       |      |                   |   |   |

\*1: pins for ML610Q407

\*2: pins for ML610Q408

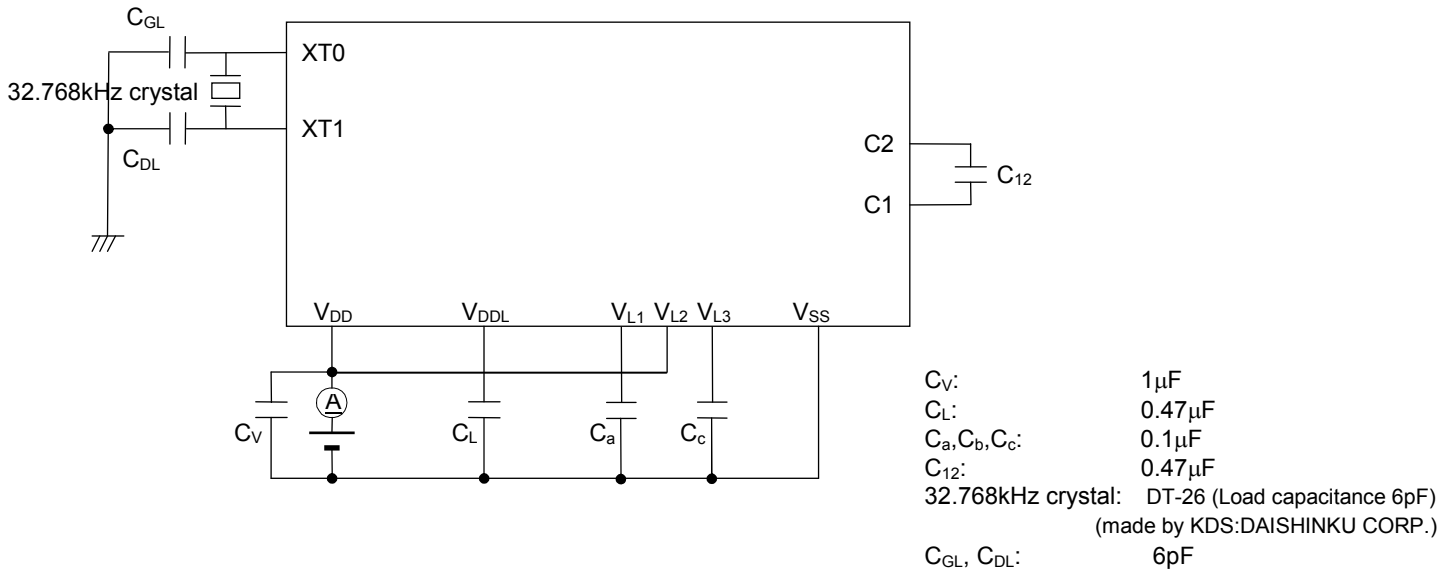
\*3: pins for ML610Q409

**DC CHARACTERISTICS (5/5)**(V<sub>DD</sub> = 1.25 to 3.6V, V<sub>SS</sub> = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

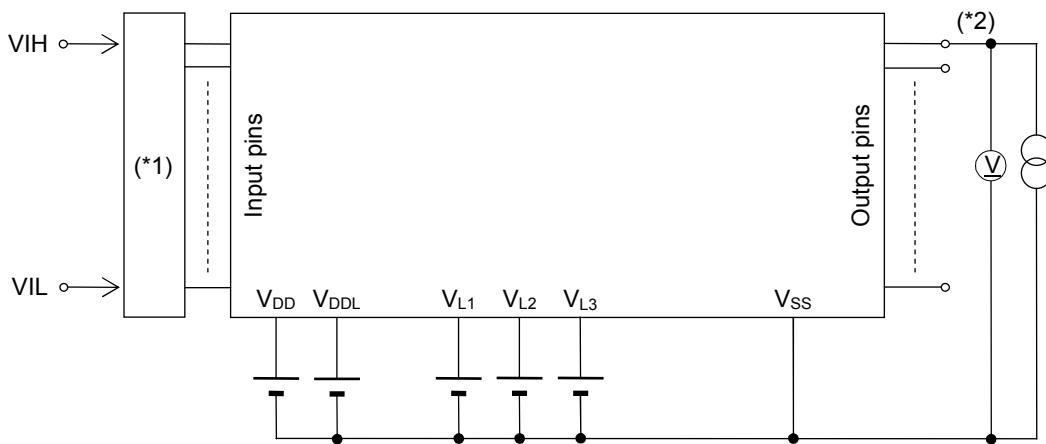
| Parameter   | Symbol | Condition   | Rating                  |      |                         | Unit | Measuring circuit |
|---|--------|---|-------------------------|------|-------------------------|------|-------------------|
|   |        |   | Min.                    | Typ. | Max.                    |      |                   |
| Input voltage 1<br>(RESET_N)<br>(TEST0,<br>TEST1_N)<br>(P00-P04)<br>(P30-P35)<br>(P40-P47)<br>(P50-P57) | VIH1   | —   | 0.7<br>×V <sub>DD</sub> | —    | V <sub>DD</sub>         | V    | 5                 |
|   | VIL1   | V <sub>DD</sub> = 1.8 to 3.6V                     | 0                       | —    | 0.3<br>×V <sub>DD</sub> |      |                   |
|   |        | V <sub>DD</sub> = 1.25 to 3.6V                    | 0                       | —    | 0.2<br>×V <sub>DD</sub> |      |                   |
| Input pin capacitance<br>(P00-P04)<br>(P30-P35)<br>(P40-P47)<br>(P50-P57)                               | CIN    | f = 10kHz<br>V <sub>rms</sub> = 50mV<br>Ta = 25°C | —                       | —    | 5                       | pF   | —                 |

MEASURING CIRCUITS

MEASURING CIRCUIT 1

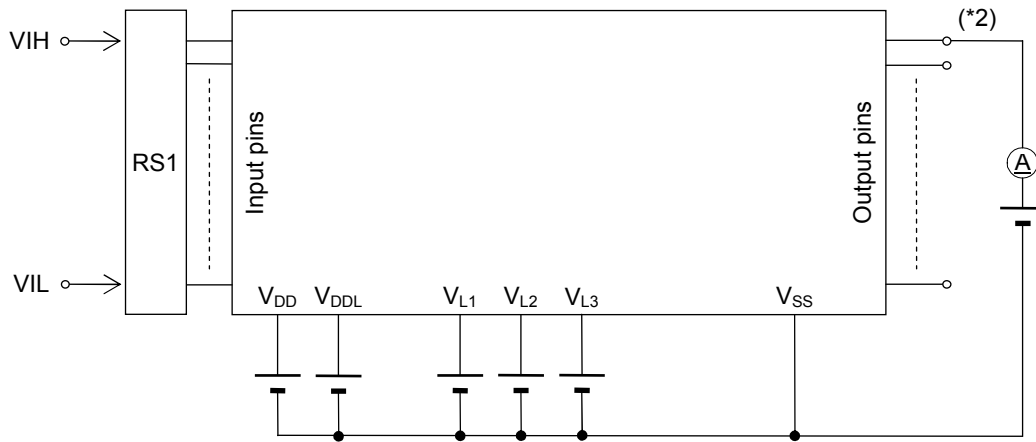


MEASURING CIRCUIT 2



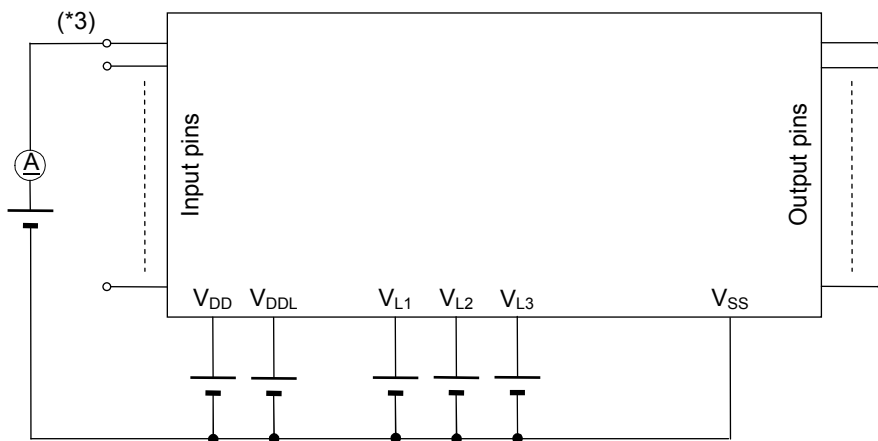
(\*1) Input logic circuit to determine the specified measuring conditions.  
 (\*2) Measured at the specified output pins.

**MEASURING CIRCUIT 3**



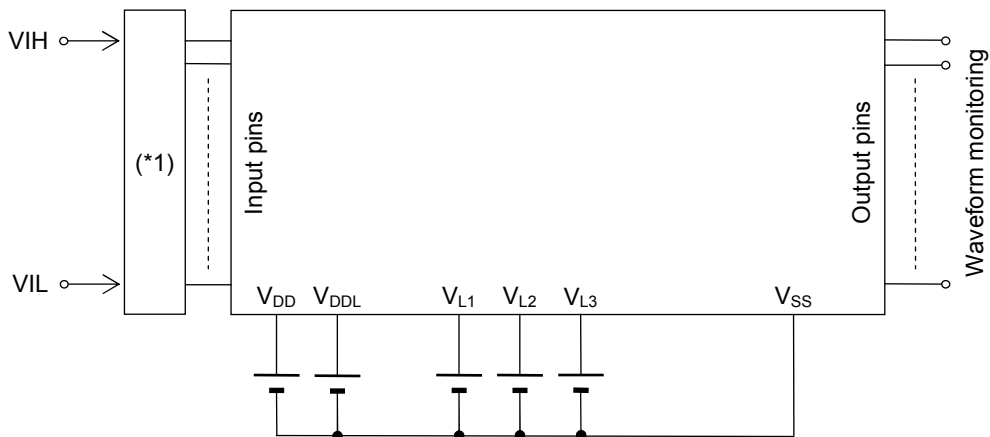
\*1: Input logic circuit to determine the specified measuring conditions.  
 \*2: Measured at the specified output pins.

**MEASURING CIRCUIT 4**



\*3: Measured at the specified output pins.

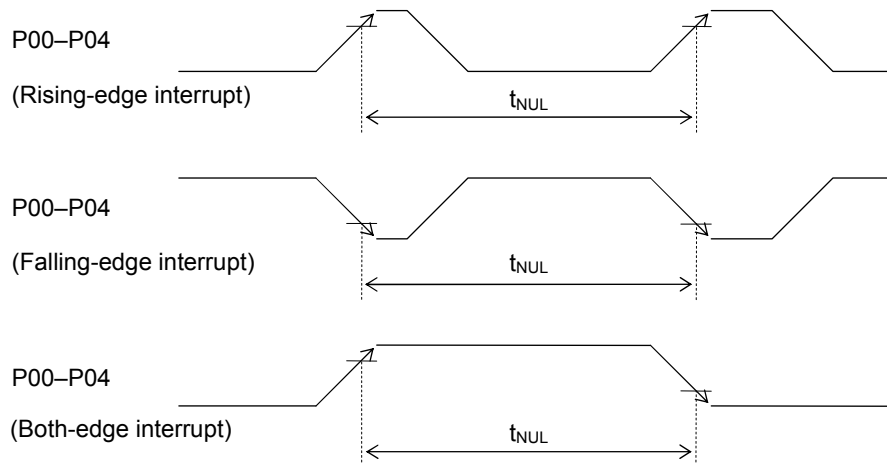
**MEASURING CIRCUIT 5**



\*1: Input logic circuit to determine the specified measuring conditions.

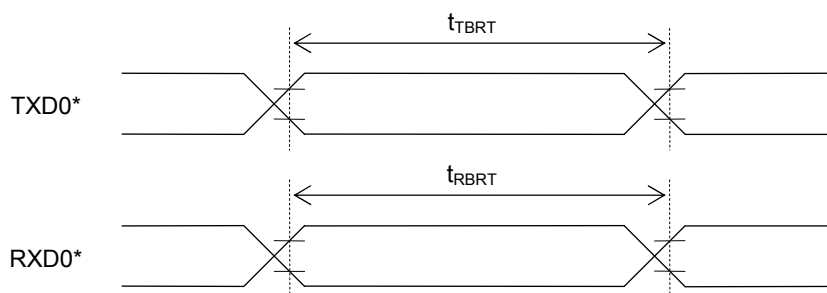
**AC CHARACTERISTICS (External Interrupt)**(V<sub>DD</sub> = 1.25 to 3.6V, V<sub>SS</sub> = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

| Parameter                         | Symbol           | Condition  | Rating |      |       | Unit |
|-----------------------------------|------------------|--|--------|------|-------|------|
|                                   |                  |  | Min.   | Typ. | Max.  |      |
| External interrupt disable period | T <sub>NUL</sub> | Interrupt: Enabled (MIE = 1),<br>CPU: NOP operation<br>System clock: 32.768kHz | 76.8   | —    | 106.8 | μs   |

**AC CHARACTERISTICS (Serial Port)**(V<sub>DD</sub> = 1.25 to 3.6V, V<sub>SS</sub> = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

| Parameter          | Symbol            | Condition | Rating                   |                   |                          | Unit |
|--------------------|-------------------|-----------|--------------------------|-------------------|--------------------------|------|
|                    |                   |           | Min.                     | Typ.              | Max.                     |      |
| Transmit baud rate | t <sub>TBRT</sub> | —         | —                        | BRT* <sup>1</sup> | —                        | s    |
| Receive baud rate  | t <sub>RBRT</sub> | —         | BRT* <sup>1</sup><br>-3% | BRT* <sup>1</sup> | BRT* <sup>1</sup><br>+3% | s    |

\*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



\*: Indicates the secondary function of the port.

**AC CHARACTERISTICS (Synchronous Serial Port)**(V<sub>DD</sub> = 1.25 to 3.6V, V<sub>SS</sub> = 0V, T<sub>a</sub> = -20 to +70°C, T<sub>a</sub> = -40 to +85°C for P version, unless otherwise specified)

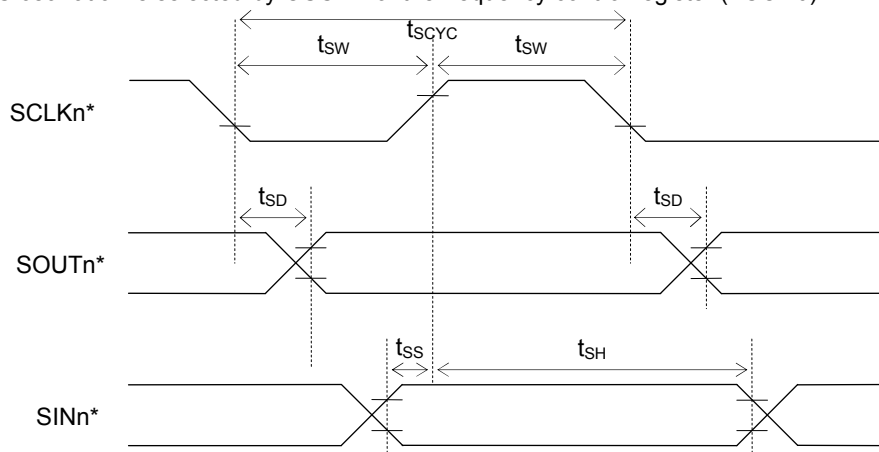
| Parameter                                 | Symbol            | Condition  | Rating          |                 |                 | Unit |
|---|-------------------|--|-----------------|-----------------|-----------------|------|
|   |                   |  | Min.            | Typ.            | Max.            |      |
| SCLKn input cycle<br>(slave mode)         | t <sub>SCYC</sub> | When RC oscillation is 500kHz<br>*2 (V <sub>DD</sub> = 1.25 to 3.6V)                     | 10              | —               | —               | μs   |
|   |                   | When RC oscillation is 2MHz<br>*3 (V <sub>DD</sub> = 1.8 to 3.6V)                        | 2               | —               | —               |      |
| SCLKn output cycle<br>(master mode)       | t <sub>SCYC</sub> | —  | —               | SCLKn*1         | —               | s    |
| SCLKn input pulse width<br>(slave mode)   | t <sub>SW</sub>   | When RC oscillation is 500kHz<br>*2 (V <sub>DD</sub> = 1.25 to 3.6V)                     | 4               | —               | —               | μs   |
|   |                   | When RC oscillation is 2MHz<br>*3 (V <sub>DD</sub> = 1.8 to 3.6V)                        | 04              | —               | —               |      |
| SCLKn output pulse width<br>(master mode) | t <sub>SW</sub>   | —  | SCLKn*1<br>×0.4 | SCLKn*1<br>×0.5 | SCLKn*1<br>×0.6 | s    |
| SOUTn output delay time<br>(slave mode)   | t <sub>SD</sub>   | When RC oscillation is 500kHz<br>*2 (V <sub>DD</sub> = 1.25 to 3.6V)<br>output load 10pF | —               | —               | 500             | ns   |
|   |                   | When RC oscillation is 2MHz<br>*3 (V <sub>DD</sub> = 1.8 to 3.6V)<br>output load 10pF    | —               | —               | 240             |      |
| SOUTn output delay time<br>(master mode)  | t <sub>SD</sub>   | When RC oscillation is 500kHz<br>*2 (V <sub>DD</sub> = 1.25 to 3.6V)<br>output load 10pF | —               | —               | 500             | ns   |
|   |                   | When RC oscillation is 2MHz<br>*3 (V <sub>DD</sub> = 1.8 to 3.6V)<br>output load 10pF    | —               | —               | 240             |      |
| SINn input setup time<br>(slave mode)     | t <sub>SS</sub>   | —  | 80              | —               | —               | ns   |
| SINn input setup time<br>(master mode)    | t <sub>SS</sub>   | When RC oscillation is 500kHz<br>*2 (V <sub>DD</sub> = 1.25 to 3.6V)                     | 500             | —               | —               | ns   |
|   |                   | When RC oscillation is 2MHz<br>*3 (V <sub>DD</sub> = 1.8 to 3.6V)                        | 240             | —               | —               |      |
| SINn input hold time                      | t <sub>SH</sub>   | When RC oscillation is 500kHz<br>*2 (V <sub>DD</sub> = 1.25 to 3.6V)                     | 300             | —               | —               | ns   |
|   |                   | When RC oscillation is 2MHz<br>*3 (V <sub>DD</sub> = 1.8 to 3.6V)                        | 80              | —               | —               |      |

n= 0,1

\*1: Clock period selected with SnCK3-0 of the serial port n mode register (SIO nMOD1)

\*2: When 500kHz RC oscillation is selected by OSCM2 of the frequency control register (FCON0)

\*3: When 2MHz RC oscillation is selected by OSCM2 of the frequency control register (FCON0)



\*: Indicates the secondary function of the port (n= 0,1)

**AC CHARACTERISTICS (RC Oscillation A/D Converter)**

Condition for  $V_{DD}=1.8$  to  $3.6V$

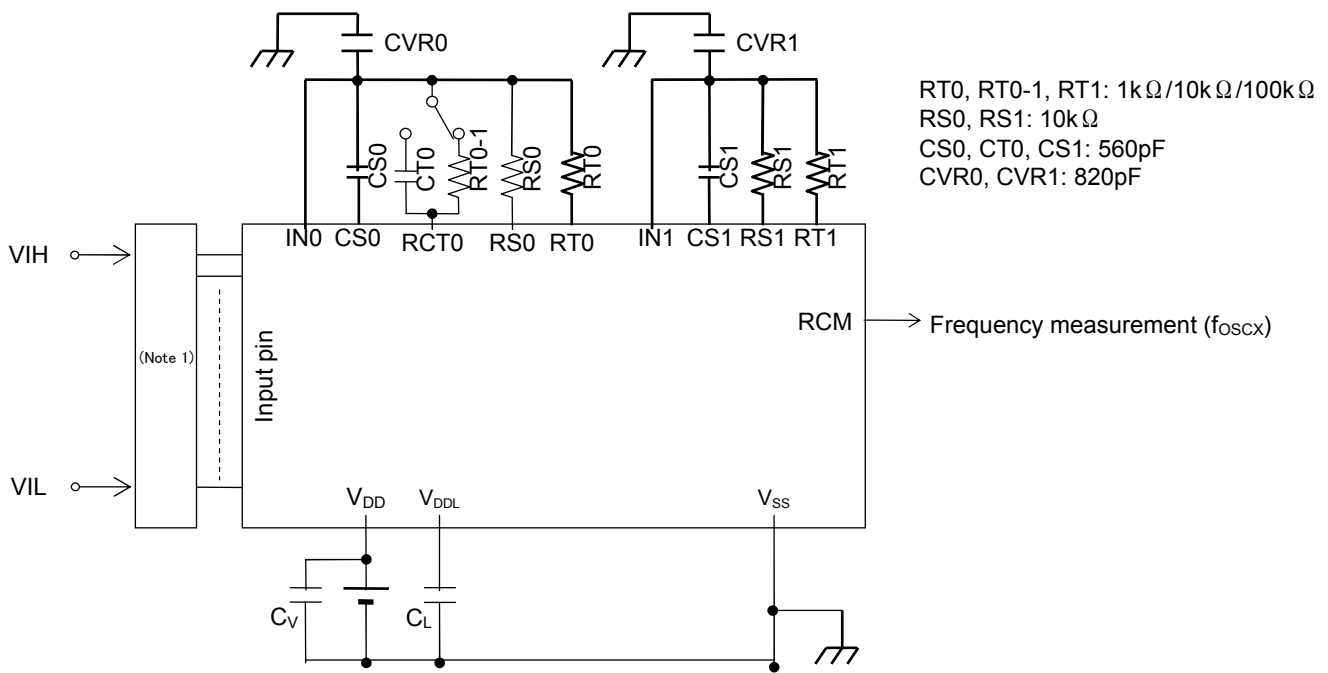
( $V_{DD}=1.8$  to  $3.6V$ ,  $V_{SS}=0V$ ,  $T_a=-20$  to  $+70^{\circ}C$ ,  $T_a=-40$  to  $+85^{\circ}C$  for P version, unless otherwise specified)

| Parameter  | Symbol                 | Condition                              | Rating |       |       | Unit       |
|--|------------------------|--|--------|-------|-------|------------|
|  |                        |  | Min.   | Typ.  | Max.  |            |
| Oscillation resistor   | RS0,RS1,RT0, RT0-1,RT1 | CS0, CT0, CS1 $\geq$ 740pF             | 1      | —     | —     | k $\Omega$ |
| Oscillation frequency<br>$V_{DD} = 3.0V$                                 | $f_{OSC1}$             | Resistor for oscillation=1k $\Omega$   | 457.3  | 525.2 | 575.1 | kHz        |
|  | $f_{OSC2}$             | Resistor for oscillation=10k $\Omega$  | 53.48  | 58.18 | 62.43 | kHz        |
|  | $f_{OSC3}$             | Resistor for oscillation=100k $\Omega$ | 5.43   | 5.89  | 6.32  | kHz        |
| RS to RT oscillation<br>frequency ratio <sup>*1</sup><br>$V_{DD} = 3.0V$ | Kf1                    | RT0, RT0-1, RT1=1k $\Omega$            | 7.972  | 9.028 | 9.782 | —          |
|  | Kf2                    | RT0, RT0-1, RT1=10k $\Omega$           | 0.981  | 1     | 1.019 | —          |
|  | Kf3                    | RT0, RT0-1, RT1=100k $\Omega$          | 0.099  | 0.101 | 0.104 | —          |

\*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{oscx}(RT0-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})} \quad , \quad \frac{f_{oscx}(RT0-1-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})} \quad , \quad \frac{f_{oscx}(RT1-CS1 \text{ oscillation})}{f_{oscx}(RS1-CS1 \text{ oscillation})}$$

( x = 1, 2, 3 )



\*1: Input logic circuit to determine the specified measuring conditions.

Condition for  $V_{DD}=1.25$  to  $3.6V$

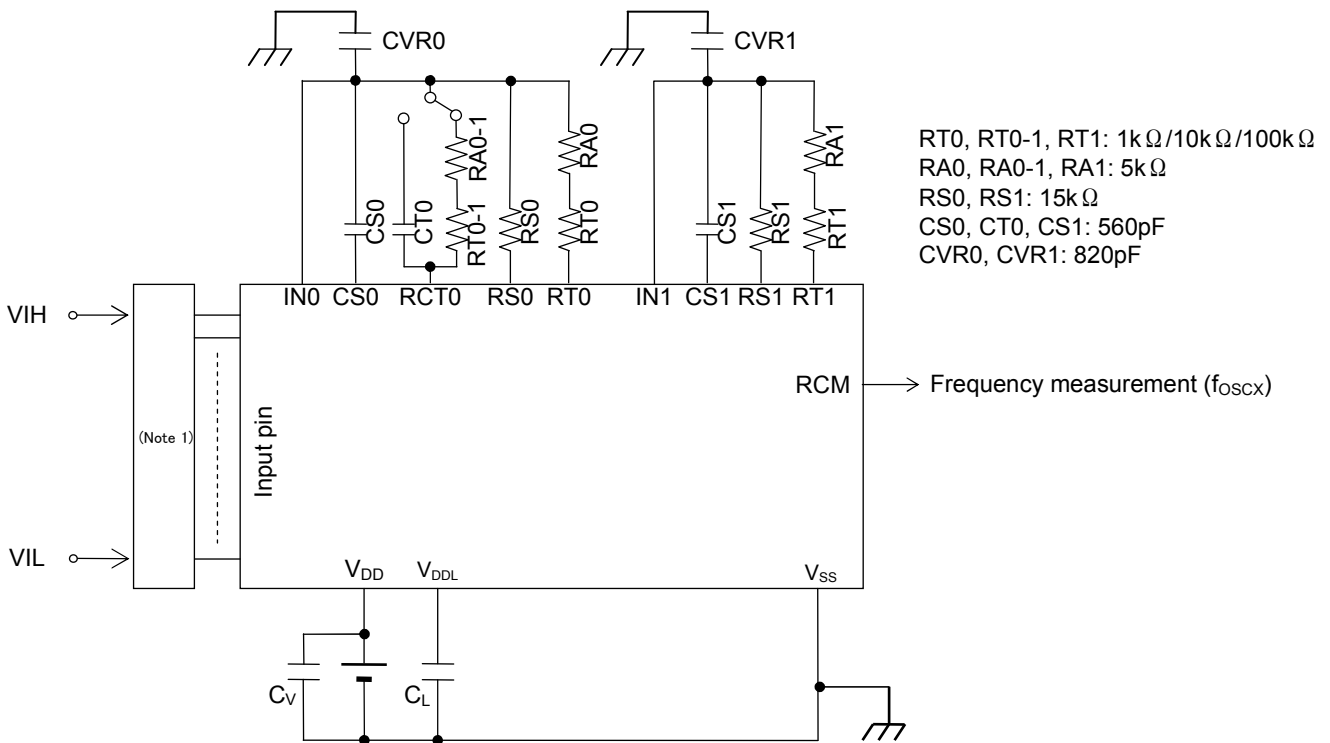
( $V_{DD}=1.25$  to  $3.6V$ ,  $V_{SS}=0V$ ,  $T_a=-20$  to  $+70^{\circ}C$ ,  $T_a=-40$  to  $+85^{\circ}C$  for P version, unless otherwise specified)

| Parameter  | Symbol                 | Condition                              | Rating |       |       | Unit       |
|--|------------------------|--|--------|-------|-------|------------|
|  |                        |  | Min.   | Typ.  | Max.  |            |
| Oscillation resistor   | RS0,RS1,RT0, RT0-1,RT1 | CS0, CT0, CS1 $\geq$ 740pF             | 1      | —     | —     | k $\Omega$ |
| Oscillation frequency<br>$V_{DD} = 1.5V$                                 | $f_{OSC1}$             | Resistor for oscillation=6k $\Omega$   | 81.93  | 93.16 | 101.2 | kHz        |
|  | $f_{OSC2}$             | Resistor for oscillation=15k $\Omega$  | 35.32  | 38.75 | 41.48 | kHz        |
|  | $f_{OSC3}$             | Resistor for oscillation=105k $\Omega$ | 5.22   | 5.65  | 6.03  | kHz        |
| RS to RT oscillation<br>frequency ratio <sup>*1</sup><br>$V_{DD} = 1.5V$ | Kf1                    | RT0, RT0-1, RT1=1k $\Omega$            | 2.139  | 2.381 | 2.632 | —          |
|  | Kf2                    | RT0, RT0-1, RT1=10k $\Omega$           | 0.973  | 1     | 1.028 | —          |
|  | Kf3                    | RT0, RT0-1, RT1=100k $\Omega$          | 0.142  | 0.147 | 0.152 | —          |
| Oscillation frequency<br>$V_{DD} = 3.0V$                                 | $f_{OSC1}$             | Resistor for oscillation=6k $\Omega$   | 85.28  | 94.58 | 103.3 | kHz        |
|  | $f_{OSC2}$             | Resistor for oscillation=15k $\Omega$  | 35.72  | 38.87 | 41.78 | kHz        |
|  | $f_{OSC3}$             | Resistor for oscillation=105k $\Omega$ | 5.189  | 5.622 | 6.012 | kHz        |
| RS to RT oscillation<br>frequency ratio <sup>*1</sup><br>$V_{DD} = 3.0V$ | Kf1                    | RT0, RT0-1, RT1=1k $\Omega$            | 2.227  | 2.432 | 2.626 | —          |
|  | Kf2                    | RT0, RT0-1, RT1=10k $\Omega$           | 0.982  | 1     | 1.018 | —          |
|  | Kf3                    | RT0, RT0-1, RT1=100k $\Omega$          | 0.141  | 0.145 | 0.149 | —          |

\*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})}, \frac{f_{OSCx}(RT0-1-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})}, \frac{f_{OSCx}(RT1-CS1 \text{ oscillation})}{f_{OSCx}(RS1-CS1 \text{ oscillation})}$$

(x = 1, 2, 3)



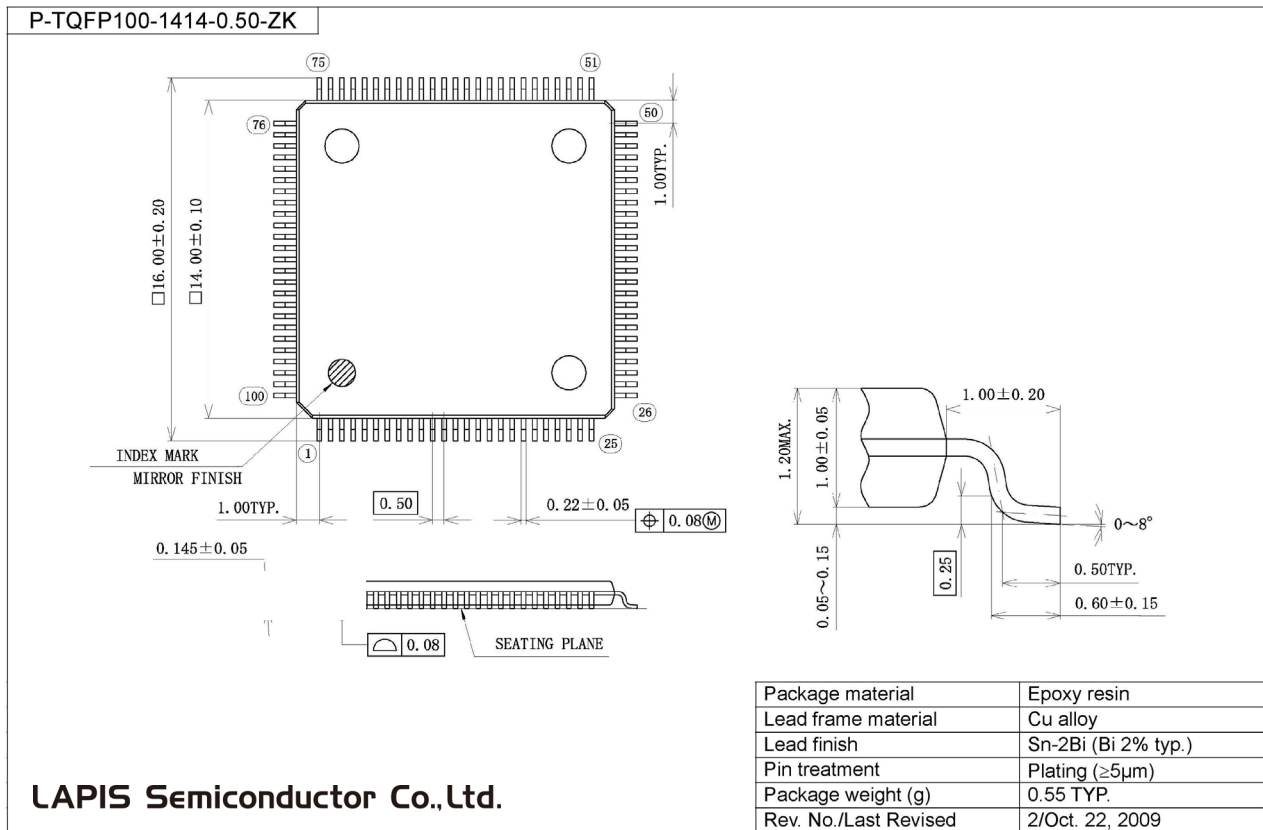
\*1: Input logic circuit to determine the specified measuring conditions.

Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Package Dimensions

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

| Document No.   | Date        | Page             |                 | Description                                   |
|----------------|-------------|------------------|-----------------|---|
|                |             | Previous Edition | Current Edition |   |
| FEDL610Q409-01 | Nov.7,2010  | –                | –               | Formally edition 1                            |
| FEDL610Q409-02 | Jul.12,2011 | 2                | 2               | Add comment of uart half duplex communication |
|                |             | 3                | 3               | Add "D" version in the supply form            |

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