
ML610401/ML610402/ML610403

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

ML610401/ML610402/ML610403 is a high-performance 8-bit CMOS microcontroller into which peripheral circuits, such as UART, melody driver, RC oscillation type A/D converter, and LCD driver, are incorporated around LAPIS Semiconductor -original 8-bit CPU nX-U8/100. ML610401/ML610402/ML610403 operates in both high/low-speed mode and power-saving mode, it is most suitable for battery operated products.

ML610401P/ ML610402P/ML610403P support industrial temperature -40°C to +85°C, are added to the product lineup.

FEATURES

- CPU
 - 8-bit RISC CPU (CPU name: nX-U8/100)
 - Instruction system: 16-bit instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - Minimum instruction execution time
 - 30.5 μ s (@32.768 kHz system clock)
 - 2 μ s (@500kHz system clock)
- Internal memory
 - Internal 6KByte Mask ROM (3K \times 16 bits) (including unusable 256 Byte TEST area)
 - Internal 192Byte Data RAM (192 \times 8 bits)
- Interrupt controller
 - 1 non-maskable interrupt sources
 - Internal source: 1 (Watch dog timer)
 - 17 maskable interrupt sources
 - Internal sources: 9 (Timer2, Timer3, UART0, Melody0, RC-A/D converter, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
 - External sources: 8 (P00, P01, P02, P03, P50, P51, P52, P53)
 - (One interrupt request is generated from P50 to P53 interrupt sources.)
- Time base counter
 - Low-speed time base counter \times 1 channel
 - Frequency compensation (Compensation range: Approx. -488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
 - High-speed time base counter \times 1 channel
- Watchdog timer
 - Non-maskable interrupt and reset
 - Free running
 - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)
- Timers
 - 8 bits \times 2 channels (16-bit \times 1 configuration available by using Timer2-3)
 - Clock frequency measurement mode (in one channel of 16-bit configuration)
- Capture
 - Time base capture \times 2 channels (4096 Hz to 32 Hz)

- UART
 - TXD/RXD × 1 channel
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- Melody driver
 - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
 - Tone length: 63 types
 - Tempo: 15 types
 - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)
- RC oscillation type A/D converter
 - 16-bit counter
 - Time division × 2 channels
- General-purpose ports
 - Input-only port × 4 channels (including secondary functions)
 - Output-only port
 - ML610401: × 12 channels (including secondary functions)
 - ML610402: × 8 channels (including secondary functions)
 - ML610403: × 4 channels (including secondary functions)
 - Input/output port × 18 channels (including secondary functions)
- LCD driver
 - The number of segments
 - ML610401: 55 dots max. (11seg×5com, 12seg×4com, 13seg×3com, and 14seg×2com selectable)
 - ML610402: 75 dots max. (15seg×5com, 16seg×4com, 17seg×3com, and 18seg×2com selectable)
 - ML610403: 95 dots max. (19seg×5com, 20seg×4com, 21seg×3com, and 22seg×2com selectable)
 - 1/1 to 1/5 duty
 - 1/2, 1/3 bias (built-in bias generation circuit)
 - Frame frequency selectable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
 - Bias voltage multiplying clock selectable (8 types)
 - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
 - Programmable display allocation function
- Reset
 - Reset through the RESET_N pin
 - Power-on reset generation when powered on
 - Reset when oscillation stop of the low-speed clock is detected (Cancellation by a mask option is possible)
 - Reset by the watchdog timer (WDT) overflow
- Clock
 - Low-speed clock: Crystal oscillation (32.768 kHz)
(This LSI can not guarantee the operation without low-speed crystal oscillation clock)
 - High-speed clock: Built-in RC oscillation (500 kHz)
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
 - Block Control Function: Resets and completely turns circuits of unused peripherals off.

- Shipment
 - Chip
 - ML610401-xxxWA
 - ML610402-xxxWA
 - ML610403-xxxWA
 - ML610401P-xxxWA
 - ML610402P-xxxWA
 - ML610403P-xxxWA
 - 64-pin plastic TQFP
 - ML610401-xxxTBZ03A
 - ML610402-xxxTBZ03A
 - ML610403-xxxTBZ03A
 - ML610401P-xxxTBZ03A
 - ML610402P-xxxTBZ03A
 - ML610403P-xxxTBZ03A

- xxx: ROM code number
- P: Wide range temperature version
- WA: Chip
- TBZ03A: TQFP

- Guaranteed operating range
 - Operating temperature: -20°C to $+70^{\circ}\text{C}$ (P version: -40°C to $+85^{\circ}\text{C}$)
 - Operating voltage: $V_{\text{DD}} = 1.25\text{V}$ to 3.6V

ML610401/ML610402/ML610403 Block Diagram

Figure 1 show the block diagram of the ML610401/ML610402/ML610403.

"*" indicates the secondary function of each port.

"(*1)": 11seg×5com, 12seg×4com, 13seg×3com, and 14seg×2com selectable

"(*2)": 15seg×5com, 16seg×4com, 17seg×3com, and 18seg×2com selectable

"(*3)": 19seg×5com, 20seg×4com, 21seg×3com, and 22seg×2com selectable

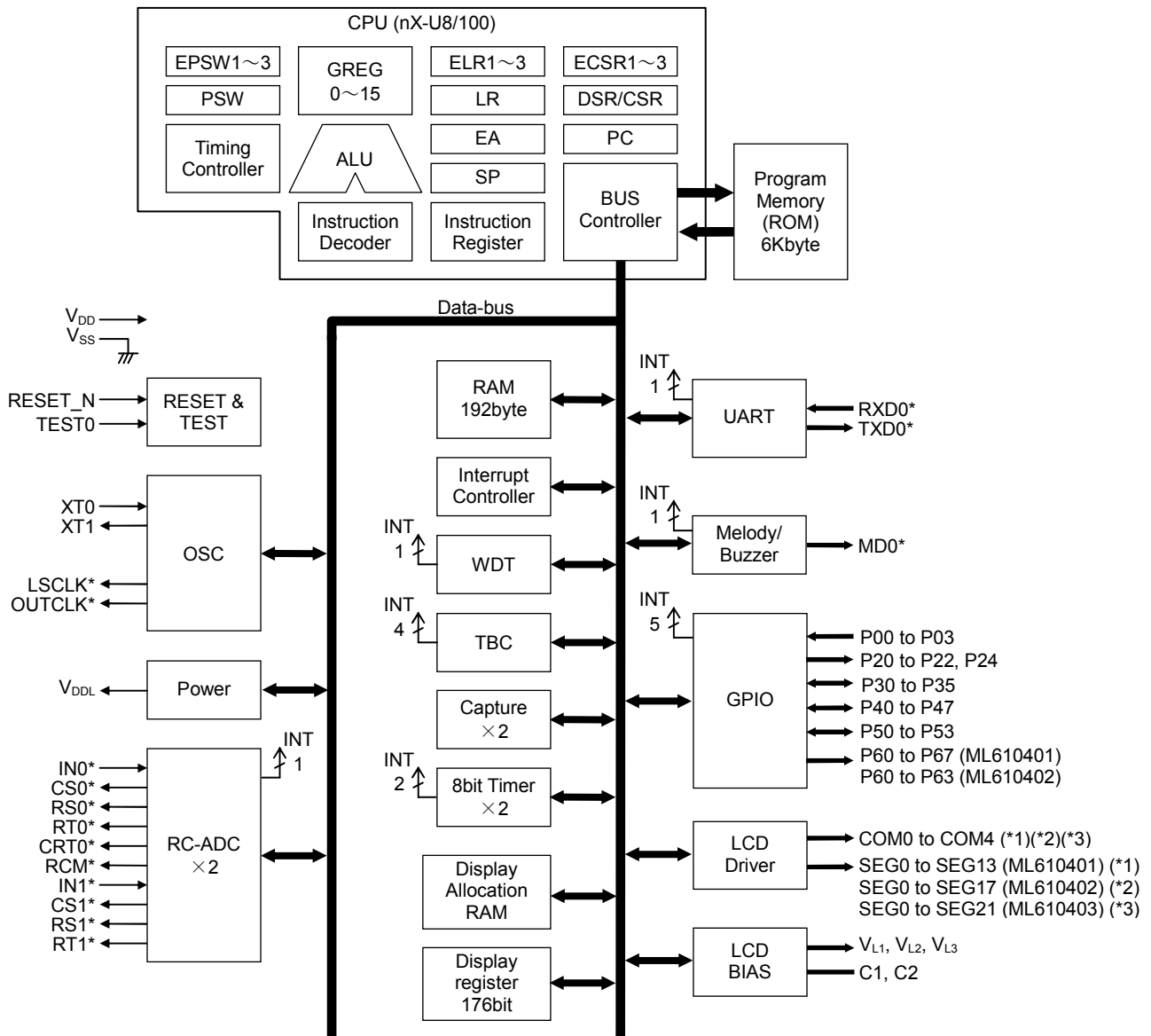
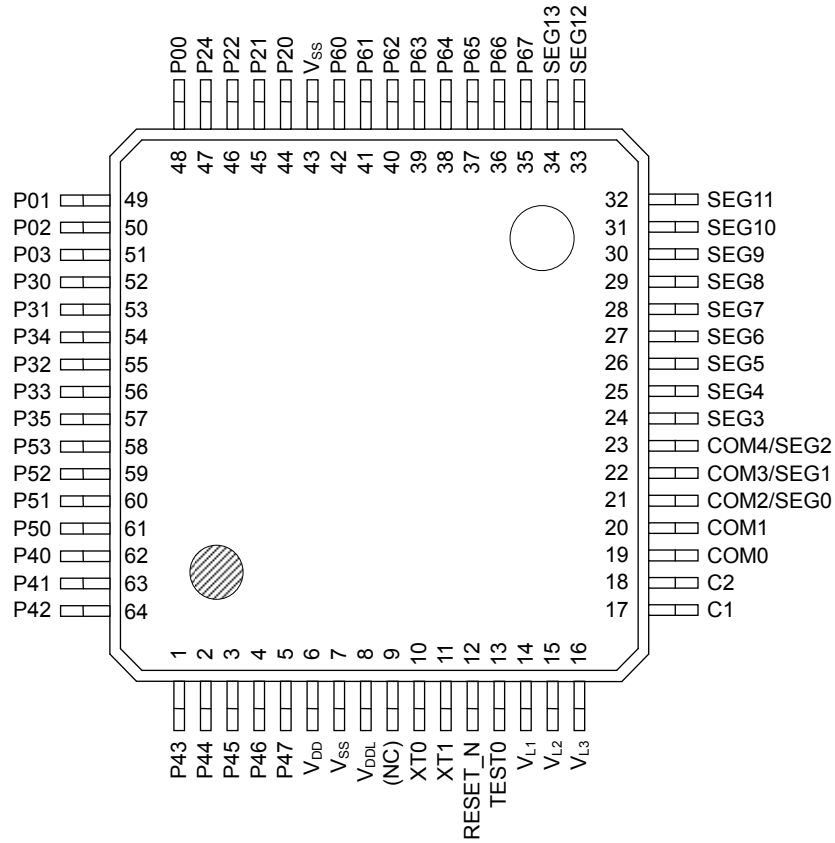


Figure 1 ML610401/ML610402/ML610403 Block Diagram

PIN CONFIGURATION

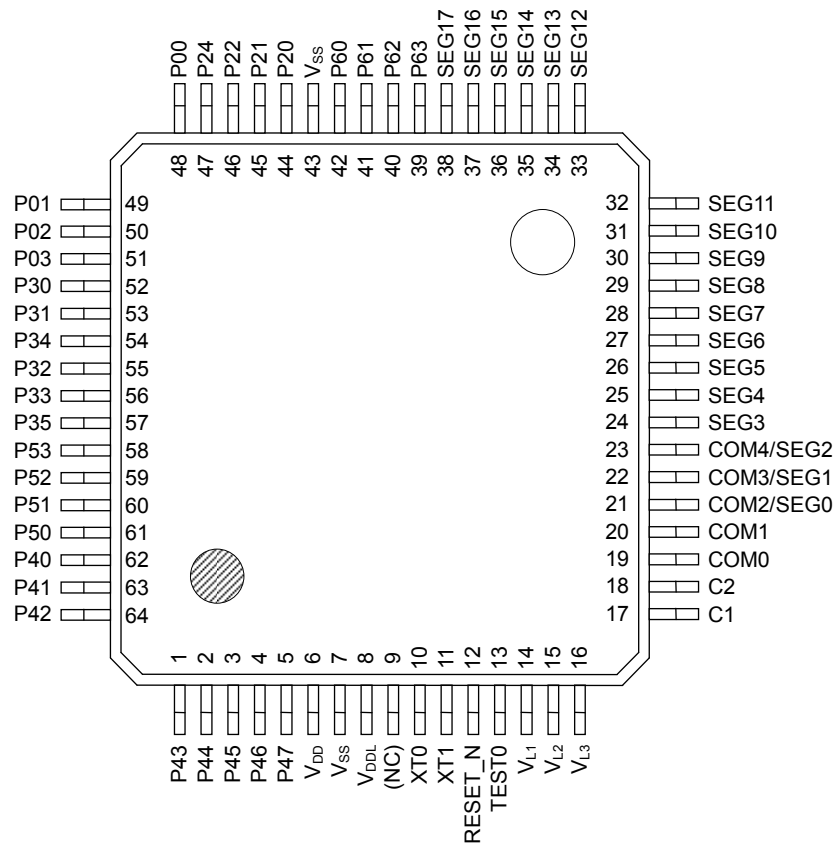
ML610401 TQFP64 Pin Layout



Note:
The assignment of the P30 to P35 are not in order.

Figure 2 ML610401 TQFP64 Pin Configuration

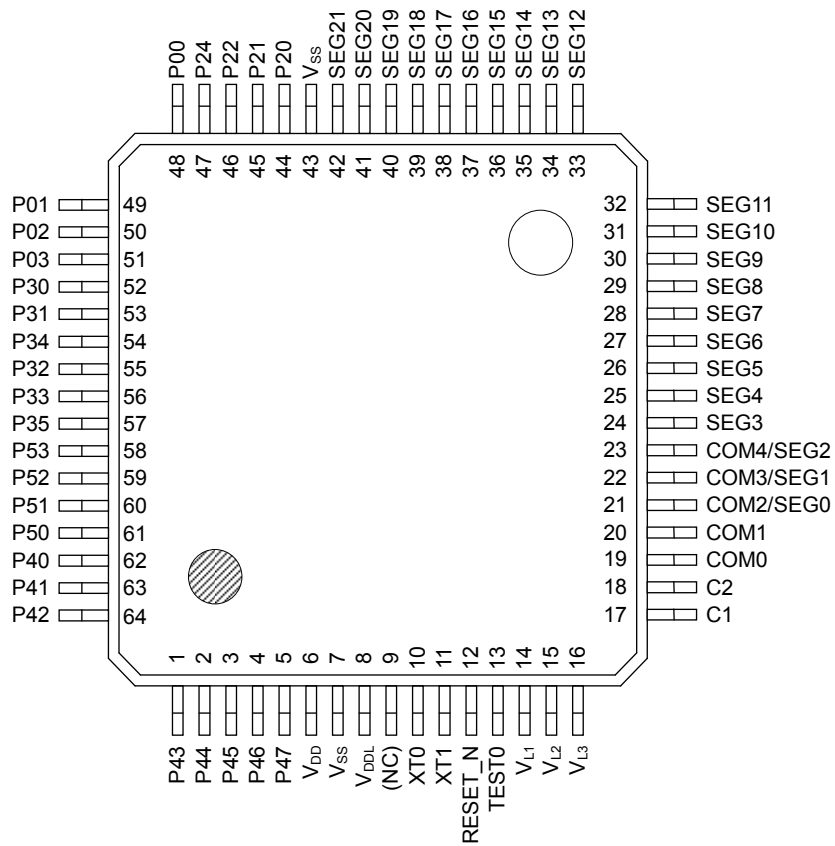
ML610402 TQFP64 Pin Layout



Note:
 The assignment of the P30 to P35 are not in order.

Figure 3 ML610402 TQFP64 Pin Configuration

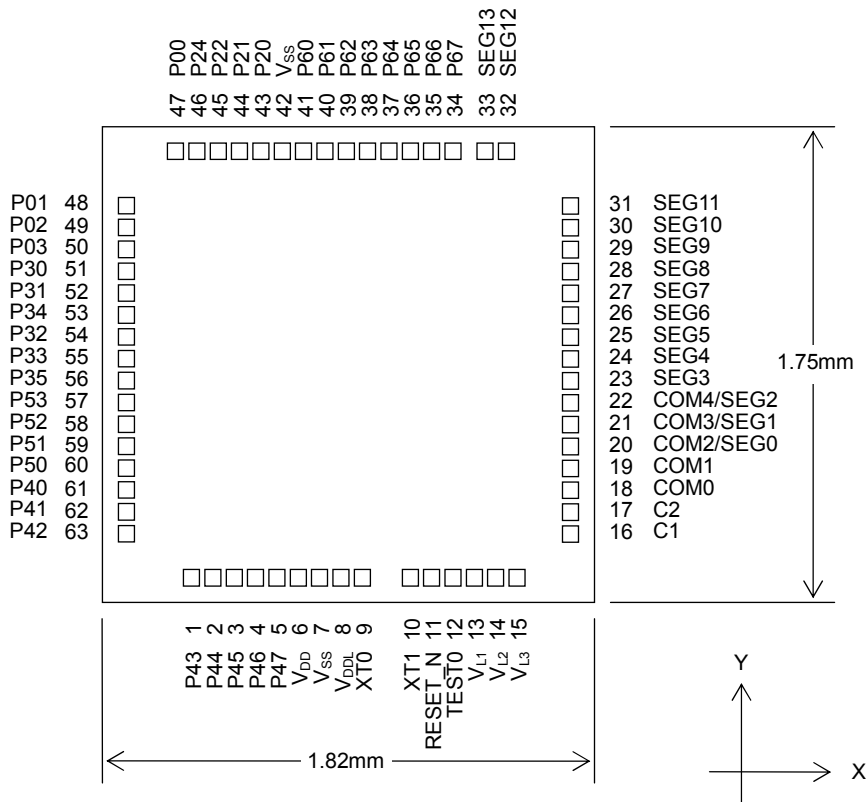
ML610403 TQFP64 Pin Layout



Note:
The assignment of the P30 to P35 are not in order.

Figure 4 ML610403 TQFP64 Pin Configuration

ML610401 Chip Pin Layout & Dimension

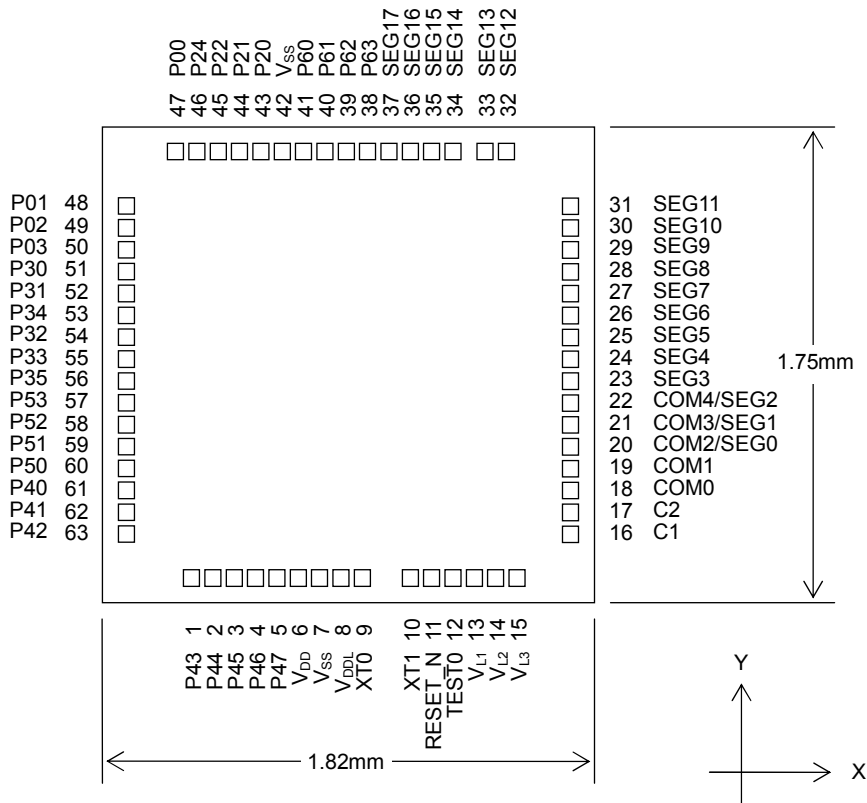


Note:
The assignment of the pads P30 to P35 are not in order.

- Chip size: 1.82 mm × 1.75 mm
- PAD count: 63 pins
- Minimum PAD pitch: 80μm
- PAD aperture: 70μm×70μm
- Chip thickness: 350μm
- Voltage of the rear side of chip: V_{SS} level.

Figure 5 ML610401 Chip Layout & Dimension

ML610402 Chip Pin Layout & Dimension

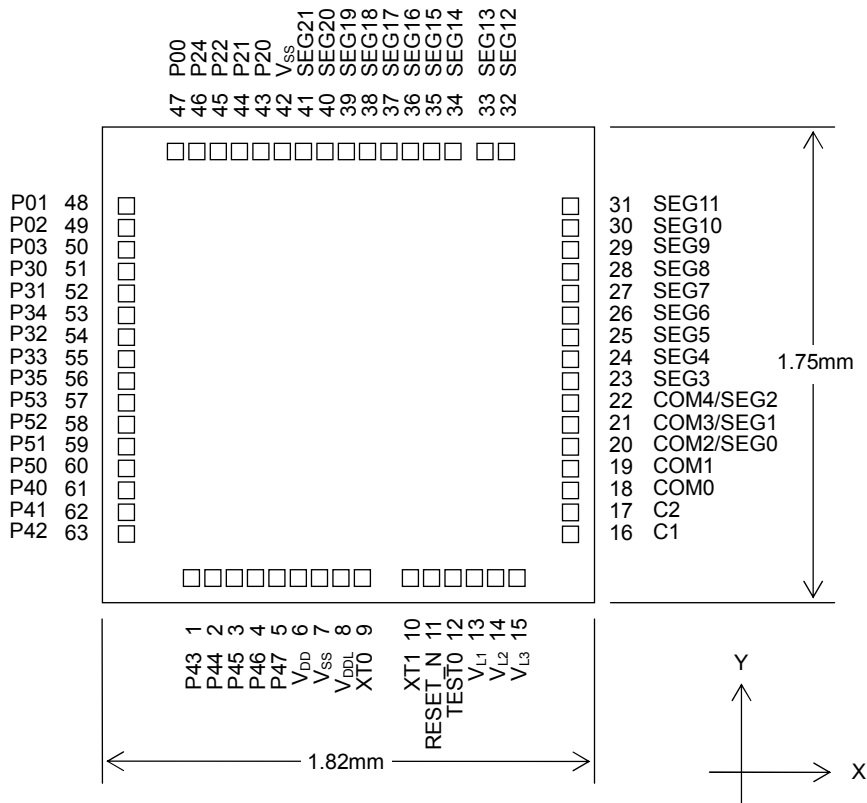


Note:
The assignment of the pads P30 to P35 are not in order.

- Chip size: 1.82 mm × 1.75 mm
- PAD count: 63 pins
- Minimum PAD pitch: 80µm
- PAD aperture: 70µm×70µm
- Chip thickness: 350µm
- Voltage of the rear side of chip: V_{SS} level.

Figure 6 ML610402 Chip Layout & Dimension

ML610403 Chip Pin Layout & Dimension



Note:
The assignment of the pads P30 to P35 are not in order.

- Chip size: 1.82 mm × 1.75 mm
- PAD count: 63 pins
- Minimum PAD pitch: 80 μm
- PAD aperture: 70 μm×70 μm
- Chip thickness: 350 μm
- Voltage of the rear side of chip: V_{SS} level.

Figure 7 ML610403 Chip Layout & Dimension

ML610401/ML610402/ML610403 Pad Coordinates

Table 1 ML610401/ML610402/ML610403 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610401/2/3		PAD No.	Pad Name	ML610401/2/3	
		X (μm)	Y (μm)			X (μm)	Y (μm)
1	P43	-598	-769	35	P66 ^(*)	375	769
2	P44	-518	-769		SEG15 ^(*) (*)		
3	P45	-438	-769	36	P65 ^(*)	295	769
4	P46	-358	-769		SEG16 ^(*) (*)		
5	P47	-278	-769	37	P64 ^(*)	215	769
6	V _{DD}	-198	-769		SEG17 ^(*) (*)		
7	V _{SS}	-118	-769	38	P63 ^(*) (*)	135	769
8	V _{DLL}	-38	-769		SEG18 ^(*)		
9	XT0	42	-769	39	P62 ^(*) (*)	55	769
10	XT1	202	-769		SEG19 ^(*)		
11	RESET_N	282	-769	40	P61 ^(*) (*)	-25	769
12	TEST0	362	-769		SEG20 ^(*)		
13	VL1	522	-769	41	P60 ^(*) (*)	-105	769
14	VL2	602	-769		SEG21 ^(*)		
15	VL3	682	-769	42	V _{SS}	-185	769
16	C1	804	-600	43	P20	-265	769
17	C2	804	-520	44	P21	-345	769
18	COM0	804	-440	45	P22	-425	769
19	COM1	804	-360	46	P24	-505	769
20	COM2/SEG0	804	-280	47	P00	-605	769
21	COM3/SEG1	804	-200	48	P01	-804	600
22	COM4/SEG2	804	-120	49	P02	-804	520
23	SEG3	804	-40	50	P03	-804	440
24	SEG4	804	40	51	P30	-804	360
25	SEG5	804	120	52	P31	-804	280
26	SEG6	804	200	53	P34	-804	200
27	SEG7	804	280	54	P32	-804	120
28	SEG8	804	360	55	P33	-804	40
29	SEG9	804	440	56	P35	-804	-40
30	SEG10	804	520	57	P53	-804	-120
31	SEG11	804	600	58	P52	-804	-200
32	SEG12	645	769	59	P51	-804	-280
33	SEG13	565	769	60	P50	-804	-360
34	P67 ^(*)	455	769	61	P40	-804	-440
	SEG14 ^(*) (*)			62	P41	-804	-520
				63	P42	-804	-600

(*) ML610401 pad name, (**) ML610402 pad name, (***) ML610403 pad name

PIN LIST

PIN No.	PAD No.	Primary function			Secondary function		
		Pin name	I/O	Function	Pin name	I/O	Function
7,43	7,42	V _{SS}	—	Negative power supply pin	—	—	—
6	6	V _{DD}	—	Positive power supply pin	—	—	—
8	8	V _{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—
14	13	V _{L1}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin) ⁽²⁾	—	—	—
15	14	V _{L2}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin) ⁽²⁾	—	—	—
16	15	V _{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—
17	16	C1	—	Capacitor connection pin for LCD bias generation	—	—	—
18	17	C2	—	Capacitor connection pin for LCD bias generation	—	—	—
13	12	TEST0	I	Test pin	—	—	—
12	11	RESET_N	I	Reset input pin	—	—	—
10	9	XT0	I	Low-speed clock oscillation pin	—	—	—
11	10	XT1	O	Low-speed clock oscillation pin	—	—	—
48	47	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—
49	48	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—
50	49	P02/EXI2/ RXD0	I	Input port, External interrupt, UART0 received data	—	—	—
51	50	P03/EXI3	I	Input port, External interrupt	—	—	—
44	43	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output
45	44	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output
46	45	P22/LED2	O	Output port	MD0	O	Melody 0 output
47	46	P24/LED4	O	Output port	—	—	—
52	51	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin
53	52	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin
54	53	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin
55	54	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin
56	55	P33	I/O	Input/output port	RT0	O	RC type ADC0 measurement resistor sensor connection pin
57	56	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor
62	61	P40	I/O	Input/output port	—	—	—
63	62	P41	I/O	Input/output port	—	—	—
64	63	P42	I/O	Input/output port	RXD0	I	UART data input
1	1	P43	I/O	Input/output port	TXD0	O	UART data output
2	2	P44/T2CK	I/O	Input/output port, Timer2 external clock input	IN1	I	RC type ADC1 oscillation input pin
3	3	P45/T3CK	I/O	Input/output port, Timer3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin
4	4	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin
5	5	P47	I/O	Input/output port	RT1	O	RC type ADC1 measurement resistor sensor connection pin
61	60	P50/EXI8	I/O	Input/output port, External interrupt	MD0	O	Melody 0 output
60	59	P51/EXI8	I/O	Input/output port, External interrupt	—	—	—

PIN No.	PAD No.	Primary function			Secondary function		
		Pin name	I/O	Function	Pin name	I/O	Function
59	58	P52/EXI8	I/O	Input/output port, External interrupt	—	—	—
58	57	P53/EXI8	I/O	Input/output port, External interrupt	—	—	—
19	18	COM0	O	LCD common pin	—	—	—
20	19	COM1	O	LCD common pin	—	—	—
21	20	COM2/SEG 0	O	LCD common/segment pin	—	—	—
22	21	COM3/SEG 1	O	LCD common/segment pin	—	—	—
23	22	COM4/SEG 2	O	LCD common/segment pin	—	—	—
24	23	SEG3	O	LCD segment pin	—	—	—
25	24	SEG4	O	LCD segment pin	—	—	—
26	25	SEG5	O	LCD segment pin	—	—	—
27	26	SEG6	O	LCD segment pin	—	—	—
28	27	SEG7	O	LCD segment pin	—	—	—
29	28	SEG8	O	LCD segment pin	—	—	—
30	29	SEG9	O	LCD segment pin	—	—	—
31	30	SEG10	O	LCD segment pin	—	—	—
32	31	SEG11	O	LCD segment pin	—	—	—
33	32	SEG12	O	LCD segment pin	—	—	—
34	33	SEG13	O	LCD segment pin	—	—	—
35	34	P67 ^(*2)	O	Output port	—	—	—
		SEG14 ^(*3)	O	LCD segment pin	—	—	—
36	35	P66 ^(*2)	O	Output port	—	—	—
		SEG15 ^(*3)	O	LCD segment pin	—	—	—
37	36	P65 ^(*2)	O	Output port	—	—	—
		SEG16 ^(*3)	O	LCD segment pin	—	—	—
38	37	P64 ^(*2)	O	Output port	—	—	—
		SEG17 ^(*3)	O	LCD segment pin	—	—	—
39	38	P63 ^(*4)	O	Output port	—	—	—
		SEG18 ^(*5)	O	LCD segment pin	—	—	—
40	39	P62 ^(*4)	O	Output port	—	—	—
		SEG19 ^(*5)	O	LCD segment pin	—	—	—
41	40	P61 ^(*4)	O	Output port	—	—	—
		SEG20 ^(*5)	O	LCD segment pin	—	—	—
42	41	P60 ^(*4)	O	Output port	—	—	—
		SEG21 ^(*5)	O	LCD segment pin	—	—	—

(*¹) Internally generated, or connect to either positive power supply pin (V_{DD}) or power supply pin for internal logic (V_{DDL}). For details, see user's manual.

(*²) Pin for ML610401/ML610402.

(*³) Pin for ML610403.

(*⁴) Pin for ML610401.

(*⁵) Pin for ML610402/ML610403.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V _{SS} .	—	—
XT1	O		—	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port.	Primary	Positive
General-purpose output port				
P20-P22,P24	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P50-P53	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P60-P63	O	General-purpose output port. These pins are for the ML610401/ML610402, but are not provided in the ML610403.	Primary	Positive
P64-P67	O	General-purpose output port. These pins are for the ML610401, but are not provided in the ML610402/ML610403.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
External interrupt				
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
EXI8		External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P50-P53 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software.	Primary	Positive/ negative
CAP1	I	These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
Timer				
T2CK	I	External clock input pin used for Timer 2. The clock for this timer is selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T3CK	I	External clock input pin used for Timer 3. The clock for this timer is selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/Buzzer signal output pin. This pin is used as the secondary function of the P22 pin and P50 pin.	Secondary	Positive/ negative
LED drive				
LED0-2,4	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive signal				
COM0-4	O	Common output pins.	—	—
SEG0-13	O	Segment output pins.	—	—
SEG14-17	O	Segment output pin. These pins are for the ML610402/ML610403, but are not provided in the ML610401.	—	—
SEG18-21	O	Segment output pin. These pins are for the ML610403, but are not provided in the ML610401/ML610402.	—	—
LCD driver power supply				
V _{L1}	—	Power supply pins for LCD bias (internally generated or positive power supply pin connected). Depending on LCD Bias setting and V _{DD} voltage level, V _{DD} or V _{DDL} or capacitor is connected. For details of the connection method, see user's manual.	—	—
V _{L2}	—		—	—
V _{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2.	—	—
C2	—		—	—
For testing				
TEST0	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V _{SS}	—	Negative power supply pin.	—	—
V _{DD}	—	Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.	—	—
V _{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitor CL (see Appendix C measuring circuit 1) is connected between this pin and V _{SS} .	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin termination
V _{L1} , V _{L2} , V _{L3}	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
P00 to P03	V _{DD} or V _{SS}
P20 to P22, P24	Open
P30 to P35	Open
P40 to P47	Open
P50 to P53	Open
P60 to P67	Open
COM0 to 4	Open
SEG0 to 21	Open

Note:

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS**(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	-0.3 to +4.6	V
Power supply voltage 2	V _{DDL}	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 3	V _{L1}	Ta = 25°C	-0.3 to +2.0	V
Power supply voltage 4	V _{L2}	Ta = 25°C	-0.3 to +4.0	V
Power supply voltage 5	V _{L3}	Ta = 25°C	-0.3 to +6.0	V
Input voltage	V _{IN}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Output voltage	V _{OUT}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port3-6, Ta = 25°C	-12 to +11	mA
Output current 2	I _{OUT2}	Port2, Ta = 25°C	-12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T _{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	non-P version	-20 to +70	°C
		P version	-40 to +85	
Operating voltage	V _{DD}	f _{OP} = 30k to 625kHz	1.25 to 3.6	V
Operating frequency (CPU)	f _{OP}	V _{DD} = 1.25 to 3.6V	30k to 625k	Hz
Low-speed crystal oscillation frequency	f _{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C _{DL}	—	3 to 18	pF
	C _{GL}	—	3 to 18	
Capacitor externally connected to V _{DDL} pin	C _L	—	0.47±30%	μF
Capacitors externally connected to V _{L1, 2, 3} pins	C _{a, b, c}	—	0.1±30%	μF
Capacitors externally connected across C1 and C2 pins	C ₁₂	—	0.47±30%	μF

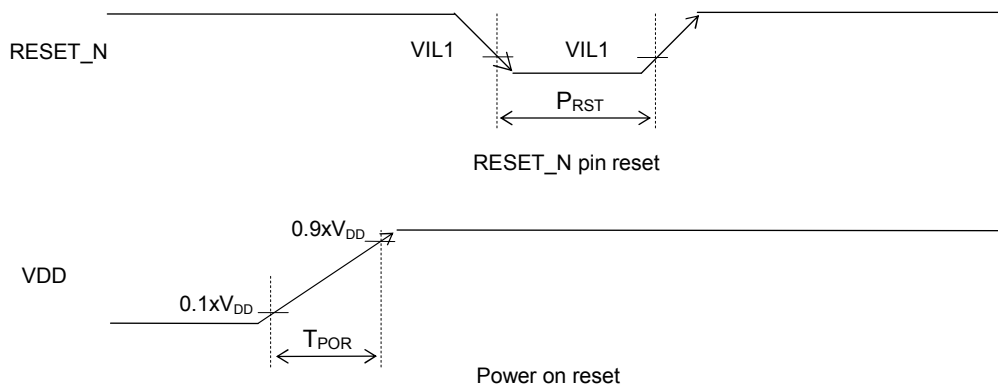
DC CHARACTERISTICS (1/5)(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit	
			Min.	Typ.	Max.			
500kHz/2MHz RC oscillation frequency	f _{RC}	V _{DD} = 1.25 to 3.6V	Ta = 25°C	Typ. -10%	500	Typ. +10%	kHz	1
			*3	Typ. -25%	500	Typ. +25%		
Low-speed crystal oscillation start time*2	T _{XTL}	—	—	0.6	2	s		
500kHz/2MHz RC oscillation start time	T _{RC}	—	—	—	3	μs		
Low-speed oscillation stop detect time*1	T _{STOP}	—	12	16.4	41	ms		
Reset pulse width	P _{RST}	—	200	—	—	μs		
Reset noise elimination pulse width	P _{NRST}	—	—	—	0.3			
Power-on reset activation power rise time	T _{POR}	—	—	—	10	ms		

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

*2: Use 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=12pF).

*3: Recommended operating temperature (Ta = -20 to +70°C, Ta = -40 to +85°C for P version)

RESET

DC CHARACTERISTICS (2/5)(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
V _{DDL} voltage	V _{DDL}	f _{OP} = 30k to 625kHz	1.1	1.2	1.3	V	1
V _{DDL} temperature deviation *1	ΔV _{DDL}	V _{DD} = 3.0V	—	-1	—	mV/°C	
V _{DDL} voltage dependency *1	ΔV _{DDL}	—	—	5	20	mV/V	

*1: V_{DDL} can not exceed V_{DD} level. The maximum V_{DDL} becomes V_{DD} level when the V_{DDL} calculated by the temperature deviation and voltage dependency is going to exceed the V_{DD} level.

DC CHARACTERISTICS (3/5)

(V_{DD} = 3.0V, V_{SS} = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit	
			Min.	Typ.	Max.			
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed RC500kHz oscillation: stopped.	Ta= 25°C	—	0.3	0.8	μA	1
			*5	—	—	3		
Supply current 2	IDD2	CPU: In HALT state (LTBC and WDT are Operating). ^{*3*4} High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. ^{*6}	Ta= 25°C	—	0.9	1.8	μA	
			*5	—	—	4		
Supply current 3	IDD3	CPU: In 32.768kHz operating state. ^{*1*3} High-speed 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. ^{*2}	Ta= 25°C	—	3	6	μA	
			*5	—	—	9		
Supply current 4	IDD4	CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. ^{*2}	Ta= 25°C	—	50	70	μA	
			*5	—	—	80		

*1: When the CPU operating rate is 100% (No HALT state).

*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

*3: Use 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)

*4: Significant bits of BLKCON0~BLKCON4 registers except DLCD bit on BLKCON4 are all "1".

*5: Recommended operating temperature (Ta = -20 to +70°C, Ta = -40 to +85°C for P version)

*6: LCD Stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC CHARACTERISTICS (4/5)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20-P22,P24/ 2 nd function is selected) (P30-P35) (P40-P47) (P50-P53) (P60-P63) ^{*1 *2} (P64-P67) ^{*1}	VOH1	IOH1 = -0.5mA, V _{DD} = 1.8 to 3.6V	V _{DD} -0.5	—	—	V	2
		IOH1 = -0.03mA, V _{DD} = 1.25 to 3.6V	V _{DD} -0.3	—	—		
	VOL1	IOL1 = +0.5mA, V _{DD} = 1.8 to 3.6V	—	—	0.5		
		IOL1 = +0.1mA, V _{DD} = 1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20-P22,P24/ 2 nd function is Not selected)	VOL2	IOL2 = +5mA, V _{DD} = 1.8 to 3.6V	—	—	0.5		
Output voltage 3 (COM0-4) (SEG0-13) ^{*1} (SEG0-17) ^{*2} (SEG0-21) ^{*3}	VOH3	IOH3 = -0.05mA, VL1=1.2V	V _{L3} -0.2	—	—		
	VOMH3	IOMH3 = +0.05mA, VL1=1.2V	—	—	V _{L2} +0.2		
	VOMH3S	IOMH3S = -0.05mA, VL1=1.2V	V _{L2} -0.2	—	—		
	VOML3	IOML3 = +0.05mA, VL1=1.2V	—	—	V _{L1} +0.2		
	VOML3S	IOML3S = -0.05mA, VL1=1.2V	V _{L1} -0.2	—	—		
	VOL3	IOL3 = +0.05mA, VL1=1.2V	—	—	0.2		
Output leakage (P20-P22, P24) (P30-P35) (P40-P47) (P50-P53) (P60-P63) ^{*1 *2} (P64-P67) ^{*1}	IOOH	VOH = V _{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL = V _{SS} (in high-impedance state)	-1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V _{DD}	0	—	1	μA	4
	IIL1	VIL1 = V _{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH2 = V _{DD}	2	300	600		
	IIL2	VIL2 = V _{SS}	-1	—	—		
Input current 3 (P00-P03) (P30-P35) (P40-P47) (P50-P53)	IIH3	VIH3 = V _{DD} , V _{DD} = 1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3 = V _{DD} , V _{DD} = 1.25 to 3.6V (when pulled-down)	0.01	30	200		
	IIL3	VIL3 = V _{SS} , V _{DD} = 1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3 = V _{SS} , V _{DD} = 1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3 = V _{DD} (in high-impedance state)	—	—	1		
IIL3Z	VIL3 = V _{SS} (in high-impedance state)	-1	—	—			

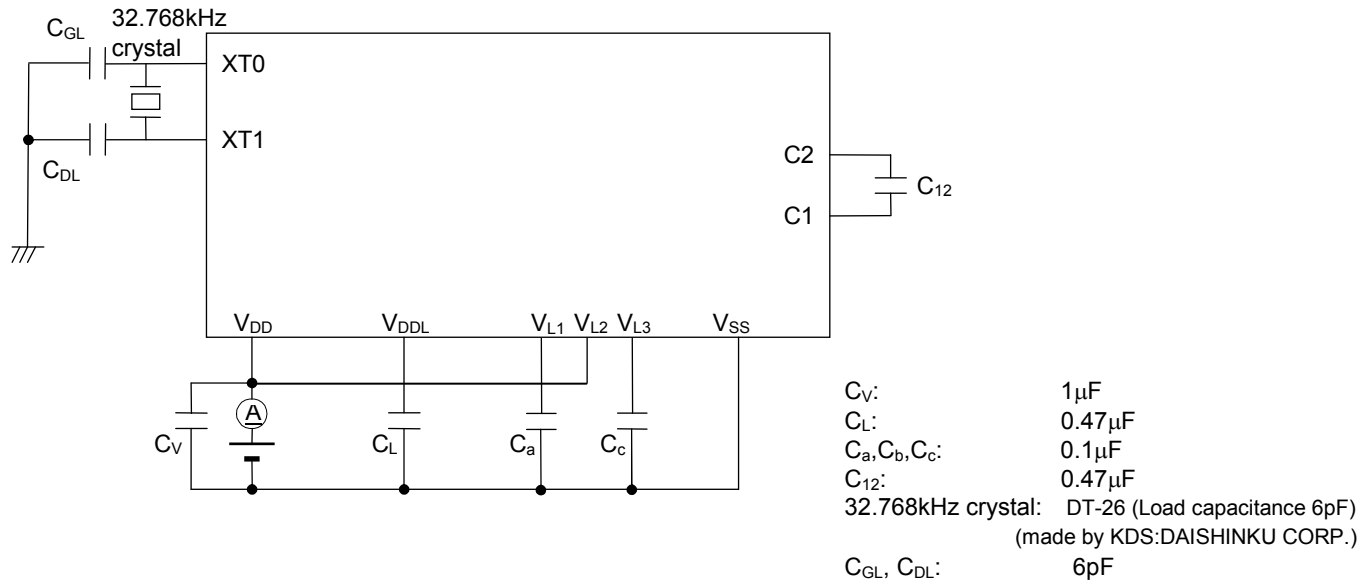
*¹: pins for ML610401*²: pins for ML610402*³: pins for ML610403

DC CHARACTERISTICS (5/5)(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, T_a = -20 to +70°C, T_a = -40 to +85°C for P version, unless otherwise specified)

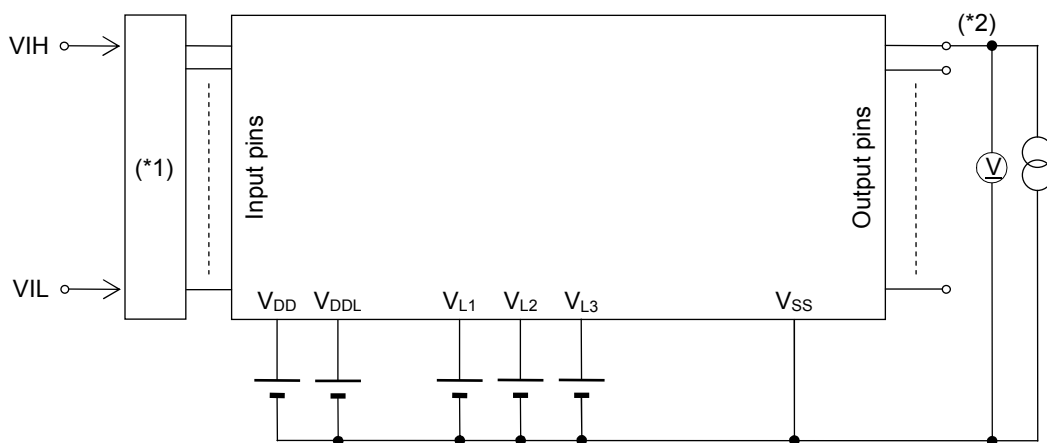
Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (P00-P03) (P30-P35) (P40-P47) (P50-P53)	VIH1	—	0.7 ×V _{DD}	—	V _{DD}	V	5
	VIL1	V _{DD} = 1.8 to 3.6V	0	—	0.3 ×V _{DD}		
		V _{DD} = 1.25 to 3.6V	0	—	0.2 ×V _{DD}		
Input pin capacitance (P00-P03) (P30-P35) (P40-P47) (P50-P53)	CIN	f = 10kHz V _{rms} = 50mV T _a = 25°C	—	—	5	pF	—

MEASURING CIRCUITS

MEASURING CIRCUIT 1

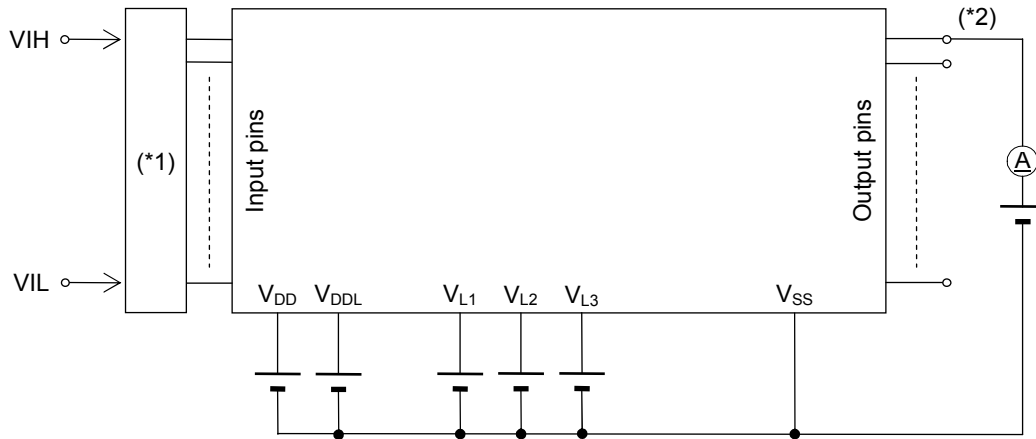


MEASURING CIRCUIT 2



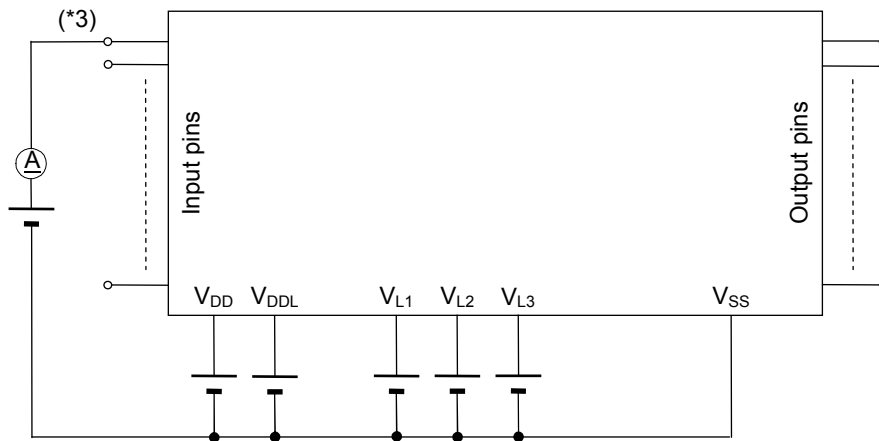
(*1) Input logic circuit to determine the specified measuring conditions.
 (*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



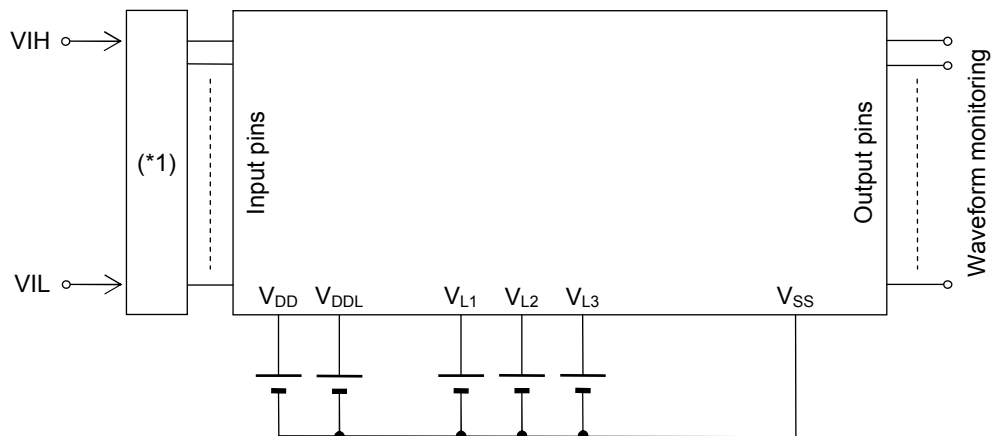
*1: Input logic circuit to determine the specified measuring conditions.
 *2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

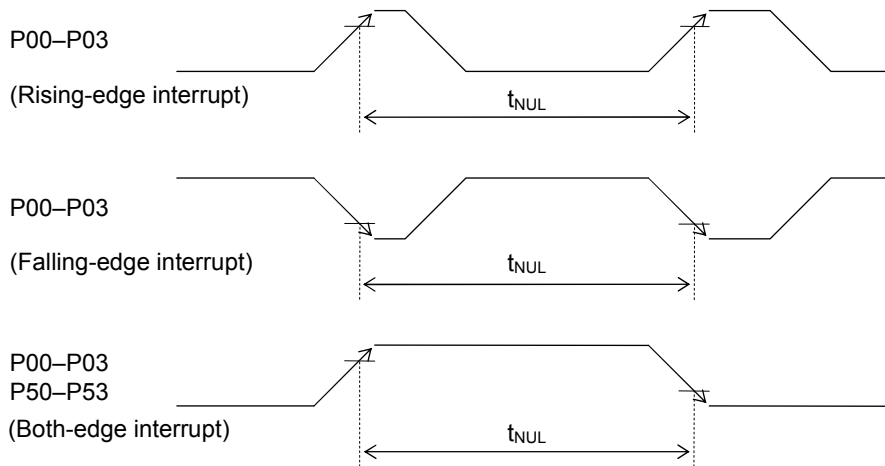


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

($V_{DD} = 1.25$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

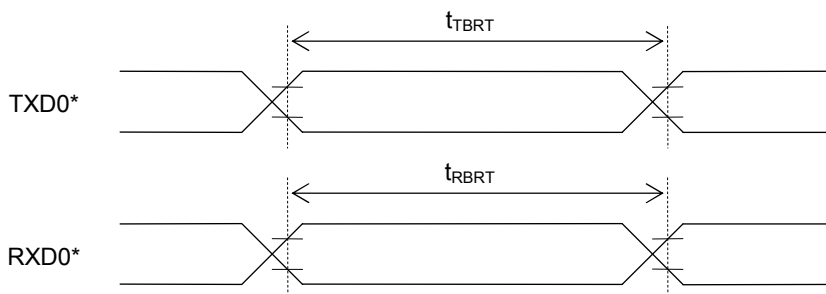


AC CHARACTERISTICS (UART)

($V_{DD} = 1.25$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT^{*1}	—	s
Receive baud rate	t_{RBRT}	—	BRT^{*1} -3%	BRT^{*1}	BRT^{*1} +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (UA0BRTL,H) and the serial port mode register 0 (UA0MOD0).



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (RC Oscillation A/D Converter)

Condition for $V_{DD}=1.8$ to $3.6V$

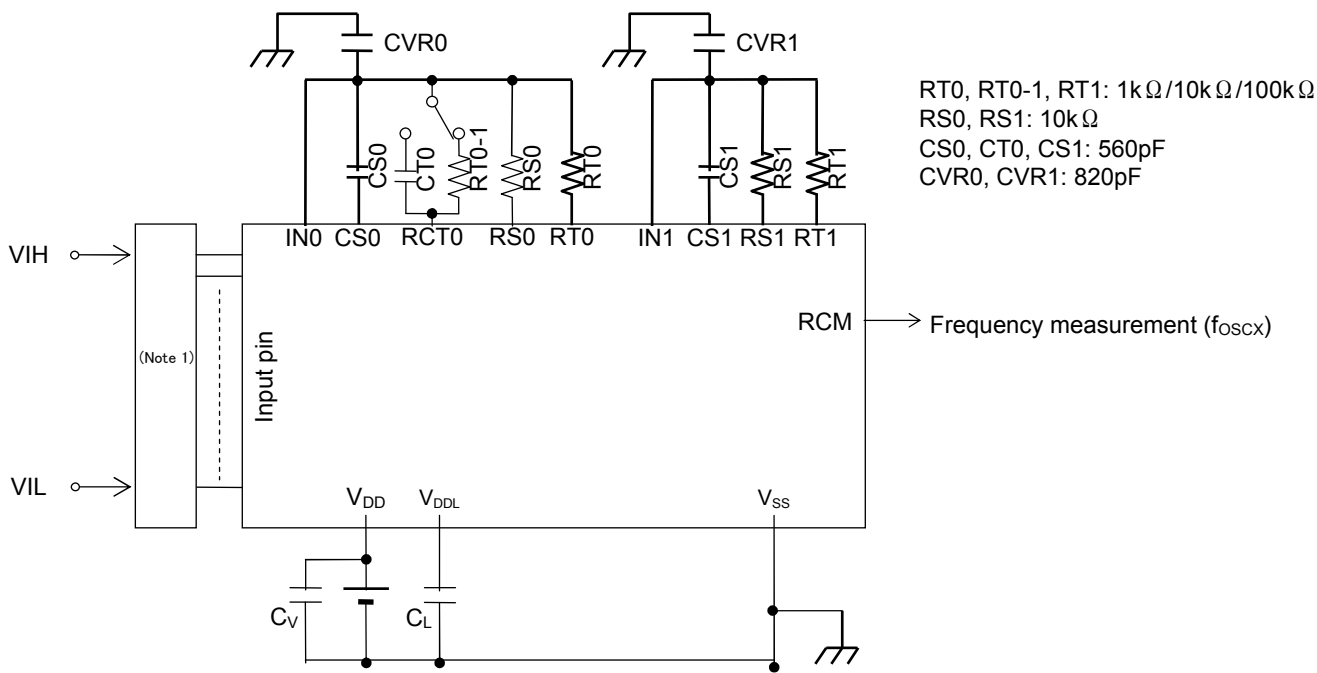
($V_{DD}=1.8$ to $3.6V$, $V_{SS}=0V$, $T_a=-20$ to $+70^{\circ}C$, $T_a=-40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1 \geq 740pF	1	—	—	k Ω
Oscillation frequency $V_{DD} = 3.0V$	f_{OSC1}	Resistor for oscillation=1k Ω	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation=10k Ω	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation=100k Ω	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 3.0V$	Kf1	RT0, RT0-1, RT1=1k Ω	7.972	9.028	9.782	—
	Kf2	RT0, RT0-1, RT1=10k Ω	0.981	1	1.019	—
	Kf3	RT0, RT0-1, RT1=100k Ω	0.099	0.101	0.104	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{oscx}(RT0-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})} \quad , \quad \frac{f_{oscx}(RT0-1-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})} \quad , \quad \frac{f_{oscx}(RT1-CS1 \text{ oscillation})}{f_{oscx}(RS1-CS1 \text{ oscillation})}$$

(x = 1, 2, 3)



*1: Input logic circuit to determine the specified measuring conditions.

Condition for $V_{DD}=1.25$ to $3.6V$

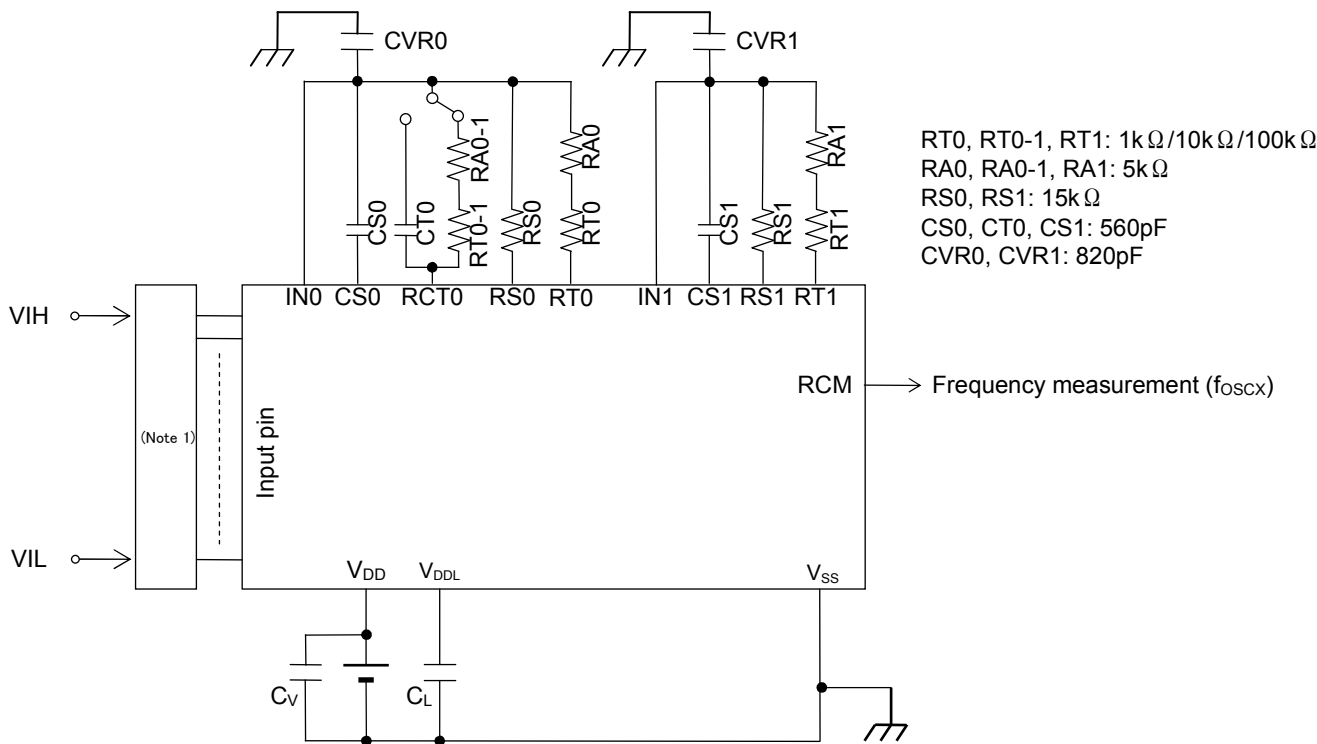
($V_{DD}=1.25$ to $3.6V$, $V_{SS}=0V$, $T_a=-20$ to $+70^\circ C$, $T_a=-40$ to $+85^\circ C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1 \geq 740pF	1	—	—	k Ω
Oscillation frequency $V_{DD} = 1.5V$	f_{OSC1}	Resistor for oscillation=6k Ω	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15k Ω	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105k Ω	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 1.5V$	Kf1	RT0, RT0-1, RT1=1k Ω	2.139	2.381	2.632	—
	Kf2	RT0, RT0-1, RT1=10k Ω	0.973	1	1.028	—
	Kf3	RT0, RT0-1, RT1=100k Ω	0.142	0.147	0.152	—
Oscillation frequency $V_{DD} = 3.0V$	f_{OSC1}	Resistor for oscillation=6k Ω	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15k Ω	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105k Ω	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 3.0V$	Kf1	RT0, RT0-1, RT1=1k Ω	2.227	2.432	2.626	—
	Kf2	RT0, RT0-1, RT1=10k Ω	0.982	1	1.018	—
	Kf3	RT0, RT0-1, RT1=100k Ω	0.141	0.145	0.149	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{oscx}(RT0-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})}, \frac{f_{oscx}(RT0-1-CS0 \text{ oscillation})}{f_{oscx}(RS0-CS0 \text{ oscillation})}, \frac{f_{oscx}(RT1-CS1 \text{ oscillation})}{f_{oscx}(RS1-CS1 \text{ oscillation})}$$

(x = 1, 2, 3)



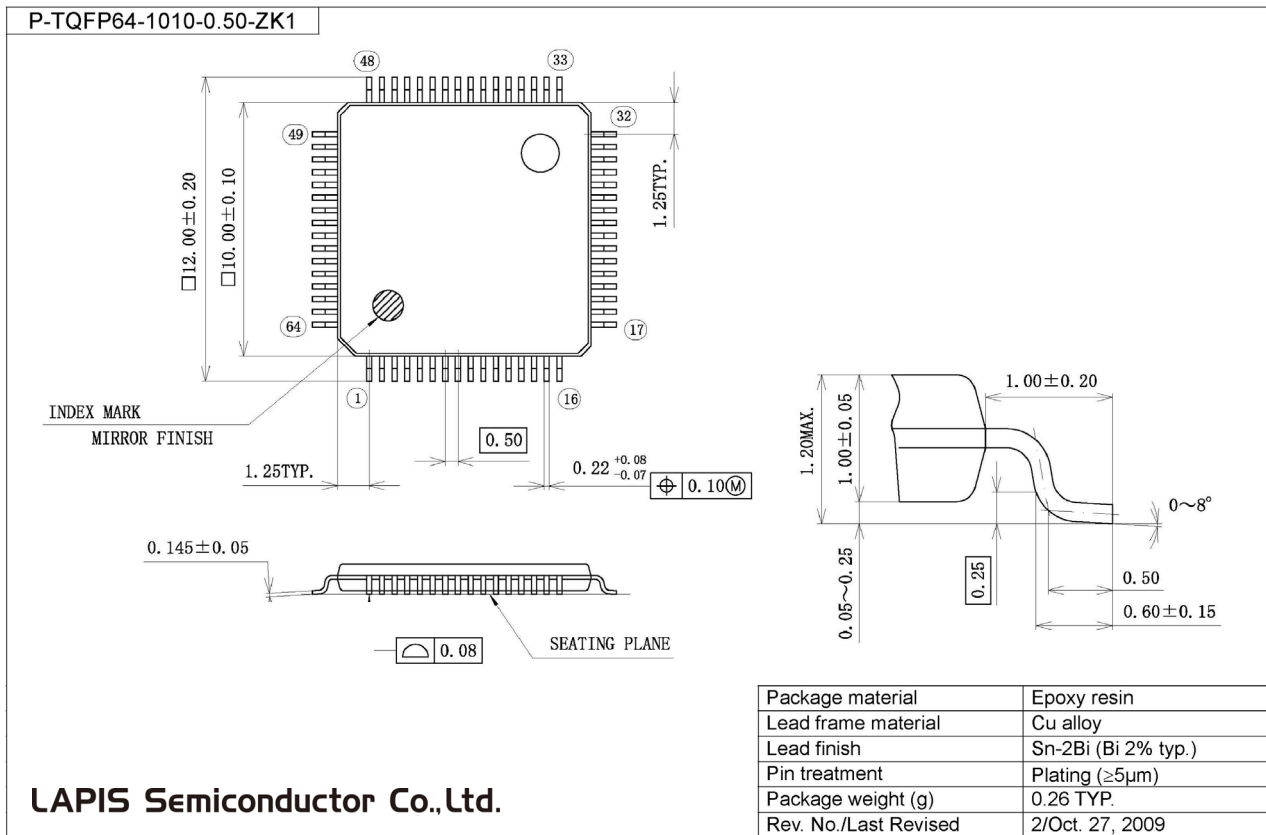
*1: Input logic circuit to determine the specified measuring conditions.

Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Package Dimensions

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610403-01	Dec.6,2010	-	-	Formally edition 1

NOTICE

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

Copyright 2010 - 2011 LAPIS Semiconductor Co., Ltd.