
ML9472

Static,1/2Duty 60 Output LCD Driver

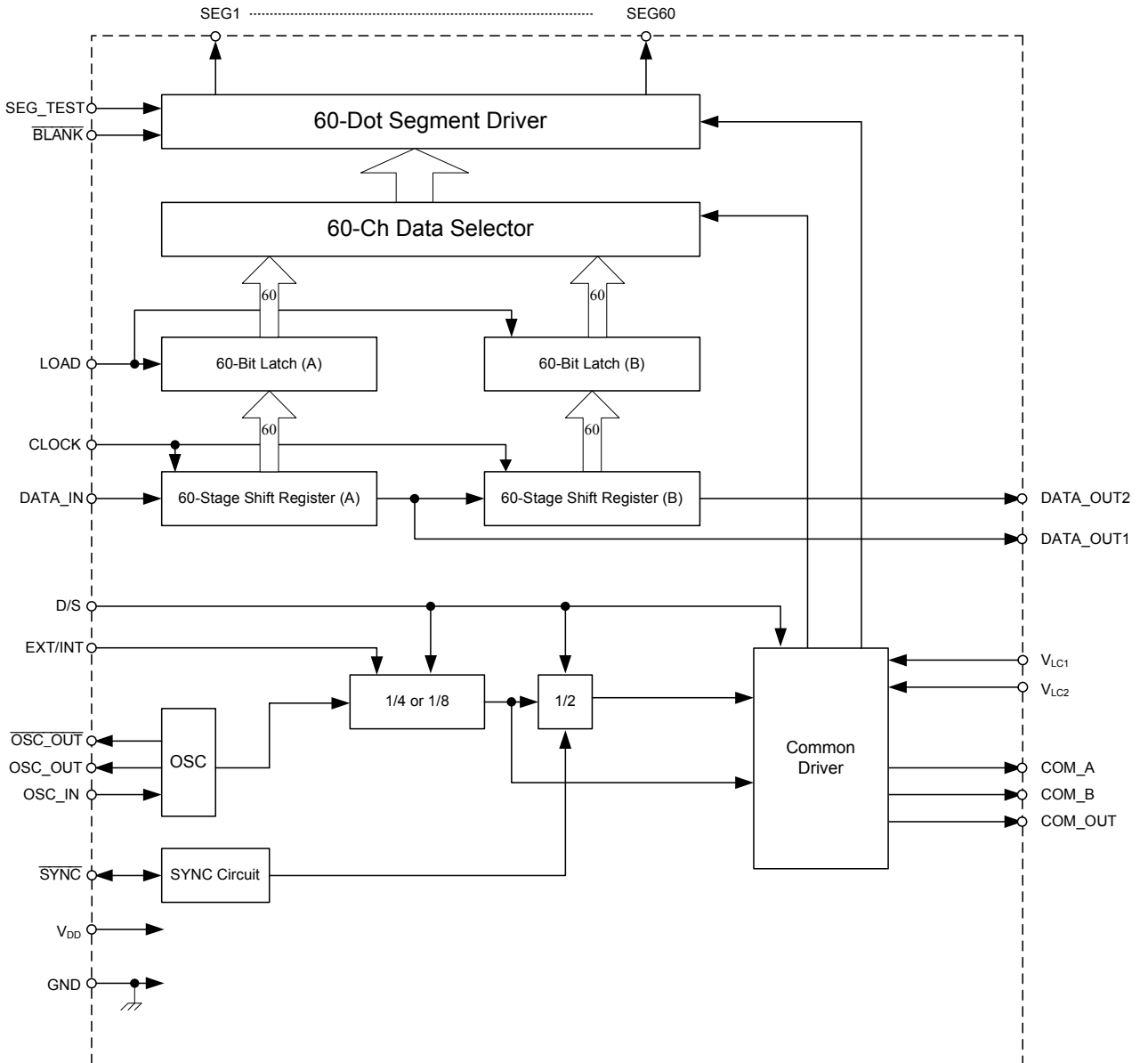
GENERAL DESCRIPTION

The ML9472 is a LCD driver which can directly drive up to 60 segments in the static display mode and up to 120 segments in the 1/2 duty dynamic display mode.

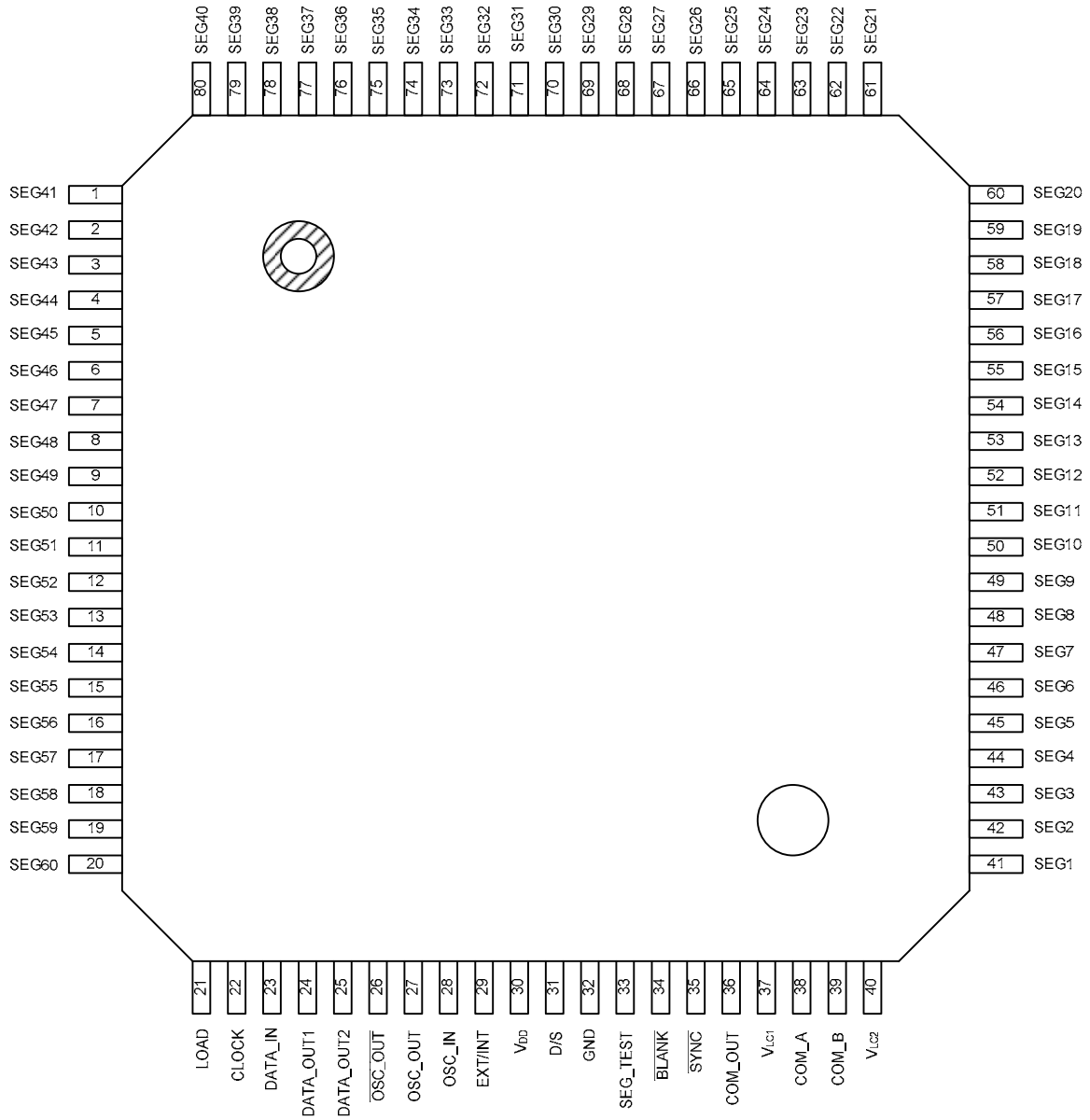
FEATURES

- Operating range
 - Supply voltage : 3.0 to 5.5 V
 - Operating temperature range : -40 to + 105°C
- Segment output
 - Static display mode : Up to 60 segments can be displayed.
 - 1/2 duty : Up to 120 segments can be displayed.
- Simple interface with microcomputer
- Built-in common signal generator
- One-to-one correspondence between input data and output data
 - When input data is at “H” level : Display goes on.
 - When input data is at “L” level : Display goes off.
- Test pin for all-on (SEG_TEST) and all-off (BLANK)
- Can be cascade-connected
- Can be synchronized with the external common signal
- Applicable as an output expander
- Package
 - 80-pin plastic TQFP (TQFP80-P-1212-0.50-K) (Product name: ML9472TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic TQFP

PIN DESCRIPTION

| Symbol | Type | Description |
|---|-------------|---|
| OSC_IN OSC_OUT $\overline{\text{OSC_OUT}}$ | I O O | Pins for oscillation. The oscillator circuit is configured by externally connecting two resistors and a capacitor. Make the wiring length as short as possible, because the resistor connected to the OSC_IN pin has a higher value and the circuit is susceptible to external noise. |
| DATA_IN | I | Serial data input pin. The display goes on when input data is at a "H" level, and it goes off when input data is at a "L" level. |
| CLOCK | I | Shift clock input pin. Data from the DATA pin is transferred in synchronization with the rising edge of the shift clock. |
| LOAD | I | Load signal input pin. Serially input data is transferred to the 60-bit latch at a "H" level of this load signal, then held at a "L" level. |
| $\overline{\text{BLANK}}$ | I | Input pin that turns off all segments. The entire display goes off when a "L" level is applied to this pin. The display returns to the previous state when a "H" level is applied. When SEG_TEST pin is at a "H" level, the input on this pin is disabled. |
| SEG_TEST | I | Input pin is used to test the segment outputs (SEG ₁ to SEG ₆₀). All displays are turned on when "H" is applied to this pin. The display returns to the previous state when a "L" level is applied. When this pin is at a "H" level, the input on the $\overline{\text{BLANK}}$ pin is disabled. |
| D/S | I | When "H" is applied to this pin, the ML9472 operates in the 1/2 duty dynamic display mode. When this pin is set at a "L" level, the ML9472 operates in the static display mode. |
| EXT/INT | I | When the external common signal is used, fix this pin at a "H" level and input the external common signal from the OSC_IN pin. The input common signal is used as the internal common signal and is output from the COM_OUT pin through the buffer. When the built-in common signal generator is used, fix this pin at a "L" level. When the ML9472 is used as an output expander, fix this pin at a "H" level and the OSC_IN pin at a "L" level. The output logic can be reversed with respect to the input data by setting OSC_IN to a "H" level. |
| $\overline{\text{SYNC}}$ | I/O | This pin is an input/output pin which is used when two or more ML9472s are connected in series (cascade connection) in the 1/2 duty dynamic display mode. All of the involved ML9472's $\overline{\text{SYNC}}$ pins should be connected by the common line and they should be pulled up with a common resistor, which makes a phase level of all involved ML9472's COM_A and COM_B pins equal. When a single ML9472 is used in the dynamic display mode, $\overline{\text{SYNC}}$ should be pulled up with a resistor. Connect this pin to GND if any of the following conditions is true: - The ML9472 is operated in the static display mode. - The ML9472 is used as an output expander. |
| DATA_OUT1 | O | The 60 th stage data of the shift register is output from this pin. When two or more ML9472s are connected in series (cascade connection) in the static display mode, this pin should be connected to the next ML9472's DATA_IN Pin. |
| DATA_OUT2 | O | The 120 th stage data of the shift register is output from this pin. When two or more ML9472s are connected in series (cascade connection) in the 1/2 duty dynamic display mode, this pin should be connected to the next ML9472's DATA_IN pin. |
| COM_OUT | O | When two or more ML9472s are connected in series (cascade connection), this pin should be connected with all of the slave ML9472's OSC_IN pins. |

| Symbol | Type | Description |
|--------------------|--------|---|
| COM_A COM_B | O O | <p>LCD driving common signals is output from these pins. These pins should be connected to the COMMON side of the LCD panel.</p> <ul style="list-style-type: none"> - In the static display mode A pulse in phase with the COM_OUT is output from both COM_A and COM_B. In this case, the high level is V_{DD}, and the low level is V_{LC2}. - In the 1/2 duty dynamic display mode The COM_A and COM_B output signals are alternately changed within each COM_OUT output cycle, resulting in alternate repetition of select and non-select modes. |
| SEG1 to SEG60 | O | Display output pins for LCD. These pins are connected to the SEGMENT side of the LCD panel. For the correspondence between the output of these pins and input data, see Section, "Data Structure". |
| V_{LC1}, V_{LC2} | — | <p>Bias pins for LCD driver. Through these pins, bias voltages for the LCD are externally supplied.</p> <p>In the static display mode, V_{LC1} should be open.</p> <p>$V_{LC1} = V_{DD} / 2$ $V_{DD} > V_{LC1} > V_{LC2} = GND$</p> |
| V_{DD}, GND | — | Supply voltage pin and ground pin. |

Note: Built-in schmitt circuit is used for all input pins.

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|---------------------|-----------|---------------------------|----------------------|------------------|
| Supply Voltage | V_{DD} | $T_a = 25^\circ\text{C}$ | -0.3 to 6.5 | V |
| Input Voltage | V_I | $T_a = 25^\circ\text{C}$ | -0.3 to $V_{DD}+0.3$ | V |
| Storage Temperature | T_{STG} | — | -55 to 150 | $^\circ\text{C}$ |
| Power Dissipation | P_D | $T_a < 105^\circ\text{C}$ | 650 | mW |
| Output Current | I_{O1} | Driver Outputs | -2.0 to 2.0 | mA |
| | I_{O2} | Logic Outputs | -2.0 to 2.0 | mA |

RECOMMENDED OPERATING CONDITIONS

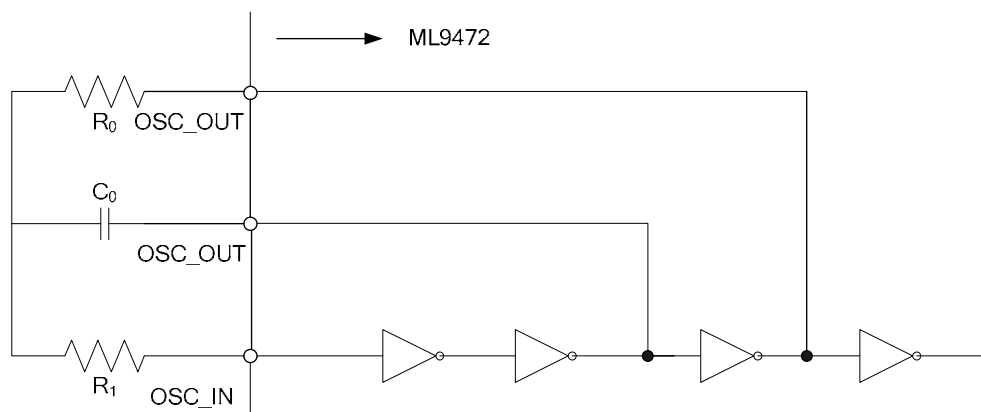
| Parameter | Symbol | Condition | Range | Unit |
|-----------------------|-----------|--------------------|---------------|------------------|
| Supply Voltage | V_{DD} | — | 3 to 5.5 | V |
| LCD Driving Voltage | V_{LCD} | $V_{DD} - V_{LC2}$ | 3 to V_{DD} | V |
| CLOCK Frequency | f_{CP} | — | 0.3 to 4 | MHz |
| Operating Temperature | T_a | — | -40 to 105 | $^\circ\text{C}$ |

OSCILLATOR CIRCUIT

| Parameter | Symbol | Applicable pin | Condition | Min. | Typ. | Max. | Unit |
|-----------------------------|-----------|------------------------------|------------------|-------|------|-------|------------------|
| Oscillator Resistance | R_0 | $\overline{\text{OSC_OUT}}$ | — | 56 | 100 | 220 | $\text{k}\Omega$ |
| Oscillator Capacitance | C_0 | OSC_OUT | Film capacitor | 0.001 | — | 0.047 | μF |
| Current Limiting Resistance | R_1 | OSC_IN | $R_1 \geq 10R_0$ | 560 | 1000 | 2220 | $\text{k}\Omega$ |
| Common Signal Frequency | f_{COM} | COM_A COM_B | — | 25 | — | 150 | Hz |

Note: See Section, “Reference Data”, for the resistor and capacitor values in the table.

Example of an oscillator circuit:



ELECTRICAL CHARACTERISTICS

DC Characteristics

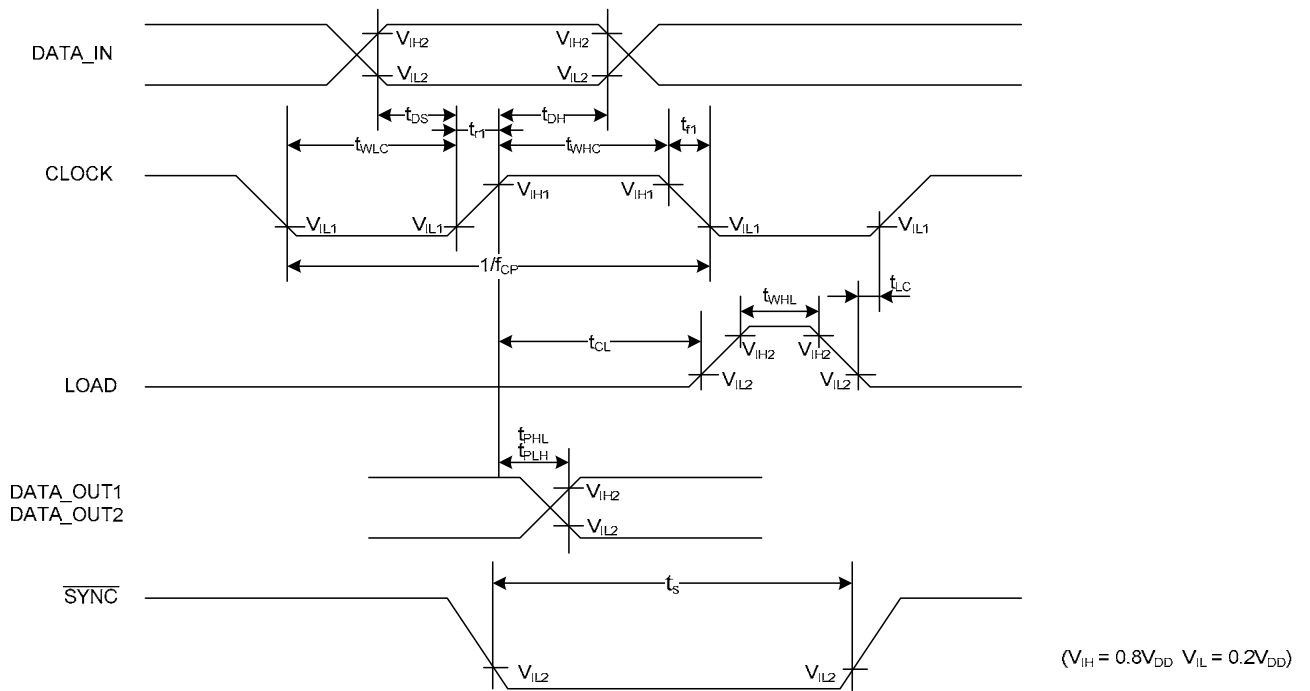
(V_{DD} = 3.0 to 5.5 V, T_a = -40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Applicable pin | Condition | Min. | Max. | Unit | |
|-----------------------------|------------------|--------------------------------------|---|-------------------------|---------------------|------|---|
| “H” Input Voltage | V _{IH} | SEG_TEST, BLANK, LOAD, | — | 0.8 V _{DD} | V _{DD} | V | |
| “L” Input Voltage | V _{IL} | DATA_IN, | — | GND | 0.2 V _{DD} | V | |
| “H” Input Current | I _{IH} | CLOCK, D/S, EXT/INT, | V _I = V _{DD} | — | 1 | μA | |
| “L” Input Current | I _{IL} | OSC_IN | V _I = 0 V | -1 | — | μA | |
| “H” Output Voltage | V _{OH1} | DATA_OUT1 DATA_OUT2 COM_OUT | I _O = -100 μA, V _{DD} = 5.0 V | 4.5 | — | V | |
| | V _{OH2} | OSC_OUT OSC_OUT | I _O = -200 μA, V _{DD} = 5.0 V | 4.5 | — | V | |
| “L” Output Voltage | V _{OL1} | DATA_OUT1 DATA_OUT2 COM_OUT | I _O = 100 μA, V _{DD} = 5.0 V | — | 0.5 | V | |
| | V _{OL2} | OSC_OUT OSC_OUT | I _O = 200 μA, V _{DD} = 5.0V | — | 0.5 | V | |
| | V _{OL3} | SYNC | I _O = 250 μA, V _{DD} = 5.0 V | — | 0.8 | V | |
| COMMON Output Voltage | V _{OCH} | COM_A COM_B | V _{DD} = 5.0 V, V _{LC1} = 2.5 V, V _{LC2} = 0 V, I _O = -150 μA | 4.8 | — | V | |
| | V _{OCM} | COM_A COM_B | V _{DD} = 5.0 V, V _{LC1} = 2.5 V, V _{LC2} = 0 V, I _O = ±150 μA | 2.3 | 2.7 | V | |
| | V _{OCL} | COM_A COM_B | V _{DD} = 5.0 V, V _{LC1} = 2.5 V, V _{LC2} = 0 V, I _O = 150 μA | — | 0.2 | V | |
| Segment Output Voltage | V _{OSH} | SEG ₁ - SEG ₆₀ | V _{DD} = 5.0 V, V _{LC1} = 2.5 V V _{LC2} = 0 V | I _O = -30 μA | 4.8 | — | V |
| | V _{OSL} | | | I _O = +30 μA | — | 0.2 | V |
| Output Leakage Current | I _{LO} | SYNC | V _{DD} = 5.0 V and V _O = 5 V when internal Tr is off | — | 5 | μA | |
| Segment Output Impedance | R _{SEG} | SEG ₁ - SEG ₆₀ | V _{DD} = 5.0 V, V _{LC1} = 2.5V, V _{LC2} = 0V | — | 10 | kΩ | |
| Common Output Impedance | R _{COM} | COM_A COM_B | V _{DD} = 5.0 V, V _{LC1} = 2.5V, V _{LC2} = 0V | — | 1.5 | kΩ | |
| Static Supply Current | I _{DD1} | V _{DD} | Fix all input levels at either V _{DD} or GND | — | 100 | μA | |
| Dynamic Supply Current | I _{DD2} | V _{DD} | V _{DD} = 5.0V, No load. R ₀ = 100 kΩ, C ₀ = 0.01 μF, R ₁ = 1 MΩ | — | 0.5 | mA | |

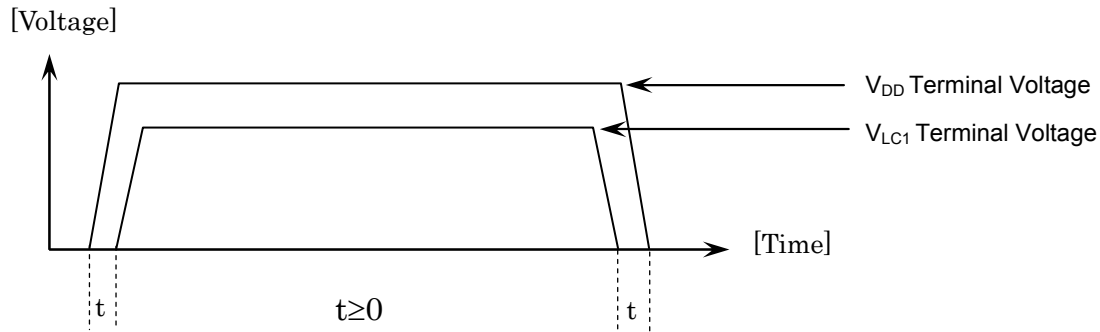
AC Characteristics

($V_{DD} = 3$ to 5.5 V, $T_a = -40$ to $+105^\circ\text{C}$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------------|------------------------|---|------|------|------|---------------|
| Clock "H" Time | t_{WHC} | — | 70 | — | — | ns |
| Clock "L" Time | t_{WLC} | — | 70 | — | — | ns |
| Data Set-up Time | t_{DS} | — | 50 | — | — | ns |
| Data Hold Time | t_{DH} | — | 50 | — | — | ns |
| Load "H" Time | t_{WHL} | — | 100 | — | — | ns |
| Clock-to-load Time | t_{CL} | — | 100 | — | — | ns |
| Load-to-Clock Time | t_{LC} | — | 100 | — | — | ns |
| "H", "L" Propagation Delay Time | t_{PHL} t_{PLH} | Load capacitance of DATA_OUT1, DATA_OUT2: 15 pF | — | — | 0.14 | μs |
| Clock Rise time, Fall time | t_{r1} , t_{f1} | — | — | — | 50 | ns |
| SYNC Pulse "L" Time | t_s | — | 0.2 | — | — | μs |
| OSC_IN Input Frequency | f_{OSC} | — | — | — | 5 | kHz |

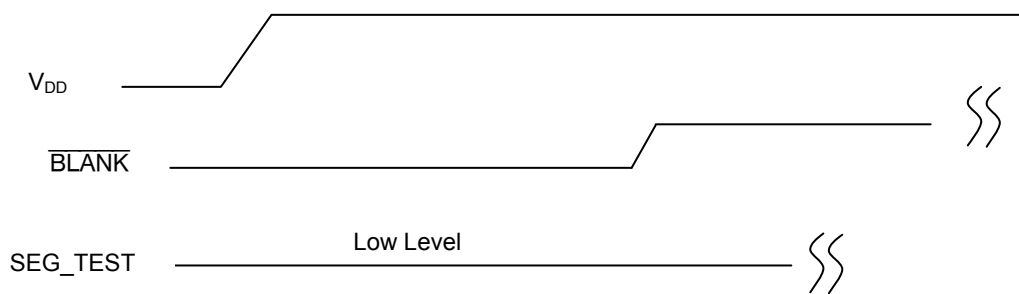


POWER-ON/OFF TIMING



* Please start up V_{LC1} after turning on the V_{DD} power supply. Or, please start up at the same time.

INITIAL SIGNAL TIMING

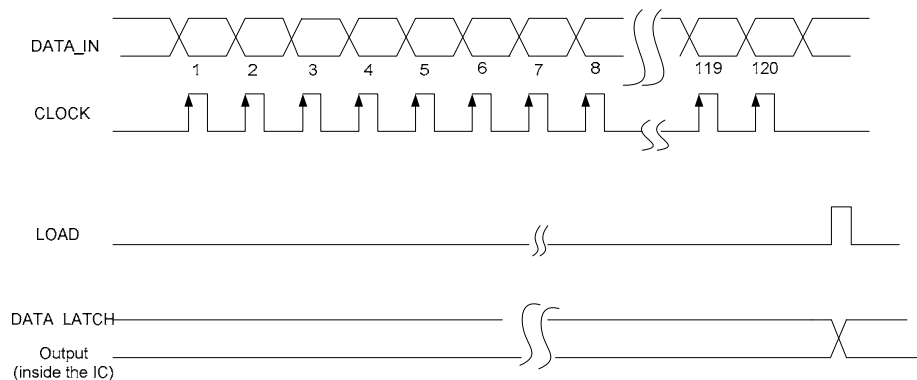


* After V_{DD} is applied, \overline{BLANK} and SEG_TEST should be applied to 'L' level to make all SEGMENTS off until first group of display data is latched.

FUNCTIONAL DESCRIPTION

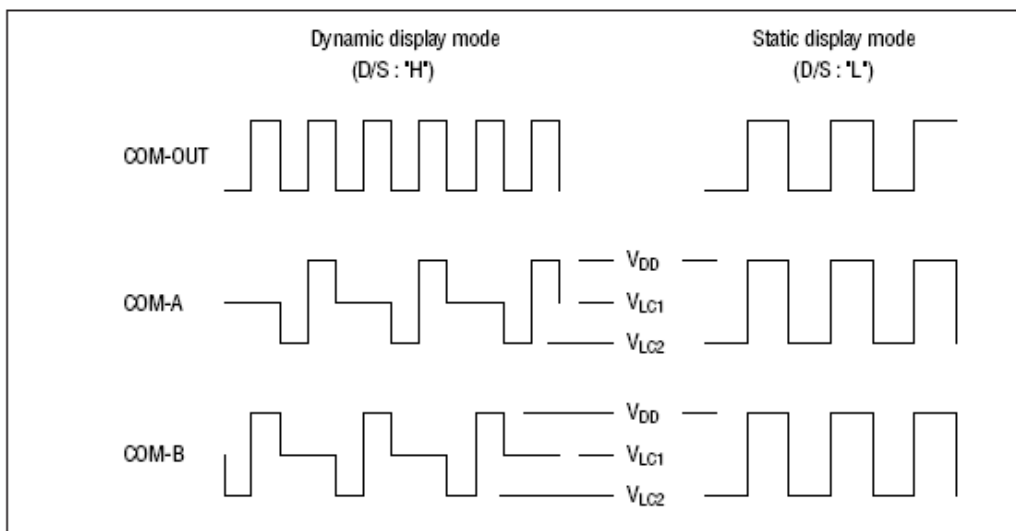
Operation Description

The ML9472 consists of a 120-stage shift register, 120-bit data latch, and 60 pairs of LCD drivers. The display data is input from the $DATA_IN$ pin to the 120-stage shift register at the rising edge of the $CLOCK$ pulse and it is shifted to the 120-bit data latch when the $LOAD$ signal is set at "H" level, then it is directly output from the 60 pairs of LCD drivers to the LCD panel. Input the display data in the order of $SEG60, SEG59, SEG58, \dots, SEG2, SEG1$.



COM_A, COM_B

In the select mode, a signal in phase with the COM_OUT signal is output at “H” (V_{DD}) and “L” (V_{LC2}).
 In the non-select mode a voltage is output at “M” (V_{LC1}). In the select mode of COM_A (non-select mode of COM_B), signals that correspond to the 1st-to 60th-bit data of the data latch are output to the segment outputs.
 In the select mode of COM_B (non-select mode of COM_A), signals that correspond to the 61st- to 120th-bit data of the data latch are output to the segment outputs.



SEGN Truth Table

| Mode | Display data in LatchA | Display data in LatchB | COMA | COMB | SEGN |
|------------------|------------------------|------------------------|------|------|------|
| Static | 1 | — | “H” | “H” | 0 |
| | | — | “L” | “L” | 1 |
| | 0 | — | “H” | “H” | 1 |
| | | — | “L” | “L” | 0 |
| 1/2 duty Dynamic | 1 | 1 | “H” | “M” | 0 |
| | | | “L” | “M” | 1 |
| | | | “M” | “H” | 0 |
| | | | “M” | “L” | 1 |
| | 1 | 0 | “H” | “M” | 0 |
| | | | “L” | “M” | 1 |
| | | | “M” | “H” | 1 |
| | | | “M” | “L” | 0 |
| | 0 | 1 | “H” | “M” | 1 |
| | | | “L” | “M” | 0 |
| | | | “M” | “H” | 0 |
| | | | “M” | “L” | 1 |
| | 0 | 0 | “H” | “M” | 1 |
| | | | “L” | “M” | 0 |
| | | | “M” | “H” | 1 |
| | | | “M” | “L” | 0 |

*Note: “H” = V_{DD} ; “M” = V_{LC1} ; “L” = V_{LC2} .

SEG1-SEG60

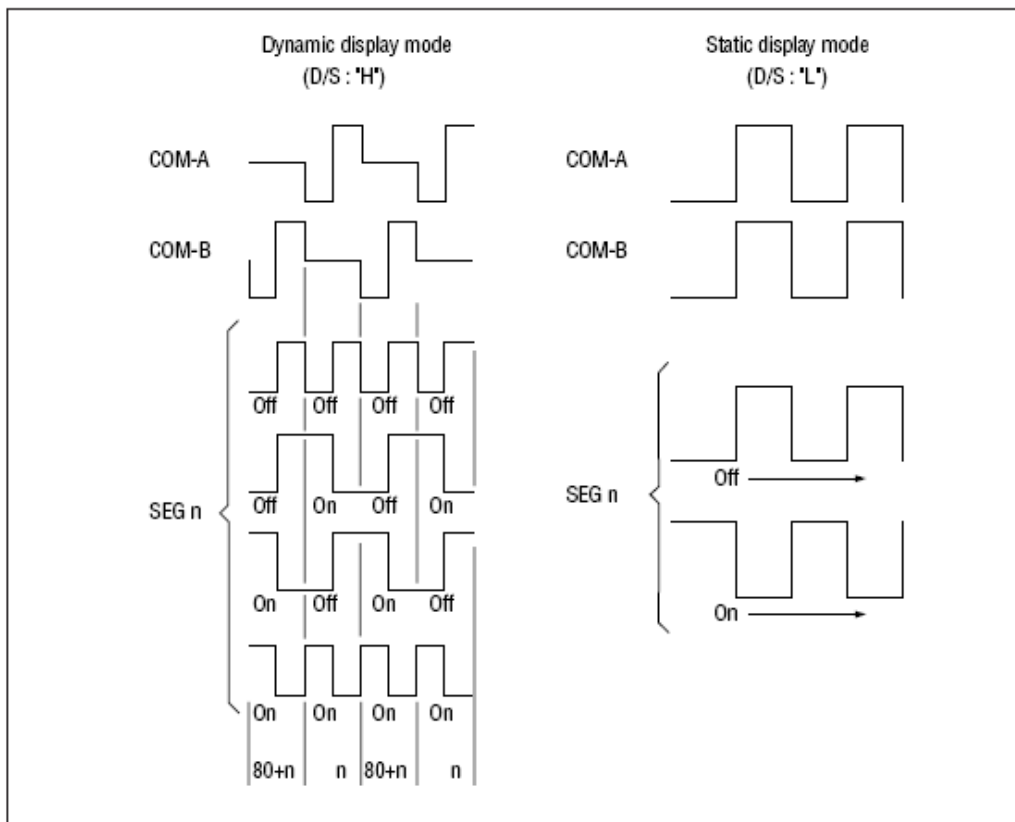
LCD segment driving signals are output from these pins and they should be connected to the segment side of the LCD panel.

“H” level: V_{DD} , “L” level: V_{LC2}

In the static display mode, the nth bit data of the data latch (A) corresponds to the SEGn. The data of the data latch (B) is invalid.

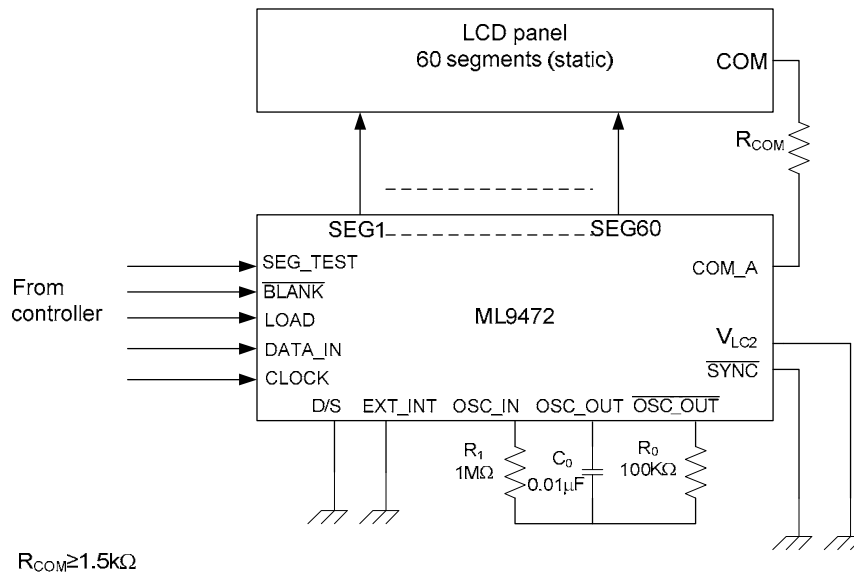
A signal out of phase with the COM_OUT signal is output to the segment outputs when the display is turned on, while a signal in phase with it is output when the display is turned off.

In the 1/2 duty dynamic mode, the output of the SEGn corresponds to the nth bit data of the data latch (A) when COM_A is in select mode and corresponds to the nth bit data of the data latch (B) when COM_B is in select mode. When the display is turned on, a signal out of phase with the common signal corresponding to the data is output, while a signal in phase with the common signal is output when the display is turned off.

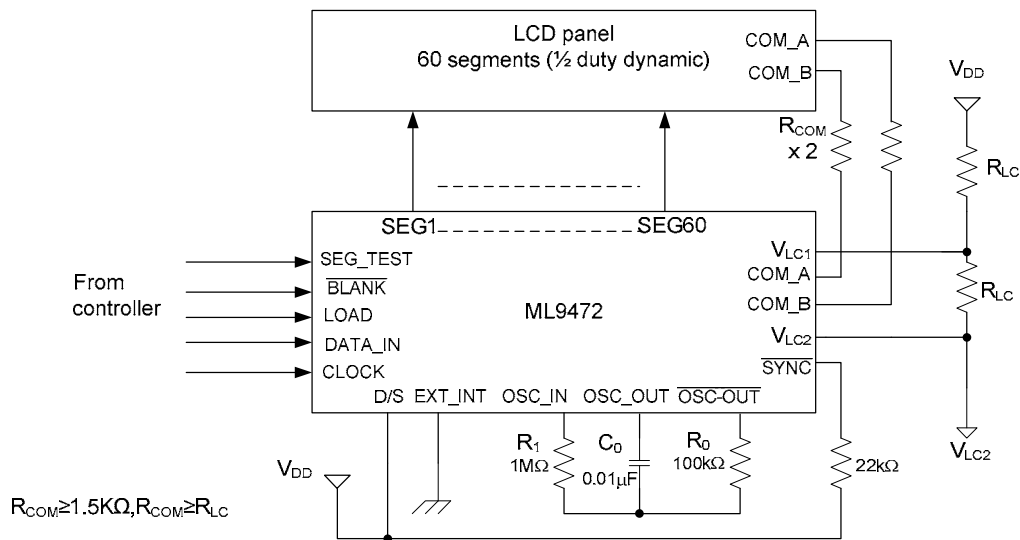


APPLICATION CIRCUITS

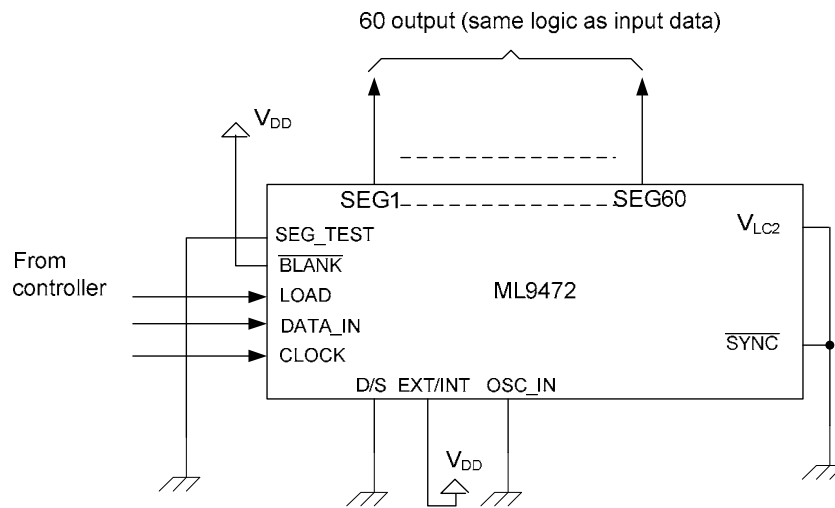
1) Single ML9472 operation in the static display mode



2) Single ML9472 operation in the 1/2 duty dynamic display mode



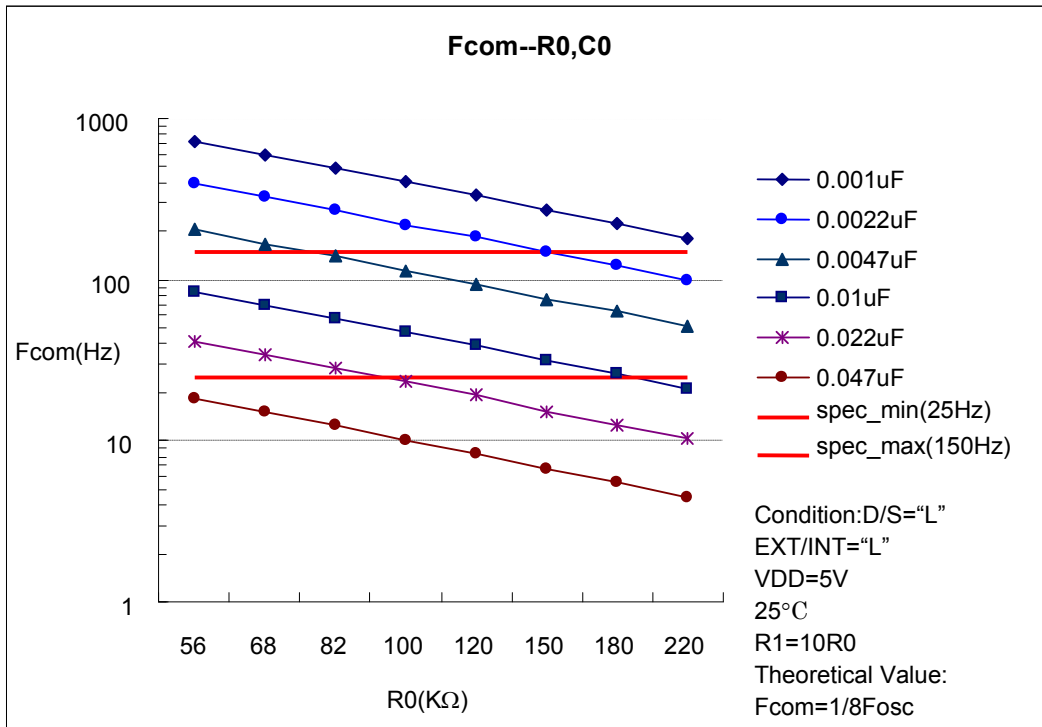
5) Output-expander



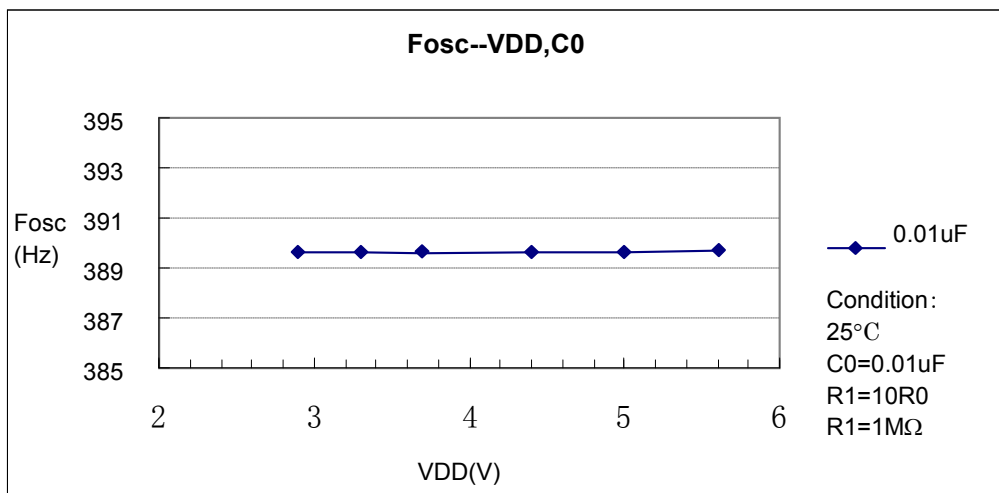
*The output logic can be reversed with respect to the input data by setting OSC_IN to "H" level.

REFERENCE CHARACTERISTICS

Fcom — R0,C0

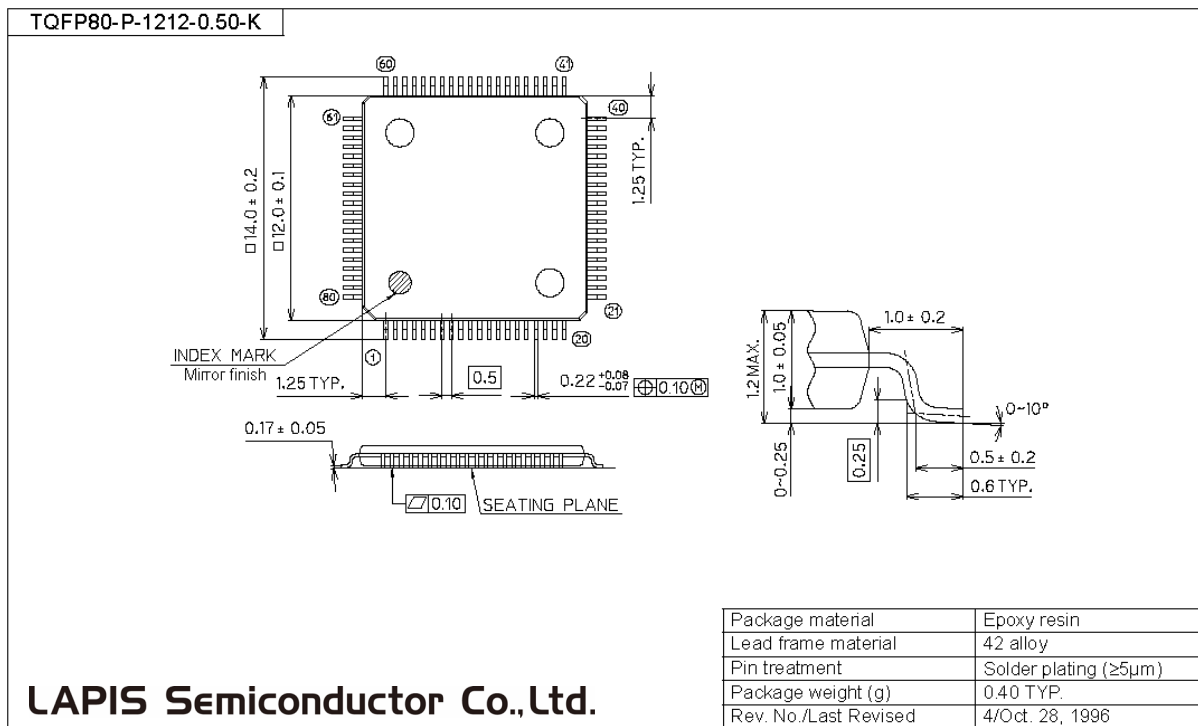


Fosc — VDD,C0



PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

| Document No. | Date | Page | | Description |
|--------------|---------------|------------------|-----------------|---|
| | | Previous Edition | Current Edition | |
| FEDL9472-01 | July. 2, 2007 | – | – | Final edition 1 |
| FEDL9472-02 | Feb. 1, 2008 | 2 | 2 | BLOCK DIAGRAM |
| | | 6 | 6 | Power Dissipation 794mW→650mW |
| | | 7 | 7 | Segment Output Impedance Condition Common Output Impedance Condition |
| | | 9 | 9 | POWER-ON/OFF TIMING |
| | | 10 | 10 | SEn Truth Table |
| | | 14 | 14 | Output-expander |
| | | – | 15 | Reference Characteristics |

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