ML610Q486

8-bit Microcontroller

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface (master), battery level detect circuit, and 12-bit successive approximation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipe line architecture parallel procesing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications.
The on-chip debug function that is installed enables program debugging and programming.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    32.0 µs (@31.25kHz system clock)
    2.0µs (@500kHz system clock)

- Internal memory
  - Internal 32KByte Flash ROM (16K×16 bits) (including unusable 1KByte TEST area)
  - Internal 1KByte Data RAM (1024×8 bits)

- Interrupt controller
  - 2 non-maskable interrupt sources
    Internal source: 1 (Watch dog timer)
    External source: 1 (NMI)
  - 17 maskable interrupt sources
    Internal sources: 13 (SSIO, SA-A/D converter, I2C, Timer0, Timer1, Timer2, Timer3, UART, PWM, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    External sources: 4 (P00, P01, P02, P03)

- Time base counter
  - Low-speed time base counter ×1 channel
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - O verflow period: 4 types selectable
    approx. 131ms, 524ms, 2.1s, 8.4s

- Timers
  - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)

- PWM
  - Resolution 16 bits × 1 channel

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART(Only an external baund rate input clock can be used.)
  - Half-Duplex Communication
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator
  - External baud rate clock

- I^2C bus interface
  - Master function only
  - Standard mode (approx. 25kbps)

- Successive approximation type A/D converter
  - 12-bit A/D converter
  - Input × 4 channels

- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 6 channels (including secondary functions)
  - Output-only port × 5 channels (including secondary functions)
  - Input/output port × 21 channels (including secondary functions)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 12 levels
  - Judgment accuracy: ±2%
  - Temperature deviation: 0%/°C

- Clock
  - Low-speed clock(31.25kHz)
    1/16 of Built-in RC oscillation 500kHz
  - High-speed clock:
    Built-in RC oscillation (500 kHz)
    External clock (500kHz or less)

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - 48-pin plastic TQFP (TQFP48-P-0707-0.50-K)
    ML610Q486-xxxTBZ03A (Blank product: ML610Q486-NNNTBZ03A)
    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: –40°C to +85°C
  - Operating voltage: V_{DD} = 1.6V to 3.6V, AV_{DD} = 2.2V to 3.6V

BLOCK DIAGRAM

ML610Q486 Block Diagram

"*" indicates the secondary function of each port.

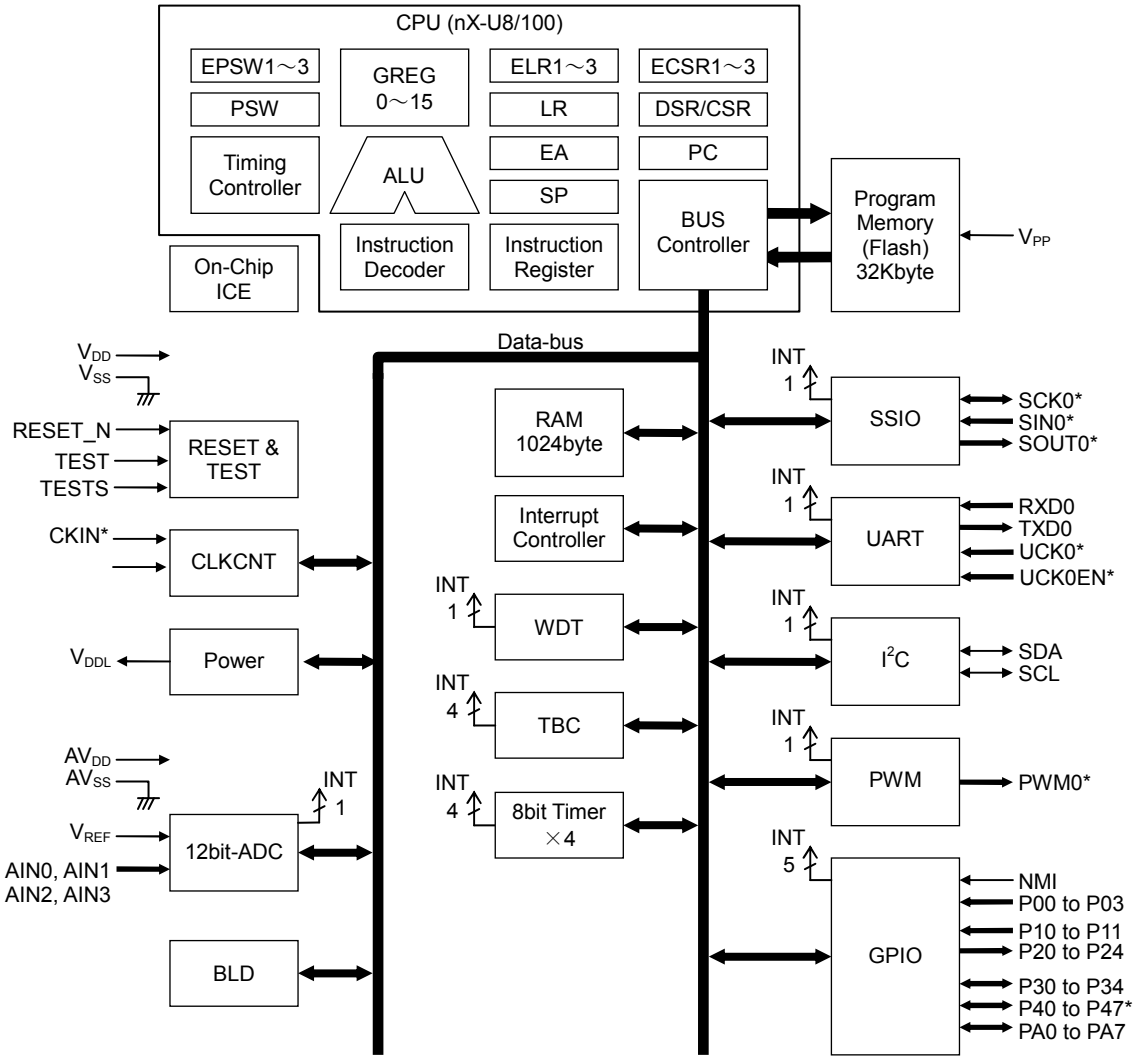


Figure 1 ML610Q486 Block Diagram

PIN CONFIGURATION

ML610Q486 TQFP48 Pin Layout

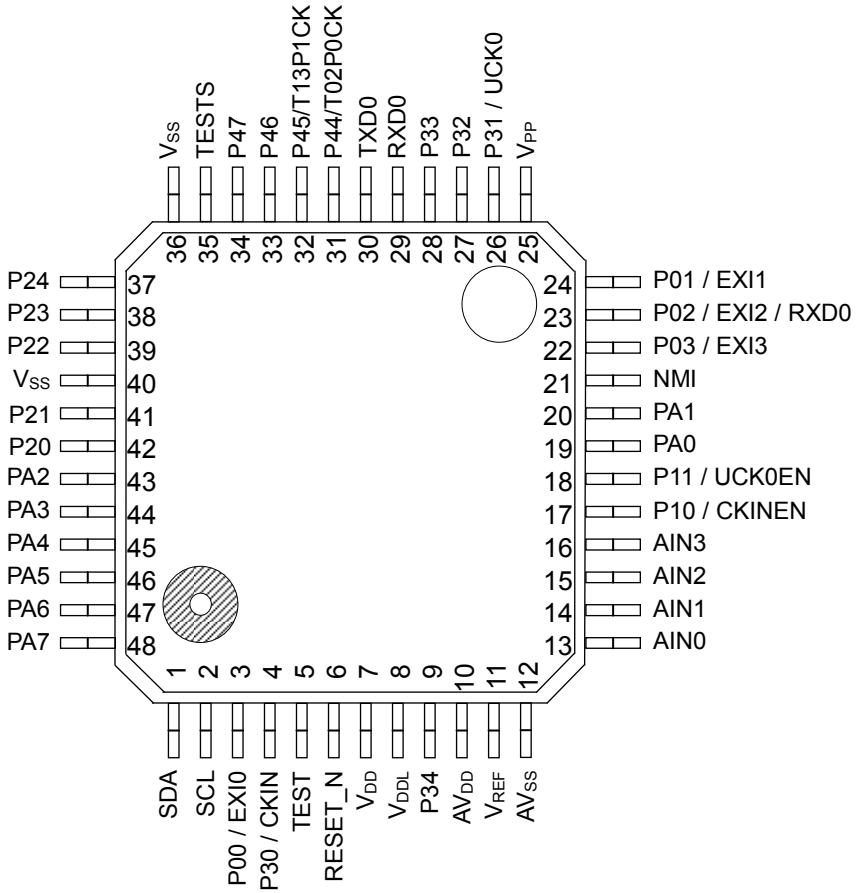


Figure 2 ML610Q486 TQFP48 Pin Configuration

PIN LIST

PIN No.	Primary function			Secondary function		
	Pin name	I/O	Function	Pin name	I/O	Function
36, 40	V_{SS}	—	Negative power supply pin	—	—	—
7	V_{DD}	—	Positive power supply pin	—	—	—
8	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—
25	V_{PP}	—	Power supply pin for Flash ROM	—	—	—
12	AV_{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—
10	AV_{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—
35	TESTS	I	Input pin for testing			
5	TEST	I/O	Input/output pin for testing	—	—	—
6	RESET_N	I	Reset input pin	—	—	—
11	V_{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—
13	AIN0	I	Successive approximation type ADC input	—	—	—
14	AIN1	I	Successive approximation type ADC input	—	—	—
15	AIN2	I	Successive approximation type ADC input	—	—	—
16	AIN3	I	Successive approximation type ADC input	—	—	—
21	NMI	I	Non-maskable interrupt pin	—	—	—
3	P00/EXI0	I	Input port, External interrupt 0	—	—	—
24	P01/EXI1	I	Input port, External interrupt 1	—	—	—
23	P02/EXI2/ RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—
22	P03/EXI3	I	Input port, External interrupt 3	—	—	—
17	P10/ CKINEN	I	Input port External clock enable	—	—	—
18	P11/ UCK0EN	I	Input port UART0 external clock enable pin	—	—	—
42	P20	O	Output port	—	—	—
41	P21	O	Output port	—	—	—
39	P22	O	Output port	—	—	—
38	P23	O	Output port	—	—	—
37	P24	O	Output port	—	—	—
4	P30/CKIN	I/O	Input/output port External clock input	—	—	—
26	P31/UCK0	I/O	Input/output port UART external clock input	—	—	—
27	P32	I/O	Input/output port	—	—	—
28	P33	I/O	Input/output port	—	—	—
9	P34	I/O	Input/output port	PWM0	O	PWM0 output
1	SDA	I/O	I^2C data input/output	P40	I/O	Input/output port
2	SCL	I/O	I^2C clock input/output	P41	I/O	Input/output port
29	RXD0	I	UART data input	P42	I/O	Input/output port
30	TXD0	O	UART data output	P42	I/O	Input/output port
31	P44/T02P0 CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	SIN0	I	SSIO0 data input
32	P45/T13P1 CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	SCK0	I/O	SSIO0 synchronous clock
33	P46	I/O	Input/output port	SOUT0	O	SSIO0 data output
34	P47	I/O	Input/output port	—	—	—
19	PA0	I/O	Input/output port	—	—	—

PIN No.	Primary function			Secondary function		
	Pin name	I/O	Function	Pin name	I/O	Function
20	PA1	I/O	Input/output port	—	—	—
43	PA2	I/O	Input/output port	—	—	—
44	PA3	I/O	Input/output port	—	—	—
45	PA4	I/O	Input/output port	—	—	—
46	PA5	I/O	Input/output port	—	—	—
47	PA6	I/O	Input/output port	—	—	—
48	PA7	I/O	Input/output port	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
CKIN	I	High-speed external clock input pin. This pin is used as the primary function of the P30.	Primary	—
CKINEN	I	High-speed external clock enable pin. This pin is used as the primary function of the P10 pin.	Primary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
Input port				
P10-P11	I	High-speed external clock enable pin and UART0 external clock enable pin.	Primary	Positive
General-purpose output port				
P20-P24	O	Nch open drain output pins to drive LED.	Primary	Positive
General-purpose input/output port				
P30-P34	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Primary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary	Positive
UCK0	I	UART0 external clock input pin. This pin is used as the primary function of the P31.	Primary	—
UCK0EN	I	UART0 external clock enable pin. This pin is used as the primary function of the P11 pin.	Primary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the primary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Primary	Positive
SCL	I/O	I^2C clock output pin. This pin is used as the primary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Primary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P45 pin.	Secondary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P44 pin.	Secondary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P46 pin.	Secondary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P34 pin.	Secondary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/ negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—

Pin name	I/O	Description	Primary/ Secondary	Logic
Successive approximation type A/D converter				
AV_{SS}	—	Negative power supply pin for successive approximation type A/D converter.	—	—
AV_{DD}	—	Positive power supply pin for successive approximation type A/D converter.	—	—
V_{REF}	—	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0	I	Channel 0 analog input for successive approximation type A/D converter.	—	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter.	—	—
AIN2	I	Channel 2 analog input for successive approximation type A/D converter.	—	—
AIN3	I	Channel 3 analog input for successive approximation type A/D converter.	—	—
For testing				
TESTS	I	Input pin for testing. A pull-down resistor is internally connected.	—	—
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
AV_{DD}	V_{SS}
AV_{SS}	V_{SS}
V_{REF}	V_{SS}
AIN0, AIN1、AIN2, AIN3	Open
RESET_N	V_{DD}
TEST	Open
TESTS	Open
NMI	V_{DD}
P00 to P03	V_{DD} or V_{SS}
P10 to P11	V_{DD}
P20 to P24	Open
P30 to P34	Open
P40 to P47	Open
PA0 to PA7	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 2	AV_{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 3	V_{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 4	V_{DDL}	Ta = 25°C	−0.3 to +3.6	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output voltage 1	V_{OUT1}	Port3-A, Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output voltage 2	V_{OUT2}	Port2, Ta = 25°C	−0.3 to +7.0	V
Output current 1	I_{OUT1}	Port3–A, Ta = 25°C	−12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	1.0	W
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	−40 to +85	°C
Operating voltage	V_{DD}	—	1.6 to 3.6	V
	AV_{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f_{OP}	—	30k to 625k	Hz
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	1.0±30%	μF
	C_{L1}	—	0.1±30%	

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase[*1]	2.75 to 3.6	V
	V_{DDL}	At write/erase[*1]	2.5 to 2.75	
	V_{PP}	At write/erase[*1]	7.7 to 8.3	
			0	
Write cycles	C_{EP}	—	10	cycles
Data retention	Y_{DR}	—	10	years

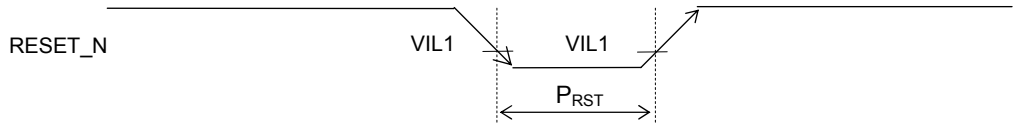
[*1]: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and eraseing Flash ROM. V_{PP} pin has an internal pulldown resister.

DC CHARACTERISTICS (1/4)

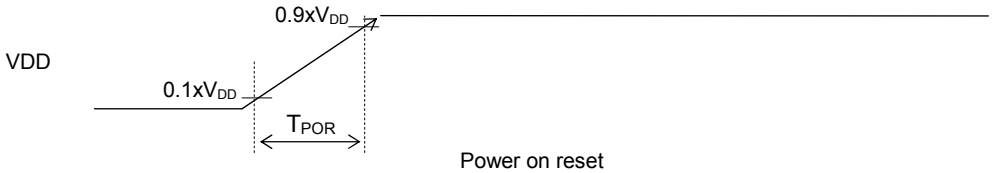
(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −40 to +85°C, unless otherwise specified) (1/4)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
500kHz RC oscillation frequency	f_{RC}	Ta = 25°C	Typ. −10%	500	Typ. +10%	kHz	1
		Ta = −40 to +85°C	Typ. −25%	500	Typ. +25%	kHz	
Reset pulse width	P_{RST}	—	200	—	—	μs	
Reset noise elimination pulse width	P_{NRST}	—	—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—	—	—	10	ms	

RESET



RESET_N pin reset



Power on reset

DC CHARACTERISTICS (2/4)

(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −40 to +85°C, unless otherwise specified) (2/4)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
BLD threshold voltage	V_{BLD}	—	LD3–0 = 4H	Typ. −2%	1.6	Typ. +2%	V	1
			LD3–0 = 5H		1.7			
			LD3–0 = 6H		1.8			
			LD3–0 = 7H		1.9			
			LD3–0 = 8H		2.0			
			LD3–0 = 9H		2.1			
			LD3–0 = 0AH		2.2			
			LD3–0 = 0BH		2.3			
			LD3–0 = 0CH		2.4			
			LD3–0 = 0DH		2.5			
			LD3–0 = 0EH		2.7			
			LD3–0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	—		—	0	—	%/°C	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed RC500kHz oscillation: stopped.		—	0.2	5.	μA	

Supply current 2	IDD2	CPU: In HALT state (LTBC and WDT are Operating.) *1 High-speed 500kHz oscillation: Stopped.	—	15	30	μA	
Supply current 3	IDD3	CPU: In 31.25kHz operating state.	—	25	40	μA	
Supply current 4	IDD4	CPU: In RC 500kHz operating state.	—	100	150	μA	
Supply current 5	IDD5	CPU: In RC 500kHz operating state. A/D: In operating state. V_{DD} = AV_{DD} = 3.0V	—	400	900	μA	

*1: Significant bits of BLKCON0~BLKCON4 registers are all “1”.

DC CHARACTERISTICS (3/4)

(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = −40 to +85°C, unless otherwise specified) (3/4)

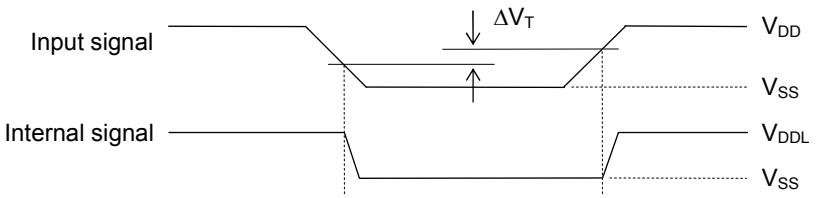
Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P30–P34) (P40–P47) (PA0–PA7)	VOH1	IOH1 = −0.5mA	V_{DD} −0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA	—	—	0.5		
Output voltage 2 (P20–P24)	VOL2	IOL2 = +10mA, V_{DD} = 3.3V	—	—	0.5		
		IOL2 = +5mA, V_{DD} = 1.8 to 3.6V	—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = +3mA, V_{DD} = 2.0 to 3.6V (when I^2C mode is selected)	—	—	0.4		
Output leakage (P20–P24) (P30–P34) (P40–P47) (PA0–PA7)	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	−1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}	0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	−600	−300	-10		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD}	10	300	600		
	IIL1	VIL1 = V_{ss}	-1	—	—		
Input current 2 (NMI) (P00-P03) (P10-P11) (P30-P34) (P40-P47) (PA0-PA7)	IIH2	VIH2 = V_{DD} (when pulled-down)	0.2	30	200		
	IIL2	VIL2 = V_{SS} (when pulled-up)	−200	−30	-0.2		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)	—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)	−1	—	—		
Maximum voltage (P20–P24)	VOUTH	—	0	—	5.0	V	—
Maximum curennt (P20–P24)	IOL2	—	0	—	10	mA	—

DC CHARACTERISTICS (4/4)

(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified) (4/4)

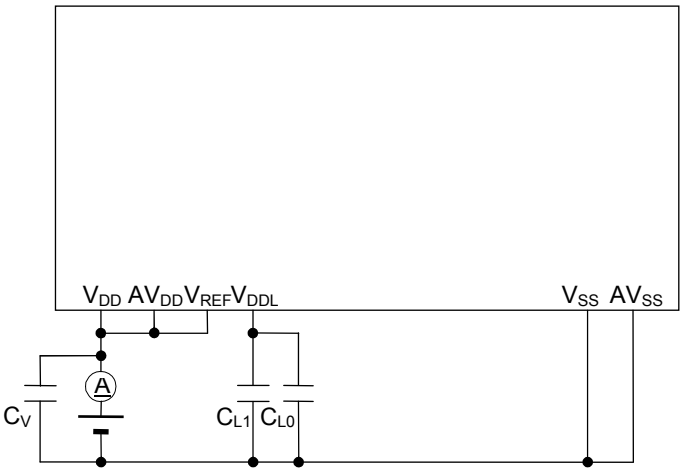
Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10–P11) (P30–P34) (P40–P47) (PA0–PA7)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3 ×V_{DD}		
Hysteresis width (RESET_N) (TEST_N) (NMI) (P00–P03) (P10–P11) (P30–P34) (P40–P47) (PA0–PA7)	ΔVT	—	0.02 ×V_{DD}	0.18 ×V_{DD}	0.4 ×V_{DD}		

HYSTERESIS WIDTH



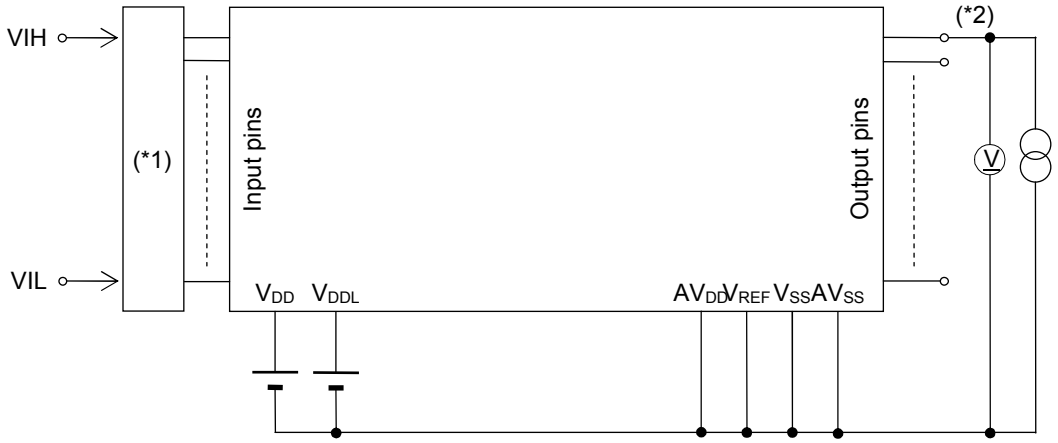
MEASURING CIRCUITS

MEASURING CIRCUIT 1



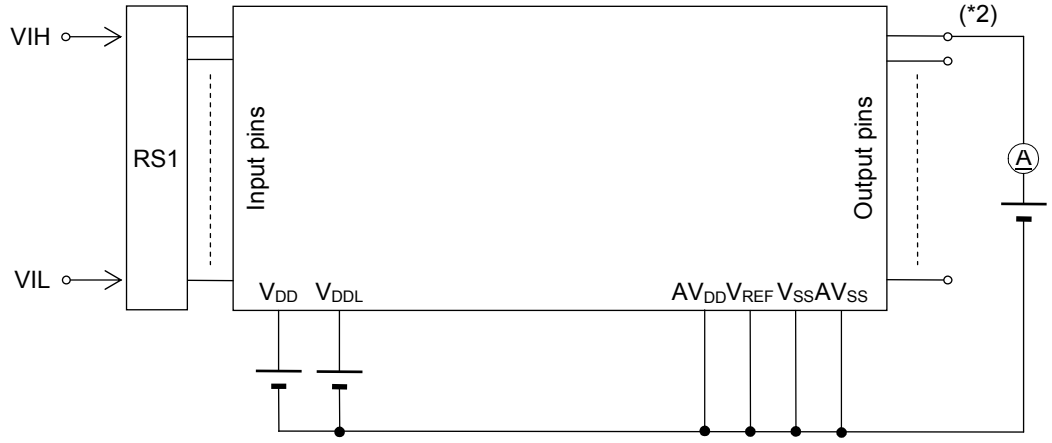
C_V: 1μF
C_{L0}: 1μF
C_{L1}: 0.1μF

MEASURING CIRCUIT 2



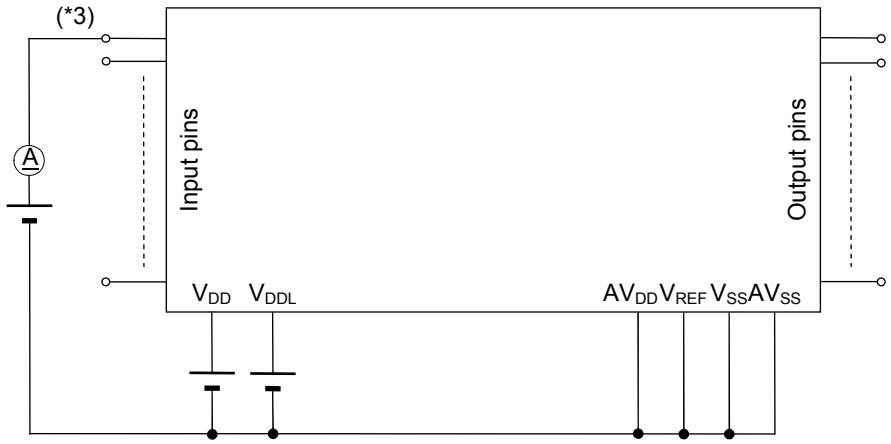
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



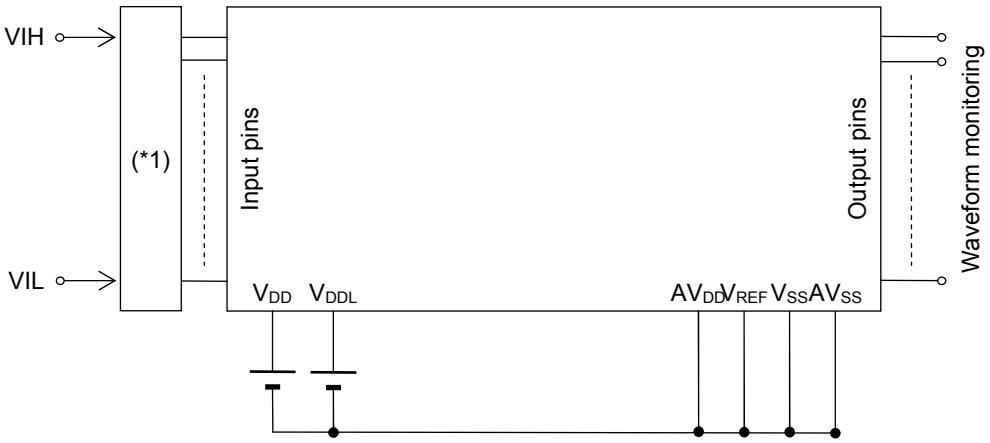
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5



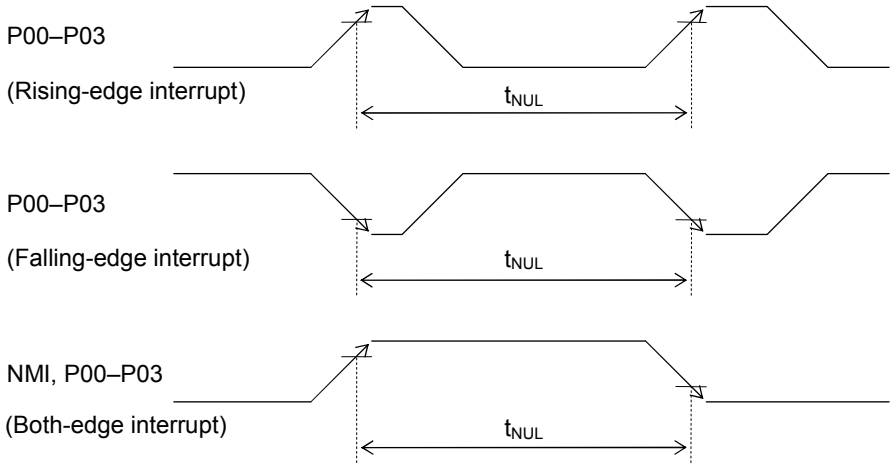
*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	—	—	4.0	ϕ*1

*1: ϕ : Period of System clock (SYSCLK)

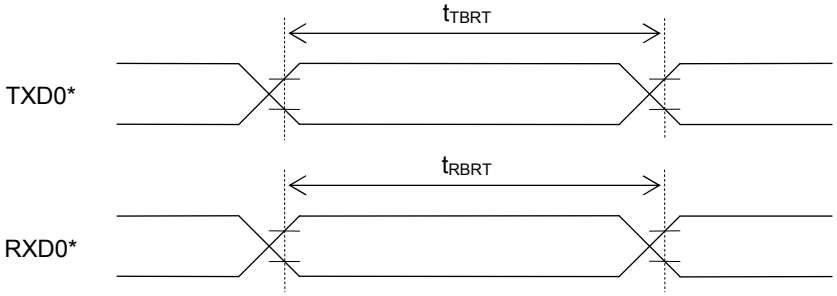


AC CHARACTERISTICS (Serial Port)

(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*1	—	s
Receive baud rate	t_{RBRT}	—	BRT*1 –3%	BRT*1	BRT*1 +3%	s
External baud rate clock	$1/t_{UCK}$	—	—	—	500	kHz

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



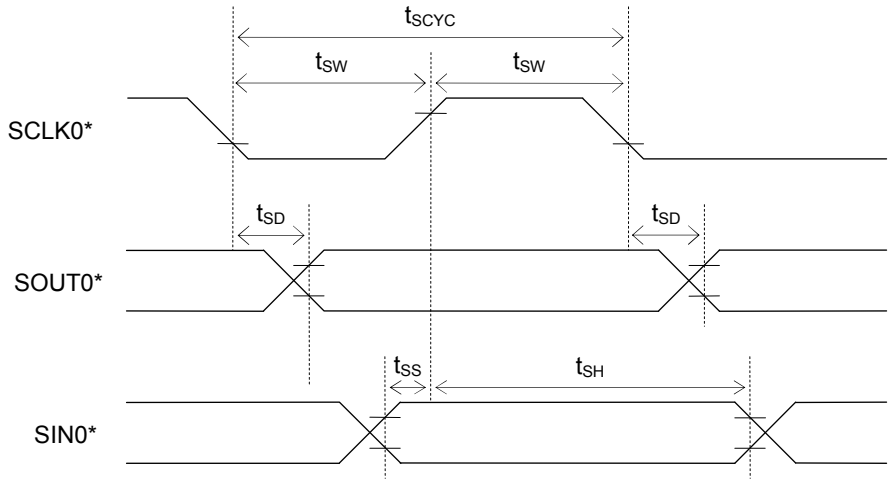
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	µs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*1	—	s
SCLK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	µs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	—	180	—	—	ns
SIN input hold time	t_{SH}	—	80	—	—	ns

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)

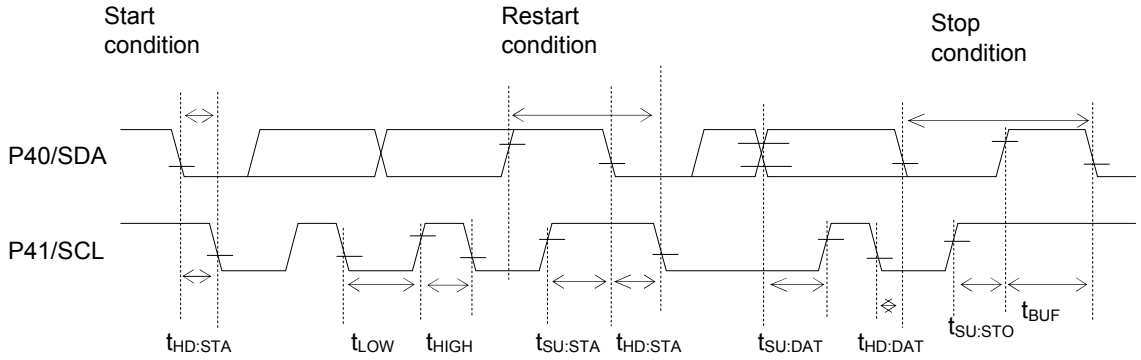


*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I^2C Bus Interface: Standard Mode)

(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	—	25.0, 27.7, 31.25, 35.7	—	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

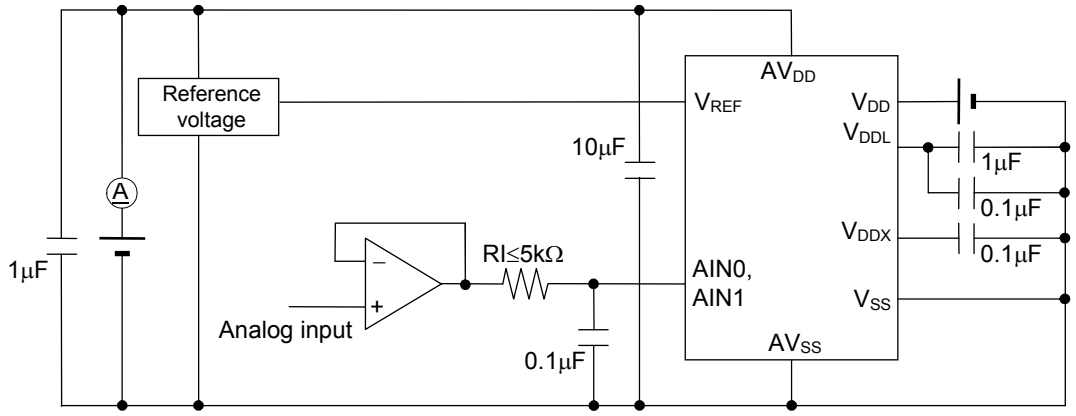


Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD} = 1.6 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

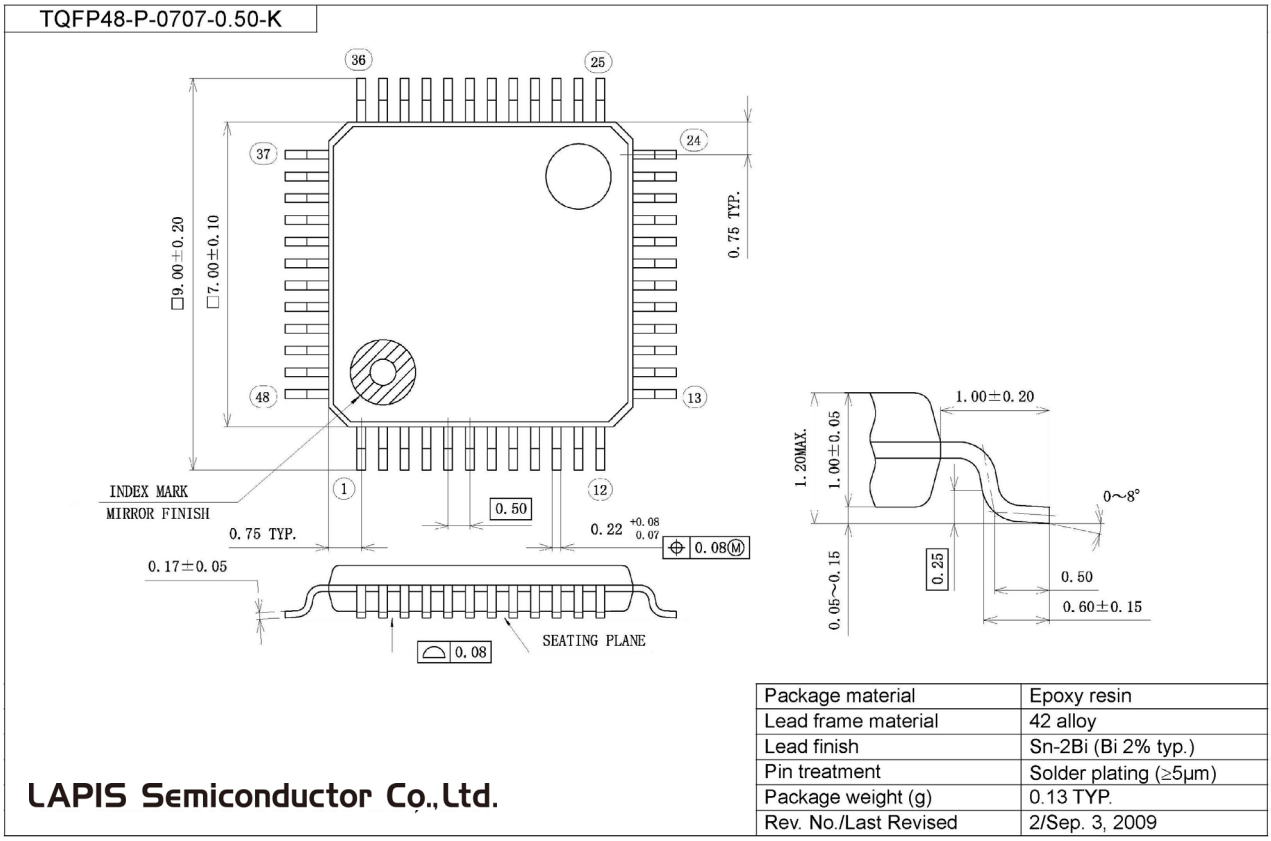
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 3.6V	–4	—	+4	LSB
		2.2V ≤ V_{REF} ≤ 2.7V	–6	—	+6	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	–3	—	+3	
		2.2V ≤ V_{REF} ≤ 2.7V	–5	—	+5	
Zero-scale error	V_{OFF}	—	–6	—	+6	
Full-scale error	FSE	—	–6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	—	—	23*1	—	ϕ/CH

ϕ: Period of high-speed clock (HSCLK)
*1: 2ϕ / CH is required as an interval time for each conversion in the case of consecutive A/D conversion.



Package Dimensions

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.13 TYP.
Rev. No./Last Revised	2/Sep. 3, 2009

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q486-01	Apr.19, 2010	–	–	Formally edition 1
FEDL610Q486-02	Jan. 5, 2011	23	23	Change of package dimensions.

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