FEDL610Q484-01
Issue Date: Mar.13, 2012

ML610Q484

8-bit Microcontroller

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, PWM, and RC oscillation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications.
The on-chip debug function that is installed enables program debugging and programming.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5 µs (@32.768 kHz system clock)
    0.250µs (@4 MHz system clock)

- Internal memory
  - Internal 16KByte Flash ROM (8K×16 bits) (including unusable 1KByte TEST area)
  - Internal 1KByte Data RAM (1024×8 bits)

- Interrupt controller
  - 1 non-maskable interrupt sources (Internal source)
  - 23 maskable interrupt sources (Internal sources: 16, External sources: 7)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48 ppm) (*)
  - High-speed time base counter ×1 channel

  (*) without low speed clock frequency deviation

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s @32kHz)

- Timers
  - 8 bits × 6 channels (Timer0-5: 16-bit x 2 configuration available by using Timer0-1 or TimerA-B or TimerC-D)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)
  - Continuous timer mode/One shot timer mode
  - Timer count start/stop by software and external trigger

- Captures
  - Time base capture × 2 channels(4096Hz-32Hz)

- PWM
  - Resolution 16 bits × 2 channel
  - Continuous PWM mode/One shot PWM mode
  - PWM start/stop by software and external trigger

- Synchronous serial port × 1 channel
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Half-Duplex Communication
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 1 channel

- Analog Comparator
  - Operating voltage: V_{DD}=1.8V～3.6V
  - Common mode input voltage: 0.2V～VDD－1.0V
  - Input offset voltage: 50mV(max)
  - Interrupt allow edge selection and sampling selection

- General-purpose ports
  - Input-only port × 3 channels (including secondary functions)
  - Output-only port × 4 channels (including secondary functions)
  - Input/output port × 13 channels (including secondary functions)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow

- Clock
  - Low-speed clock:
    Build-in RC oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (500kHz/4MHz selectable by software)

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - Chip
    ML610Q484-xxxWA
    ML610Q484P-xxxWA
  - 28-pin plastic WQFN
    ML610Q484-xxxGDZ07A
    ML610Q484P-xxxGDZ07A
    xxx: ROM code number (xxx is NNN for blank product)
    Q: Flash version
    P: Wide range temperature version
    WA: Chip
    GDZ07A: WQFN

- Guaranteed operating range
  - Operating temperature: –20°C to +70°C (P version: –40°C to +85°C)
  - Operating voltage: V_{DD} = 1.25V to 3.6V

BLOCK DIAGRAM

ML610Q484 Block Diagram

Figure 1 show the block diagram of the ML610Q484.
"*" indicates the secondary and tertiary function of each port.

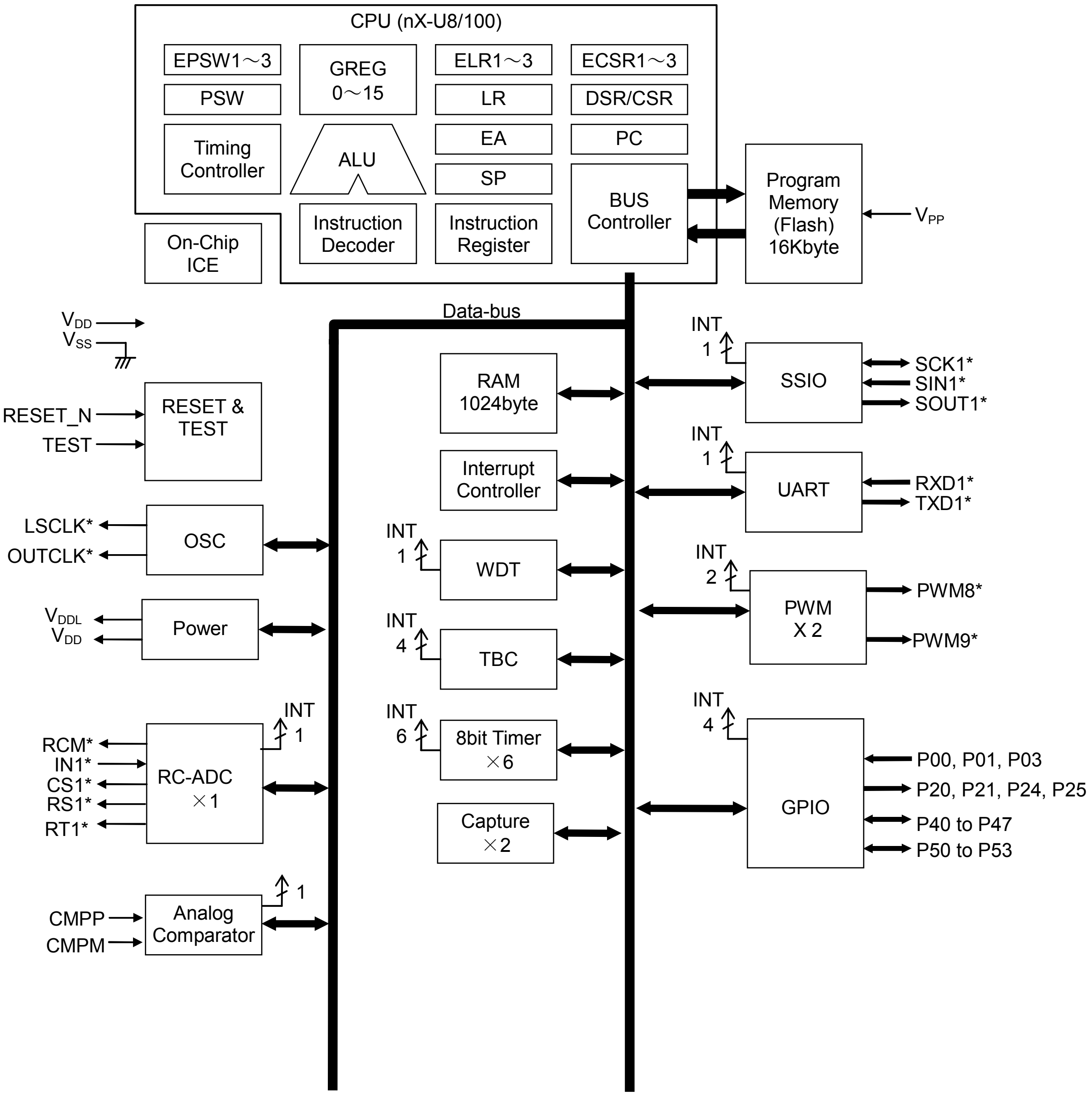
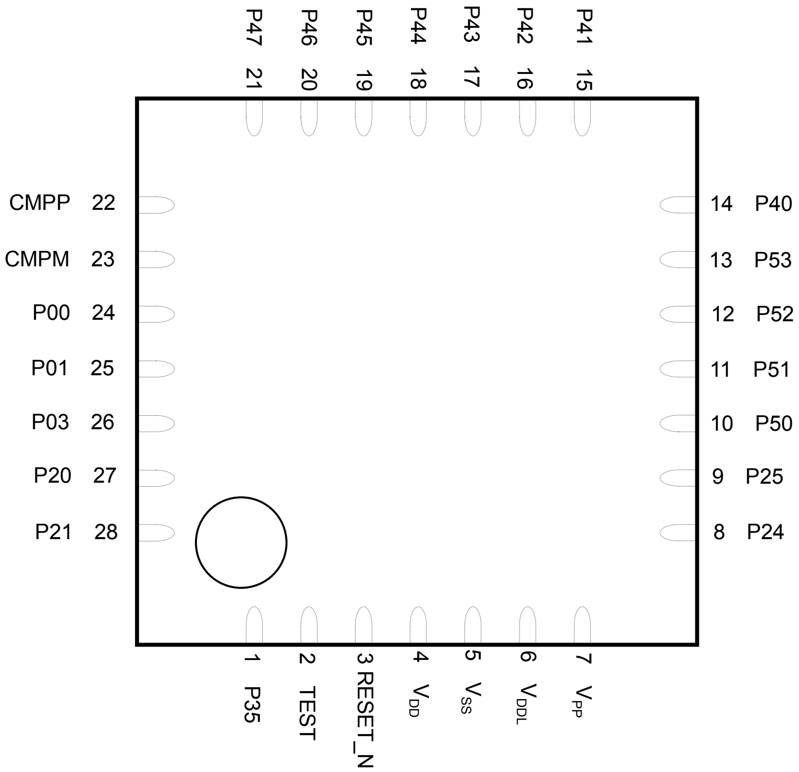


Figure 1 ML610Q484 Block Diagram

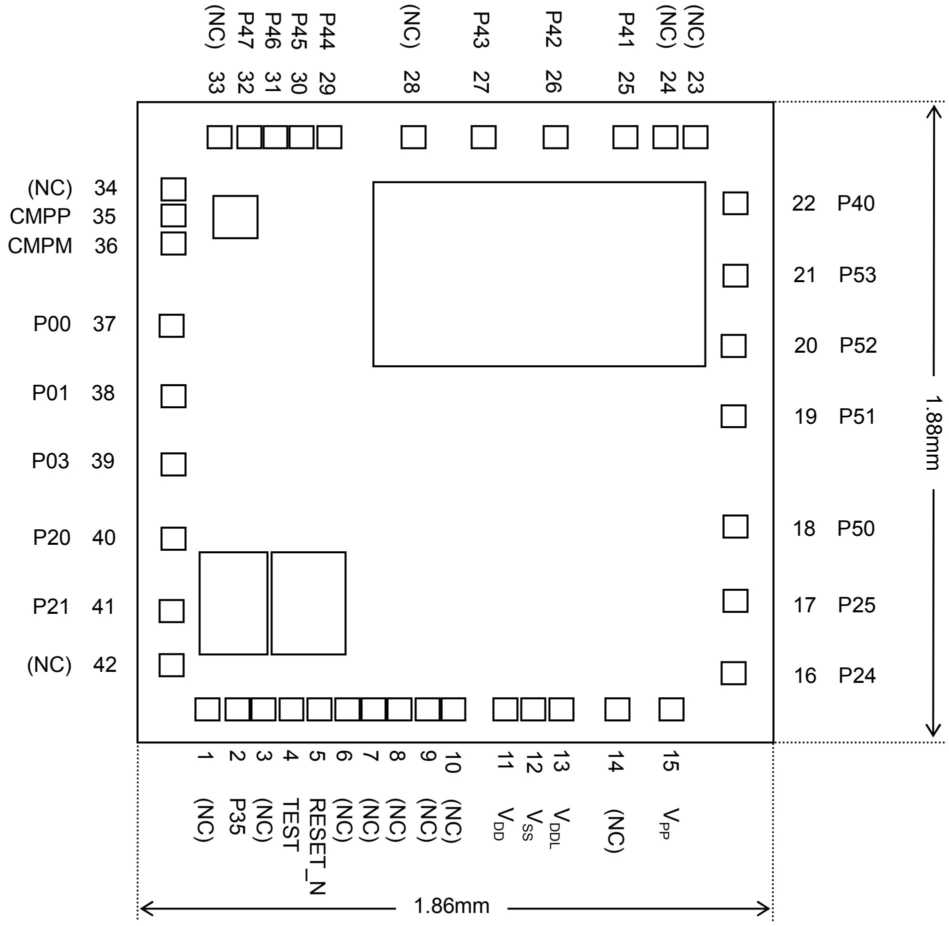
PIN CONFIGURATION

ML610Q484 WQFN28 Pin Layout



ML610Q484 WQFN28 Pin Configuration

ML610Q484 Chip Pin Layout & Dimension



Chip size: 1.86 mm × 1.88 mm
PAD count: 42 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

ML610Q484 Chip Layout & Dimension

Note: Please do not bond to the “(NC)” pad.

ML610Q484 Pad Coordinates

Table 1 ML610Q484 Pad Coordinates

Chip Center: X=0, Y=0

No	Name	X(mm)	Y(mm)	No	Name	X(mm)	Y(mm)
1	(NC)	-716	-834	22	P40	824	638
2	P35	-636	-834	23	(NC)	703	834
3	(NC)	-556	-834	24	(NC)	623	834
4	TEST	-476	-834	25	P41	499	834
5	RESET_N	-396	-834	26	P42	293	834
6	(NC)	-316	-834	27	P43	87	834
7	(NC)	-236	-834	28	NC	-119	834
8	(NC)	-156	-834	29	P44	-361	834
9	(NC)	-76	-834	30	P45	-441	834
10	(NC)	4	-834	31	P46	-521	834
11	VDD	154	-834	32	P47	-601	834
12	VSS	234	-834	33	(NC)	-681	834
13	VDDL	314	-834	34	(NC)	-824	682
14	(NC)	477	-834	35	CMPP	-824	602
15	VPP	635	-834	36	CMPM	-824	522
16	P24	824	-728	37	P00	-824	283
17	P25	824	-516	38	P01	-824	80
18	P50	824	-304	39	P03	-824	-123
19	P51	824	20	40	P20	-824	-335
20	P52	824	226	41	P21	-824	-547
21	P53	824	432	42	(NC)	-824	-705

PIN LIST

PIN No.	PAD No.	Primary function			Secondary /Tertiary function			
		Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
5	12	Vss	—	Negative power supply pin	—	—	—	—
4	11	V_{DD}	—	Positive power supply pin	—	—	—	—
6	13	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—
7	15	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—
2	4	TEST	I/O	Input/output pin for testing	—	—	—	—
3	5	RESET_N	I	Reset input pin	—	—	—	—
24	37	P00/EXI0/ CAP0/ TPRUN0	I	Input port, External interrupt 0, Capture 0 input, Timer and PWM common external trigger input	—	—	—	—
25	38	P01/EXI1/ CAP1/ TPRUN1	I	Input port, External interrupt 1, Capture 1 input, Timer and PWM common external trigger input	—	—	—	—
26	39	P03/EXI3/ RXD1/ TPRUN3	I	Input port, External interrupt 3, UART1 data input, Timer and PWM common external trigger input	—	—	—	—
22	35	CMPP	I	Analog comparator non-inverted input	—	—	—	—
23	36	CMPM	I	Analog comparator inverted input	—	—	—	—
27	40	P20/LED0	O	Output port	Secondary	LSCLK	O	Low-speed clock output
28	41	P21/LED1	O	Output port	Secondary	OUTCLK	O	High-speed clock output
8	16	P24/LED4	O	Output port	Secondary	PWM8	O	PWM8 output
9	17	P25/LED5	O	Output port	Secondary	PWM9	O	PWM9 output
1	2	P35	I/O	Input/output port	Secondary	RCM	O	RC type ADC oscillation monitor
					Tertiary	PWM9	O	PWM9 output
14	22	P40	I/O	Input/output port	—	—	—	—
15	25	P41	I/O	Input/output port	—	—	—	—
16	26	P42/ TABRUN	I/O	Input/output port, TimerA/TimerB external trigger input	—	—	—	—
17	27	P43/ TABRUN	I/O	Input/output port, TimerA/TimerB external trigger input	Tertiary	PWM8	O	PWM8 output
18	29	P44/ T0AP8CK/ TCDRUN	I/O	Input/output port, Timer0/TimerA/ PWM8 external clock input, TimerC/TimerD external trigger input	Secondary	IN1	I	RC type ADC1 oscillation input pin
19	30	P45/ T1BP9CK/ TCDRUN	I/O	Input/output port, Timer1/TimerB/PWM9 external clock input, TimerC/TimerD external trigger input	Secondary	CS1	O	RC type ADC1 reference capacitor connection pin
20	31	P46/ TCCK	I/O	Input/output port, TimerC external clock input	Secondary	RS1	O	RC type ADC1 reference resistor connection pin
21	32	P47/ TDCK	I/O	Input/output port, TimerD external clock input	Secondary	RT1	O	RC type ADC1 resistor sensor connection pin
					Tertiary	PWM9	O	PWM9 output

PIN No.	PAD No.	Primary function			Secondary /Tertiary function			
		Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
10	18	P50/EXI8/ P89RUN	I/O	Input/output port, External interrupt 8, PWM8/PWM9 external trigger input	Tertiary	SIN1	I	SSIO1 data input
11	19	P51/EXI8/ P89RUN	I/O	Input/output port, External interrupt 8, PWM8/PWM9 external trigger input	Tertiary	SCK1	I/O	SSIO1 synchronous clock
12	20	P52/EXI8	I/O	Input/output port, External interrupt 8	Secondary	RXD1	I	UART1 data input
					Tertiary	SOUT0	I	SSIO1 data output
13	21	P53/EXI8	I/O	Input/output port, External interrupt 8	Tertiary	TXD1	I	UART1 data output

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00,P01,P03	I	General-purpose input port.	Primary	Positive
General-purpose output port				
P20,P21, P24,P25	O	General-purpose output port. Since these pins have secondary functions or tertiary functions, the pins cannot be used as a port when the secondary functions or tertiary functions are used.	Primary	Positive
General-purpose input/output port				
P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary function is used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions or tertiary functions, the pins cannot be used as a port when the secondary functions or tertiary functions are used.	Primary	Positive
P50-P53	I/O	General-purpose input/output port. Since these pins have secondary functions or tertiary functions, the pins cannot be used as a port when the secondary functions or tertiary functions are used.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD1	O	UART1 data output pin. This pin is used as the secondary function of the P53 pin.	Secondary	Positive
RXD1	I	UART1 data input pin. This pin is used as the secondary function of the P52 pin.	Secondary	Positive
Synchronous serial (SSIO)				
SCK1	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P51 pin.	Tertiary	—
SIN1	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P50 pin.	Tertiary	Positive
SOUT1	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P52 pin.	Tertiary	Positive
PWM				
PWM8	O	PWM8 output pin. This pin is used as the secondary function of the P24 or the tertiary function P43 pin.	Secondary/ Tertiary	Positive
T0AP8CK	I	PWM8 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
PWM9	O	PWM9 output pin. This pin is used as the secondary function of the P25 pin or the tertiary function of the P47 pin.	Tertiary	Positive
T1BP9CK	I	PWM9 external clock input pin. This pin is used as the primary function of the P46 pin.	Primary	—
P89RUN	I	PWM8/PWM9 external trigger input pin. This pin is used as the primary function of the P50 pin and the primary function of the P50 pin.	Primary	Positive/ negative
TPRUN0, TPRUN1, TPRUN3	I	PWM8/PWM9 common external trigger input pin. This pin is used as the primary function of the P00, P01 and P03 pin.	Primary	Positive/ negative
External interrupt				
EXI0,1,3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00, P01 and P03 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P50-P53 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin (CAP1).	Primary	—
CAP1	I		Primary	—
Timer				
T0AP8CK	I	External clock input pin used for both Timer 0 and Timer A. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T1BP9CK	I	External clock input pin used for both Timer 1 and Timer B. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
TCCK	I	External clock input pin used for Timer C. The clock for this timer is selected by software. This pin is used as the primary function of the P46 pin.	Primary	—
TDCK	I	External clock input pin used for Timer D. The clock for this timer is selected by software. This pin is used as the primary function of the P47 pin.	Primary	—
TABRUN	I	TimerA/TimerB external trigger input. This pin is used as the primary function of the P42 pin and the primary function of the P43 pin.	Primary	Positive/ negative
TCDRUN	I	TimerC/TimerD external trigger input. This pin is used as the primary function of the P44 pin and the primary function of the P45 pin.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
TPRUN0, TPRUN1, TPRUN3	I	TimerA/TimerB/TimerC/TimerD common external trigger input. These pins are used as the primary functions of the P00, P01 and P03 pins.		Positive/ negative
LED drive				
LED0,1,4,5	O	NMOS open drain output pins to drive LED. These pins are used as the primary function of the P20,P21,P24,P25 pins.	Primary	Positive/ negative
RC oscillation type A/D converter				
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of P35 pin.	Secondary	—
Analog comparator				
CMPP	I	Non-inverted input pin.	—	—
CMPM	I	Inverted input pin.	—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors C_L (see measuring circuit 1) is connected between this pin and V_{SS}.	—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
RESET_N	Open
TEST	Open
P00 ,P01,P03	V_{DD} or V_{SS}
P20, P21, P24, P25	Open
P35	Open
P40 to P47	Open
P50 to P53	Open
CMPP,CMPM	V_{DD}

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–5, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	non-P version	–20 to +70	°C
		P version	–40 to +85	
Operating voltage	V_{DD}	—	1.25 to 3.6	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.25 to 3.6V	30k to 625k	Hz
		V_{DD} = 1.8 to 3.6V	32k to 4.08M	
Capacitor externally connected to V_{DD} pin	C_V	—	2.2	μF
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	0.1	μF
	C_{L1}	—	2.2	μF

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase[*1]	2.75 to 3.6	V
	V_{DDL}	At write/erase[*1]	2.5 to 2.75	
	V_{PP}	At write/erase[*1]	7.7 to 8.3	
erase/program cycles	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

[*1]: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and eraseing Flash ROM.
V_{PP} pin has an internal pulldown resister.

OPERATING CONDITIONS OF ANALOG COMPARATOR

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +75°C , Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Common mode Input voltage	CMV_{IN}	V_{DD} = 1.8 to 3.6V	0.2	—	V_{DD}−1	V	1
Input offset voltage	V_{CMPOF}	V_{DD} = 1.8 to 3.6V, Ta = 25°C	—	—	50	mV	
Response time	T_{CMP}	V_{DD} = 1.8 to 3.6V, Ta = 25°C Over drive = 100mV	—	—	100	μs	
Wake-up time	T_{CMPw}		—	—	3	ms	
Circuit current (during operation)	I_{CMP}	V_{DD} = 1.8 to 3.6V,Ta = 25°C	—	2	4	μA	

DC CHARACTERISTICS (1/4)

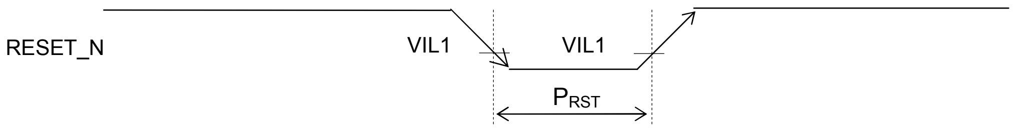
(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +75°C , Ta = −40 to +85°C for P version, unless otherwise specified) (1/4)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
4MHz RC oscillation frequency	f_{RC}	V_{DD} = 2.5 to 3.6V Ta = 0 to +40°C (*2)		Typ. −1.5%	4M	Typ. +1.5%	Hz	1
		V_{DD} = 1.8 to 3.6V Ta = −40 to +85°C		Typ. −3%	4M	Typ. +3%	Hz	
500kHz RC oscillation frequency		V_{DD} = 1.8 to 3.6V (*1)	Ta = 0 to +40°C	Typ. −1.5%	500k	Typ. +1.5%	Hz	
		All recommended condition		Typ. −20%	500k	Typ. +20%	Hz	
32.768kHz RC oscillation frequency		V_{DD} = 1.8 to 3.6V (*1)	Ta = 0 to +40°C	Typ. −1.5%	32.768k	Typ. +1.5%	Hz	
		All recommended condition		Typ. −4%	32.768k	Typ. +4%	Hz	
500kHz/4MHz RC oscillation start time	t_{RCH}	—		—	—	5	µs	
32kHz RC oscillation start time	t_{RCL}	—		—	—	65	µs	
Reset pulse width	P_{RST}	—		200	—	—	µs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	

(*1) VDDLB bit of POWC register is set as “1”

(*2) Program operation mode (Both STP bit and HLT bits of Standby control register(SBYCON) are “0”)

RESET



RESET_N pin reset

Power on reset

DC CHARACTERISTICS (2/4)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +75°C , Ta = –40 to +85°C for P version, unless otherwise specified) (2/4)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped. *[2]	Ta= 25°C	—	0.9	1.4	μA	1
			*[4]	—	—	8.0		
Supply current 2	IDD2	CPU: In HALT state (LTBC,WDT:Operating*[1]). High-speed oscillation: Stopped.	Ta= 25°C	—	6.0	11	μA	
			*[4]	—	—	16		
Supply current 3	IDD3	CPU: In 32.768kHz operating state. *[2] High-speed oscillation: Stopped.	Ta= 25°C	—	10	15	μA	
			*[4]	—	—	20		
Supply current 4-1	IDD4-1	CPU: In 500kHz CR operating state. *[3]	Ta= 25°C	—	110	135	μA	
			*[4]	—	—	140		
Supply current 4-2	IDD4-2	CPU: In 4MHz CR operating state. *[3]	Ta= 25°C	—	650	690	μA	
			*[4]	—	—	700		

*[1] : Significant bits of BLKCON0~BLKCON4 registers are all “1”.
*[2] : VDDLB bit of POWC register is set as “0”.
*[3] : VDDLB bit of POWC register is set as “1”.
*[4] : Recommended operating temperature (Ta = −20 to +70°C, Ta = −40 to +85°C for P version)

DC CHARACTERISTICS (3/4)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +75°C , Ta = −40 to +85°C for P version, unless otherwise specified) (3/4)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
Output voltage 1 (P20-P21,P24-P25/N-ch open drain mode is not selected) (P35) (P40–P47) (P50–P53)	VOH1	IOH1 = −0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD} −0.5	—	—	V	2
		IOH1 = −0.03mA, V_{DD} = 1.25 to 3.6V		V_{DD} −0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.25 to 3.6V		—	—	0.3		
Output voltage 2 (P20-P21,P24-P25/N-ch open drain mode is selected)	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
Output leakage (P20-P21, P24-P25) (P35) (P40–P47) (P50–P53)[*1]	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		−1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		0	—	1	μA	4
	IIL1	VIL1 = V_{SS}		−600	−300	−20		
Input current 2 (TEST)	IIH2	VIH1 = V_{DD}		20	300	600		
	IIL2	VIL1 = V_{ss}		-1	—	—		
Input current 3 (P00–P01, P03) (P35) (P40–P47) (P50–P53)	IIH3	VIH3 = V_{DD} (when pulled-down)	V_{DD} = 1.8 to 3.6V	2	30	200		
			V_{DD} = 1.25 to 3.6V	0.01	30	200		
	IIL3	VIL3 = V_{SS}(when pulled-up)	V_{DD} = 1.8 to 3.6V	−200	−30	−2		
			V_{DD} = 1.25 to 3.6V	−200	−30	−0.01		
	IIH3Z	VIH3 = V_{DD} (in high-impedance state)		—	—	1		
	IIL3Z	VIL3 = V_{SS} (in high-impedance state)		−1	—	—		

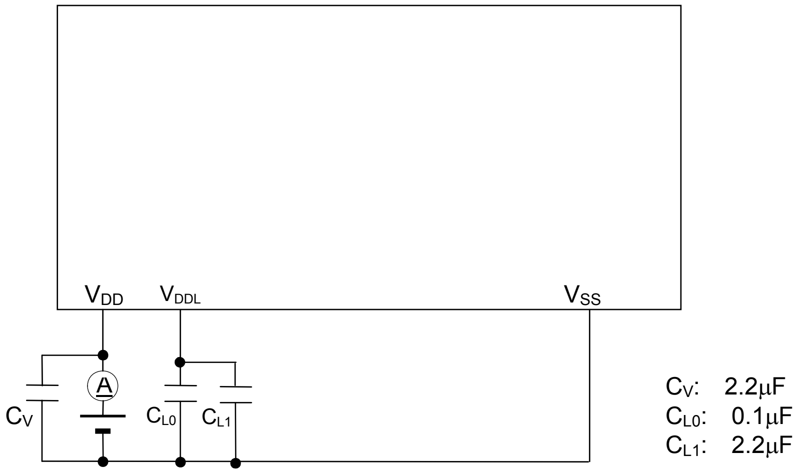
DC CHARACTERISTICS (4/4)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +75°C , Ta = –40 to +85°C for P version, unless otherwise specified) (4/4)

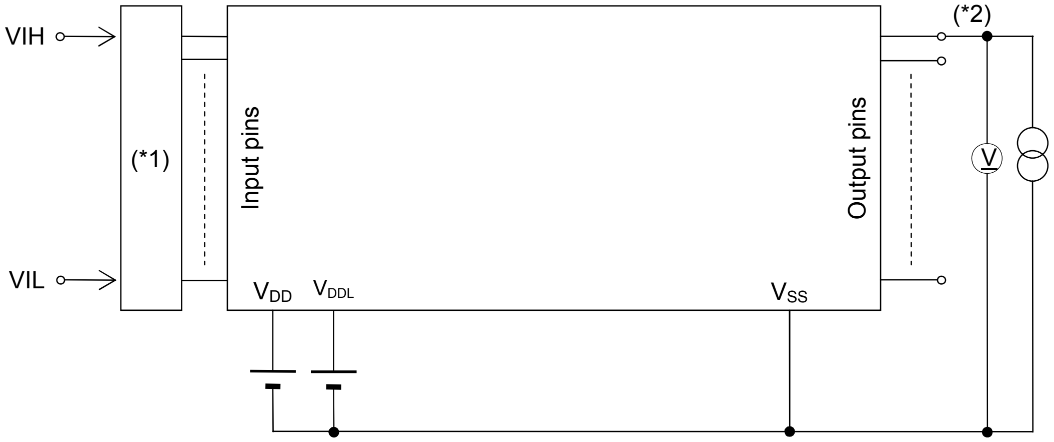
Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (P00–P01,P03) (P40–P47) (P50–P53)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	V_{DD} = 1.8 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.25 to 3.6V	0	—	0.2 ×V_{DD}		
Input pin capacitance (P00–P01, P03) (P35) (P40–P47) (P50–P53)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	5	pF	—

MEASURING CIRCUITS

MEASURING CIRCUIT 1

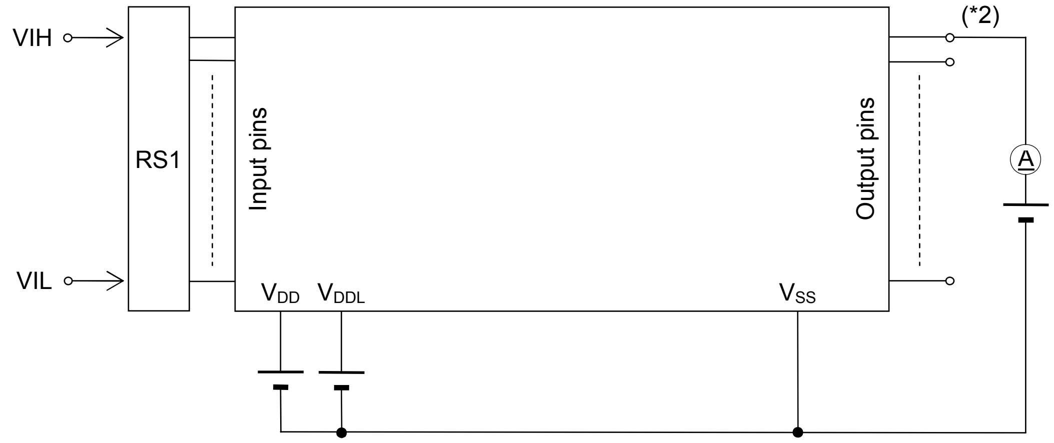


MEASURING CIRCUIT 2



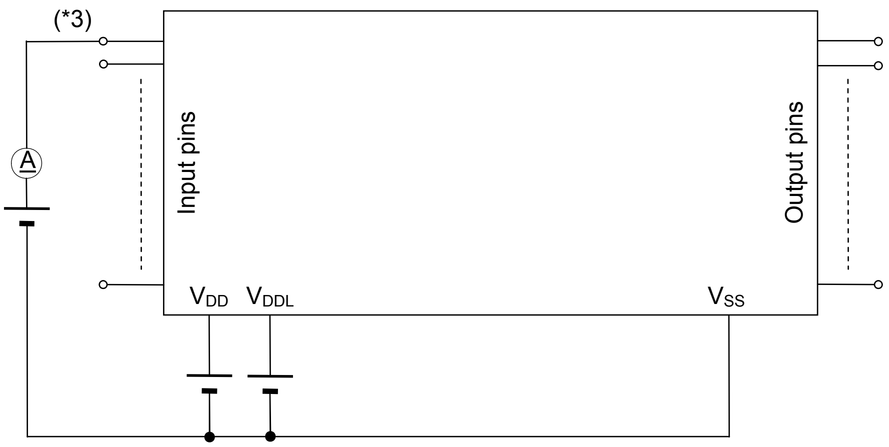
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



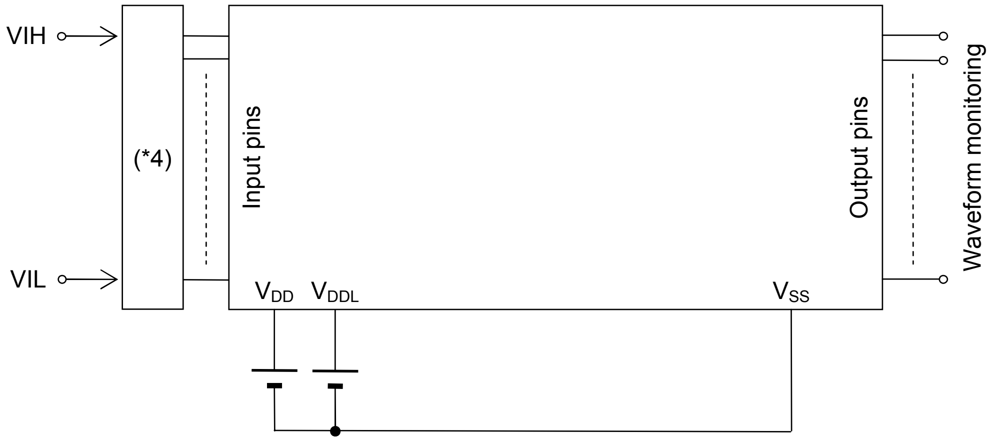
*1: Input logic circuit to determine the specified measured conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

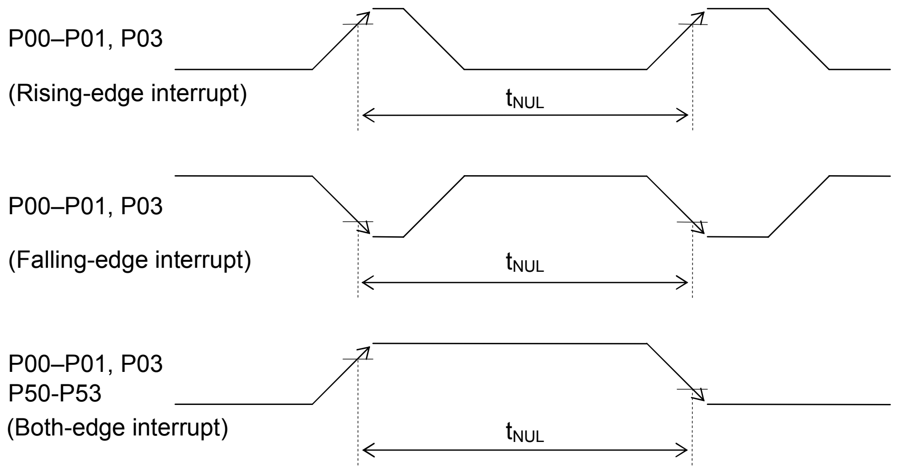


*4: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +75°C , Ta = −40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock : 32.768kHz	76.8	—	106.8	μS

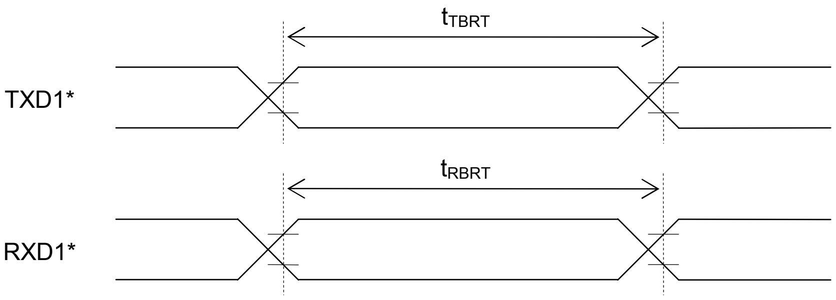


AC CHARACTERISTICS (UART)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +75°C , Ta = −40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT*[1] −3%	BRT*[1]	BRT*[1] +3%	s

*[1]: Baud rate period (including the error of the clock frequency selected) set with the UART1 baud rate register (UA1BRTL,H) and the UART1 mode register 0 (UA1MOD0).



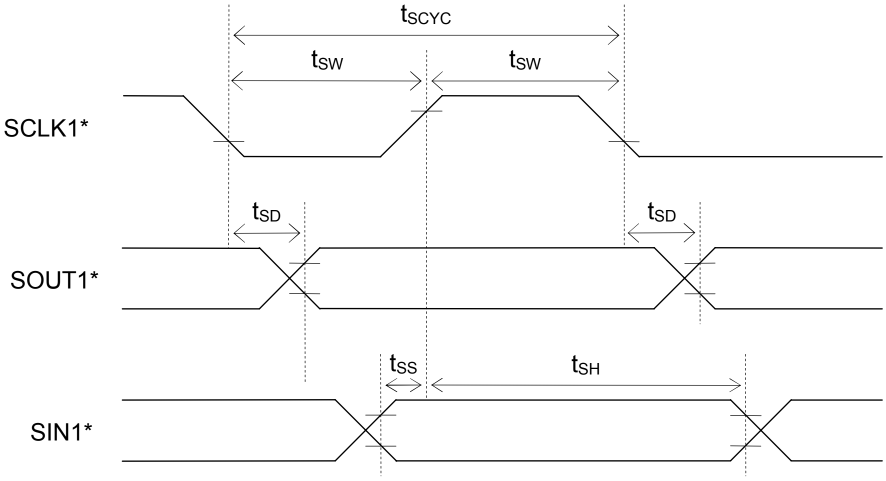
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = −20 to +75°C , Ta = −40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When 500kHz RC oscillation is active *[2] V_{DD} = 1.25 to 3.6V	10	—	—	μs
		When 4MHz RC oscillation is active *[3] V_{DD} = 1.8 to 3.6V	1	—	—	μs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*[1]	—	s
SCLK input pulse width (slave mode)	t_{SW}	When 500kHz RC oscillation is active *[2] V_{DD} = 1.25 to 3.6V	4	—	—	μs
		When 4MHz RC oscillation is active *[3] V_{DD} = 1.8 to 3.6V	0.4	—	—	μs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*[1] ×0.4	SCLK*[1] ×0.5	SCLK*[1] ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	When 500kHz RC oscillation is active *[2] V_{DD} = 1.25 to 3.6V , output load 10pF	—	—	500	ns
		When 4MHz RC oscillation is active *[3] V_{DD} = 1.8 to 3.6V, output load 10pF	—	—	240	
SOUT output delay time (master mode)	t_{SD}	When 500kHz RC oscillation is active *[2] V_{DD} = 1.25 to 3.6V , output load 10pF	—	—	500	ns
		When 4MHz RC oscillation is active *[3] V_{DD} = 1.8 to 3.6V, output load 10pF	—	—	240	
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	When 500kHz RC oscillation is active *[2] V_{DD} = 1.25 to 3.6V	500	—	—	ns
		When 4MHz RC oscillation is active *[3] V_{DD} = 1.8 to 3.6V	240	—	—	
SIN input hold time	t_{SH}	When 500kHz RC oscillation is active *[2] V_{DD} = 1.25 to 3.6V	300	—	—	ns
		When 4MHz RC oscillation is active *[3] V_{DD} = 1.8 to 3.6V	80	—	—	

*[1]: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)
*[2]: When 500kHz RC oscillation is selected with OSCM3 of the frequency control register (FCON0)
*[3]: When 4MHz RC oscillation is selected with OSCM3 of the frequency control register (FCON0)



*: Indicates the tertially function of the port.

AC CHARACTERISTICS (RC Oscillation A/D Converter)

Characteristics for V_{DD}=1.8 to 3.6V

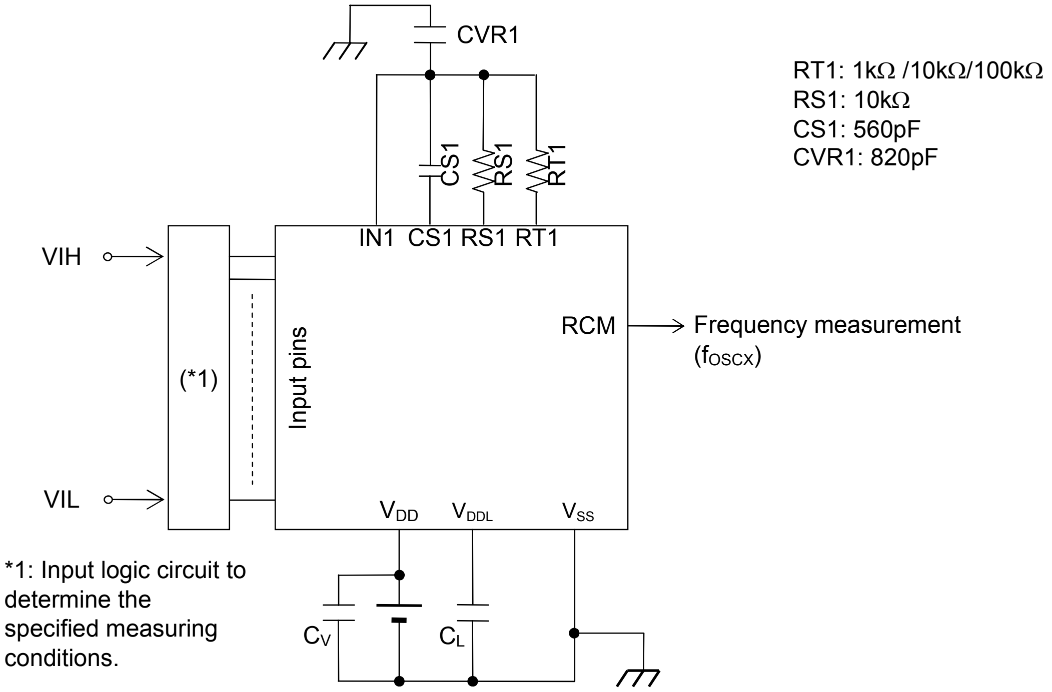
(V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = –20 to +75°C , Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resistors for oscillation	RS1,RT1	CS1 ≥ 740pF	1	—	—	kΩ
Oscillation frequency VDD = 3.0V	f_{OSC1}	Resistor for oscillation = 1kΩ	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio [*1] VDD = 3.0V	Kf1	RT1 = 1kHz	7.972	9.028	9.782	—
	Kf2	RT1 = 10kHz	0.981	1	1.019	—
	Kf3	RT1 = 100kHz	0.099	0.101	0.104	—

[*1]: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$\text{Kfx} = \frac{f_{OSCX}(\text{RT1–CS1 oscillation})}{f_{OSCX}(\text{RS1–CS1 oscillation})}$$

(x = 1, 2, 3)



Characteristics for V_{DD}=1.25 to 3.6V

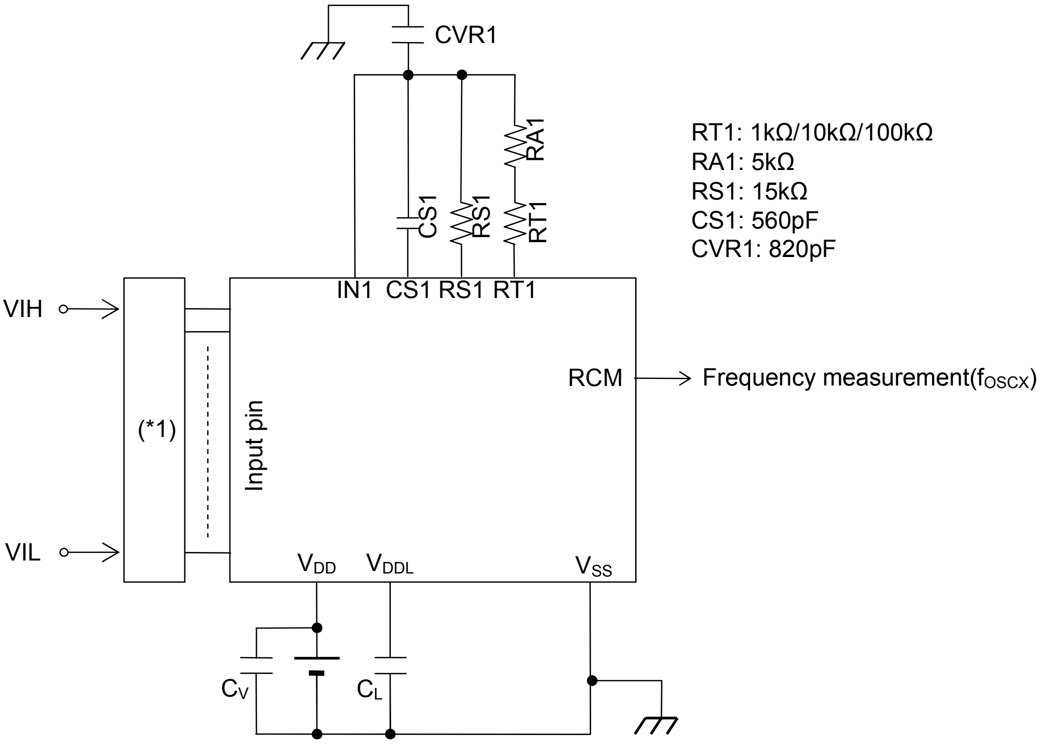
(V_{DD} = 1.25 to 3.6V, V_{SS} = 0V, Ta = –20 to +75°C , Ta = –40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resistors for oscillation	RS1,RT1	CS1 ≥ 740pF	1	—	—	kΩ
Oscillation frequency VDD = 1.5V	f_{OSC1}	Resistor for oscillation = 1kΩ	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio [*1] VDD = 1.5V	Kf1	RT1 = 1kHz	2.139	2.381	2.632	—
	Kf2	RT1 = 10kHz	0.973	1	1.028	—
	Kf3	RT1 = 100kHz	0.142	0.147	0.152	—
Oscillation frequency VDD = 3.0V	f_{OSC1}	Resistor for oscillation = 1kΩ	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio [*1] VDD = 3.0V	Kf1	RT1 = 1kHz	2.227	2.432	2.626	—
	Kf2	RT1 = 10kHz	0.982	1	1.018	—
	Kf3	RT1 = 100kHz	0.141	0.145	0.149	—

[*1]: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$\text{Kfx} = \frac{f_{OSCX}(\text{RT1}-\text{CS1 oscillation})}{f_{OSCX}(\text{RS1}-\text{CS1 oscillation})}$$

(x = 1, 2, 3)



(*1) input logic circuit to determine the specified measuring conditions

Note:

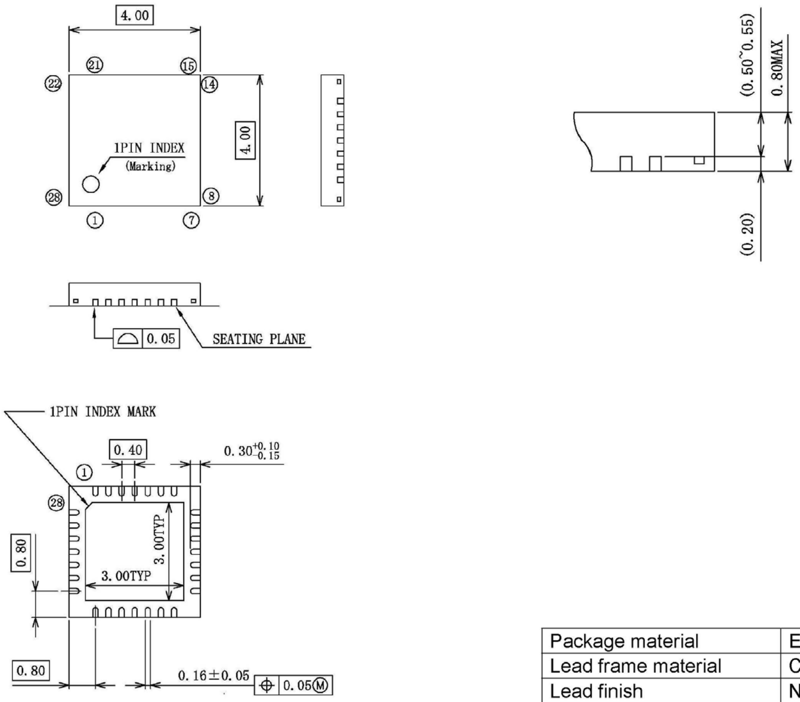
- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN1 pin), including CVR1. Especially, do not have long wire between IN1 and RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.

- Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

PACKAGE DIMENSIONS

(Unit: mm)

P-WQFN28-0404-0.40-63



LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 max./0.15 max.
Package weight (g)	0.040 TYP.
Rev. No./Last Revised	2/Apr. 5, 2011

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q484-01	Mar.13, 2012	–	–	Formally edition 1.0

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