ML2282X-XXX/ML2286X-XXX

Speech Synthesis LSI with Built-in P2ROM Including 2-Channel Mixing Function

GENERAL DESCRIPTION

ML2282X(ML22825/ML22824/ML22823-XXX) and ML2286X (ML22865/ML22864/ML22783-XXX) are voice synthesis LSIs with built-in P2ROM that stores speech data.
These LSIs include edit ROM, ADPCM2 decoder, 16-bit DA converter, low pass filter and monaural speaker amplifier. Also, ML2282X supports the synchronous serial interface and ML22865/ML22864/ML22863 supports the I2C interface.
By integrating all the functions required for voice output into a single chip, these LSIs can be more easily incorporated in compact portable devices.

- Built-in memory capacity and maximum vocal reproduction time:

(at the case of 4-bit ADPCM2 algorithm)

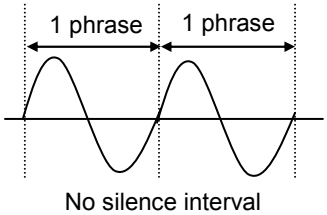
Product name	ROM capacity	Maximum vocal reproduction time (sec)		
		F_S = 4.0 kHz	F_S = 8.0 kHz	F_S = 16 kHz
ML22825-XXX/ML22865	16 Mbits	1,044	522	261
ML22824-XXX/ML22864	8 Mbits	520	260	130
ML22823-XXX/ML22863	4 Mbits	258	129	64

- Voice synthesis method: 4-bit ADPCM2
  8-bit Nonlinear PCM
  8-bit PCM , 16-bit PCM
  Can be specified for each phrase.
- Sampling frequency(Fs): 4.0 / 5.3 / 6.4 / 8.0 / 10.6 / 12.0 / 12.8 / 16.0 / 21.3 / 24.0 / 25.6 / 32.0 / 48.0 kHz
  f_s can be specified for each phrase.
- Built-in low-pass filter and 16-bit DA converter
- Speaker driving amplifier: 0.7 W (when 8Ω , DV_{DD}=5 V, Ta=25°C)
  2ch analog input (internal: 1ch; external: 1ch)
- CPU command interface: 3-wired serial clock-synchronized (ML2282X)
  I2C interface (ML2286X)
- Maximum number of phrases: 4,096 phrases from 000h to 3FFh (1024 phrases/bank)
- Memory bank switching: Enabled between bank 1 and bank 4 using the SEL0 and SEL1 pins
- Volume control: 32 levels (OFF is included) can be set by CVOL command.
  50 levels (OFF is included) can be set by AVOL command
- Repeat function: LOOP commands
- 2-channel mixing function: Available except case using 32kHz as sampling frequencys
- Source oscillation frequency: 4.096 MHz
- Power supply voltage: 2.7 to 3.6V / 4.5 to 5.5 V
- Operating temperature range: –40 to +85°C
- Package: 30-pin plastic SSOP (SSOP30-P-56-0.65-K-MC)
- Product name: ML22825-xxxMB, ML22824-xxxMB, ML22823-xxxMB
  ML22865-xxxMB, ML22864-xxxMB, ML22863-xxxMB
  (xxx: ROM code No.)

The following table shows the differences among the other speech synthesis LSIs.

Parameter	ML2216	ML22800 series	ML22825/ML22824/ ML22823-XXX	ML22865/ML22864/ ML22863-XXX
CPU interface	Serial	←	←	I2C
Playback method	4-bit ADPCM2 8-bit nonlinear PCM 8-bit straight PCM 16-bit straight PCM	←	←	←
Maximum number of phrases	256	1,024 (256/bank)	4,096 (1,024/bank)	←
Sampling frequency (kHz)	4.0/5.3/6.4/ 8.0/10.6/12.8 16.0	←	4.0/5.3/6.4/8.0/ 10.6/12.0/12.8/ 16.0/21.3/24.0/ 25.6/32.0/48.0	←
Clock frequency	4.096MHz (with a built-in crystal oscillator circuit)	←	←	←
DA converter	12 bits	12 bits	16 bits	←
Low-pass filter	3rd order comb filter	3rd order comb filter	FIR interpolation filter	←
Speaker driving amplifier	Built-in 0.3W (8Ω, DV_{DD} = 5 V)	No	Built-in 0.7W (8Ω, DV_{DD} = 5 V)	←
Edit ROM function	Yes	←	←	←
Simultaneous sound production function (mixing function)	No	←	2-channel	←
Volume control	16 levels	←	32 levels	←
Silence insertion	Yes 20 ms to 1024 ms (4 ms/step)	←	←	←
Repeat function	Yes	←	←	←
Interval at which a seam is silent during continuous playback (Note)	No	←	←	←
Memory bank switching	No	Yes	←	←
Power supply voltage	2.7 V to 5.5 V	2.7 V to 3.6 V	2.7 to 3.6V 4.5 to 5.5 V	2.7 to 3.6V 4.5 to 5.5 V
Package	44-pin QFP	30-pin SSOP	←	←

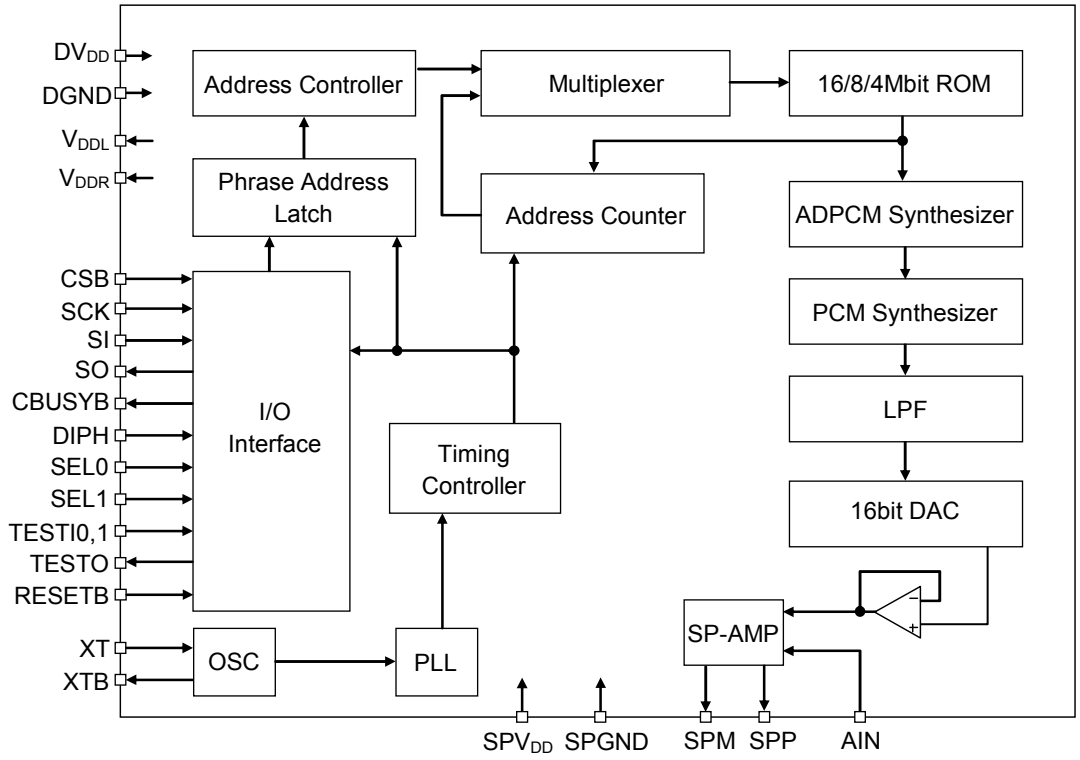
*1: Continuous playback as shown below is possible.



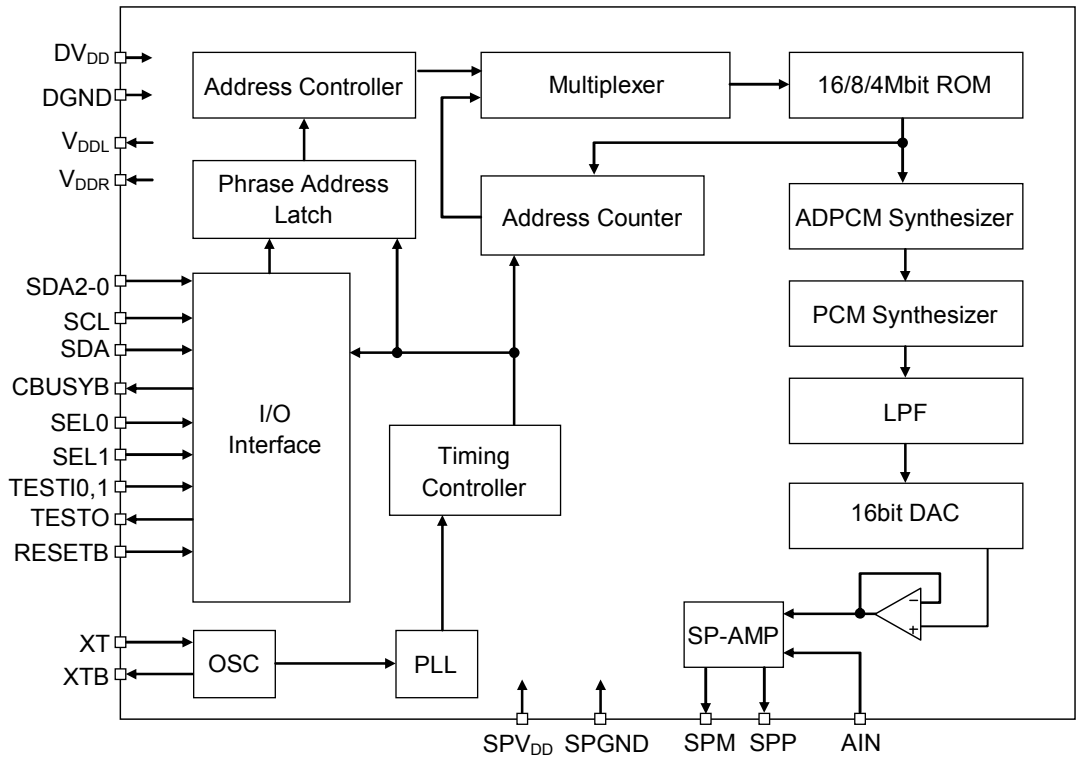
No silence interval

BLOCK DIAGRAMS

(ML22825/ML22824/ML22823-XXX : Synchronous serial interface)

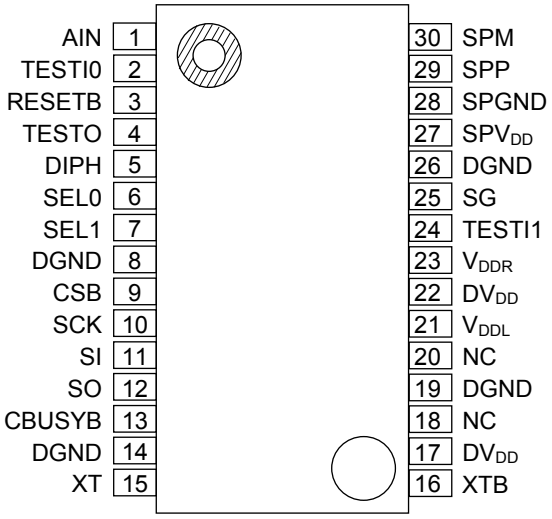


(ML22865/ML22864/ML22863-XXX : I2C interface)



PIN CONFIGURATIONS (TOP VIEW)

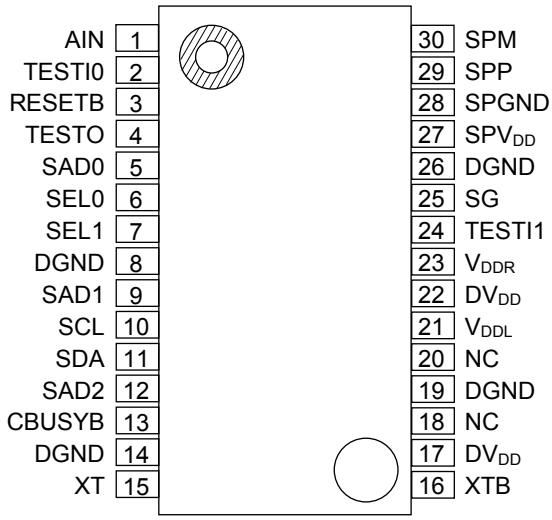
(ML22825/ML22824/ML22823-XXXMB : Synchronous serial interface)



NC: No Connection

30-Pin Plastic SSOP

(ML22865/ML22864/ML22863-XXXMB : I2C interface)



NC: No Connection

30-Pin Plastic SSOP

PIN DESCRIPTION (COMMON TO ALL PRODUCTS)

Pin	Symbol	I/O	Initial value (*1)	Description
1	AIN	I	0	Input pin for speaker amplifier.
2	TESTI0	I	0	Input pin for testing. Fix this pin to “L” level (DGND level). This pin has a pull-down resistor built in.
3	RESETB	I	0 (*2)	Input pin for reset. At the “L” level, the LSI enters initial state. During reset, the entire circuitry stops and enters power down state. Input “L” level when power is supplied. After the power supply voltage is stable, drive this pin to “H” level. Then the entire circuitry can be powered up. This pin has a pull-up resistor built in.
4	TESTO	O	Hi-Z	Output pins for testing. Leave these pins open.
6, 7	SEL0 SEL1	I	0	Memory bank switching pins. Fix these pins to “L” level when the memory bank function is not used.
8, 14, 19, 26	DGND	—	—	Digital ground pin. Also serves as a ground pin for the internal memory.
13	CBUSYB	O	1	Output pin for command processing status. This pin outputs “L” level during command processing. Any command should be entered when this pin is “H” level.
15	XT	I	0	Connect to the crystal or ceramic resonator. A feedback resistor around 1 MΩ is built in between this pin and the XTB pin. Use this pin if need to use an external clock. If the resonator is used, connect it as close to this pin as possible.
16	XTB	O	1	Connect to the crystal or ceramic resonator. When to use an external clock, leave this pin open. If the resonator is used, connect it as close to this pin as possible.
17, 22	DV_{DD}	—	—	Power supply pins for logic circuitry. Connect a capacitor of 0.1μF or more between these pins and DGND pins.
18, 20	N.C	—	—	Non connected pins. Leave these pins open.
21	V_{DDL}	—	0	Regulator output pin for internal logic circuitry. Connect a capacitor recommended between this pin and DGND pin.
23	V_{DDR}	—	0	Regulator output pin for Built-in ROM. Connect a capacitor recommended between this pin and DGND pin.
24	TESTI1	—	0	Test pin. Fix this pin to a DGND level.
25	SG	—	0	Reference voltage output pin for the speaker amplifier built-in. Connect a capacitor recommended between this pin and DGND pin.
27	SPV_{DD}	—	—	Power supply pin for the speaker amplifier. Connect a bypass capacitor of 0.1μF or more between this pin and SPGND pin.
28	SPGND	—	—	Ground pin for the speaker amplifier.
29	SPP	O	0	Positive(+) output pin of the speaker amplifier built-in. Serves as the LINE output (*3), if built-in speaker amplifier is not used.
30	SPM	O	Hi-Z	Negative(-) output pin of the speaker amplifier built-in.

*1: Indicates the initial value during reset input or power down.
*2: “H” during power down.
*3: Outputs a voice signal before amplified by the speaker amplifier built-in.

PIN DESCRIPTION (FOR ML2282X SYNCHRONOUS SERIAL INTERFACE)

Pin	Symbol	I/O	Initial value (*1)	Description
5	DIPH	I	0	Set pin of the SCK clock edge. When this pin is “L” level, rising edge is available for input(SI) and falling edge is available for output(SO). When this pin is “H” level, falling edge is available for input(SI) and rising edge is available for output(SO).
9	CSB	I	1	Chip select pin. At the “L” level, data input/output is available.
10	SCK	I	0	Synchronous clock input pin for serial interface.
11	SI	I	0	Input pin of synchronous serial data. When the DIPH pin is “L” level, data is shifted in at the rising edges of the SCK clock pulses. When the DIPH pin is “H” level, data is shifted in at the falling edges of the SCK clock pulses.
12	SO	O	Hi-Z	Output pin of synchronous serial data. When the DIPH pin is “L” level, data is output at the falling edges of the SCK clock pulses. When the DIPH pin is “H” level, data is output at the rising edges of the SCK clock pulses. When the CSB pin is “H” level, this pin is Hi-Z state.

*1: Indicate the initial value during reset or power down.

PIN DESCRIPTION (FOR ML2286X I2C INTERFACE)

Pin	Symbol	I/O	Initial value (*1)	Description
5, 9, 12	SAD0 SAD1 SAD2	I	0	Set pin of the slave address.
10	SCL	I	1	Clock input pin for I2C serial interface. This pin should be connected to pull-up resistor.
11	SDA	IO	1	Input/output pin for I2C serial data. Use for setting the mode of write/read and writing address, writing data or reading data. This pin should be connected to pull-up resistor. (N-ch MOS) open drain, when output mode. High impedance(Hi-Z), when input mode.

*1: Indicate the initial value during reset or power down.

ABSOLUTE MAXIMUM RATINGS

(DGND = SPGND = 0 V, Ta = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	DV_{DD}, SPV_{DD}	—	−0.3 to +7.0	V
Input voltage	V_{IN}	—	−0.3 to DV_{DD}+0.3	V
Power dissipation	P_D		938	mW
Output short-circuit current	I_{OS}	Applies to all pins except SPM, SPP, V_{DDL}, and V_{DDR}.	10	mA
		Applies to SPM and SPP pins.	300	mA
		Applies to V_{DDL} and V_{DDR} pins.	50	mA
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = SPGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	DV_{DD}, SPV_{DD}	—	2.7 to 3.6 4.5 to 5.5			V
Operating temperature	T_{OP}	—	−40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
External capacitors for crystal oscillator	Cd, Cg	—	15	30	45	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics (for the 3V applications)

DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86×DV_{DD}	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	0.14×DV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = –1 mA	DV_{DD}–0.4	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	I_{OH} = –50 µA	DV_{DD}–0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	I_{OL} = 50 µA	—	—	0.4	V
"L" output voltage 3 (*2)	V_{OL3}	I_{OL} = 3 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*3)	I_{IH2}	V_{IH} = DV_{DD}	0.3	2.0	15	µA
"H" input current 3 (*4)	I_{IH3}	V_{IH} = DV_{DD}	2	30	200	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (*3)	I_{IL2}	V_{IL} = GND	–15	–2.0	–0.3	µA
"L" input current 3 (*5)	I_{IL3}	V_{IL} = GND	–200	–30	–2	µA
"H" output leak current 3 (*6)	I_{ILOH}	V_{OH} = DV_{DD}	—	—	10	µA
"L" output leak current 3 (*6)	I_{ILOL}	V_{OL} = GND	–10	—	—	µA
Supply current during playback	I_{DD}	f_{OSC} = 4.096 MHz No output load	—	—	20	mA
Power-down supply current	I_{DDS}	Ta = –40 to +40°C	—	1	10	µA
		Ta = –40 to +85°C	—	1	20	µA

*1: Applies to the XTB pin.
*2: Applies to the SCL, SDA pin.
*3: Applies to the XT pin.
*4: Applies to the TESTI0 pin.
*5: Applies to the RESETB pin.
*6: Applies to the TESTO pin.

DC Characteristics (for the 5V applications)

DV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8×DV_{DD}	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	0.2×DV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = –1 mA	DV_{DD}–0.4	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	I_{OH} = –50µA	DV_{DD}–0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	I_{OL} = 50 µA	—	—	0.4	V
"L" output voltage 3 (*2)	V_{OL3}	I_{OL} = 3 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*3)	I_{IH2}	V_{IH} = DV_{DD}	0.8	5.0	20	µA
"H" input current 3 (*4)	I_{IH3}	V_{IH} = DV_{DD}	20	100	400	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (*3)	I_{IL2}	V_{IL} = GND	–20	–5.0	–0.8	µA
"L" input current 3 (*5)	I_{IL3}	V_{IL} = GND	–400	–100	–20	µA
"L" output leak current 2 (*6)	I_{ILOH}	V_{OH} = DV_{DD}	—	—	10	µA
"L" output leak current 3 (*6)	I_{ILOL}	V_{OL} = GND	–10	—	—	µA
Supply current during playback	I_{DD}	f_{OSC} = 4.096 MHz No output load	—	—	25	mA
Power-down supply current	I_{DDS}	Ta = –20 to +40°C	—	1	15	µA
		Ta = –20 to +85°C	—	1	30	µA

*1: Applies to the XTB pin.
*2: Applies to the SCL and SDA pins.
*3: Applies to the XT pin.
*4: Applies to the TESTI0 pin.
*5: Applies to the RESETB pin.
*6: Applies to the TESTO pin.

Characteristics of Analog Circuitry (for the 3V applications)

DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	kΩ
AIN input voltage range	V_{AIN}		—	—	DV_{DD}×2/3	Vp-p
LINE output load resistance	R_{LA}	During 1/2 DV_{DD} output	10	—	—	kΩ
LINE output voltage range	V_{AO}	No output load	DV_{DD}/6	—	DV_{DD}×5/6	V
SG output voltage	V_{SG}	—	0.95×V_{DDL}/2	V_{DDL}/2	1.05×V_{DDL}/2	V
SG output resistance	R_{SG}	During power down	57	96	135	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	SPV_{DD} = 3.3V, f = 1kHz R_{SPO} = 8Ω, THD≥10%	100	300	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

Characteristics of Analog Circuitry (for the 5V applications)

DV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	kΩ
AIN input voltage range	V_{AIN}		—	—	DV_{DD}×2/3	Vp-p
LINE output load resistance	R_{LA}	During 1/2 DV_{DD} output	10	—	—	kΩ
LINE output voltage range	V_{AO}	No output load	DV_{DD}/6	—	DV_{DD}×5/6	V
SG output voltage	V_{SG}	—	0.95×V_{DDL}/2	V_{DDL}/2	1.05×V_{DDL}/2	V
SG output resistance	R_{SG}	During power down	57	96	135	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	SPV_{DD} = 5.0V, f = 1kHz R_{SPO} = 8Ω, THD≥10% Ta=25°C	500	700	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

AC Characteristics (Common to All Products)

DV_{DD} = SPV_{DD} = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C,

Parameter	Applicable command	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle		f_{duty}	—	40	50	60	%
RESETB input pulse width		t_{RST}	—	100	—	—	μs
Reset noise rejection pulse width		t_{NRST}	—	—	—	0.1	μs
Command input interval time	STOP, SLOOP, CLOOP, CVOL, AVOL	t_{INT}	f_{OSC} = 4.096 MHz	2	—	—	ms
	PUP	t_{INTP}		10	—	—	ms
	RDSTAT (After status read)	t_{INTRD}		500	—	—	μs
Command input enable time	SLOOP Continuous play by PLAY/MUON	t_{cm}	f_{OSC} = 4.096 MHz	—	—	10	ms
CBUSYB “L” level output time	PUP	t_{PUP1}	f_{OSC} = 4.096 MHz	2.0	2.5	3.0	ms
	PDWN	t_{PD1}	f_{OSC} = 4.096 MHz	—	—	20	μs
	2nd byte of AMODE (POP = “0” DAEN or SPEN = “0” →”1”)	t_{POPA1}	f_{OSC} = 4.096 MHz	58	60	62	ms
	2nd byte of AMODE (POP = “1” DAEN = “0” →”1” SPEN = “0”)	t_{POPA2}	f_{OSC} = 4.096 MHz	90	93	95	ms
	2nd byte of AMODE (POP = “0” DAEN or SPEN = “1” →”0”)	t_{PDA1}	f_{OSC} = 4.096 MHz	108	110	112	ms
	2nd byte of AMODE (POP = “1” DAEN = “1” →”0” SPEN = “0”))	t_{PDA2}	f_{OSC} = 4.096 MHz	140	142	144	ms
	(*1)	t_{CB1}	f_{OSC} = 4.096 MHz	—	—	2	ms

Note: Output pin load capacitance = 45 pF

*1: Applies to cases where a command is input except after a PUP, PDWN, or 2nd byte of AMODE command input.

AC Characteristics of Synchronous Serial Command Interface (Applied to ML2282X)

DV_{DD} = SPV_{DD} = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Applicable command	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input enable time from CSB fall edge		t_{ESCK}	—	100	—	—	ns
SCK hold time from CSB rise edge		t_{CSH}	—	100	—	—	ns
Data floating time from CSB rise edge		t_{DOZ}	R_L = 3 kΩ	—	—	100	ns
Data setup time from SCK rise edge		t_{DIS1}	DIPH = “0”	50	—	—	ns
Data hold time from SCK rise edge		t_{DIH1}	DIPH = “0”	50	—	—	ns
Data output delay time from SCK rise edge		t_{DOD1}	R_L = 3 kΩ	—	—	80	ns
Data setup time from SCK fall edge		t_{DIS2}	DIPH = “1”	50	—	—	ns
Data hold time from SCK fall edge		t_{DIH2}	DIPH = “1”	50	—	—	ns
Data output delay time from SCK rise edge		t_{DOD2}	R_L = 3 kΩ	—	—	80	ns
SCK “H” level pulse width		t_{SCKH}	—	100	—	—	ns
SCK “L” level pulse width		t_{SCKL}	—	100	—	—	ns
CBUSYB output delay time from SCK rise edge		t_{DBSY1}	DIPH = “0”	—	—	150	ns
CBUSYB output delay time from SCK fall edge		t_{DBSY2}	DIPH = “1”	—	—	150	ns

Note: Output pin load capacitance = 45 pF

AC Characteristics of I2C Command Interface (Applied to ML2286X)

DV_{DD} = SPV_{DD} = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	(High-speed mode)		Unit
		Min.	Max.	
SCL clock frequence	t_{SCL}	0	400	kHz
Hold time (repeated) START condition After this period, the first clock pulse is generated.	$t_{HD;STA}$	0.6	—	μs
SCL “L” level pulse width	t_{LOW}	1.3	—	μs
SCL “H” level pulse width	t_{HIGH}	0.6	—	μs
Setup time for repeated START condition	$t_{SU;STA}$	0.6	—	μs
Data hold time: For I2C bus devices	$t_{HD;DAT}$	0	0.9	μs
Data setup time	$t_{SU;DAT}$	100	—	ns
SDA and SCL signal rise time	t_r	20	300	ns
SDA and SCL signal fall time	t_f	20	300	ns
STOP condition setup time	$t_{SU;STO}$	0.6	—	μs
Bus free time between STOP condition and START condition	t_{BUF}	1.3	—	μs
Capacitive load for each bus line	C_b	—	400	PF
Noise margin at a “L” level in each device connected (including hysteresis)	V_{nL}	0.1× DV_{DD}	—	V
Noise margin at a “H” level in each device connected (including hysteresis)	V_{nH}	0.1× DV_{DD}	—	V
Pulse width of spikes which must be suppressed by the input filter	t_{sp}	0	50	ns

Note: Output pin load capacitance = 45 pF

FUNCTIONAL DESCRIPTION

Synchronous Serial Command Interface

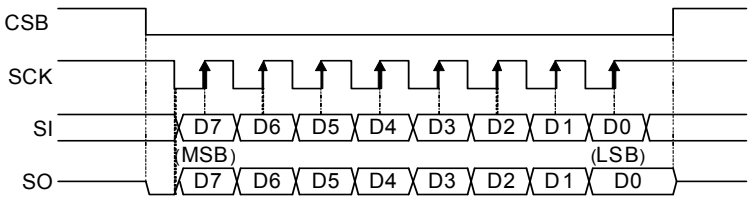
The CSB, SCK, SI, and SO pins are used to input the command data or to read the status. Driving the CSB pin to "L" level enables the serial CPU interface.
After the CSB pin is driven to "L" level, the command data are input through the SI pin from the MSB synchronized with the SCK clock. The command data shifts in through the SI pin at the rising or falling edge of the SCK clock pulse. Then, a command is executed at the rising or falling edge of the eighth pulse of the SCK clock.
As for status reading, status is output from the SO pin, synchronized with the SCK clock after the CSB pin is driven to "L" level.
The SCK clock edge is specified by the input level of the DIPH pin.

- When the DIPH pin is "L" level, rising edge is available for input from SI pin and falling edge is available for output from SO pin.
- When the DIPH pin is "H" level, falling edge is available for input from SI pin and rising edge is available for output from SO pin.

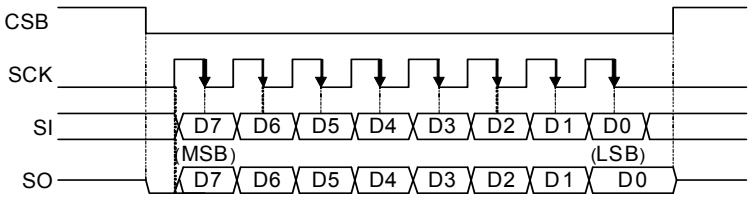
It is possible to input command data, even if the CSB pin is fixed by "L" level. However, if unexpected pulses caused by noise are induced through the SCK pin, SCK clock pulses are incorrectly counted, causing a failure in normal recognition of command. Then it is recommended that the CSB pin is "L" level only for command input.
The count of the SCK clock pulse is initialized when the CSB pin goes to "H" level.

Command Data Input or Status Read Timing

• When DIPH pin is "L" level



• When DIPH pin is "H" level



The following table shows the contents of each data output at a status read.

	Output status signal
MSB	—
7SB	—
6SB	Channel 2 BUSYB output (BUSYB1)
5SB	Channel 1 BUSYB output (BUSYB0)
4SB	—
3SB	—
2SB	Channel 2 NCR output (NCR1)
LSB	Channel 1 NCR output (NCR0)

The BUSYB output is “L” level when a command is being processed or the playback of a particular channel is going on. In other states, the BUSYB output is “H” level. The NCR output is “L” level when a command is being processed or particular channel is in standby for playback. In other states, the NCR output is “H” level.

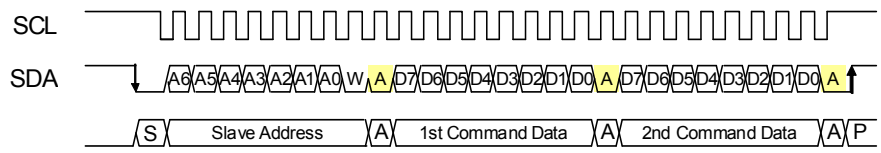
I2C Command Interface (Applies to ML2286X)

The I2C Interface built-in is an serial interface (: slave side) that is compliant with I2C bus specification. It supports Fast mode and enables data transmission/reception at 400 kbps. The SCL and SDA pins are used to input the command data or to read the status. Pins (:SAD0, 1 and 2) are used to set the slave address.
Pull-up resister should be connected to SCL pin and SDA pin.
For the master on the I2C bus to communicate with this device (: slave), input the slave address with the first seven bits after setting the start condition. The upper three bits of the slave address can be set using the SAD0 to 2 pins. The eighth bit of slave address is used to set the direction (: write or read) of communication. If the eighth bit is "0" level, it is write mode from master to slave. And, if the eighth bit is "1" level, it is read mode from master.
The communication is made in the unit of byte. And acknowledge is needed for each byte.

The protocol of I2C communication is shown below.

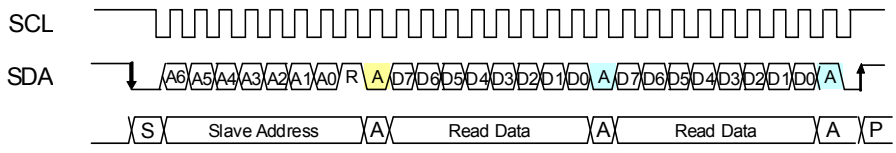
– Command flow at data write
  START condition
  Slave address +W (0)
  Write address (ex. 1st byte of a command)
  Write data (ex. 2nd byte of a command)
  STOP condition

• Data write timing



– Command flow at data read
  Start condition
  Slave address +R(1)
  Read data (ex. Status read)
  STOP condition

• Data read timing



Setting of the slave address using the SAD0 to 2 pins

SAD2	SAD1	SAD0	Lower 4 bits
0	0	0	0101
0	0	1	0101
0	1	0	0101
0	1	1	0101
1	0	0	0101
1	0	1	0101
1	1	0	0101
1	1	1	0101

The following table shows the contents of each data output at a status read. Status is updated by the RDSTAT command; therefore, be sure to input the RDSTAT command in order to read status.

	Output status signal
MSB	
7SB	
6SB	Channel 2 BUSYB output (BUSYB1)
5SB	Channel 1 BUSYB output (BUSYB0)
4SB	
3SB	
2SB	Channel 2 NCR output (NCR1)
LSB	Channel 1 NCR output (NCR0)

The BUSYB signal is “L” level when either a command is being processed or the playback of a particular channel is going on. In other states, the BUSYB signal is “H” level.
The NCR signal is “L” level when either a command is being processed or a particular channel is in standby for playback. In other states, the NCR signal is “H” level.

Command List

Each command is configured by the unit of byte (8-bit). The following commands, AMODE, AVOL FADR, PLAY, MUON, and CVOL, use two bytes.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP	0	0	0	0	0	0	S1	S0	Power-up command. Shifts from the power down state to the command waiting state. Also, sets the number of memory banks.
PDWN	0	0	1	0	0	0	0	0	Power-down command. Shifts form the command waiting state to the power down state.
RDSTAT	1	0	1	1	0	0	0	0	Status read command. Reads the command status on each channel.
AMODE	0	0	0	0	0	1	0	0	Control command of analog circuitry. Setoperation of power-up/dpwn and input/output.
	FAD	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	POP	
PLAY	0	1	0	0	F9	F8	0	CH	Playback start command. Use the data of the 2nd byte to specify a phrase number. Can be specified for each channel.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	0	0	CH1	CH0	Playback stop command. Can be set for each channel.
FADR	0	0	1	1	F9	F8	0	CH	Set command of playback phrase. Can be set for each channel. Use START command to start.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	0	0	CH1	CH0	Playback start command without phrase spec. Use FADR command to set phrase.Can start playback on multiple channels simultaneously. After played back by PLAY command, the same phrase can be played back with this command.
MUON	0	1	1	1	0	0	CH1	CH0	Silence insertion command. Set the silent time length for each channel using M7 to M0 bits in the 2nd byte.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	0	0	CH1	CH0	Set command of repeat playback. Setting is enabled during playback. Can be specified for each channel.
CLOOP	1	0	0	1	0	0	CH1	CH0	Stop command of repeat playback. Can be specified for each channel. Also, repeat playback is released by STOP command automatically.
CVOL	1	0	1	0	0	0	CH1	CH0	Volume control command. Set volume for each channel using CV4 to CV0 bits in the 2nd byte.
	0	0	0	CV4	CV3	CV2	CV1	CV0	
AVOL	0	0	0	0	1	0	0	0	Analog volume control command. Set volume after channel mixing using AV5 to AV0 bits.
	0	0	AV5	AV4	AV3	AV2	AV1	AV0	

Voice Synthesis Algorithm

Four types of voice synthesis algorithm are supported. They are 4-bit ADPCM2, 8-bit non-linear PCM, 8-bit straight PCM and 16-bit straight PCM. Select the best one according to the characteristics of playback voice.

The following table shows key features of each algorithm.

Voice synthesis algorithm	Applied waveform	Feature
4-bit ADPCM2	Normal voice waveform	Up version of LAPIS Semiconductor's specific voice synthesis algorithm (: 4-bit ADPCM). Voice quality is improved.
8-bit Nonlinear PCM	Waveform including high frequency signals (sound effect, etc.)	Algorithm, which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit straight PCM		Normal 8-bit PCM algorithm
16-bit straight PCM		Normal 16-bit PCM algorithm

Memory Allocation and Creating Voice Data

The ROM is partitioned into four data areas: voice (i.e., phrase) control area, test area, voice area, and edit ROM area.
The voice control area manages the voice data in the ROM. It contains data for controlling the start/stop addresses of voice data for 1,024 phrases, use/non-use of the edit ROM function and so on.
The test area contains data for testing.
The voice area contains actual waveform data.
The edit ROM area contains data for effective use of voice data. For the details, refer to the section of "Edit ROM Function."
The edit ROM area is not available if the edit ROM is not used.

The ROM data is created using a dedicated tool.

Configuration of ROM data

0x00000 0x01FFF	Voice control area (Fixed 64 Kbits)
0x02000 0x0205F	Test area
0x02060 max: 0x1FFFFF	Voice area
max: 0x1FFFFF	Edit ROM area Depends on creation of ROM data.

Playback Time and Memory Capacity

The playback time depends on the memory capacity, sampling frequency, and playback method.
The equation to know the playback time is shown below. But this is not applied if the edit ROM function is used.

$$\text{Playback time [sec]} = \frac{1.024 \times (\text{Memory capacity} - 64.75\ [\text{Kbits}])}{\text{Sampling frequency [kHz]} \times \text{Bit length}}$$

(Bit length is 4 at the 4-bit ADPCM2 and 8/16 at the PCM.)

Example) In the case that the sampling frequency is 16 kHz, algorithm is 4-bit ADPCM2 and ROM capacity is 16 Mbits, the playback time is approx. 261 seconds, as shown below.

$$\text{Playback time} = \frac{1.024 \times (16834 - 64.75)\ [\text{Kbits}]}{16\ [\text{kHz}] \times 4\ [\text{bits}]} \cong 261\ [\text{sec}]$$

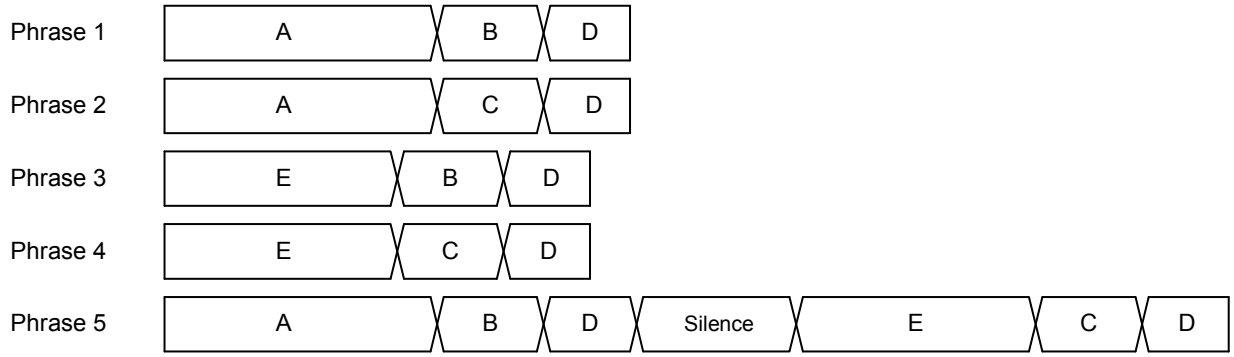
Edit ROM Function

The edit ROM function makes it possible to play back multiple phrases in succession. The following functions are set using the edit ROM function:

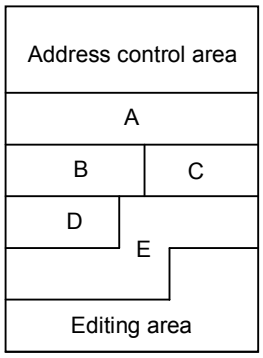
- Continuous playback: There is no limit to set the number of times of continuous playback. It depends on the memory capacity only.
- Silence insertion function: 20ms to 1,024 ms

It is possible to use voice ROM effectively to use the edit ROM function.
Below is an example of the ROM structure, case of using the edit ROM function.

Example 1) Phrases using the Edit ROM Function



Example 2) Structure of the ROM that contents of Example 1 are stored



Mixing Function

It is possible to perform mixing of two channels simultaneously. And also, it is possible to specify PLAY, STOP, and CVOL commands for each channel respectively. The mixing function is available if the sampling frequency (F_S) is 32 kHz or less.

- Precautions for Waveform Clamp
Adjust the volume of each channel using the CVOL command, if the waveform clamp is increased by channel mixing.

Memory Bank Switching Function

The memory bank switching function enables the the built-in ROM area that is divivided into up to four banks to be used. When four banks are used, the maximum number of phrases per bank is 1,024 so that up to 4096 phrases can be played back.
Using this function, multiple ROM codes can be grouped into one code.
The settings of SEL1 pin and SEL0 pin determines which memory bank is used. To playback phrases, the number of memory banks must be specified in PUP.

When using a memory bank switching function, data must be divided and saved in the specified areas at ROM data creation.

– When the number of memory banks is 1

SEL1	SEL0	ML22825 ML22865	ML22824 ML22864	ML22823 ML22863
0	0	00000h – 1FFFFFh	00000h – FFFFFh	00000h -7FFFFh

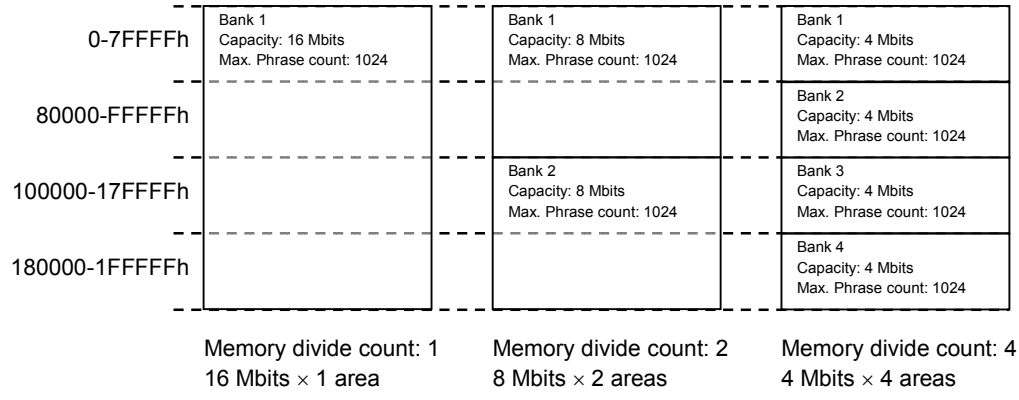
– When the number of memory banks is 2

SEL1	SEL0	ML22825 ML22865	ML22824 ML22864	ML22823 ML22863
0	0	00000h – FFFFFh	00000h – 7FFFFh	00000h – 3FFFFh
0	1	100000h – 1FFFFFh	80000h – FFFFFh	40000h – 7FFFFh

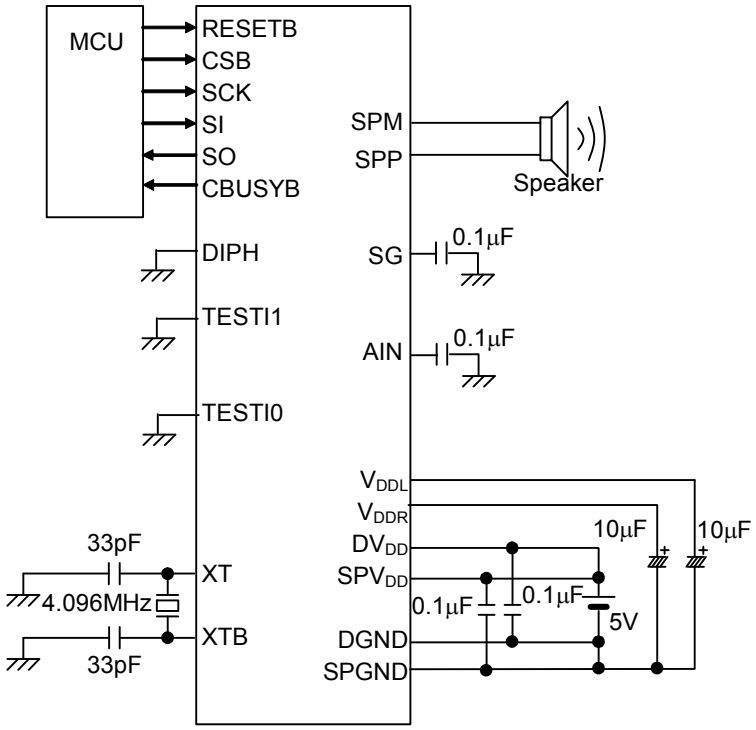
– When the number of memory banks is 4

SEL1	SEL0	ML22825 ML22865	ML22824 ML22864	ML22823 ML22863
0	0	00000h – 7FFFFh	00000h – 3FFFFh	00000h – 1FFFFh
0	1	80000h – FFFFFh	40000h – 7FFFFh	20000h – 3FFFFh
1	0	100000h – 17FFFFh	80000h – BFFFFh	40000h – 5FFFFh
1	1	180000h – 1FFFFFh	C0000h – FFFFFh	60000h – 7FFFFh

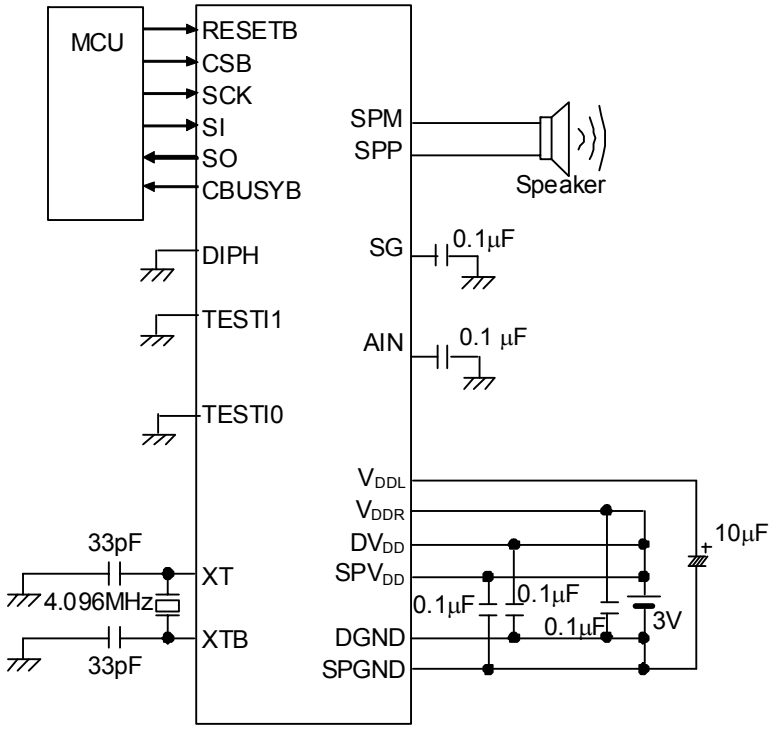
The memory (16 Mbits) in the ML22825 is divided as shown below.



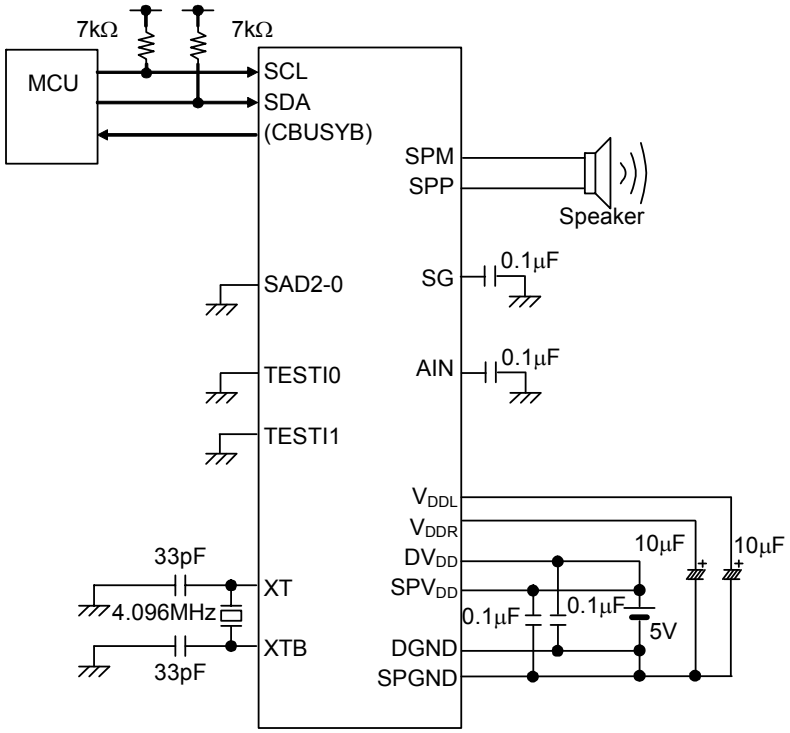
APPLICATION CIRCUIT (ML2282X: DV_{DD} = SPV_{DD} = 5V)



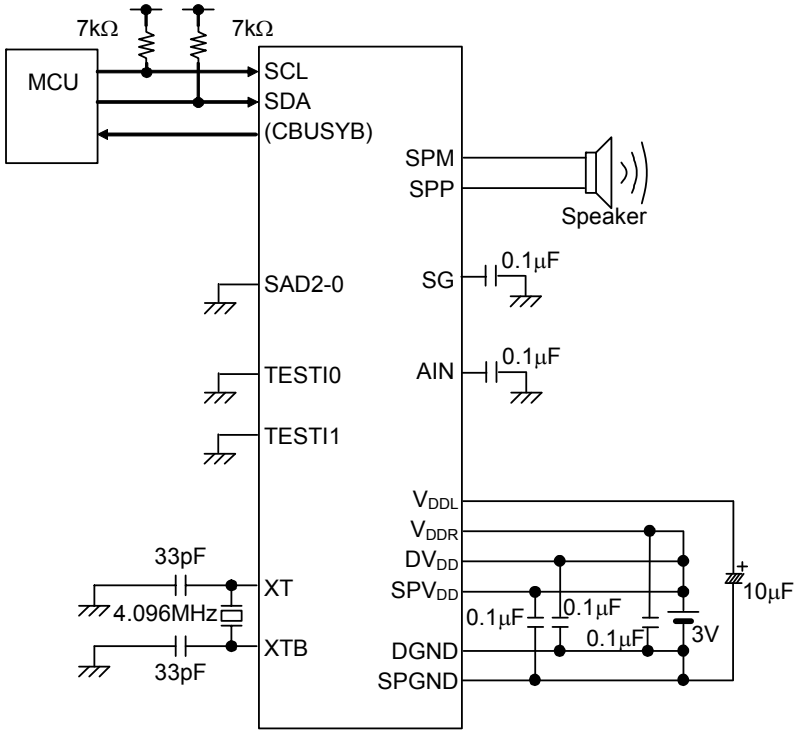
APPLICATION CIRCUIT (ML2282X: DV_{DD} = SPV_{DD} = 3V)



APPLICATION CIRCUIT (ML2286X: DV_{DD}=SPV_{DD}=5V)



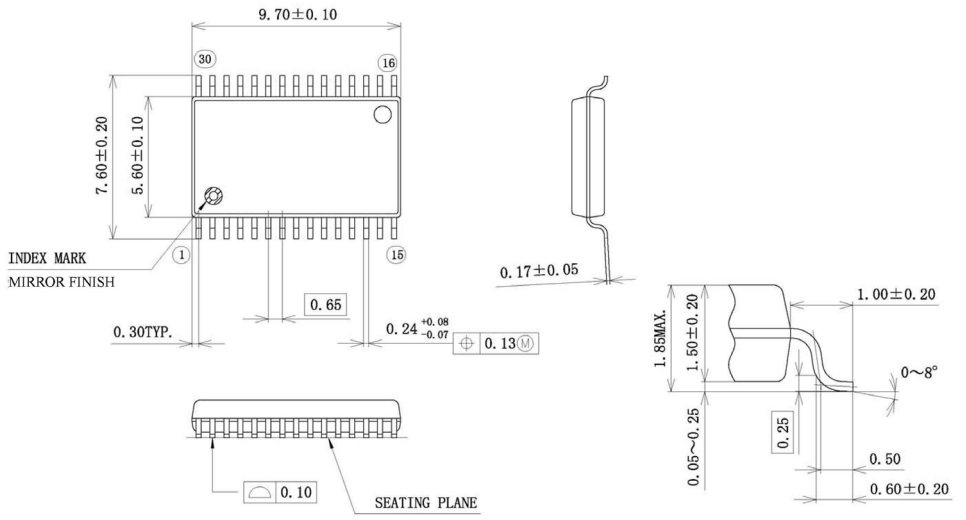
APPLICATION CIRCUIT (ML2286X: DV_{DD}=SPV_{DD}=3V)



PACKAGE DIMENSIONS

(Unit: mm)

SSOP30-P-56-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	1/Aug. 15, 2007

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL2282XFULL-01	Dec. 17, 2007	–	–	Preliminary edition 1
FEDL228XXFULL-01	Apr. 18, 2008	–	–	Final edition 1
FEDL228XXFULL-02	May. 29, 2008	–	–	Final edition 2
FEDL228XXFULL-03	Mar. 24, 2009	1	1	2-channel mixing function 48kHz-> 32kHz
		2	2	Power supply voltage 2.7 to 5.5V -> 2.7 to 3.6V / 4.5 to 5.5 V
		10	10	LINE output voltage range MAX. DVDD x 4/6 -> DVDD x 5/6
		10	10	SG output resistance Min 52 -> Min 57
		10	10	AIN input voltage range(for the 5V app..) Max. DVDD x 2/4 -> DVDD x 2/3
		15	15	PUP(AMODE) -> POP(AMODE)
		17	17	Correct ROM address and calculation
		20,21	20,21	Modify application circuit

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