

## MD56V62169M-xxTA07AL

4-Bank×1,048,576-Word×16-Bit SYNCHRONOUS DYNAMIC RAM

### DESCRIPTION

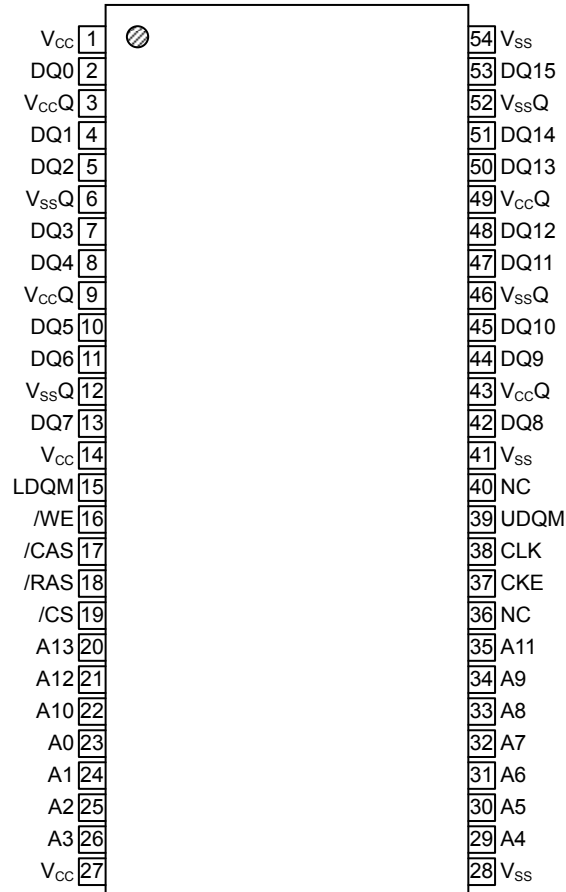
The MD56V62169M-xxTA07AL is a 4-Bank 1,048,576-word 16-bit Synchronous dynamic RAM fabricated in LAPIS Semiconductor's silicon-gate CMOS technology. The device operates at 3.3V. The inputs and outputs are LVTTTL compatible.

### FEATURES

Product Name	MD56V62169M-xxTA07AL xx indicates speed rank.
Organization	4Bank x 1,048,576Word x 16Bit
Address Size	4,096Row x 256Column
Power Supply VCC (Core)	3.3V±0.3V
Power Supply VCCQ (I/O)	3.3V±0.3V
Interface	LVTTTL compatible
Operating Frequency	Max. 166MHz (Speed Rank 6)
Operating Temperature	0 to +70°C
Functions	General-purpose SDRAM command interface
/CAS Latency	Mode register CL setting: 2, 3
Burst Length	Mode register BL setting: 1, 2, 4, 8, Full page
Burst Type	Mode register BT setting: Sequential, Interleave
Write Mode	Mode register WM setting: Burst, Single
Refresh	Auto-Refresh: 4,096cycle/64ms(0 to 70°C) Self-Refresh
Package	54 pin 400 mil Plastic TSOP(2) Cu Frame, Halogen-Free, Pb-Free (P-TSOP(2)54-P-400-0.80-ZK)

### PRODUCT FAMILY

VCC	Speed rank	Family	Max. Frequency	Access Time (Max.)	
				tAC2	tAC3
3.0V to 3.6V	-6	MD56V62169M-6TA07AL	166MHz	5.4ns	5.4ns
	-7	MD56V62169M-7TA07AL	143MHz	5.4ns	5.4ns
	-75	MD56V62169M-75TA07AL	133MHz	5.4ns	5.4ns
	-10	MD56V62169M-10TA07AL	100MHz	6ns	6ns

**PIN CONFIGURATION (TOP VIEW)**54-Pin Plastic TSOP(II)  
(K Type)

Pin Name	Function	Pin Name	Function
CLK	System Clock	UDQM, LDQM	Data Input / Output Mask
/CS	Chip Select	DQi	Data Input / Output
CKE	Clock Enable	VCC	Power Supply (3.3V)
A0 to A11	Address	VSS	Ground (0V)
A12,A13	Bank Select Address	VCCQ	Data Output Power Supply (3.3V)
/RAS	Row Address Strobe	VSSQ	Data Output Ground (0V)
/CAS	Column Address Strobe	NC	No Connection
/WE	Write Enable		

Note : The same power supply voltage must be provided to every VCC pin .

The same power supply voltage must be provided to every VCCQ pin.

The same GND voltage level must be provided to every VSS pin and VSSQ pin.

**PIN DESCRIPTION**

CLK	Clock (Input) Fetches all inputs at the "H" edge.
CKE	Clock Enable (Input) Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
/CS	Chip Select (Input) Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE and UDQM, LDQM.
/RAS	Row Address Strobe (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
/CAS	Column Address Strobe (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
/WE	Write Enable (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
A12,A13 (BA1,BA0)	Bank Address (Input) Selects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time.
A0 to A11	Row & column multiplexed. (Input) Row address : RA0 – RA11 Column Address : CA0 – CA7
DQ0 to DQ15	3-state Data Bus (Input/Output)
UDQM, LDQM	DQ Mask (Input) Masks the read data of two clocks later when DQM are set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM are set "H" at the "H" edge of the clock signal. UDQM controls DQ8 to DQ15, LDQM controls DQ0 to DQ7.
VCC, VSS	Power Supply (Core), Ground (Core) The same power supply voltage must be provided to every VCC pin. The same GND voltage level must be provided to every VSS pin.
VCCQ, VSSQ	Power Supply (I/O), Ground (I/O) The same power supply voltage must be provided to every VCCQ pin. The same GND voltage level must be provided to every VSSQ pin.
NC	No Connection

**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage on Input/Output Pin Relative to VSS	VIN, VOUT	-0.5 to VCC+0.5	V
VCC Supply Voltage	VCC	-0.5 to 4.6	V
VCCQ Supply Voltage	VCCQ	-0.5 to 4.6	V
Power Dissipation (Ta=25°C)	PD	1000	mW
Short Circuit Output Current	IOS	50	mA
Storage Temperature	Tstg	-55 to 150	°C
Operating Temperature	Topr	0 to +70	°C

- Notes:
1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
  2. Functional operation should be restricted to recommended operating condition.
  3. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.
  4. The voltages are referenced to VSS.

**Recommended Operating Conditions (1/2)**

Ta= 0 to +70°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage (Core)	VCC	3.0	3.3	3.6	V	1,2,3
Power Supply Voltage (I/O)	VCCQ	3.0	3.3	3.6	V	1,2,3
Ground	VSS, VSSQ	0	0	0	V	

- Notes:
1. The voltages are referenced to VSS
  2. Arrange a capacitor near the power supply terminal to prevent a change in high transitional power supply.
  3. Use the power supply which became stable voltage regulations.

**Recommended Operating Conditions (2/2)**

Ta= 0 to +70°C

Parameter	Symbol	Min.	Max.	Unit	Note
Input High Voltage	VIH	2.0	VCC + 0.3	V	1, 2
Input Low Voltage	VIL	-0.3	0.8	V	1, 3

- Notes:
1. The voltages are referenced to VSS.
  2. The input voltage is VCC + 0.5V when the pulse width is less than 20ns (the pulse width is with respect to the point at which VCC is applied).
  3. The input voltage is -0.5V when the pulse width is less than 20ns (the pulse width respect to the point at which VSS and VSSQ are applied).

**Pin Capacitance**

Ta = 25°C, VCC = VCCQ = 3.3V, f = 1MHz

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (CLK)	CCLK	—	4	pF
Input Capacitance (A0 to A13, /RAS, /CAS, /WE, /CS, CKE, UDQM, LDQM)	CIN	—	5	pF
Input/Output Capacitance (DQ0 to DQ15)	COUT	—	6.5	pF

**DC Characteristics (Input/Output)**Ta = 0 to +70°C  
VCC = VCCQ = 3.3V±0.3V

Parameter	Symbol	Condition	Min.	Max.	Unit
Output High Voltage	VOH	IOH = -0.2mA	2.4	—	V
Output Low Voltage	VOL	IOL = 0.2mA	—	0.4	V
Input Leakage Current	ILI	0V ≤ VIN ≤ VCCQ	-10	10	μA
Output Leakage Current	ILO	—	-10	10	μA

Note: The voltages are referenced to VSS.

**MD56V62169M-xxTA07AL****DC Characteristics (Power Supply Current)**

Ta = 0 to +70°C  
VCC = VCCQ = 3.3V±0.3V

Parameter	Symbol	Condition			MD56V62169M-xxTA07AL								Unit	Note
					-6		-7		-75		-10			
		Bank	CKE	Others	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Average Power Supply Current (Operating)	I <sub>CC1</sub>	One Bank Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = Min. t <sub>RC</sub> = Min. No Burst	—	120	—	100	—	90	—	70	mA	1, 2
Power Supply Current (Standby)	I <sub>CC2</sub>	All Banks Precharge	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = Min.	—	50	—	40	—	35	—	30	mA	3
Average Power Supply Current (Clock Suspension)	I <sub>CC3S</sub>	4 Banks Active	CKE ≤ V <sub>IL</sub>	t <sub>CC</sub> = Min.	—	4	—	4	—	4	—	4	mA	2
Average Power Supply Current (Active Standby)	I <sub>CC3</sub>	One Bank Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = Min.	—	50	—	45	—	40	—	35	mA	3
Power Supply Current (Burst)	I <sub>CC4</sub>	4 Banks Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = Min.	—	160	—	140	—	130	—	100	mA	1, 2
Power Supply Current (Auto-Refresh)	I <sub>CC5</sub>	4 Banks Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = Min. t <sub>RC</sub> = Min.	—	160	—	140	—	130	—	100	mA	2
Average Power Supply Current (Self-Refresh)	I <sub>CC6</sub>	All Banks Precharge	CKE ≤ V <sub>IL</sub>	t <sub>CC</sub> = Min.	—	3	—	3	—	3	—	3	mA	
Average Power Supply Current (Power Down)	I <sub>CC7</sub>	All Banks Precharge	CKE ≤ V <sub>IL</sub>	t <sub>CC</sub> = Min.	—	3	—	3	—	3	—	3	mA	

- Notes: 1. Measured with outputs open.  
 2. The address and data can be changed once or left unchanged during one cycle.  
 3. The address and data can be changed once or left unchanged during two cycles.

**MD56V62169M-xxTA07AL****AC Characteristics (1/2)**

Ta = 0 to +70°C  
VCC = VCCQ = 3.3V±0.3V

Note 1,2

Parameter		Symbol	MD56V62169M-xxTA07AL								Unit	Note
			-6		-7		-75		-10			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Clock Cycle Time	CL=3	t <sub>CC3</sub>	6	—	7	—	7.5	—	10	—	ns	
	CL=2	t <sub>CC2</sub>	10	—	10	—	10	—	10	—	ns	
Access Time from Clock	CL=3	t <sub>AC3</sub>	—	5.4	—	5.4	—	5.4	—	6	ns	3,4
	CL=2	t <sub>AC2</sub>	—	5.4	—	5.4	—	5.4	—	6	ns	3,4
Clock High Pulse Time		t <sub>CH</sub>	2	—	2	—	2.5	—	3	—	ns	4
Clock Low Pulse Time		t <sub>CL</sub>	2	—	2	—	2.5	—	3	—	ns	4
Input Setup Time		t <sub>SI</sub>	1.5	—	1.5	—	1.5	—	2	—	ns	
Input Hold Time		t <sub>HI</sub>	0.8	—	0.8	—	0.8	—	1	—	ns	
Output Low Impedance Time from Clock		t <sub>OLZ</sub>	2	—	2	—	2	—	2	—	ns	
Output High Impedance Time from Clock		t <sub>OHZ</sub>	—	5.4	—	5.4	—	5.4	—	6	ns	
Output Hold from Clock		t <sub>OH</sub>	2	—	2	—	2.5	—	2.5	—	ns	3
Random Read or Write Cycle Time		t <sub>RC</sub>	60	—	60	—	65	—	70	—	ns	
RAS Precharge Time		t <sub>RP</sub>	18	—	18	—	18	—	20	—	ns	
RAS Pulse Width		t <sub>RAS</sub>	42	10 <sup>5</sup>	42	10 <sup>5</sup>	45	10 <sup>5</sup>	50	10 <sup>5</sup>	ns	
/RAS to /CAS Delay Time		t <sub>RCD</sub>	18	—	18	—	18	—	20	—	ns	
Write Recovery Time		t <sub>WR</sub>	2	—	2	—	2	—	2	—	Cycle	
/RAS to /RAS Bank Active Delay Time		t <sub>RRD</sub>	10	—	10	—	15	—	20	—	ns	
Refresh Time		t <sub>REF</sub>	—	64	—	64	—	64	—	64	ms	5
Power-down Exit setup Time		t <sub>PDE</sub>	t <sub>SI</sub> <sup>+</sup> 1CLK	—	t <sub>SI</sub> <sup>+</sup> 1CLK	—	t <sub>SI</sub> <sup>+</sup> 1CLK	—	t <sub>SI</sub> <sup>+</sup> 1CLK	—	ns	
Refresh cycle Time		t <sub>RCA</sub>	60	—	60	—	65	—	70	—	ns	

**AC Characteristics (2/2)**

Ta = 0 to +70°C  
 VCC = VCCQ = 3.3V±0.3V

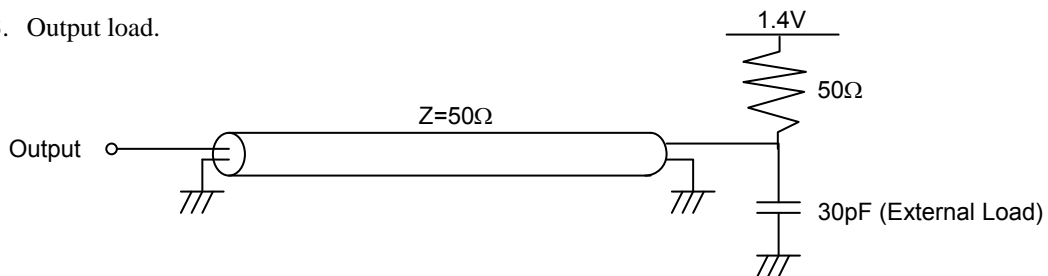
Note 1,2

Parameter	Symbol	MD56V62169M-xxTA07AL				Unit	Note
		-6	-7	-7.5	-10		
/CAS to /CAS Delay Time (Min.)	t <sub>CCD</sub>	1	1	1	1	Cycle	
Clock Disable Time from CKE	t <sub>CKE</sub>	1	1	1	1	Cycle	
Data Output High Impedance Time from UDQM, LDQM	t <sub>DOZ</sub>	2	2	2	2	Cycle	
Data Input Mask Time from UDQM, LDQM	t <sub>DOD</sub>	0	0	0	0	Cycle	
Data Input Mask Time from Write Command	t <sub>DWD</sub>	0	0	0	0	Cycle	
Data Output High Impedance Time from Precharge Command	t <sub>ROH</sub>	CL	CL	CL	CL	Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	t <sub>MRD</sub>	2	2	2	2	Cycle	
Write Command Input Time from Output	t <sub>OWD</sub>	2	2	2	2	Cycle	

- Notes: 1. AC measurements assume that t<sub>T</sub> = 1ns.,  
 2. Test condition

Parameter	Test Condition		Unit
Input voltage for AC measurement	2.4	0.4	V
Transition Time for AC measurement	t <sub>T</sub> = 1		ns
Reference level for timing of input signal (t <sub>T</sub> ≤ 1ns)	1.4		V
Reference level for timing of input signal (t <sub>T</sub> > 1ns)	V <sub>IH</sub> Min.	V <sub>IL</sub> Max.	V
Reference level for timing of output signal	1.4		V

3. Output load.



4. If t<sub>T</sub> is longer than 1ns, then the reference level for timing of input signals is V<sub>IH</sub> and V<sub>IL</sub>.  
 5. It is necessary to operate auto-refresh 4,096 cycles within t<sub>REF</sub>.

**POWER ON AND INITIALIZE****Power on Sequence**

- (1) Turn on the power after you make input a state of NOP, and input a system clock.
- (2) Take a pose of 200 $\mu$ s and more with making input a state of NOP after VCC and VCCQ reach it in the regular condition.
- (3) Issue the row precharge all bank command (PALL), and secure the row precharge time (tRP).
- (4) Issue the standard Mode Register Set command (MRS), and secure the mode register set command delay time (tMRD).
- (5) Issue 2 or more auto-refresh commands (REF), and secure the refresh cycle time (tRCA).

**Note:**

1. (4) or (5): in no special order.
2. Carry out an initialization sequence after each input terminal reaches a regulation voltage when other input terminals were the undefined setup input (High-Z) at the CKE= "H" time. And, the undefined setup input period of the CKE= "H" time can't hold data. It becomes more effective than writing data after the initialization sequence.

**Mode Register Set Command (MRS)**

The mode register stores the data for controlling the various operating modes. It programs the /CAS latency, burst type, burst length and write mode. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by mode register set command MRS. The state of address pins A0 to A11 and BA1(A12), BA0(A13) in the same cycle as MRS is the data written in the mode register. Refer to the table for specific codes for various /CAS latencies, burst type, burst length and write mode.

**MRS**

CLK	$\uparrow$ n-1	$\uparrow$ n
CKE	H	X
/CS	X (Idle)	L
/RAS		L
/CAS		L
/WE		L
BA1(A12)	X	0
BA0(A13)	X	0
A0 to A11	X	V

V: The value of mode register set

**Mode Register Field Table To Program Mode**

Write Burst Mode		/CAS Latency				Burst Type		Burst Length				
A9	WM	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	Burst	0	0	0	Reserved	0	Sequential	0	0	0	1	1
1	Single	0	0	1	Reserved	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	Reserved			1	0	0	Reserved	Reserved
		1	0	1	Reserved			1	0	1	Reserved	Reserved
		1	1	0	Reserved			1	1	0	Reserved	Reserved
		1	1	1	Reserved			1	1	1	Full Page	Reserved

- Notes:
1. It is intended for all family products.
  2. A12 and A13 should stay "0" during mode set cycle.
  3. A7, A8, A10 and A11 should stay "0" during mode set cycle.
  4. Don't set address keys of "Reserved".

**Burst Mode**

Burst operation is the operation to continuously increase a column address inputted during read or write command. The upper bits select a column address block,

		Access order in column address block					
		Start Address (Lower bit)			Burst Type		
					BT=Sequential		BT=Interleave
Burst Length	BL=2				A0		
					0	0, 1	0, 1
					1	1, 0	1, 0
	BL=4			A1	A0		
				0	0	0, 1, 2, 3	0, 1, 2, 3
				0	1	1, 2, 3, 0	1, 0, 3, 2
				1	0	2, 3, 0, 1	2, 3, 0, 1
				1	1	3, 0, 1, 2	3, 2, 1, 0
	BL=8	A2	A1	A0			
		0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6	
		0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5	
		0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4	
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2	
		1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1	
		1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0	
	BL=Full Page (256)	A0 to A7					
		0			0, 1... 255		
		Yn			Yn, Yn+1... 255, 0... ...Yn-1		
					Non Support		

**READ / WRITE OPERATION**

**Bank**

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The A12 and A13 input is latched at the time of assertion of /RAS and /CAS to select the bank to be used for operation. The bank address A12 and A13 is latched at bank active, read, write, mode register set and precharge operations.

Bank Address

A12	A13	Bank
0	0	A
0	1	B
1	0	C
1	1	D

**Activate**

The bank activate command is used to select a random row in an idle bank. By asserting low on /RAS and /CS with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of tRCD(Min.) from the time of bank activation.

ACT

CLK	$\overline{\uparrow}_{n-1}$	$\overline{\uparrow}_n$
CKE	H	X
/CS	X (Idle)	L
/RAS		L
/CAS		H
/WE		H
A12,A13	X	BA
A0 to A11	X	RA

BA: Bank Address

RA: Row Address (Page)

**Precharge**

The precharge operation is performed on an active bank by precharge command (PRE) with valid A12 and A13 of the bank to be precharged. The precharge command can be asserted anytime after tRAS(Min.) is satisfied from the bank active command in the desired bank. All bank can be precharged at the same time by using precharge all command (PALL). Asserting low on /CS, /RAS and /WE with high on A10

PRE

CLK	$\overline{\uparrow}_{n-1}$	$\overline{\uparrow}_n$
CKE	H	X
/CS	X (Page Open)	L
/RAS		L
/CAS		H
/WE		L
A12,A13	X	BA
A10	X	0
A0 to A9, A11	X	X

BA: Bank Address

PALL

CLK	$\overline{\uparrow}_{n-1}$	$\overline{\uparrow}_n$
CKE	H	X
/CS	X (Page Open)	L
/RAS		L
/CAS		H
/WE		L
A12,A13	X	X
A10	X	1
A0 to A9, A11	X	X

after all banks have satisfied tRAS(Min.) requirement, performs precharge on all banks. At the end of tRP after performing precharge to all banks, all banks are in idle state.

### Write / Write with Auto-Precharge

The write command is used to write data into the SDRAM on consecutive clock cycles in adjacent address depending on burst length and burst sequence. By asserting low on /CS, /CAS and /WE with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even through the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length.

**WRT**

CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	X
/CS	X (Page Open)	L
/RAS		H
/CAS		L
/WE		L
A12, A13	X	BA
A10	X	0
A8, A9, A11	X	X
A0 to A7	X	CA
DQ	X	D-in

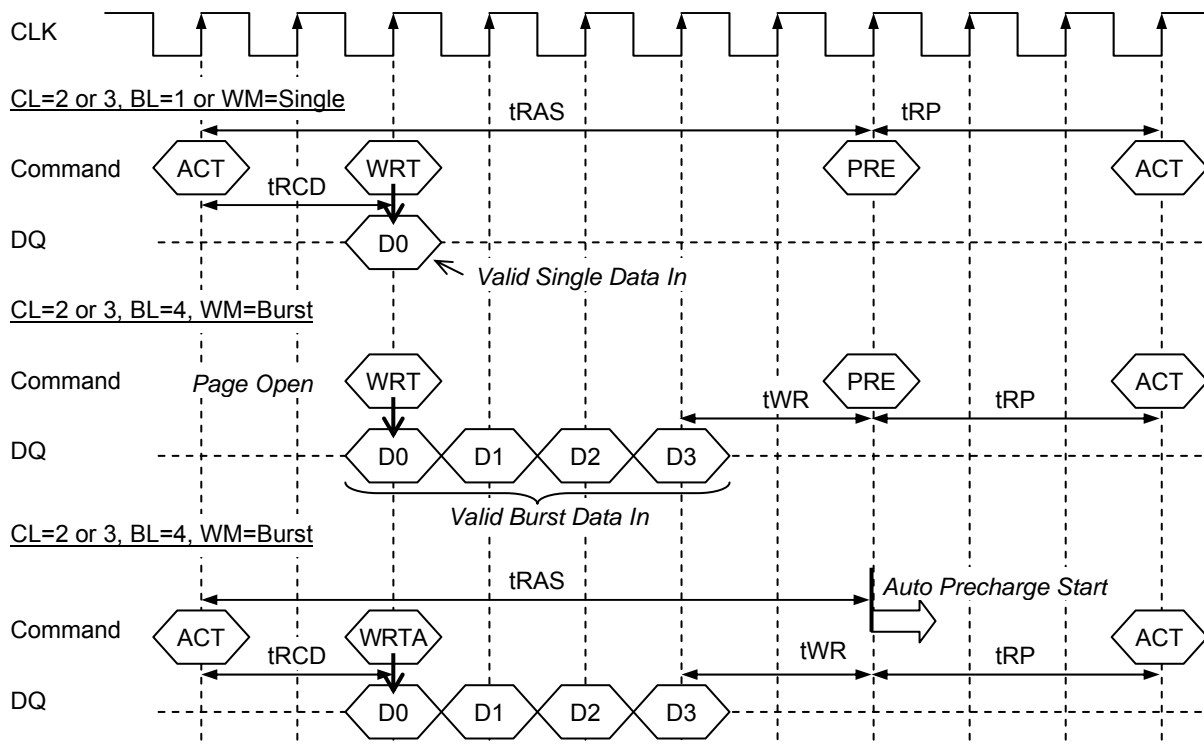
BA: Bank Address  
CA: Column Address  
D-in: Data inputs

**WRTA**

CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	X
/CS	X (Page Open)	L
/RAS		H
/CAS		L
/WE		L
A12, A13	X	BA
A10	X	1
A8, A9, A11	X	X
A0 to A7	X	CA
DQ	X	D-in

BA: Bank Address  
CA: Column Address  
D-in: Data inputs

### Write Cycle



**Read / Read with Auto-Precharge**

The read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The read command is issued by asserting low on /CS and /CAS with /WE being high on the positive edge of the clock. The bank must be active for at least tRCD(Min.) before the read command is issued. The first output appears in /CAS latency number of clock cycles after the issue of read command. The burst length, burst sequence and latency from the read command are determined by the mode register that is already programmed.

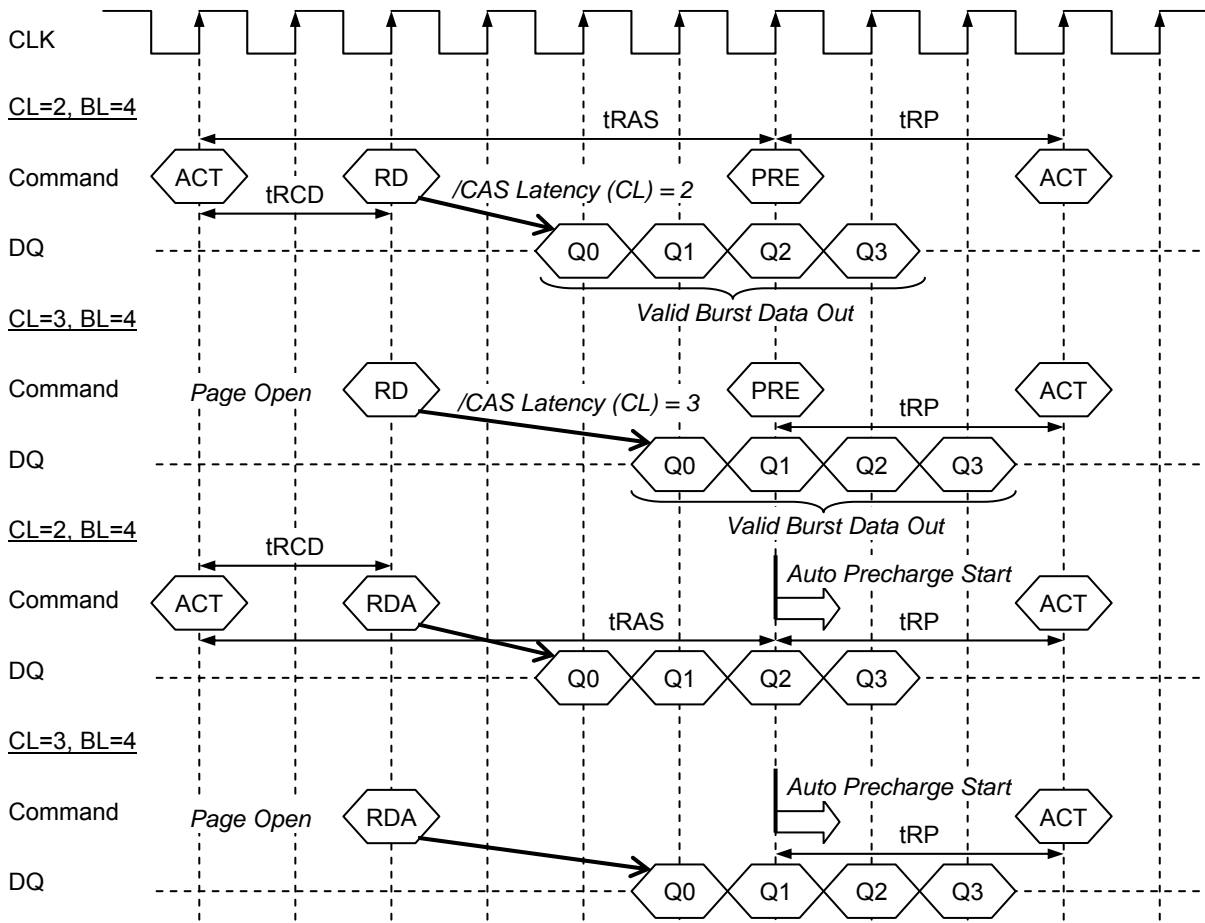
RD	CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	X	X
/CS	X	L	L
/RAS	X	H	H
/CAS	(Page Open)	L	L
/WE	X	H	H
A12, A13	X	BA	BA
A10	X	0	0
A11, A9, A8	X	X	X
A0 to A7	X	CA	CA
DQ	X	X	X

BA: Bank Address  
CA: Column Address

RDA	CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	X	X
/CS	X	L	L
/RAS	X	H	H
/CAS	(Page Open)	L	L
/WE	X	H	H
A12, A13	X	BA	BA
A10	X	1	1
A11, A9, A8	X	X	X
A0 to A7	X	CA	CA
DQ	X	X	X

BA: Bank Address  
CA: Column Address

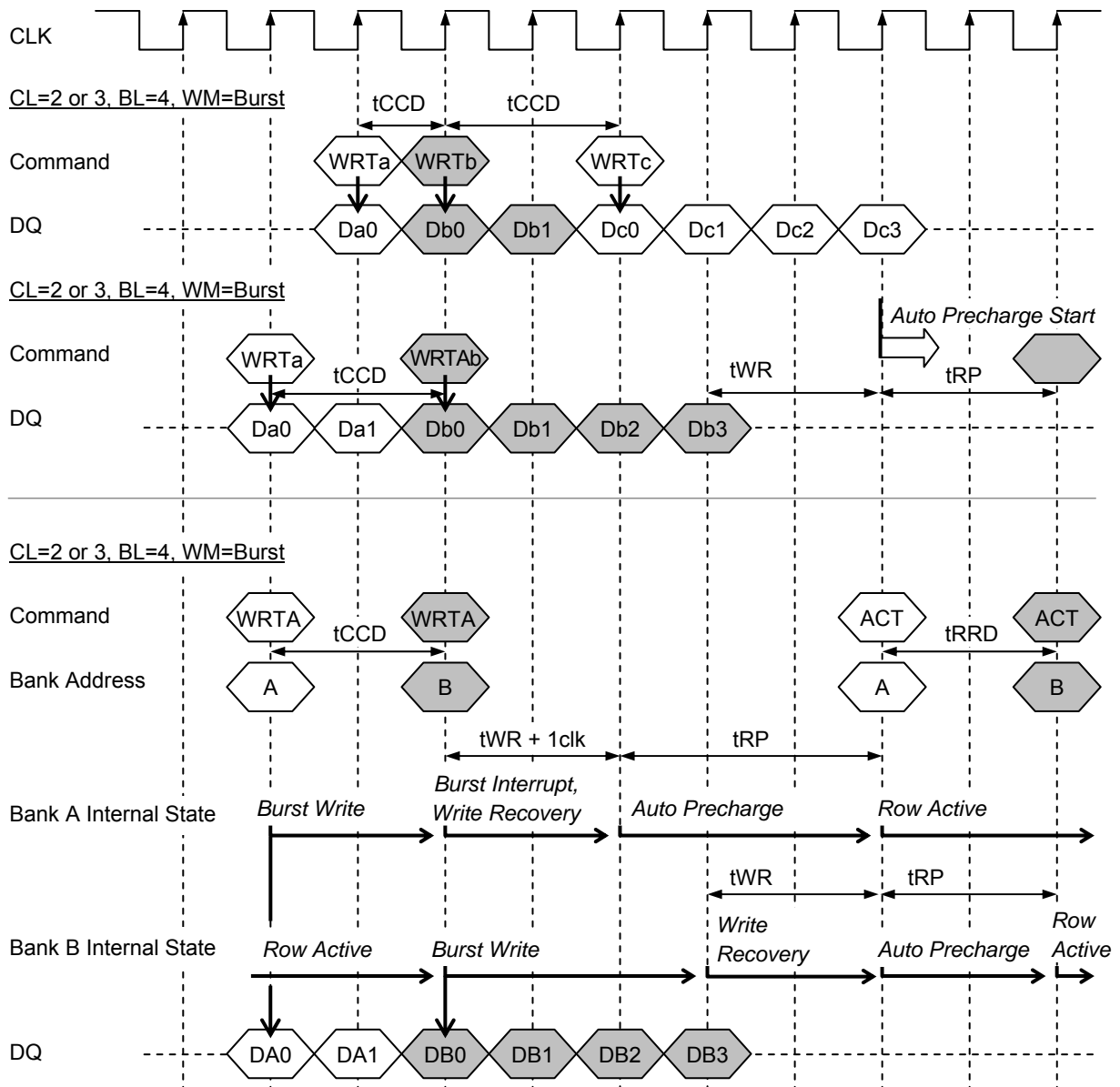
Read Cycle



**Write / Write interrupt**

When a new write command is issued to same bank during write cycle or another active bank, current burst write is terminated and new burst write start. When a new write command is issued to another bank during a write with auto-precharge cycle, current burst is terminated and a new write command start. Then, current bank is precharged after specified time. Don't issue a new write command to same bank during write with auto-precharge cycle.

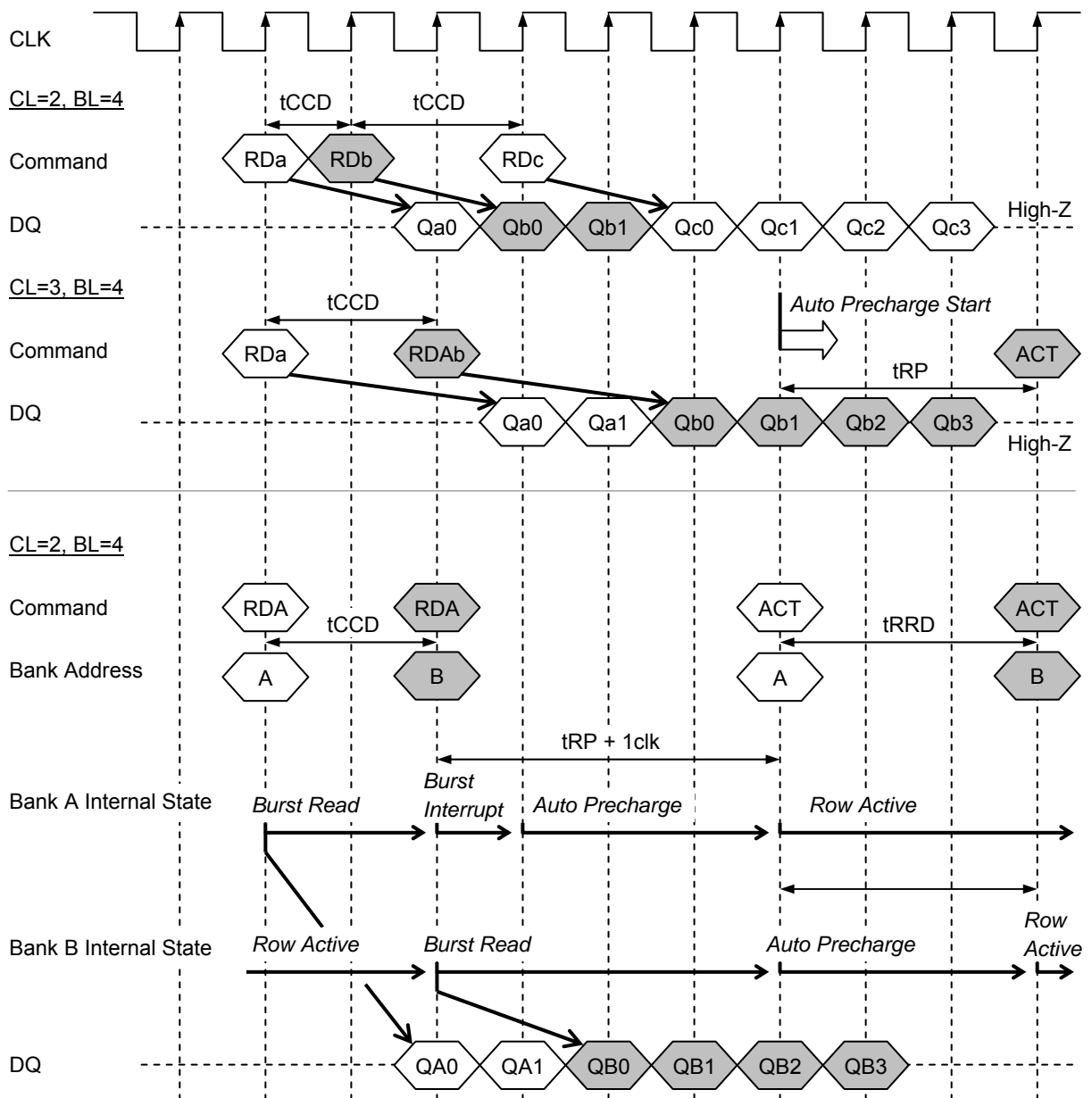
Write / Write interrupt cycle



**Read / Read interrupt**

When a new read command is issued to same bank during read cycle or another active bank, current burst read is terminated after the cycle same as /CAS latency and new burst read start. When a new read command is issued to another bank during a read with auto-precharge cycle, current burst is terminated after the cycle same as /CAS latency and a new read command start. Then, current bank is precharged after specified time. Don't issue a new read command to same bank during read with auto-precharge cycle.

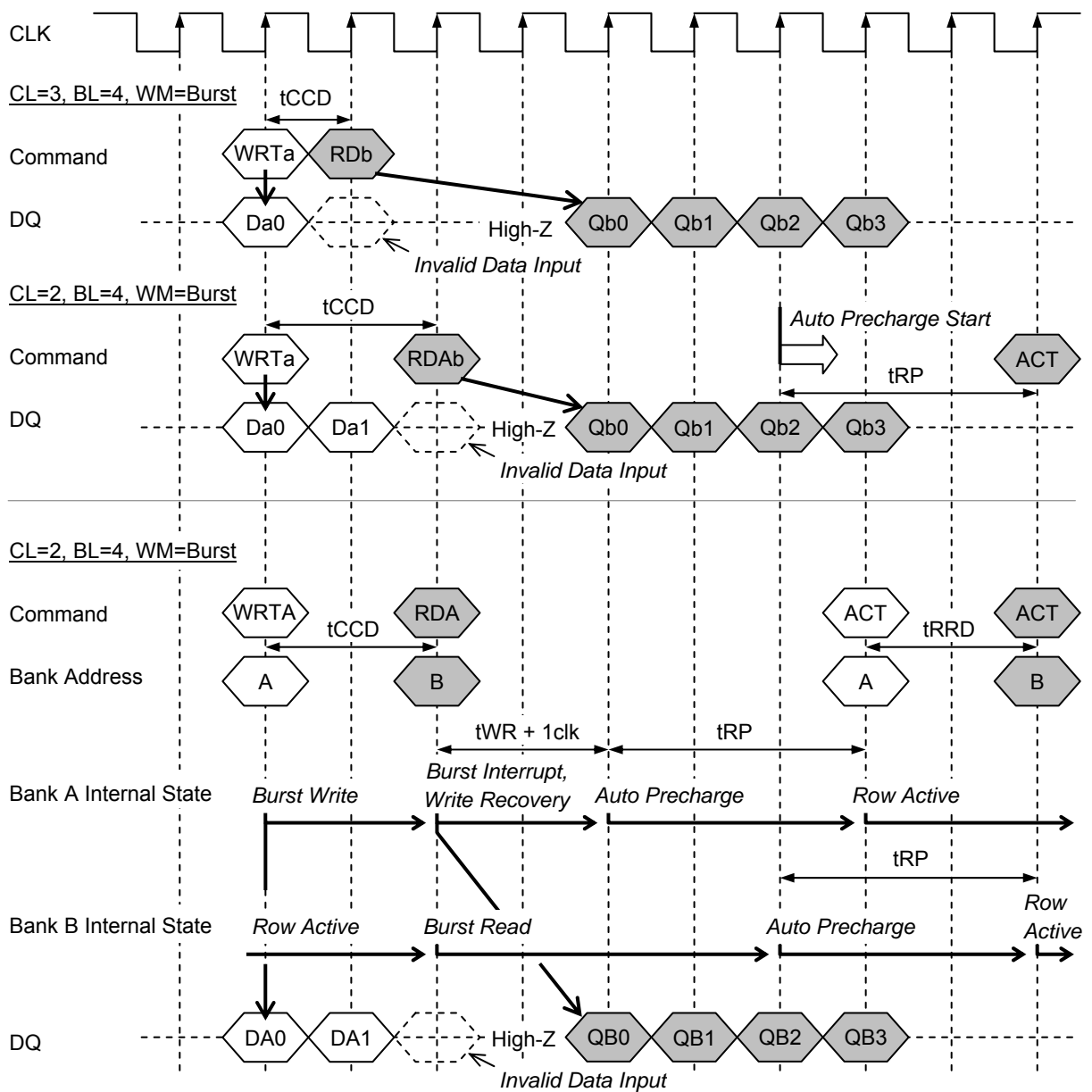
Read / Read interrupt cycle



**Write / Read interrupt**

When a new read command is issued to same bank during write cycle or another active bank, current burst write is terminated and new burst read start. When a new read command is issued to another bank during a write with auto-precharge cycle, current burst is terminated and a new read command start. Then, current bank is precharged after specified time. Don't issue a new read command to same bank during write with auto-precharge cycle. DQ must be High-Z till 1 or more clock from first read data.

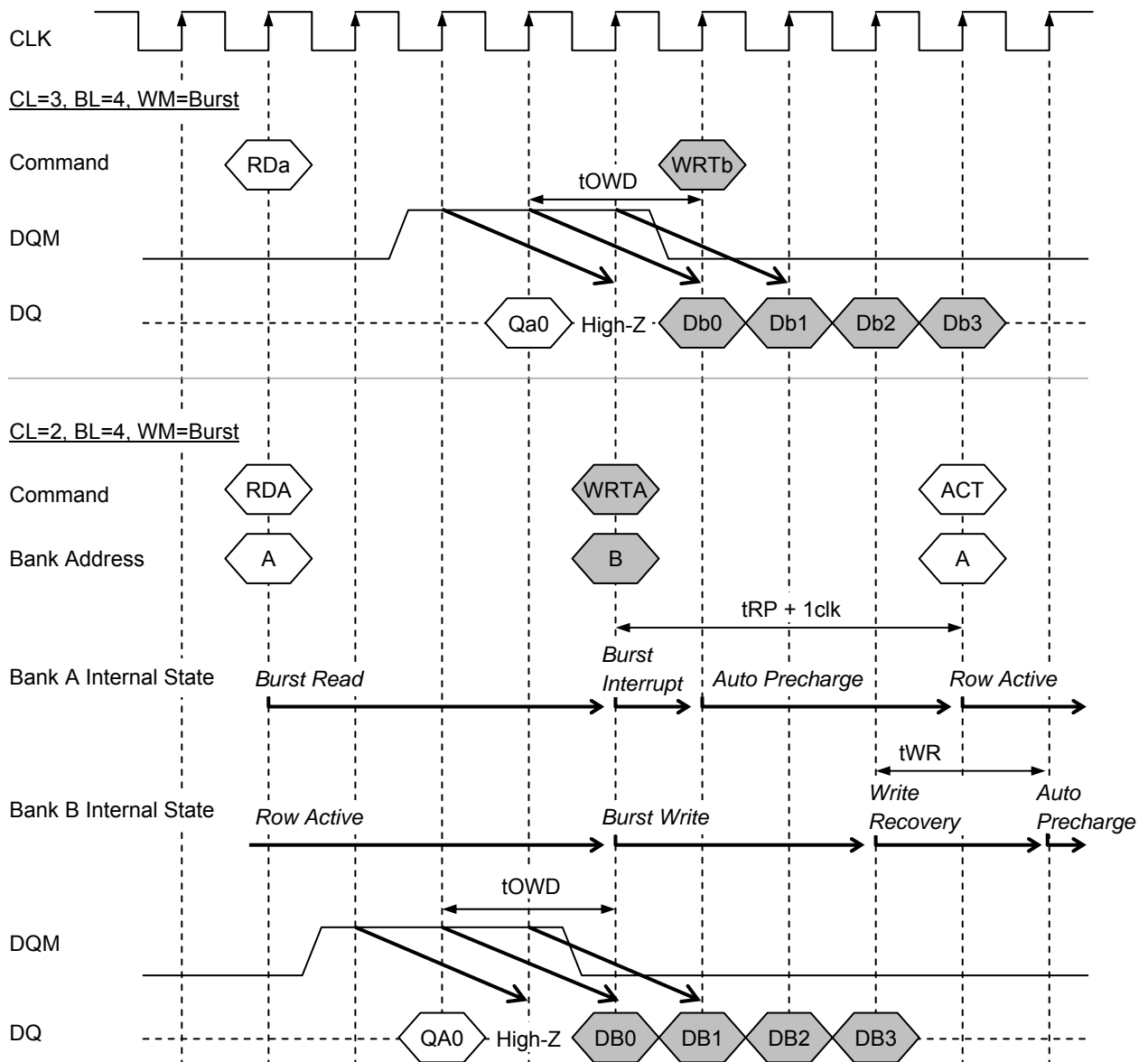
Write / Read interrupt cycle



**Read / Write interrupt**

When a new write command is issued to same bank during read cycle or another active bank, current burst read is terminated and new burst write start. When a new write command is issued to another bank during a read with auto-precharge cycle, current burst is terminated and a new write command start. Then, current bank is precharged after specified time. Don't issue a new write command to same bank during read with auto-precharge cycle. DQ must be High-Z till 1 or more clock from new write command. Therefore, DQM must be high till 3 clocks from new write command.

Read / Write interrupt cycle



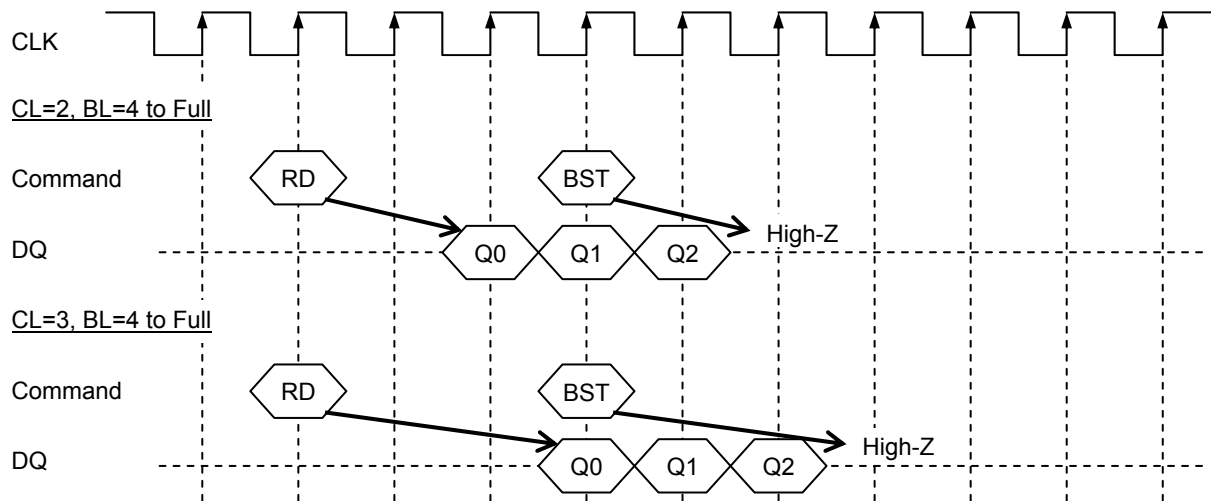
### Burst Stop

When a burst stop command is issued during read cycle, current burst read is terminated. The DQ is to High-Z after the cycle same as /CAS latency and page keep open. When a burst stop command is issued during write cycle, current burst write is terminated. The input data is ignored after burst stop command. Don't issue burst stop command during read with auto-precharge cycle or write with auto-precharge cycle.

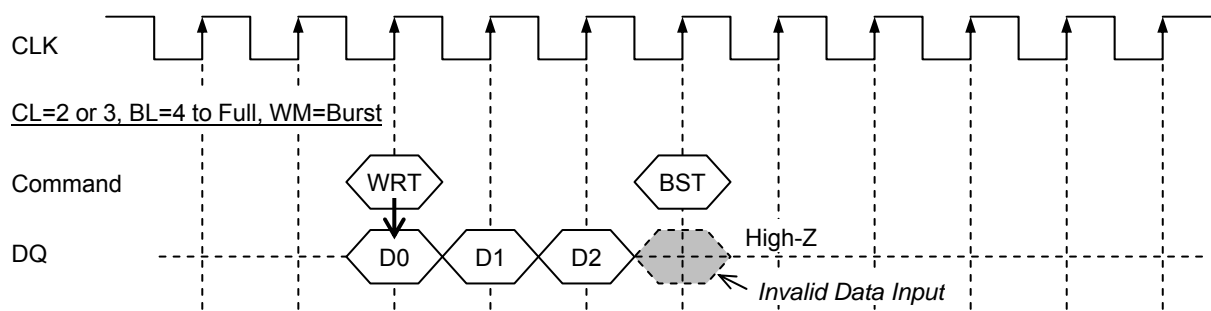
**BST**

CLK	$\uparrow$ n-1	$\uparrow$ n
CKE	H	H
/CS	X (Burst)	L
/RAS		H
/CAS		H
/WE		L
A12, A13		X
A0 to A11	X	X

#### Read / Burst Stop cycle



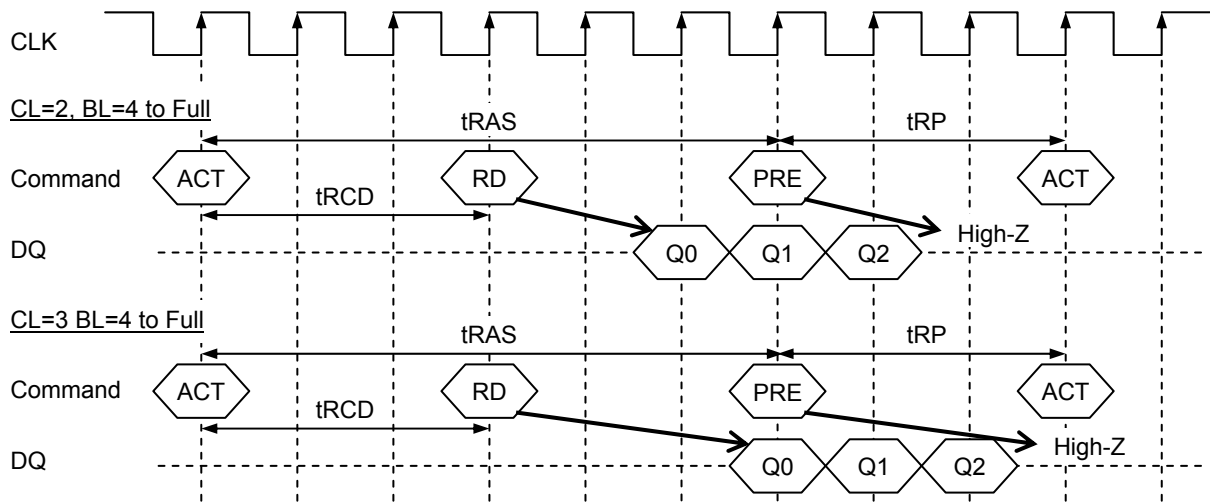
#### Write / Burst Stop cycle



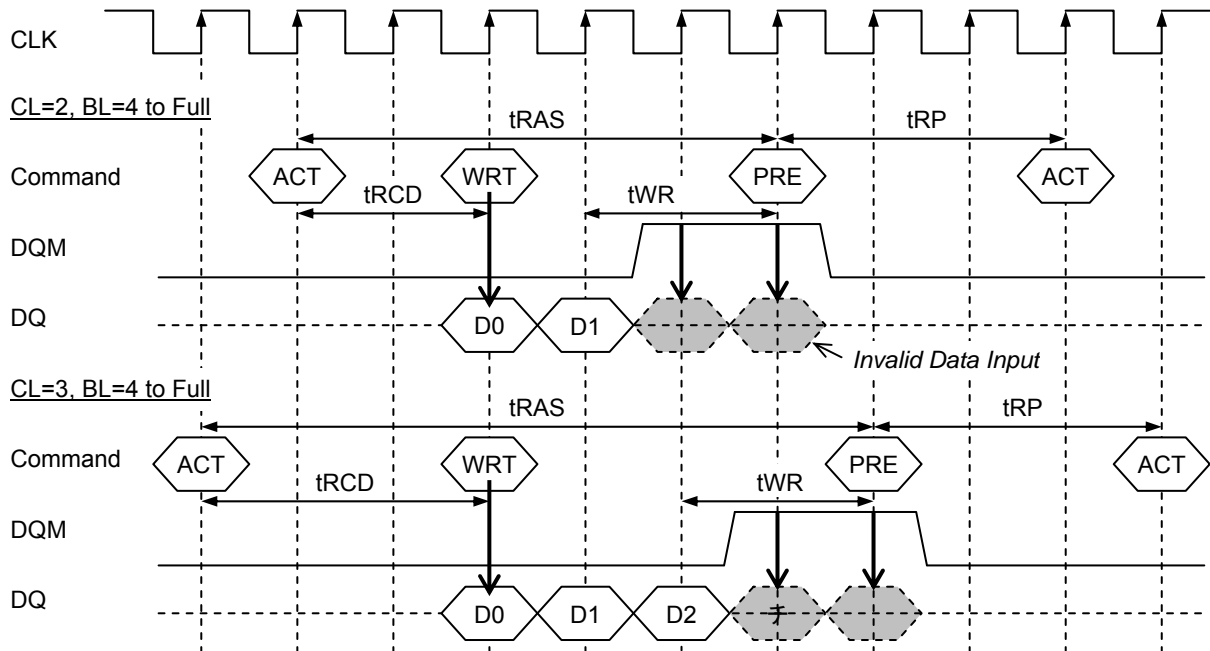
**Precharge Break**

When a precharge command is issued to the same bank during read cycle or precharge all command is issued, current burst read is terminated and DQ is to High-Z after the cycle same as /CAS latency. The objected bank is precharged. When a precharge command is issued to the same bank during write cycle or precharge all command is issued, current burst write is terminated and the objected bank is precharged. The input data after precharge command is ignored.

Read / Precharge Break cycle



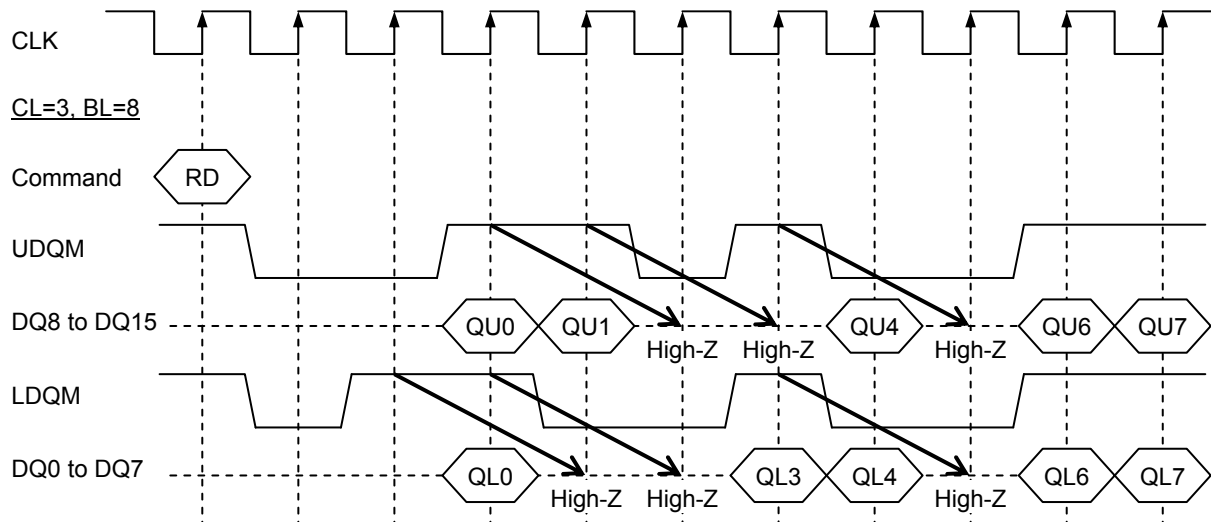
Write / Precharge Break cycle



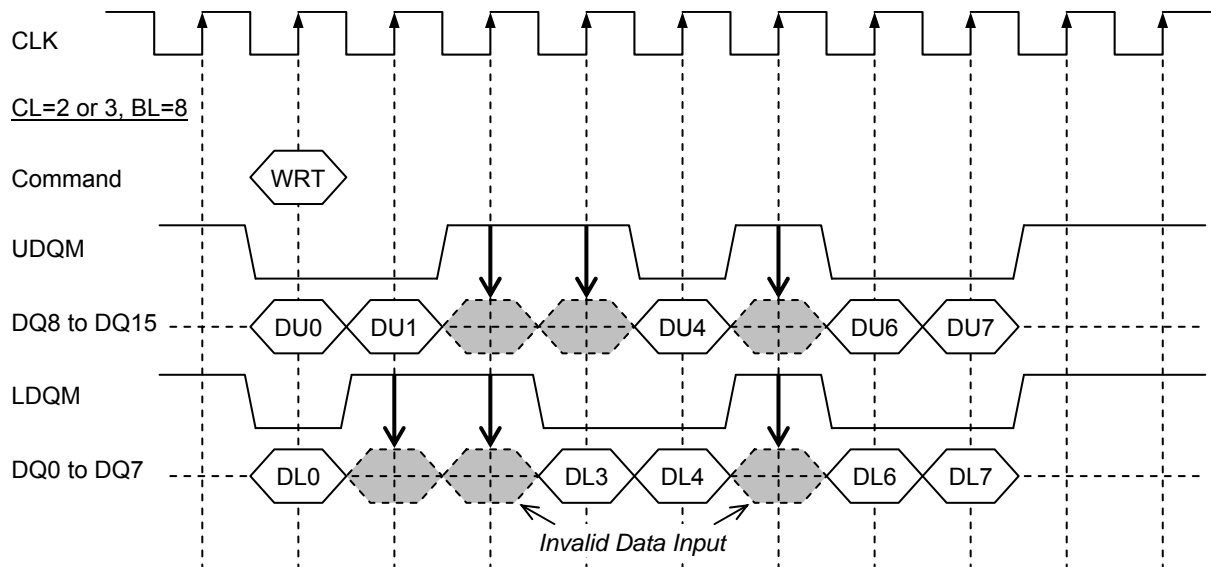
**DQM Function**

DQM masks input / output data at every byte. UDQM controls DQ8 to DQ15 and LDQM controls DQ0 to DQ7. During read cycle, DQM mask output data after 2 clocks. During write cycle, DQM mask input data at same clock.

Read / DQM Function



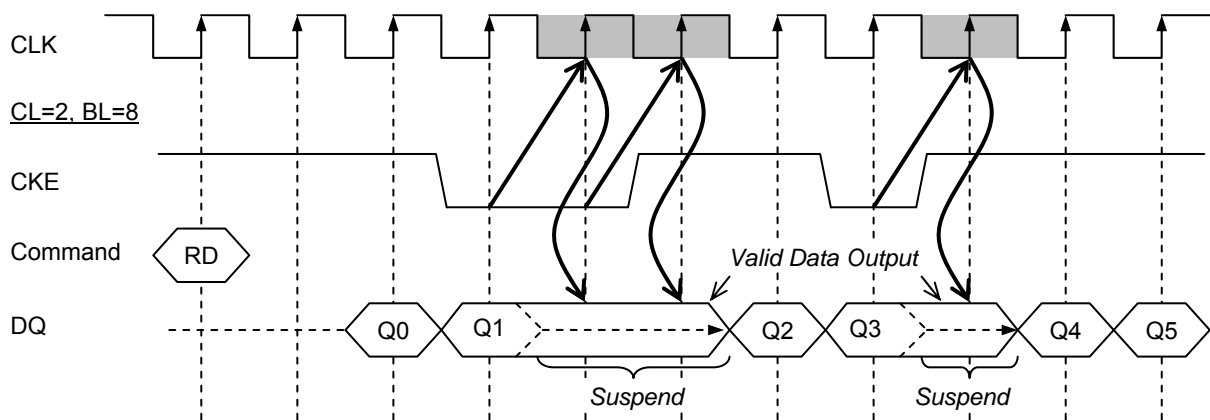
Write / DQM Function



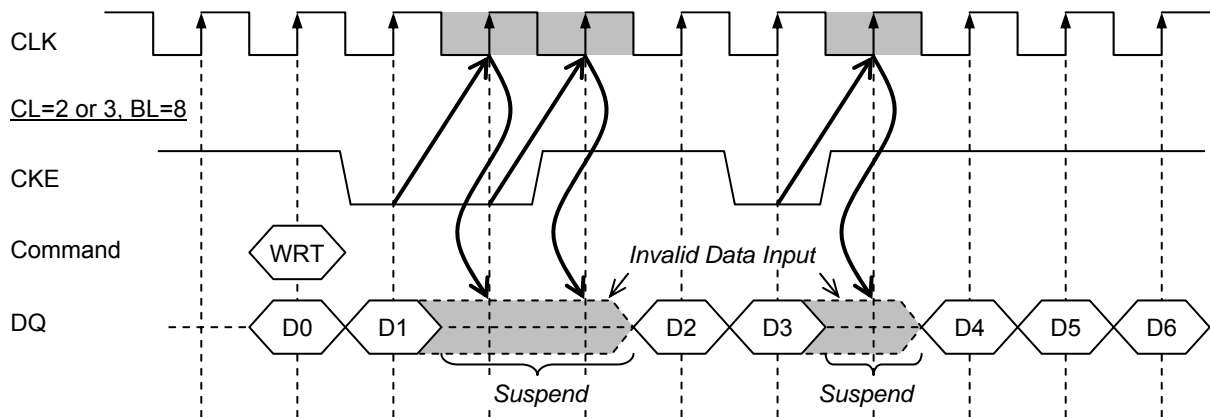
### Clock Suspend

The read / write operation can be stopped by CKE temporarily. When CKE is set low, the next clock is ignored. When CKE is set low during read cycle, the burst read is stopped temporarily and the current output data is kept. When CKE is set high, burst read is resumed. When CKE is set low during write cycle, the burst write is stopped temporarily. When CKE is set high, burst write is resumed.

#### Read / Clock Suspend



#### Write / Clock Suspend





**Self Refresh**

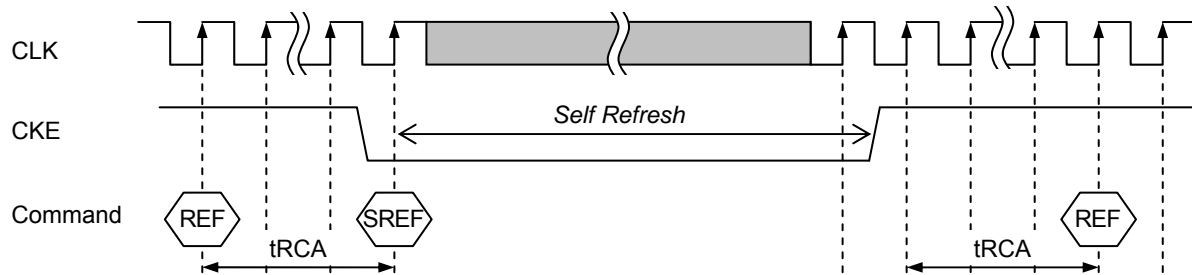
When read or write is not operated in the long period, self refresh can reduce power consumption for refresh operation. Refresh operation is controlled automatically by refresh timer and row address counter during self refresh mode. All signals except CKE are ignored and data bus DQ is set High-Z during self refresh mode.

When CKE is set to high level, self refresh mode is finished. Then, CLK must be operated before 1 clock or more. And, maintain NOP condition within a period of tRCA(Min.) after CKE is set to be high level.

**SREF**

CLK	$\frac{\uparrow}{n-1}$	$\frac{\uparrow}{n}$
CKE	H	L
/CS	X (Idle)	L
/RAS		L
/CAS		L
/WE		H
A12, A13	X	X
A0 to A11	X	X

**Self Refresh Cycle**

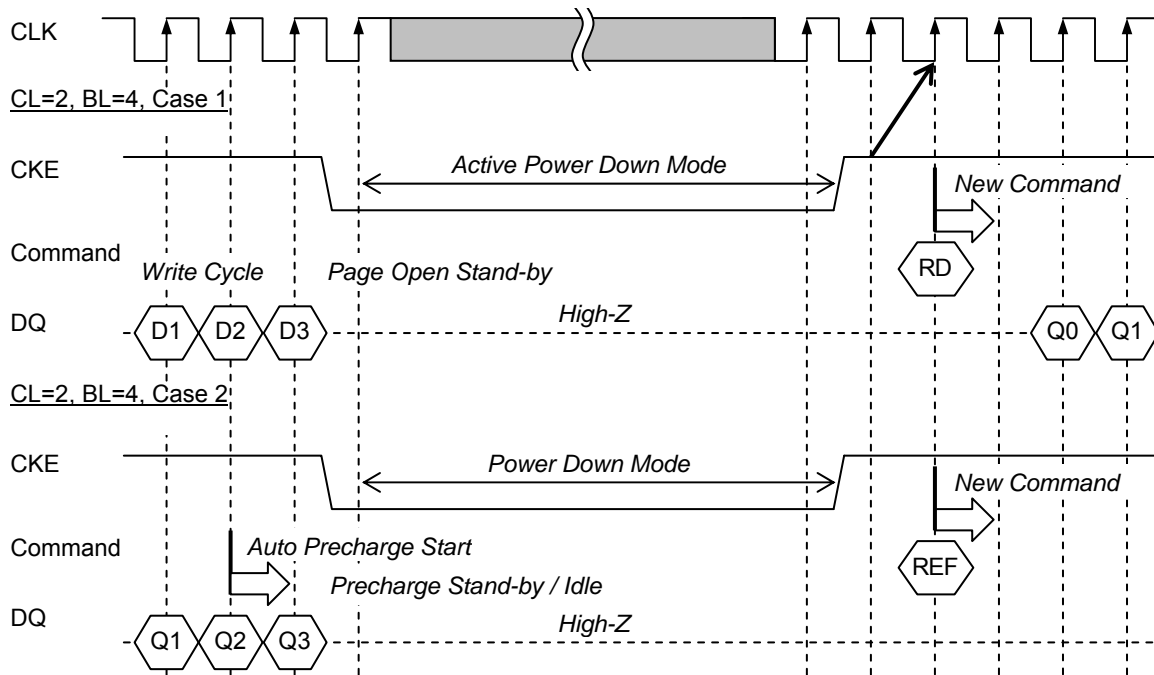


Notes : 1. When intensive refresh is used, 4,096 times refresh must be issued before and after the self refresh.

**Power Down**

SDRAM can be set to low power consumption condition with CKE function. CKE is reflected at 1 clocks later regardless /CAS latency. When CKE is set to low level, SDRAM go into power down mode. All signals except CKE are ignored and DQ is set to High impedance in this state. When CKE is set to high level, SDRAM exit power down mode. Then, Clock must be resumed before 1 or more clocks.

Power Down



**Signal Condition in Power Down Mode**

Signal	Input to SDRAM	Output from SDRAM
CLK	Don't Care	—
CKE	"L" level	—
/CS,/RAS, /CAS, /WE	Don't Care	—
A0 to A11, A12, A13	Don't Care	—
DQ0 to DQ15	Don't Care	High-Z
UDQM,LDQM	Don't Care	—
VCC,VCCQ,VSS,VSSQ	Power Supply	—

Notes : 1. "Don't Care" means high or low level input.

FUNCTION TRUTH TABLE (Table 1) (1/3)

Current State *1	/CS	/RAS	/CAS	/WE	ADDR	Command	Action
Idle	H	X	X	X	X	NOP	NOP
	L	H	H	X	X	NOP/BST	NOP
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL *2
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL *2
	L	L	H	H	BA, RA	ACT	Row Active
	L	L	H	L	BA, A10	PRE/PALL	NOP *3
	L	L	L	H	X	REF	Auto-Refresh or Self-Refresh *4
	L	L	L	L	V, A12=0, A13=0	MRS	Mode Register Set *4
	L	L	L	L	V, A12=1, A13=0	EMRS	ILLEGAL *4*10
Row Active	H	X	X	X	X	NOP	NOP
	L	H	H	X	X	NOP/BST	NOP
	L	H	L	H	BA, CA, A10	RD/RDA	Read
	L	H	L	L	BA, CA, A10	WRT/WRTA	Write
	L	L	H	H	BA, RA	ACT	ILLEGAL *6
	L	L	H	L	BA, A10	PRE/PALL	Precharge
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL
Read	H	X	X	X	X	NOP	Continue Row Active after Burst ends
	L	H	H	H	X	NOP	Continue Row Active after Burst ends
	L	H	H	L	X	BST	Term Burst → Row Active
	L	H	L	H	BA, CA, A10	RD/RDA	Term Burst, start new Burst Read
	L	H	L	L	BA, CA, A10	WRT/WRTA	Term Burst, start new Burst Write
	L	L	H	H	BA, RA	ACT	ILLEGAL *6
	L	L	H	L	BA, A10	PRE/PALL	Term Burst, execute Row Precharge
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL
Write	H	X	X	X	X	X	Continue Row Active after Burst ends
	L	H	H	H	X	X	Continue Row Active after Burst ends
	L	H	H	L	X	X	Term Burst → Row Active
	L	H	L	H	BA, CA, A10	CA, A10	Term Burst, start new Burst Read
	L	H	L	L	BA, CA, A10	CA, A10	Term Burst, start new Burst Write
	L	L	H	H	BA, RA	RA	ILLEGAL *6
	L	L	H	L	BA, A10	A10	Term Burst, execute Row Precharge
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL

FUNCTION TRUTH TABLE (Table 1) (2/3)

Current State <sup>*1</sup>	/CS	/RAS	/CAS	/WE	ADDR	Command	Action
Read with Auto Precharge	H	X	X	X	X	NOP	Continue Burst to End and enter Row Precharge
	L	H	H	H	X	NOP	Continue Burst to End and enter Row Precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*7</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*7</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*8</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	NOP	Continue Burst to End and enter Row Precharge
	L	H	H	H	X	NOP	Continue Burst to End and enter Row Precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*7</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*7</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*8</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL
Precharge	H	X	X	X	X	NOP	Idle after t <sub>RP</sub>
	L	H	H	H	X	NOP	Idle after t <sub>RP</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*2</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*2</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*3</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL
Write Recovery <sup>*9</sup>	H	X	X	X	X	NOP	Row Active after t <sub>WR</sub>
	L	H	H	H	X	NOP	Row Active after t <sub>WR</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*2</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*2</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*8</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL

FUNCTION TRUTH TABLE (Table 1) (3/3)

Current State <sup>*1</sup>	/CS	/RAS	/CAS	/WE	ADDR	Command	Action
Write Recovery in Auto Precharge <sup>*9</sup>	H	X	X	X	X	NOP	enter Row Precharge after t <sub>WR</sub>
	L	H	H	H	X	NOP	enter Row Precharge after t <sub>WR</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*7</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*7</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*8</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL
Auto Refresh	H	X	X	X	X	NOP	Idle after t <sub>RCA</sub>
	L	H	H	H	X	NOP	Idle after t <sub>RCA</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS	ILLEGAL
Mode Register Access	H	X	X	X	X	NOP	Idle after t <sub>MRD</sub>
	L	H	H	H	X	NOP	Idle after t <sub>MRD</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	REF	ILLEGAL
L	L	L	L	X	MRS	ILLEGAL	

## ABBREVIATIONS

ADDR = Address      RA = Row Address      BA = Bank Address      CA = Column Address  
 NOP = No OPERATION command      V = Value of Mode Register Set

- \*Notes :
1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
  2. RD/RDA or WRT/WRTA command to same bank is forbidden. But RD/RDA or WRT/WRTA command to activated page in another bank is valid.
  3. PRE command to another activated bank is valid. PALL command is valid to only activated bank.
  4. Illegal if any bank is not idle.
  5. RD/RDA or WRT/WRTA command to activated bank is valid after t<sub>RCD</sub>(Min.) from ACT command.
  6. Activate command to the same bank is forbidden. But activate command to another bank in idle state is valid.
  7. RD/RDA or WRT/WRTA command to same bank is forbidden. But RD/RDA or WRT/WRTA command to activated page in another bank is valid.
  8. PRE to same bank is forbidden. PRE to another bank must be issued after t<sub>RAS</sub>(Min.). PALL command is forbidden.
  9. Write recovery states means a period from last data to the time that t<sub>WR</sub>(Min.) passed.
  10. Extended Mode Register Set Command (EMRS) is illegal.

**FUNCTION TRUTH TABLE for CKE (Table 2)**

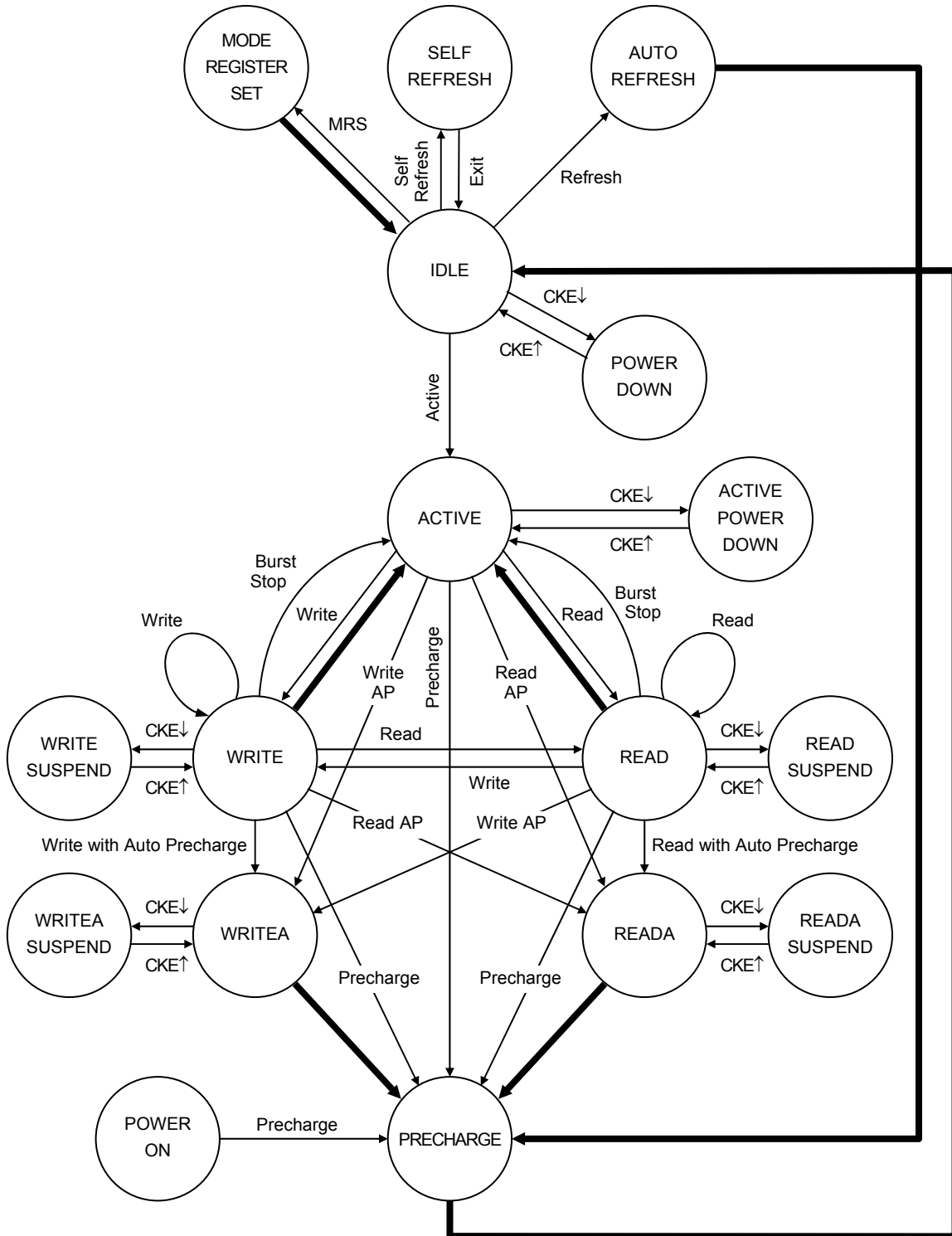
Current State n-1	CKE n-1	CKE n	/CS n	/RAS n	/CAS n	/WE n	ADDR n	Action
All Banks Idle (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	BA, RA	Enter Active Power Down after Activate
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh <sup>*2</sup>
	H	L	L	L	L	L	BA, V	Enter Power Down after MRS
	L	X	X	X	X	X	X	INVALID
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh → ABI <sup>*3</sup>
	L	H	L	H	H	H	X	Exit Self Refresh → ABI <sup>*3</sup>
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down → ABI <sup>*4</sup>
	L	L	X	X	X	X	X	NOP (Continue Power Down)
Active Power Down	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Active Power Down → Row Active <sup>*4</sup>
	L	L	X	X	X	X	X	NOP (Continue Active Power Down)
Row Active	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Active Power Down
	H	L	L	H	H	H	X	Enter Active Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	Clock Suspension (Refer to Table 1)
	H	L	L	L	H	X	X	Clock Suspension (Refer to Table 1)
	H	L	L	L	L	X	X	ILLEGAL
	L	X	X	X	X	X	X	INVALID
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

**ABBREVIATIONS**

ADDR = Address      RA = Row Address      BA = Bank Address      NOP = No Operation command  
V = Value of Mode Register Set      ABI = All Banks Idle

- \*Notes : 1. Deep Power Down can be entered only when all the banks are in an idle state.  
2. Self Refresh can be entered only when all the banks are in an idle state.  
3. tRCA must be set after exit self refresh.  
4. New command is enabled in the next clock.

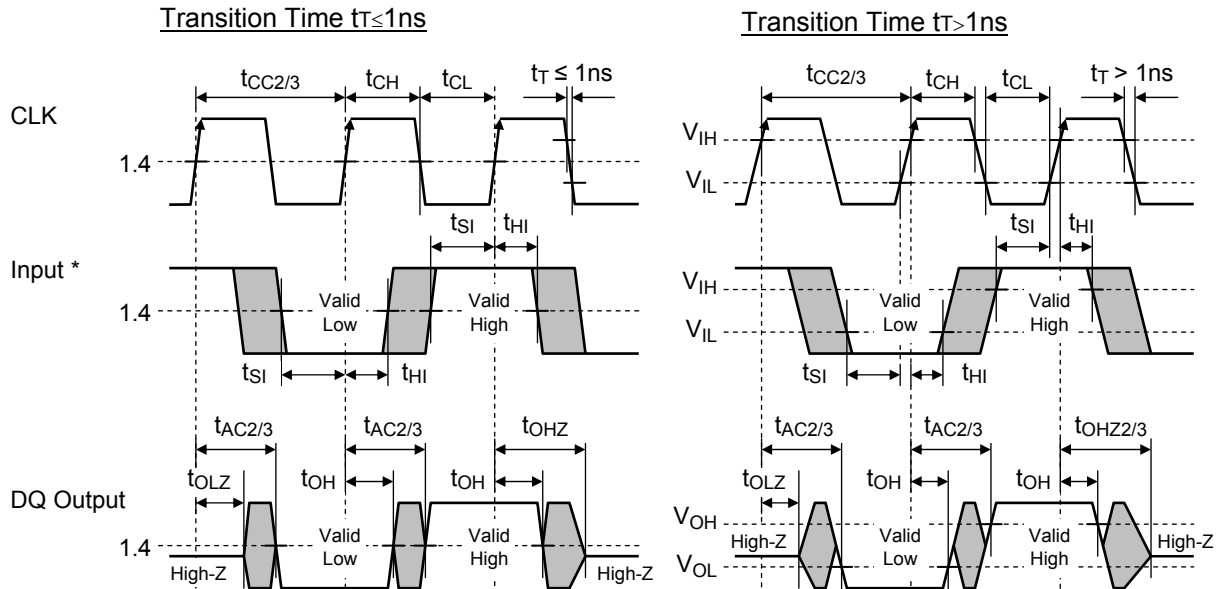
**SIMPLIFIED STATE DIAGRAM**



↙ Command / input signal      ↘ Auto Sequence

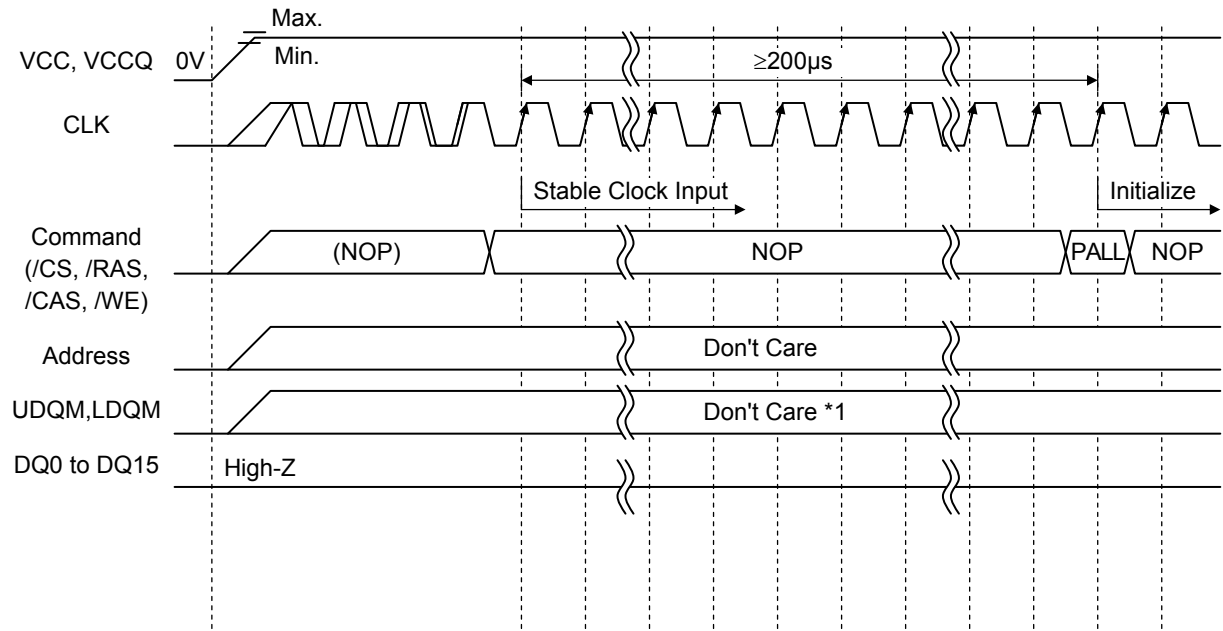
## TIMING CHART

### Synchronous Characteristics



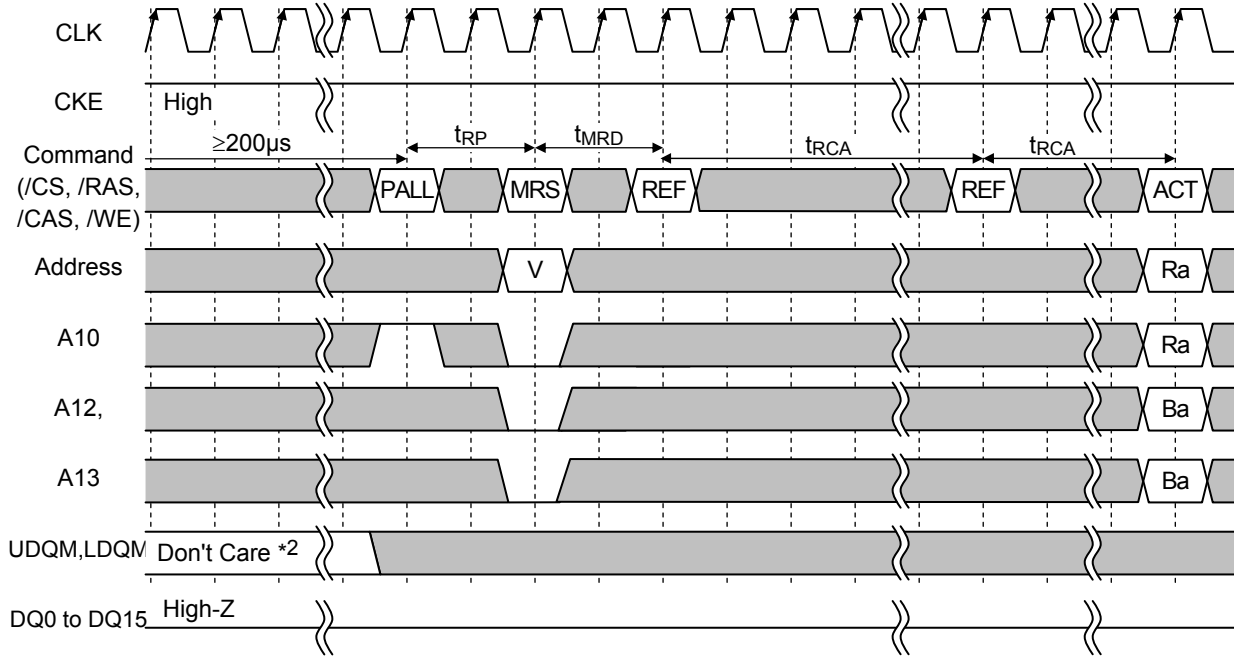
Note : The object of input are /CS, /RAS, /CAS, /WE, UDQM, LDQM and DQ0 to DQ15 (input).

### Power on Sequence



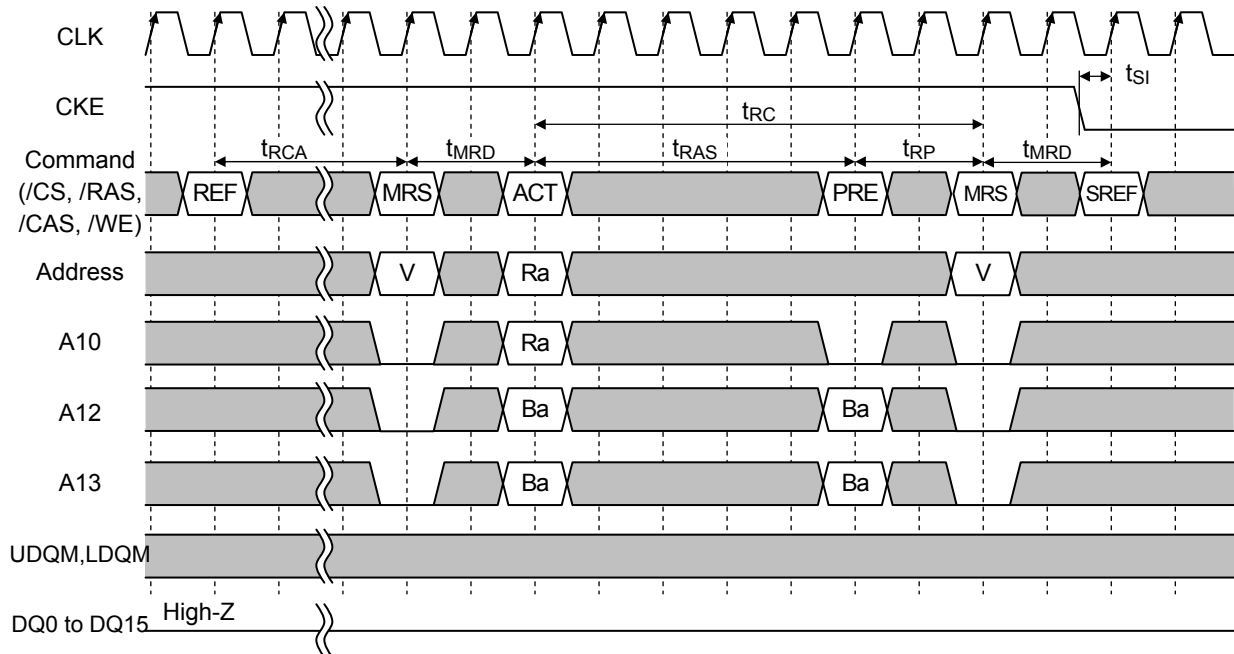
Notes : 1. It is advisable that UDQM and LDQM are set to high for set DQ to high impedance during power on sequence.

**Initialization**



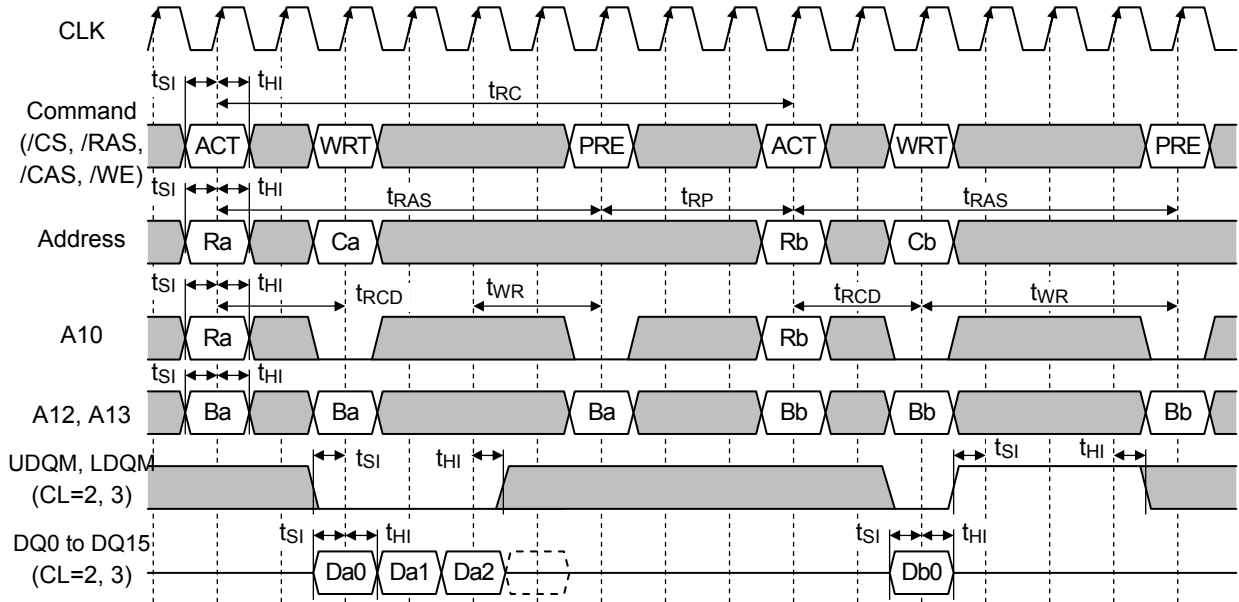
- Notes :
1. V = Value of mode register, Rx = Row Address, Bx = Bank Address  
 = NOP command or High or Low
  2. It is advisable that UDQM and LDQM are set to be high level for setting DQ to high impedance during power on sequence.

**Mode Register Set cycle**



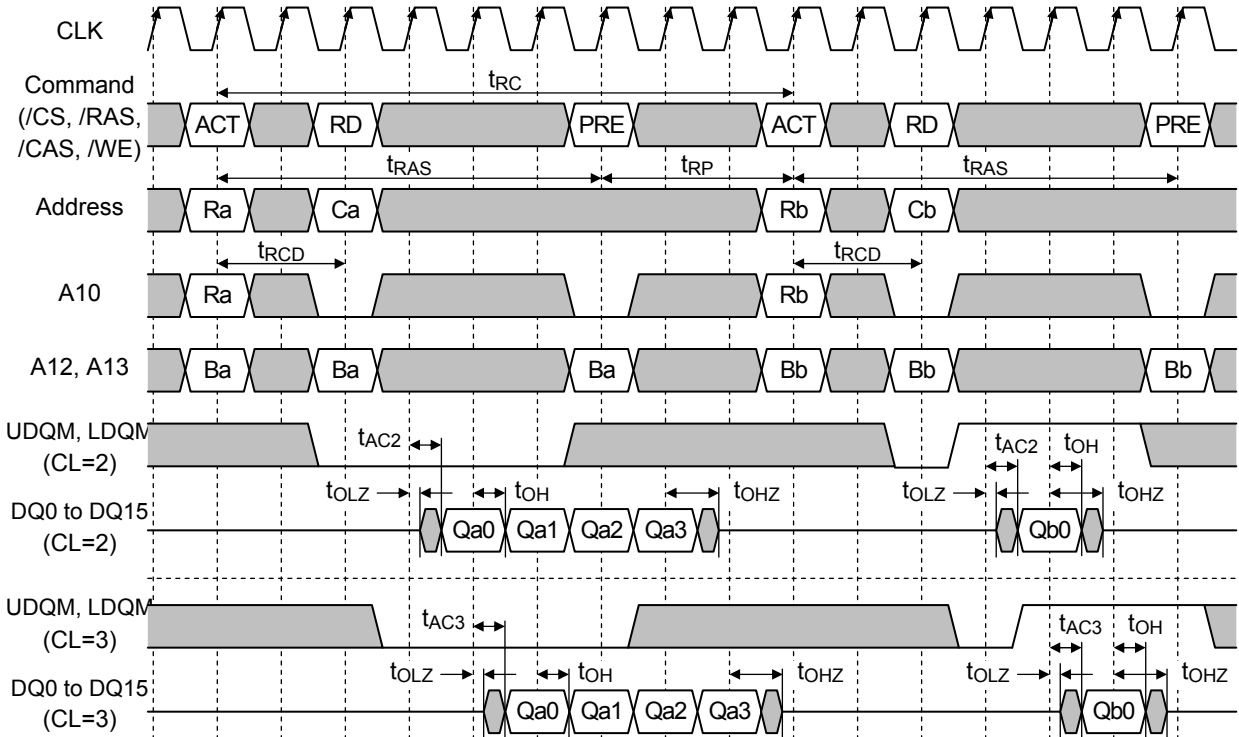
- Notes :
1. V = Value of mode register, Rx = Row Address, Bx = Bank Address  
 = NOP command or High or Low

**Burst Write Cycle (BL=4, WM=Burst)**



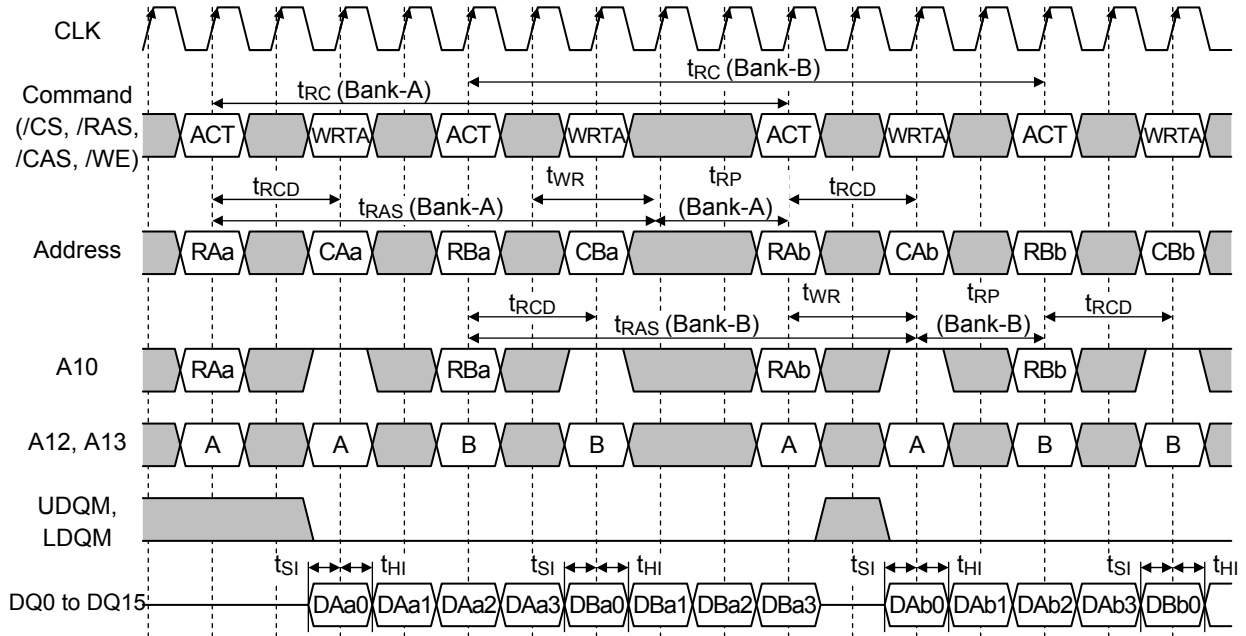
Notes : 1. Rx = Row Address, Cx = Column Address, Bx = Bank Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Burst Read Cycle (BL=4)**



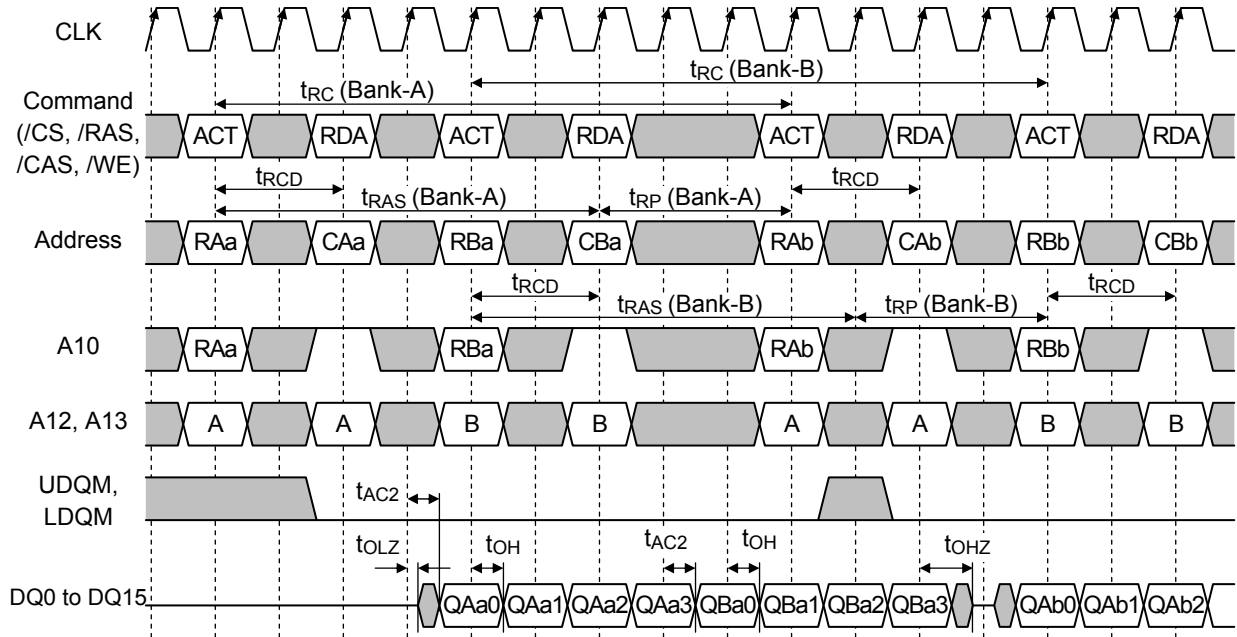
Notes : 1. Rx = Row Address, Cx = Column Address, Bx = Bank Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Bank Interleave • Write with Auto Precharge Cycle (CL=2, BL=4, WM=Burst)**



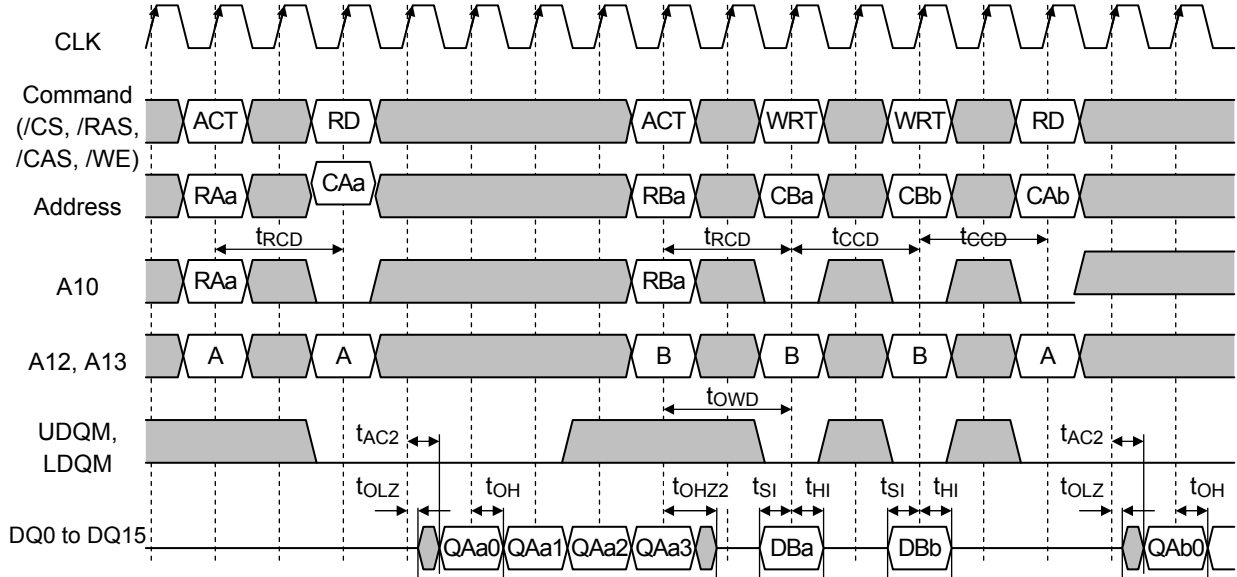
Notes : 1. Rxx = Row Address, Cxx = Column Address, X = Bank, x = Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Bank Interleave • Read with Auto Precharge Cycle (CL=2, BL=4)**



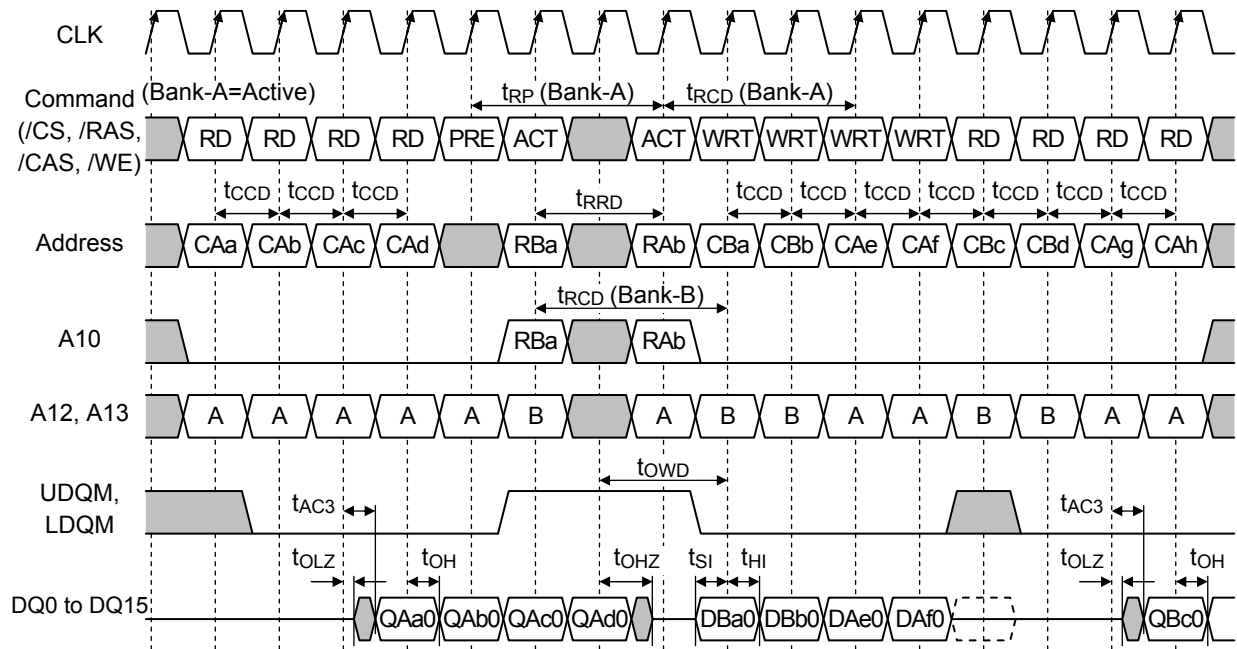
Notes : 1. Rxx = Row Address, Cxx = Column Address, X = Bank, x = Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Burst Read • Single Write Cycle (CL=2, BL=4, WM=Single)**



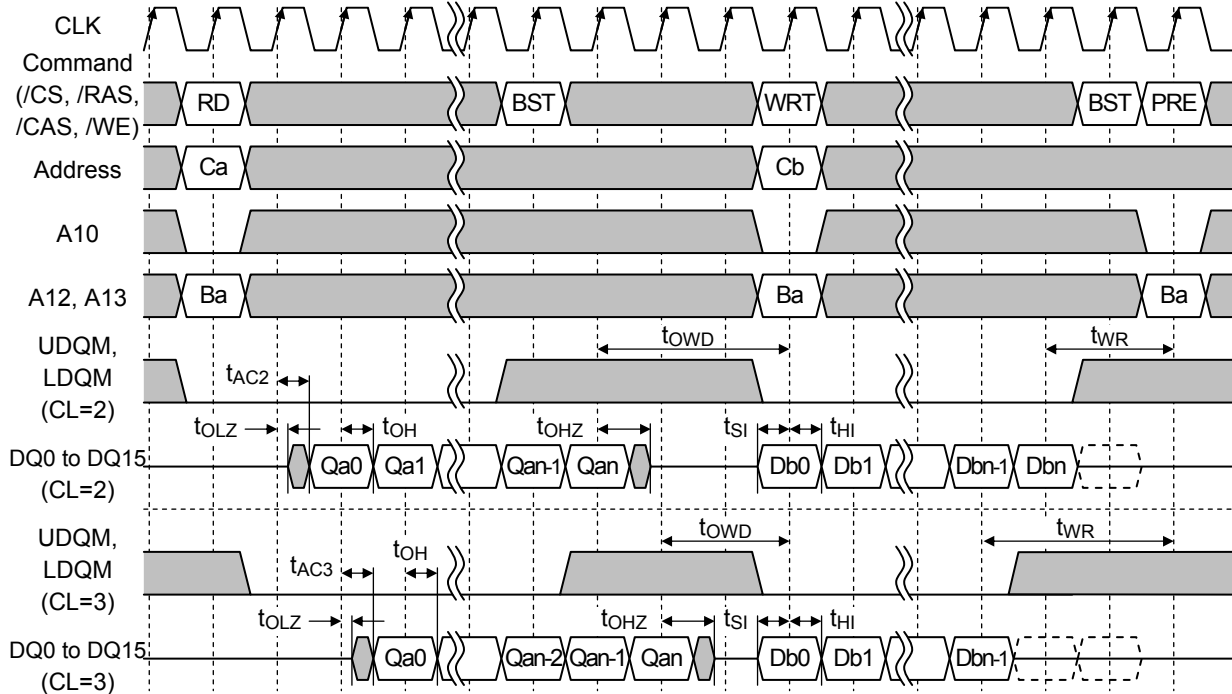
Notes : 1. Rxx = Row Address, Cxx = Column Address, X = Bank, x = Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Random Column • Read / Write Cycle (CL=3, BL=2, 4, 8, Full Page)**



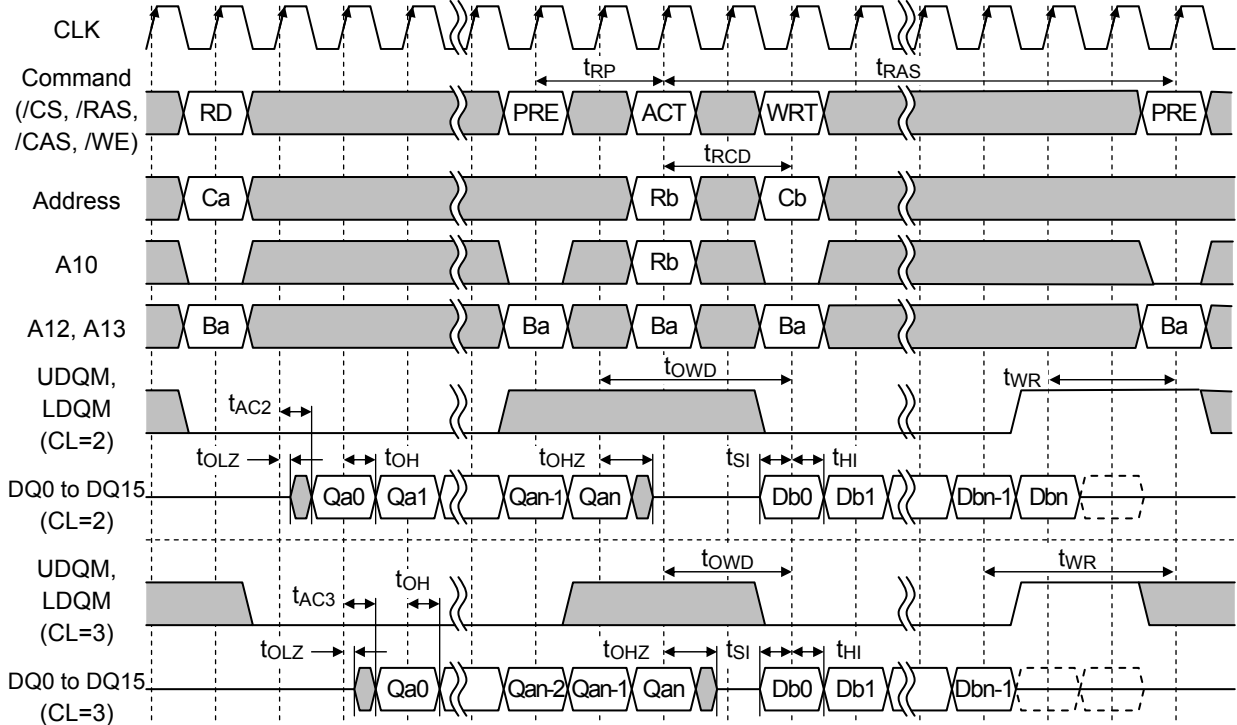
Notes : 1. Rxx = Row Address, Cxx = Column Address, X = Bank, x = Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level, [Dashed Box] = Invalid Data Input

**Burst Stop • Read / Write Cycle (BL=Full Page, WM=Burst)**



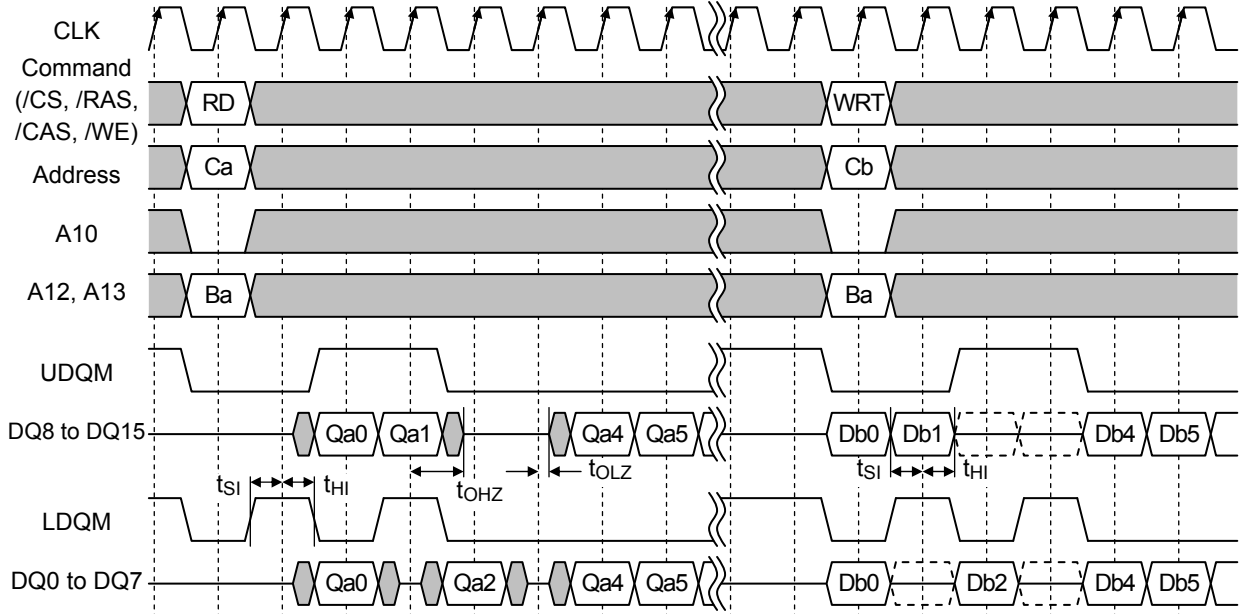
Notes : 1. Cx = Column Address, Bx = Bank Address  
 [Solid Gray] = NOP command or High or Low level, CKE = High level, [Dashed Box] = Invalid Data Input

**Precharge Break • Read / Write Cycle (BL=Full Page, WM=Burst)**



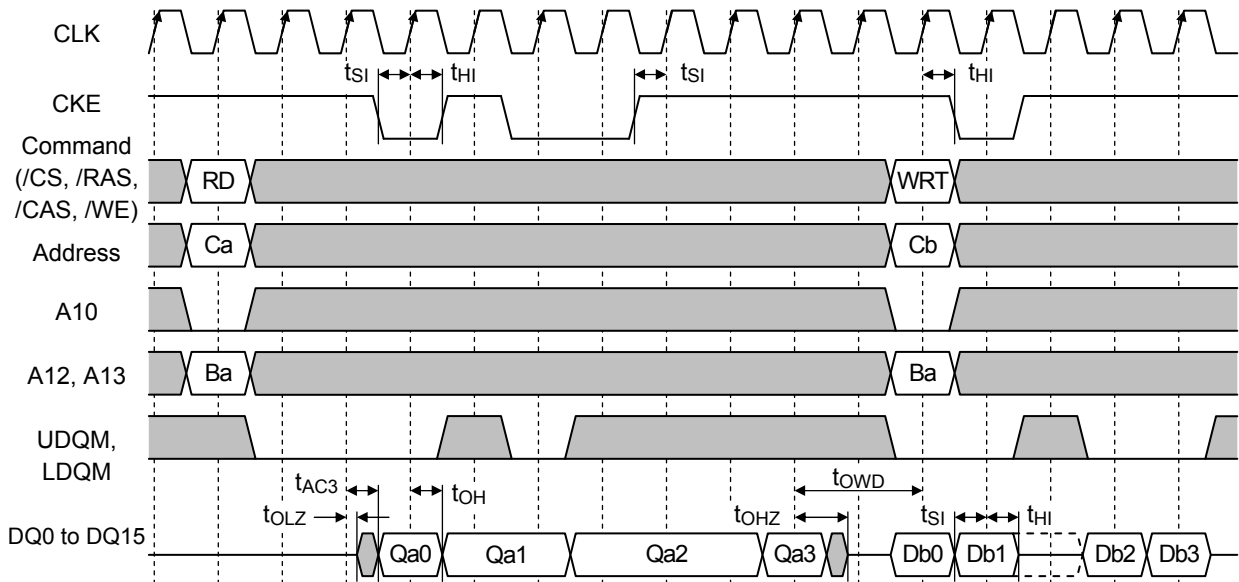
Notes : 1. Rxx = Row Address, Cxx = Column Address, X = Bank, x = Address  
 [Solid Gray] = NOP command or High or Low level, CKE = High level, [Dashed Box] = Invalid Data Input

**Byte Read / Byte Write Cycle (CL=2, BL=8, WM=Burst)**



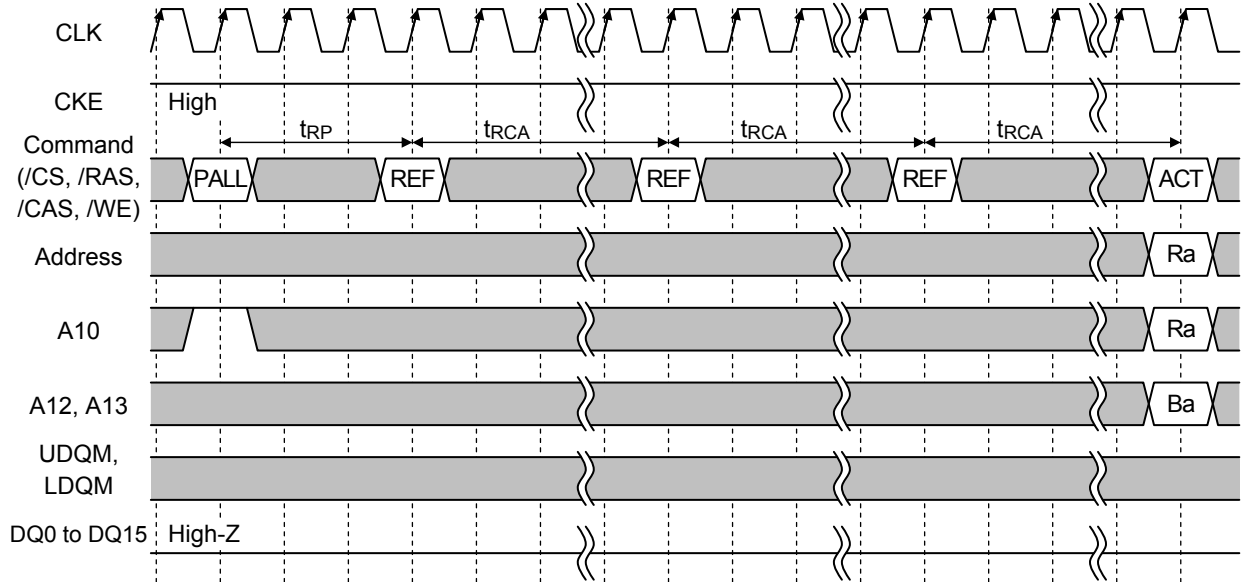
Notes : 1. Cx = Column Address, Bx = Bank Address  
 [█] = NOP command or High or Low level, CKE = High level, [---] = Invalid Data Input

**Clock Suspend • Read / Write Cycle (CL=3, BL=4, WM=Burst)**



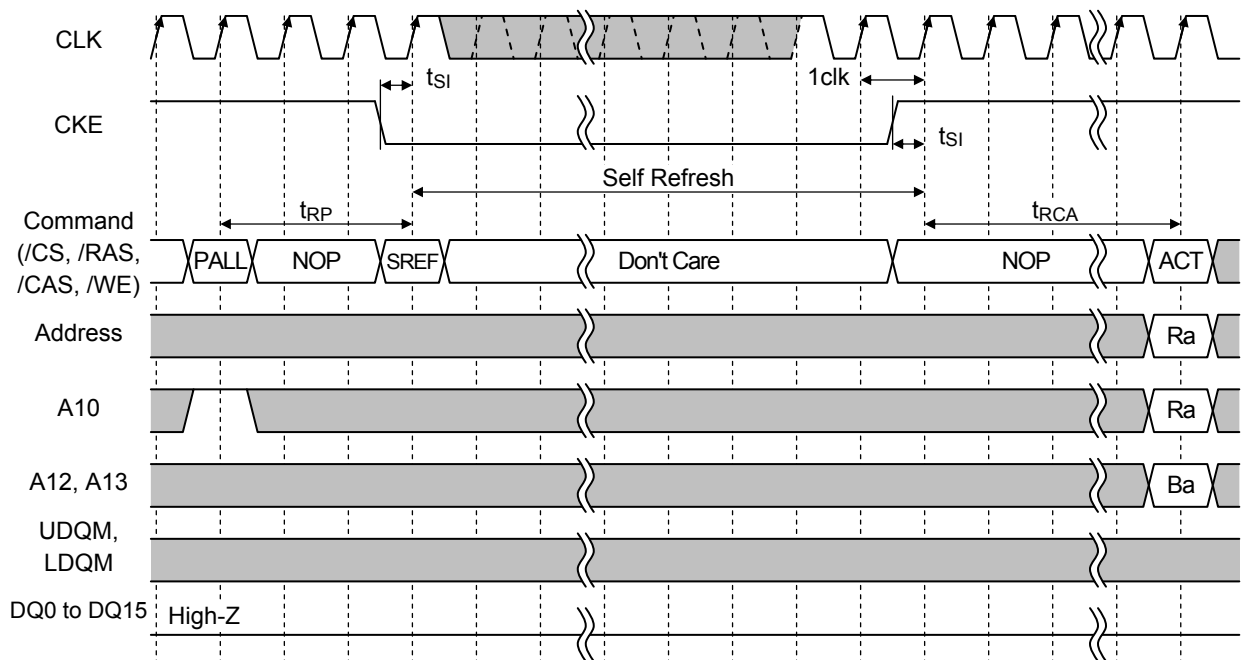
Notes : 1. Cx = Column Address, Bx = Bank Address  
 [█] = NOP command or High or Low level, CKE = High level, [---] = Invalid Data Input

**Auto Refresh Cycle**



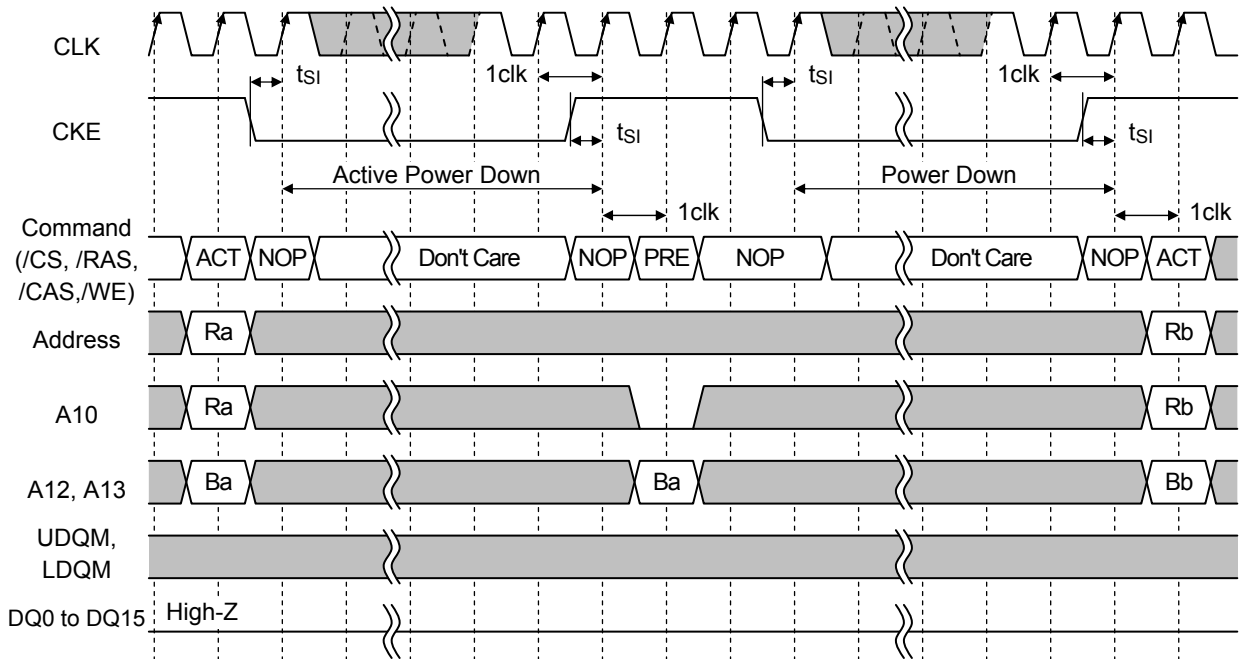
Notes : 1. Rx = Row Address, Bx = Bank Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level, [Dashed Box] = Invalid Data Input

**Self Refresh Cycle**



Notes : 1. Rx = Row Address, Bx = Bank Address  
 [Grey Box] = High or Low level

**Power Down Cycle**



- Notes : 1. Rx = Row Address, Bx = Bank Address  
 [Grey Box] = High or Low level

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDD56V62169MTA07AL-01	Apr. 2, 2012	–	–	First edition

## NOTICE

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

Copyright 2011 - 2012 LAPIS Semiconductor Co., Ltd.