ML22Q563-NNNMB/ML22Q563-xxxMB/ML2256X-xxxMB Datasheet

2-Channel Mixing Speech Synthesis LSI with Built-in FLASH/MASK ROM

GENERAL DESCRIPTION

The ML22Q563-NNN, ML22Q563-xxx and ML2256X-xxx are 2-channel mixing speech synthesis LSIs with built-in FLASH/MASK ROM for voice data. These LSIs incorporate into them an HQ-ADPCM decoder that enables high sound quality, 16-bit D/A converter, low-pass filter, and 1.0 W monaural speaker amplifier for driving speakers. Since functions necessary for voice output are all integrated into a single chip, a system can be upgraded with audio features by only using one of these LSIs.

- Capacity of internal memory and the maximum voice production time (when HQ-ADPCM※1 method used)

Product name	ROM capacity	Maximum voice production time (sec)		
		f_{sam} = 8.0 kHz	f_{sam} = 16.0 kHz	f_{sam} = 32.0 kHz
ML22Q563-NNN ML22Q563-xxx ML22563-xxx	4 Mbits	161	80	40
ML22562-xxx	2 Mbits	79	39	19

FEATURES

- Speech synthesis method: Can be specified for each phrase.
  HQ-ADPCM / 8-bit non-linear PCM / 8-bit PCM / 16-bit PCM
- Sampling frequency: Can be specified for each phrase.
  12.0/24.0/48.0 kHz, 8.0 / 16.0/32.0 kHz, 6.4/12.8/25.6 kHz
- Built-in low-pass filter and 16-bit D/A converter
- Built-in speaker driver amplifier: 1.0 W, 8Ω (at DV_{DD} = 5 V)
- External analog voice input (built-in analog mixing function)
- CPU command interface: Clock synchronous serial interface
- Maximum number of phrases: 1024 phrases, from 000h to 3FFh
- Edit ROM
- Volume control: CVOL command: Adjustable through 32 levels (including OFF)
  AVOL command: Adjustable through 50 levels (including OFF)
- Repeat function: LOOP command
- Channel mixing function: 2channels
- Power supply voltage detection function: Can be controlled at six levels from 2.7 to 4.0 V (including the OFF setting)
- Source oscillation frequency: 4.096 MHz
- Power supply voltage: 2.7 to 5.5 V
- Operating temperature range: –40°C to +85°C※2
- Package: 30-pin plastic SSOP(P-SSOP30-56-0.65-6K-MC)
- Product name: ML22Q563-NNNMB/ML22Q563-xxxMB
  ML22563-xxxMB/ML22562-xxxMB
  (“xxx” denotes ROM code number)

※1 Ky's Technology HQ-ADPCM is a high sound quality audio compression technology of "Ky's". “Ky’s” is a Registered trademark of National Universities corporate Kyushu Institute of Technology

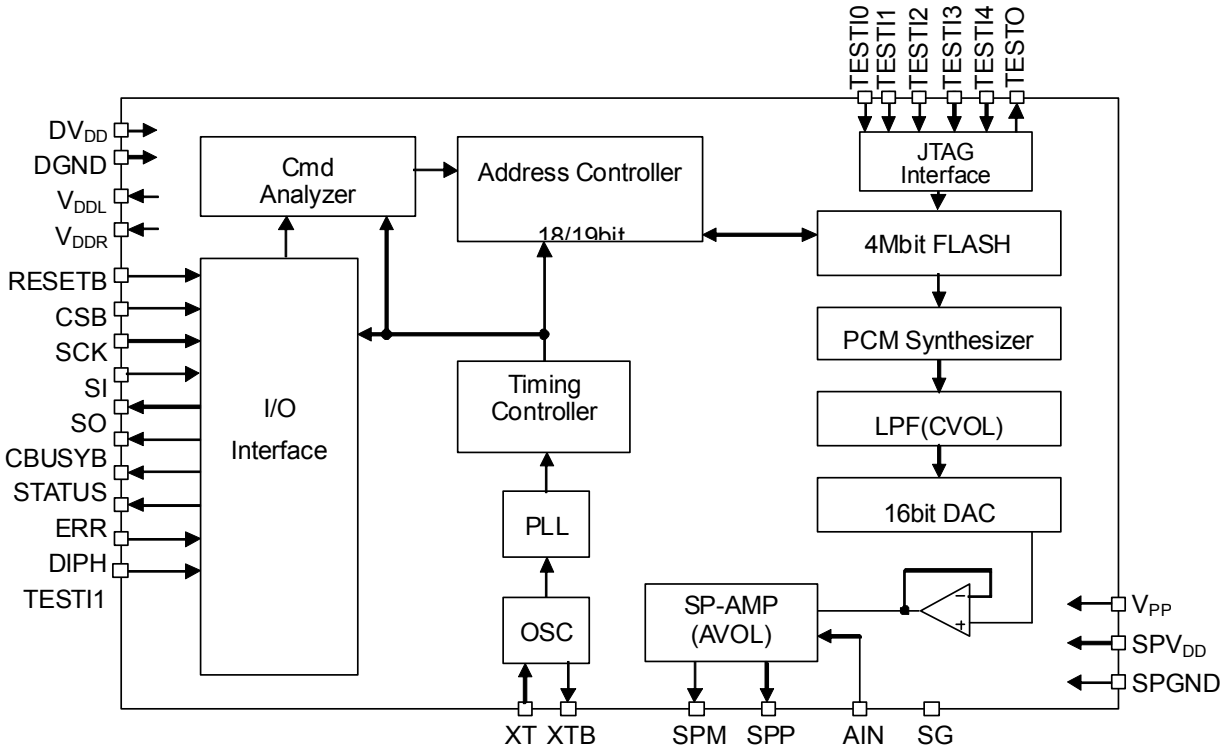
※2 The limitation on the operation time changes by the using condition. (Refer to Page62)

The table below summarizes the differences between the exsisting speech synthesis LSIs (ML225X and ML2282X) and the ML22Q563/ML2256X.

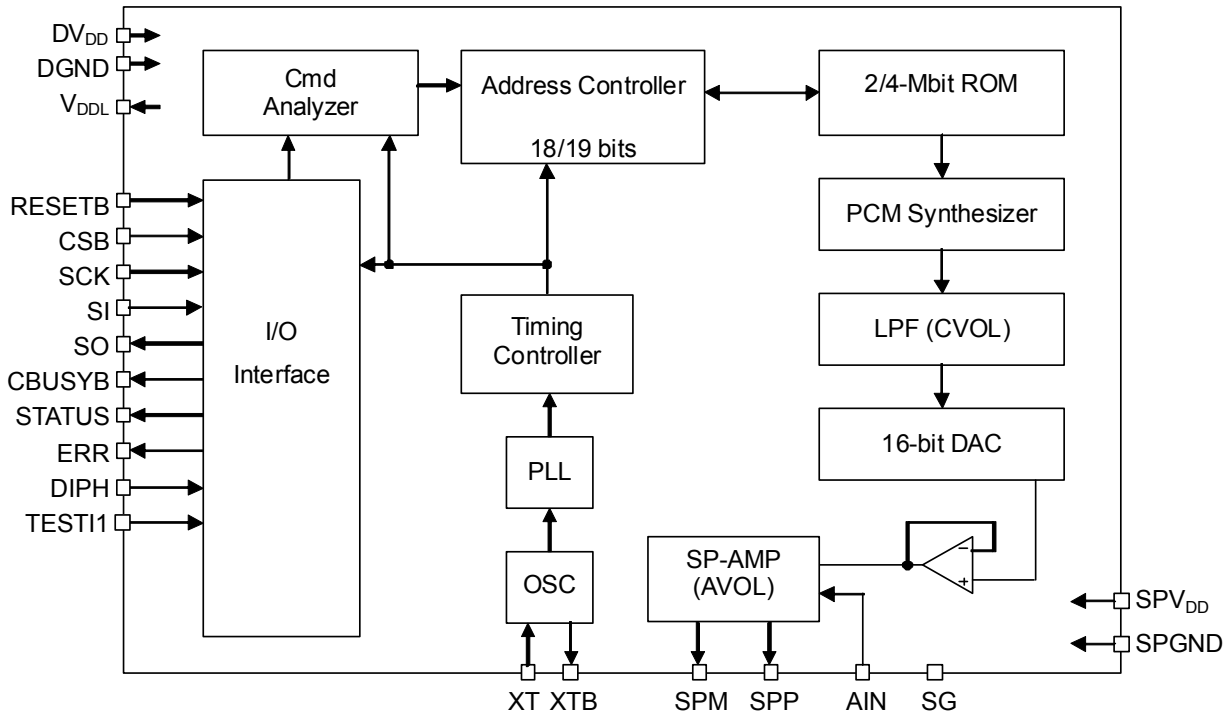
Item	ML225X	ML2282X	ML22Q563	ML2256X
CPU interface	Parallel/Serial	Serial/I2C	Serial	←
ROM type	MASK	P2ROM	FLASH	MASK
ROM capacity	3/4/6 Mbits	4/8/16 Mbits	4 Mbits	2/4 Mbits
Playback method	2-bit ADPCM2 4-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM	4-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM	HQ-ADPCM 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM	HQ-ADPCM 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM
Maximum number of phrases	256	1024	←	←
Sampling frequency (kHz)	4.0/5.3/6.4/8.0/ 10.7/12.0/12.8/ 16.0/21.3/24.0/ 25.6/32.0/48.0	←	6.4/8.0/12.0/ 12.8/16.0/24.0/ 25.6/32.0/48.0	←
Clock frequency	4.096 MHz (has a crystal oscillator circuit built-in)	←	←	←
D/A converter	14-bit voltage-type	16-bit voltage-type	←	←
Low-pass filter	FIR interpolation filter	FIR interpolation filter (SRC)	FIR interpolation filter (High-pass interpolation)	←
Speaker driving amplifier	No	Built-in 0.7 W (8Ω, DV_{DD} = 5 V)	Built-in 1.0 W (8Ω, DV_{DD} = 5 V)	←
Simultaneous sound production function (mixing function)	2-channel	←	←	←
Edit ROM	Yes	←	←	←
Volume control	29 levels	32 levels	←	←
Silence insertion	20 to 1024 ms (4 ms steps)	←	←	←
Repeat function	Yes	←	←	←
External analog input	No	Yes	←	←
External speech data input	Yes	No	←	←
Interval at which a seam is silent during continuous playback	No	←	←	←
Power supply voltage	2.7 V to 5.5 V	←	←	←
Ambient temperature	−40°C to +105°C	−40°C to +85°C	←	←
Package	44-pin QFP	30-pin SSOP	←	←

BLOCK DIAGRAM

The block diagrams of the ML22Q563-NNN/ML22Q563-xxx/ML2256X-xxx are shown below.



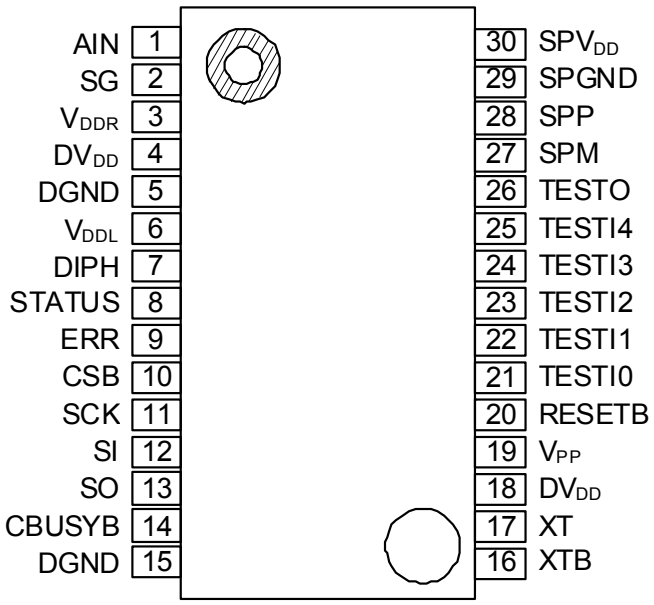
Block Diagram of ML22Q563-NNN/ML22Q563-xxx



Block Diagram of ML2256X−xxx

PIN CONFIGURATION (TOP VIEW)

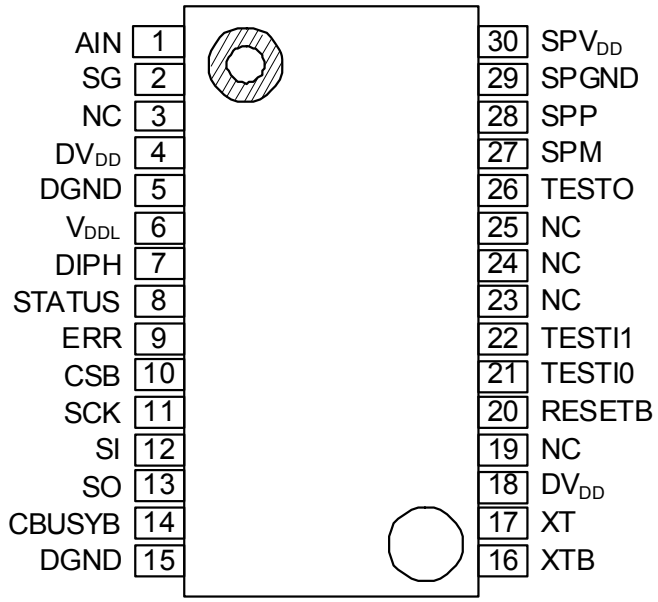
● ML22Q563-NNN/ML22Q563-xxx



30-Pin Plastic SSOP

NC: Unused pin

● ML2256X -xxx



NC: Unused pin

30-Pin Plastic SSOP

PIN DESCRIPTION (1)

Pin	Symbol	I/O	Attribute	Description	Attribute	Initial value
1	AIN	I	—	Speaker amplifier input pin.	analog	0
2	SG	O	—	Built-in speaker amplifier's reference voltage output pin. Connect a capacitor of 0.1 μF or more between this pin and DGND.	analog	0
3*2	V_{DDR}	O	—	2.5 V regulator output pin. Acts as an internal power supply (for ROM). Connect a capacitor of 10 μF or more between this pin and DGND.	analog	0
4,18	DV_{DD}	—	—	Digital power supply pin. Connect a bypass capacitor of 10μF or more between this pin and DGND.	power	—
5,15	DGND	—	—	Digital ground pin	gnd	—
6	V_{DDL}	O	—	2.5 V regulator output pin. Acts as an internal power supply (for logic). Connect a capacitor of 10 μF or more between this pin and DGND.	power	0
7	DIPH	I	Positive	Serial interface switching pin. Pin for choosing between rising edges and falling edges as to the edges of the SCK pulses used for shifting serial data input to the SI pin into the inside of the LSI. When this pin is at a "L" level, SI input data is shifted into the LSI on the rising edges of the SCK clock pulses and a status signal is output from the SO pin on the falling edges of the SCK clock pulses. When this pin is at a "H" level, SI input data is shifted into the LSI on the falling edges of the SCK clock pulses and a status signal is output from the SO pin on the rising edges of the SCK clock pulses.	digital	0
8	STATUS	O	Positive	Channel status output pin. Outputs the BUSYB or NCR signal for each channel by inputting the OUTSTAT command.	digital	1
9	ERR	O	Positive	Error output pin. Outputs a "H" level if an error occurs.	digital	0
10	CSB	I	Negative	Chip select pin. A "L" level on this pin accepts the SCK or SI inputs. When this pin is at a "H" level, neither the SCK nor SI signal is input to the LSI.	digital	1
11	SCK	I	Positive	Synchronous serial clock input pin.	clk	0
12	SI	I	—	Synchronous serial data input pin. When the DIPH pin is at a "L" level, data is shifted in on the rising edges of the SCK clock pulses. When the DIPH pin is at a "H" level, data is shifted in on the falling edges of the SCK clock pulses.	digital	0
13	SO	O	Positive	Channel status serial output pin. Outputs a status signal on the falling edges of the SCK clock pulses when the DIPH pin is at a "L" level; outputs a status signal on the rising edges of the SCK clock pulses when the DIPH pin is at a "H" level. When the CSB pin is at a "L" level, the status of each channel is output serially in sync with the SCK clock. When the CSB pin is at a "H" level, this pin goes into a high impedance state.	digital	Hi-Z

PIN DESCRIPTION (2)

Pin	Symbol	I/O	Attribute	Description	Attribute	Initial value(*1)
14	CBUSYB	O	Negative	Command processing status signal output pin. This pin outputs a “L” level during command processing. Be sure to enter commands with the CBUSYB pin driven at a “H” level.	digital	0(*1)
16	XTB	O	Negative	Connects to a crystal or a ceramic resonator. When using an external clock, leave this pin open. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.	clk	1
17	XT	I	Positive	Connects to a crystal or a ceramic resonator. A feedback resistor of around 1 MΩ is built in between this XT pin and the XTB pin. When using an external clock, input the clock from this pin. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.	clk	0
19*2	V_{PP}	I	—	Pin for FLASH analysis. Should be connected to DGND.	analog	0
20	RESETB	I	Negative	Reset input pin. At “L” level input, the LSI enters the initial state. After a reset input, the entire circuit is stopped and enters a power down state. Upon power-on, input a “L” level to this pin. After the power supply voltage is stabilized, drive this pin at a “H” level. This pin has a pull-up resistor built in.	digital	0(*1)
21	TESTI0 (MODE)	I	Positive	Input pin for testing. Also acts as a Flash rewrite enable pin. Has a pull-down resistor built in.	digital	0
22	TESTI1 (nTRST)	I	Negative	Used as either an input pin for testing or a reset input pin for Flash rewriting. Has a pull-down resistor built in.	digital	0
23*2	TESTI2 (TMS)	I	Positive	Used as either an input pin for testing or a state transition pin for Flash rewriting. Has a pull-up resistor built in.	digital	1
24*2	TESTI3 (TDI)	I	Positive	Used as either an input pin for testing or a data input pin for Flash rewriting. Has a pull-up resistor built in.	digital	1
25*2	TESTI4 (TCK)	I	Positive	Used as either an input pin for testing or a clock input pin for Flash rewriting. Has a pull-up resistor built in.	digital	0
26*2	TESTO (TSO)	O	Positive	Used as either an output pin for testing or a data output pin for Flash rewriting.	digital	Hi-Z
27	SPM	O	—	Output pin of the built-in speaker amplifier.	analog	Hi-Z
28	SPP	O	—	Output pin of the built-in speaker amplifier. Can be configured as an AOUT amplifier output by command setting.	analog	0
29	SPGND	—	—	Speaker amplifier ground pin.	gnd	—
30	SPV_{DD}	—	—	Speaker amplifier power supply pin. Connect a bypass capacitor of 10μF or more between this pin and SPGND.	power	—

*1: Indicates the initial value at reset input or during power down.
*2: These are NC pins in the ML2256X.

ABSOLUTE MAXIMUM RATINGS

DGND = SPGND = 0 V, Ta = 25°C

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	DV_{DD} SPV_{DD}	—	−0.3 to +7.0	V
Input voltage	V_{IN}	—	−0.3 to DV_{DD}+0.3	V
Power dissipation	P_D	When the LSI is mounted on JEDEC 4-layer board. When SPV_{DD} = 5V	1000	mW
Output short-circuit current	I_{OS}	Applies to all pins except SPM, SPP, V_{DDL}, and V_{DDR}.	10	mA
		Applies to SPM and SPP pins.	500	mA
		Applies to V_{DDL} and V_{DDR} pins.	50	mA
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

DGND = SPGND = 0 V

Parameter	Symbol	Condition	Range			Unit
DV_{DD}, SPV_{DD} Power supply voltage	DV_{DD} SPV_{DD}	—	2.7 to 5.5			V
Operating temperature	Top	—	−40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

FLASH Conditions

DGND = SPGND = 0 V

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +70	°C
		At read	−40 to +85	°C
Maximum rewrite count	C_{EP}	—	10	times
Data retention period	Y_{DR}	—	10	years

ELECTRICAL CHARACTERISTICS

DC Characteristics (3 V)

DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86×DV_{DD}	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	0.14×DV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = –1 mA	DV_{DD} – 0.4	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	I_{OH} = –50 µA	DV_{DD} – 0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	I_{OL} = 50 µA	—	—	0.4	V
Output leakage current(*2)	I_{OOH}	VOH = DV_{DD} (CSB="H")	—	—	10	µA
	I_{OOL}	VOL = DGND(CSB="H")	–10	—	—	µA
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*3)	I_{IH2}	V_{IH} = DV_{DD}	0.3	2.0	15	µA
"H" input current 3 (*4)	I_{IH3}	V_{IH} = DV_{DD}	2	30	200	µA
"L" input current 1	I_{IL1}	V_{IL} = DGND	–10	—	—	µA
"L" input current 2 (*3)	I_{IL2}	V_{IL} = DGND	–15	–2.0	–0.3	µA
"L" input current 3 (*5)	I_{IL3}	V_{IL} = DGND	–200	–30	–2	µA
Supply current during playback 1	I_{DD1}	f_{OSC} = 4.096 MHz fs=48kHz, f=1kHz, When 16bitPCM Playback No output load	—	—	41	mA
Supply current during playback 2	I_{DD2}	f_{OSC} = 4.096 MHz During silence playback No output load	—	—	38	mA
Power-down supply current (*6)	I_{DDS1}	Ta = –40 to +55°C	—	—	10	µA
		Ta = –40 to +85°C	—	—	20	µA
Power-down supply current (*7)	I_{DDS1}	Ta = –40 to +55°C	—	—	50	µA
		Ta = –40 to +85°C	—	—	100	µA

*1: Applies to the XTB pin.
*2: Applies to the SO and TESTO pins.
*3: Applies to the XT pin.
*4: Applies to the TESTI0 and TESTI1 pins.
*5: Applies to the RESETB, TEST2, TEST3 and TEST4 pins.
*6: Applies to the ML2256X.
*7: Applies to the ML22Q563.

DC Characteristics (5 V)

DV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8×DV_{DD}	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	0.2×DV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = –1 mA	DV_{DD}–0.4	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	I_{OH} = –50 µA	DV_{DD}–0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
Output leakage current(*2)	I_{OOH}	VOH = DV_{DD} (CSB="H")	—	—	10	µA
	I_{OOL}	VOL = DGND (CSB="H")	–10	—	—	µA
"L" output voltage 2 (*1)	V_{OL2}	I_{OL} = 50 µA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*3)	I_{IH2}	V_{IH} = DV_{DD}	0.8	5	20	µA
"H" input current 3 (*4)	I_{IH3}	V_{IH} = DV_{DD}	20	100	400	µA
"L" input current 1	I_{IL1}	V_{IL} = DGND	–10	—	—	µA
"L" input current 2 (*3)	I_{IL2}	V_{IL} = DGND	–20	–5.0	–0.8	µA
"L" input current 3 (*5)	I_{IL3}	V_{IL} = DGND	–400	–100	–20	µA
Supply current during playback 1	I_{DD1}	f_{OSC} = 4.096 MHz fs=48kHz, f=1kHz, When 16bitPCM Playback No output load	—	—	55	mA
Supply current during playback 3	I_{DD3}	f_{OSC} = 4.096 MHz During silence playback No output load	—	—	48	mA
Power-down supply current (*6)	I_{DDS1}	Ta = –40 to +55°C	—	—	10	µA
		Ta = –40 to +85°C	—	—	20	µA
Power-down supply current (*7)	I_{DDS1}	Ta = –40 to +55°C	—	—	50	µA
		Ta = –40 to +85°C	—	—	100	µA

*1: Applies to the XTB pin.
*2: Applies to the SO and TESTO pins.
*3: Applies to the XT pin.
*4: Applies to the TESTI0 and TESTI1 pins.
*5: Applies to the RESETB, TEST2, TEST3 and TEST4 pins.
*6: Applies to the ML2256X.
*7: Applies to the ML22Q563.

Analog Section Characteristics (3 V)

DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = SPGND = 0 V, Ta = −40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	Input gain: 0 dB	10	20	30	kΩ
AIN input voltage range	V_{AIN}		—	—	SPV_{DD}×2/3	Vp-p
Line output resistance	R_{LA}	At 1/2SPV_{DD} output	—	—	100	Ω
LINE output load resistance	R_{LA}	At SPGND10kΩ load	10	—	—	kΩ
LINE output voltage range	V_{AO}	At SPGND10kΩ load	SPV_{DD}/6	—	SPV_{DD}× 5/6	V
SG output voltage	V_{SG}	—	0.95×DV_{DD}/2	DV_{DD}/2	1.05×DV_{DD}/2	V
SG output resistance	R_{SG}	—	57	96	135	kΩ
SPM, SPP output load resistance	R_{LSP}	—	6	8	—	Ω
Speaker amplifier output power	P_{SPO}	SPV_{DD} = 3.3V, f = 1 kHz R_{SPO} = 8Ω, THD≦ 10%	100	300	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0 dB With a load of 8Ω	−50	—	+50	mV
Regulator output voltage	V_{DDL} V_{DDR}	Output load current = −35 mA	2.25	2.5	2.75	V

Analog Section Characteristics (5 V)

DV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

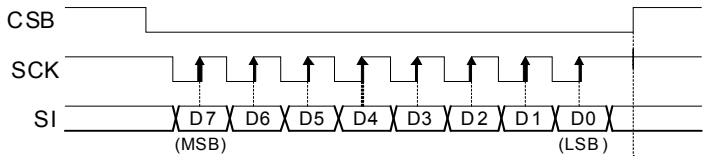
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	Input gain: 0 dB	10	20	30	kΩ
AIN input voltage range	V_{AIN}		—	—	SPV_{DD} × 2/3	Vp-p
Line output resistance	R_{LA}	At 1/2SPV_{DD} output	—	—	100	Ω
LINE output load resistance	R_{LA}	At SPGND10kΩ load	10	—	—	kΩ
LINE output voltage range	V_{AO}	At SPGND10kΩ load	SPV_{DD} /6	—	SPV_{DD} × 5/6	V
SG output voltage	V_{SG}	–	0.95x SPV_{DD} /2	SPV_{DD} /2	1.05x SPV_{DD} /2	V
SG output resistance	R_{SG}	—	57	96	135	kΩ
SPM, SPP output load resistance	R_{LSP}	—	6	8	—	Ω
Speaker amplifier output power	P_{SPO}	SPV_{DD} = 5.0V, f = 1 kHz R_{SPO} = 8Ω, THD≦ 10%	800	1000	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0 dB With a load of 8Ω	–50	—	+50	mV
Regulator output voltage	V_{DDL} V_{DDR}	Output load current = –35 mA	2.25	2.5	2.75	V

FUNCTIONAL DESCRIPTION

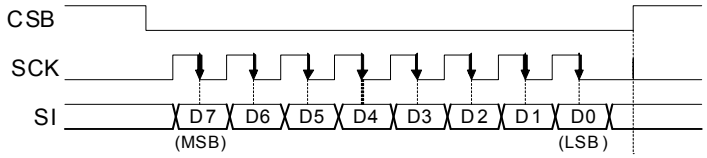
Synchronous Serial Interface

The CSB, SCK, SI, and SO pins are used to input various commands or read the status of the device.
For command input, after inputting a “L” level to the CSB pin, input data through the SI pin with MSB first in sync with the SCK clock signal. The data input through the SI pin is shifted into the LSI in sync with the SCK clock signal, then the command is executed at the eighth pulse of the rising or falling edge of the SCK clock.
For status reading, after a “L” level is input to the CSB pin, stauts is output from the SO pin in sync with the SCK clock signal.
Choosing between rising edges and falling edges of the clock pulses input through the SCK pin is determined by the signal input through the DIPH pin:
- When the DIPH pin is at a “L” level, the data input through the SI pin is shifted into the LSI on the rising edges of the SCK clock pulses and a status signal is output from the SO pin on the falling edges of the SCK clock pulses.
- When the DIPH pin is at a “H” level, the data input through the SI pin is shifted into the LSI on the falling edges of the SCK clock pulses and a status signal is output from the SO pin on the rising edges of the SCK clock pulses.
It is possible to input commands even with the CSB pin tied to a “L” level. However, if unexpected pulses caused by noise etc. are induced through the SCK pin, SCK clock pulses are incorrectly counted, causing a failure in normal input of command. In addition, the serial interface can be brought back to its initial state by driving the CSB pin at a “H” level.
When the CSB pin is at ta “L” level, the status of each channel is output serially in sync with the SCK clock. When the CSB pin is at a ”H” level, the SO pin goes into a high impedance state.

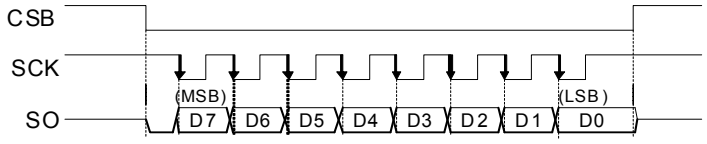
• Command Input Timing: SCK rising edge operation (when DIPH pin = “L” level)



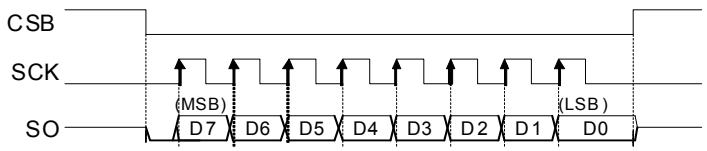
• Command Input Timing: SCK falling edge operation (when DIPH pin = “H” level)



• Command Output Timing: SCK falling edge operation (when DIPH pin = “L” level)

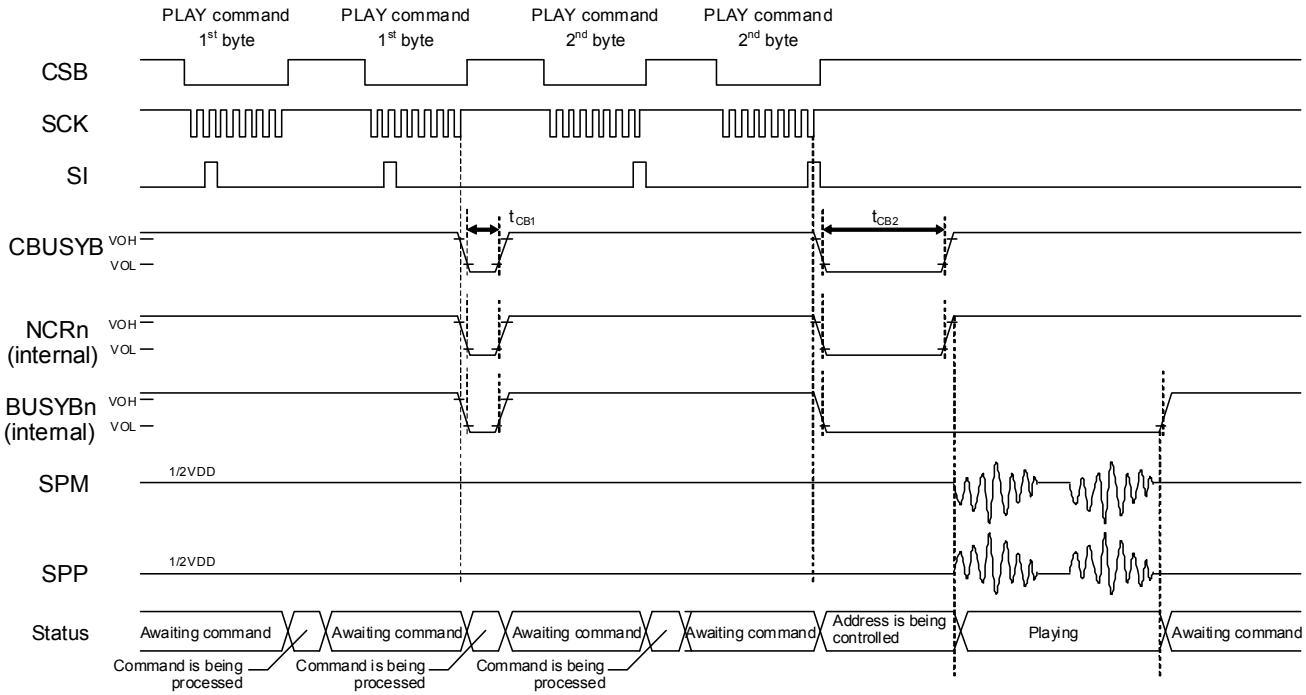


Command Output Timing: SCK rising edge operation (when DIPH pin = “H” level)



To prevent malfunction caused by serial interface pin noise, the ML22Q563/ML2256X is provided with the two-time command input mode, where the user inputs one command two times. Use the PUP command to set the two-time command input mode. For the method of setting the two-time command input mode, see the the section on "1. PUP command" described later.

In two-time command input mode, input one command two times in succession. Then, the command becomes valid only when the data input first matches the data input second. After the first data input, if a data mismatch occurs when the second data is input, a "H" level is output from the ERR pin. An error, if occurred, can be cleared by the ERCL command.



Voice Synthesis Algorithm (Common to ML22Q563 and ML2256X)

The ML22Q563/ML2256X contains four algorithm types to match the characteristic of playback voice: HQ-ADPCM algorithm, 8-bit straight PCM algorithm, 8-bit non-linear PCM algorithm, and 16-bit straight PCM algorithm.
Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Feature
HQ-ADPCM	Algorithm that enables high sound quality and high compression, which have been achieved by the improved 4-bit ADPCM that uses variable bit-length coding.
8-bit Nonlinear PCM	Algorithm that plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM	Normal 8-bit PCM algorithm
16-bit PCM	Normal 16-bit PCM algorithm

Memory Allocation and Creating Voice Data

The ROM is partitioned into four data areas: voice (i.e., phrase) control area, test area, voice area, and edit ROM area.
The voice control area manages the ROM's voice data. It contains data for controlling the start/stop addresses of voice data for 1024 phrases, use/non-use of the edit ROM function and so on.
The test area contains data for testing.
The voice area contains actual waveform data.
The edit ROM area contains data for effective use of voice data. For the details, refer to the section on "Edit ROM Function."
No edit ROM area is available unless the edit ROM is used.

The ROM data is created using a dedicated tool.

Configuration of ROM data (for ML22Q563/ML22563)

0x00000 0x01FFF	Voice control area (Fixed 64 Kbits)
0x02000 0x0206F	Test area
0x02070 max: 0x7FEBF	Voice area
max: 0x7FEBF	Edit ROM area Depends on creation of ROM data.
0x7FEC0 max: 0x7FFFF	Filter area

Playback Time and Memory Capacity

The playback time depends on the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.
The equation below gives the playback time when the edit ROM function is not used.

$$\text{Playback time} = \frac{1.024 \times (\text{Memory capacity} - 64)\ (\text{Kbits})}{\text{Sampling frequency (kHz)} \times \text{Bit length}}\ (\text{sec})$$

Example: Let the sampling frequency be 16 kHz and HQ-ADPCM algorithm. Then the playback time is approx. 80 seconds, as shown below.

$$\text{Playback time} = \frac{1.024 \times (4096 - 64)\ (\text{Kbits})}{16\ (\text{kHz}) \times 3.2\ (\text{bits})\ (\text{average})} \cong 80\ (\text{sec})$$

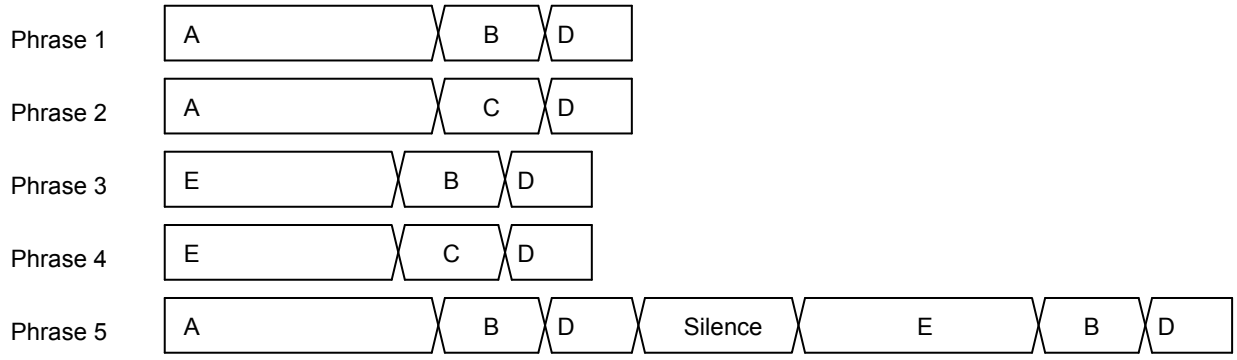
Edit ROM Function

With the edit ROM function, multiple phrases can be played in succession. The following functions can be configured using the edit ROM function:

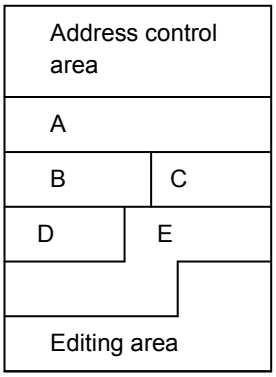
・Continuous playback: There is no limit to the continuous playback count that can be specified. It depends on the memory capacity only.
・Silence insertion: 20 to 1024 ms

Using the edit ROM function enables an effective use of the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the edit ROM function.

Examples of Phrases Using the Edit ROM Function



Example of ROM Data Where the Contents Above Are Stored in ROM



Mixing Function

The ML22Q563/ML2256X can perform simultaneous mixing of four channels. It is possible to specify FADR, PLAY, STOP, and CVOL for each channel separately.

• Precautions for Waveform Clamp at the Time of Channel Mixing
If channel mixing is done, the possibility of an occurrence of a clamp increases from the mixing calculation point of view. If it is known beforehand that a clamp will occur, then adjust the sound volume of each channel using the VOL command.

• Mixing of Different Sampling Frequency
It is not possible to perform channel mixing by a different sampling frequency group.
When performing channel mixing, the sampling frequency group of the first playback channel is selected. Therefore, note that if channel mixing is performed by a sampling frequency group other than the selected sampling frequency group, then the playback will not be of constant speed: some times faster and at other times slower.
The available sampling groups for channel mixing by a different sampling frequency are listed below.
8.0 kHz, 16.0 Hz, 32.0 kHz … (Group 1)
12.0 kHz, 24.0 kHz, 48 kHz … (Group 2)
6.4 kHz, 12.8 kHz, 25.6 kHz … (Group 3)

Figures below show cases where a phrase is played at a sampling frequency belonging to a different sampling frequency group.

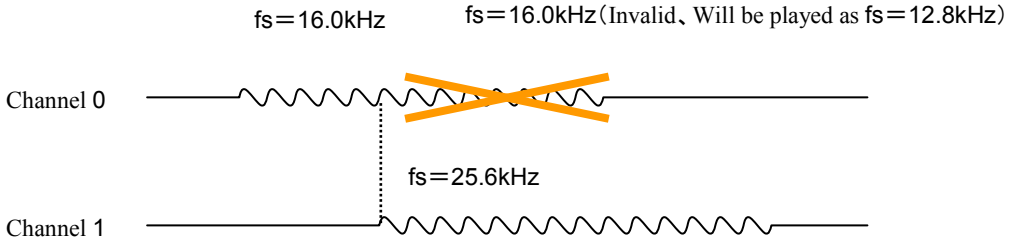


Figure 1 Case where a phrase is played at a sampling frequency belonging to a different sampling frequency group during playback on channels 0 and 1

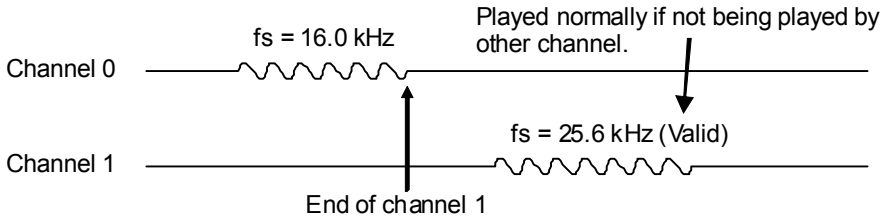


Figure 2 Case where a phrase is played at a sampling frequency belonging to a different sampling frequency group after playback is finished at the other channel

Command List

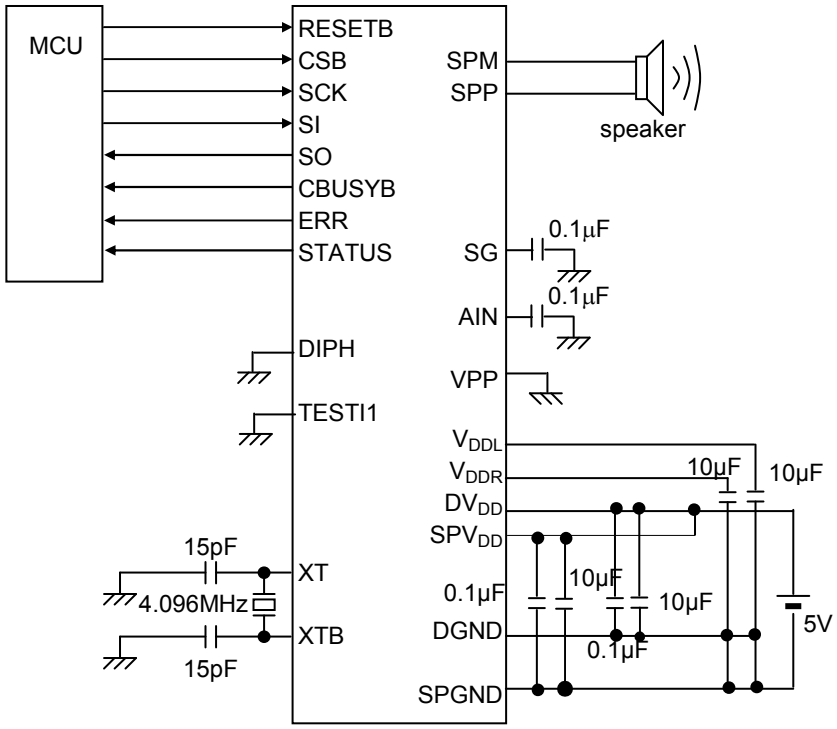
Each command is configured in 1-byte (8-bit) units. Each of the AMODE, AVOL FADR, PLAY, MUON, and CVOL commands forms one command by two bytes. Be sure to input the following commands only.
Input each command with CBUSYB set to a "H" level.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP	0	0	0	0	0	0	0	WCM	Shifts the device currently powered down to a command wait state. Also the two-time command input mode is set by this command.
AMODE	0	0	0	0	0	1	HPF1	HPF0	Analog section control command. Configures settings for power-up operation and analog input/output. Selects the type of HPF.
	0	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	POP	
AVOL	0	0	0	0	1	0	0	0	Analog mixing signal volume setting command. Use the data of the 2nd byte to specify volume.
	—	—	AV5	AV4	AV3	AV2	AV1	AV0	
FAD	0	0	0	0	1	1	0	0	Sets the fade-in time in cases where the speaker amplifier is enabled by the AMODE command.
	0	0	0	0	FAD3	FAD2	FAD1	FAD0	
PDWN	0	0	1	0	0	0	0	0	Shifts the device from a command wait state to a power-down state.
FADR	0	0	1	1	0	C0	F9	F8	Playback phrase specification command. Can be specified for each channel.
	F7	F6	F5	F4	F3	F2	F1	F0	
PLAY	0	1	0	0	0	C0	F9	F8	Playback start command. Use the data of the 2nd byte to specify a phrase number. Can be specified for each channel.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	0	0	CH1	CH0	Playback start command without phrase specification. Used to start playback on multiple channels at the same time after phrases are specified with the FADR command. After a phrase is played with the PLAY command, the same phrase can be played with this command.
STOP	0	1	1	0	0	0	CH1	CH0	Playback stop command. Can be specified for each channel.

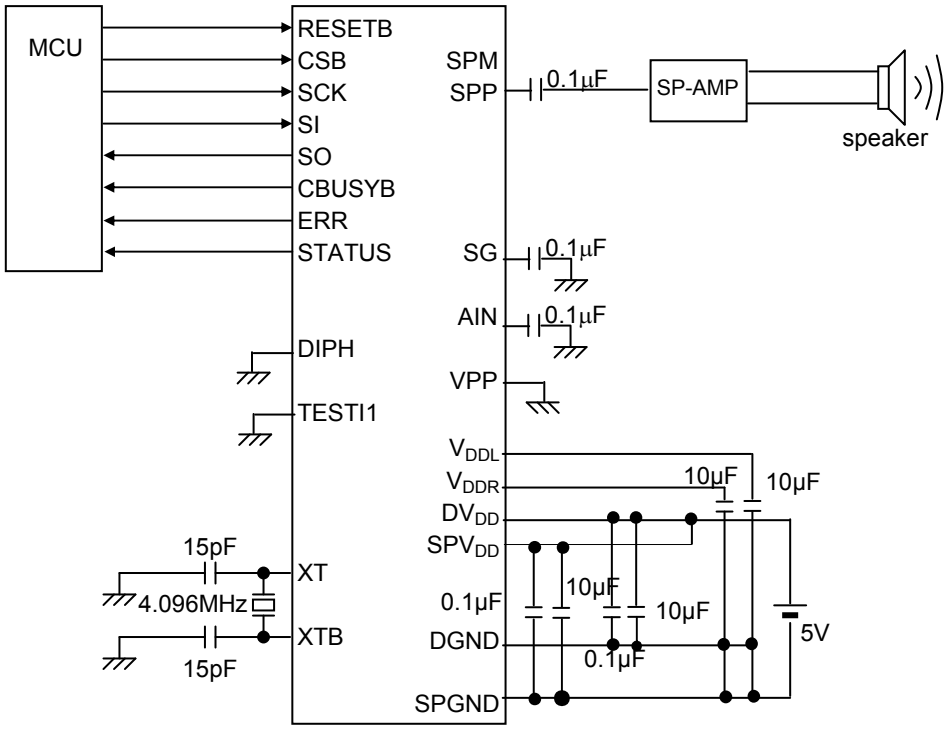
Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
MUON	0	1	1	1	0	0	CH1	CH0	Silence insertion command. Use the data of the 2nd byte to specify the length of silence. Can be specified for each channel.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	0	0	CH1	CH0	Repeat playback mode setting command. The setting is enabled during playback. Can be specified for each channel.
CLOOP	1	0	0	1	0	0	CH1	CH0	Repeat playback mode release command. When the STOP command is input, repeat playback mode is released automatically. Can be specified for each channel.
CVOL	1	0	1	0	0	0	CH1	CH0	Volume setting command. Use the data of the 2nd byte to specify volume. Can be specified for each channel.
	—	—	—	CV4	CV3	CV2	CV1	CV0	
RDSTAT	1	0	1	1	0	0	0	ERR	Status serial read command. This command reads the command status and the status of the fail safe function for each channel.
OUTSTAT	1	1	0	0	0	BUSY/NCR	0	C0	Status output command. This command outputs the command status of each channel from the STATUS pin.
SAFE	1	1	0	1	0	0	0	0	Fail safe setting command. Sets settings for power supply voltage detection, temperature detection, and monitoring time.
	TM2	TM1	TM0	TSD1	TSD0	BLD2	BLD1	BLD0	
ERCL	1	1	1	1	1	1	1	1	This command clears error while the fail safe function is operating.

APPLICATION CIRCUIT

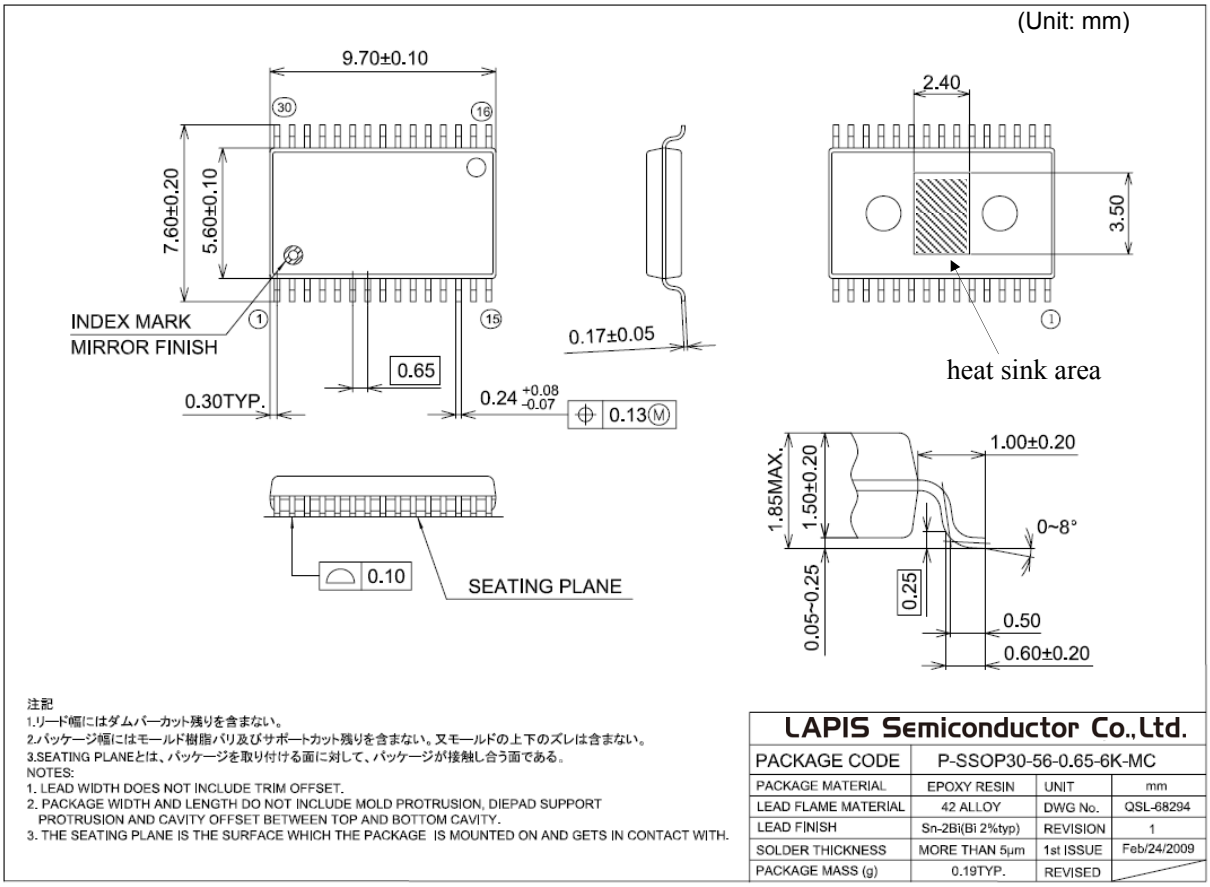
At using internal speaker amplifier (speaker output) (VDDR is only ML22Q563)



At using external speaker amplifier (line output) (VDDR is only ML22Q563)



PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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