ML9286-xx

Vacuum fluorescent display tube controller driver

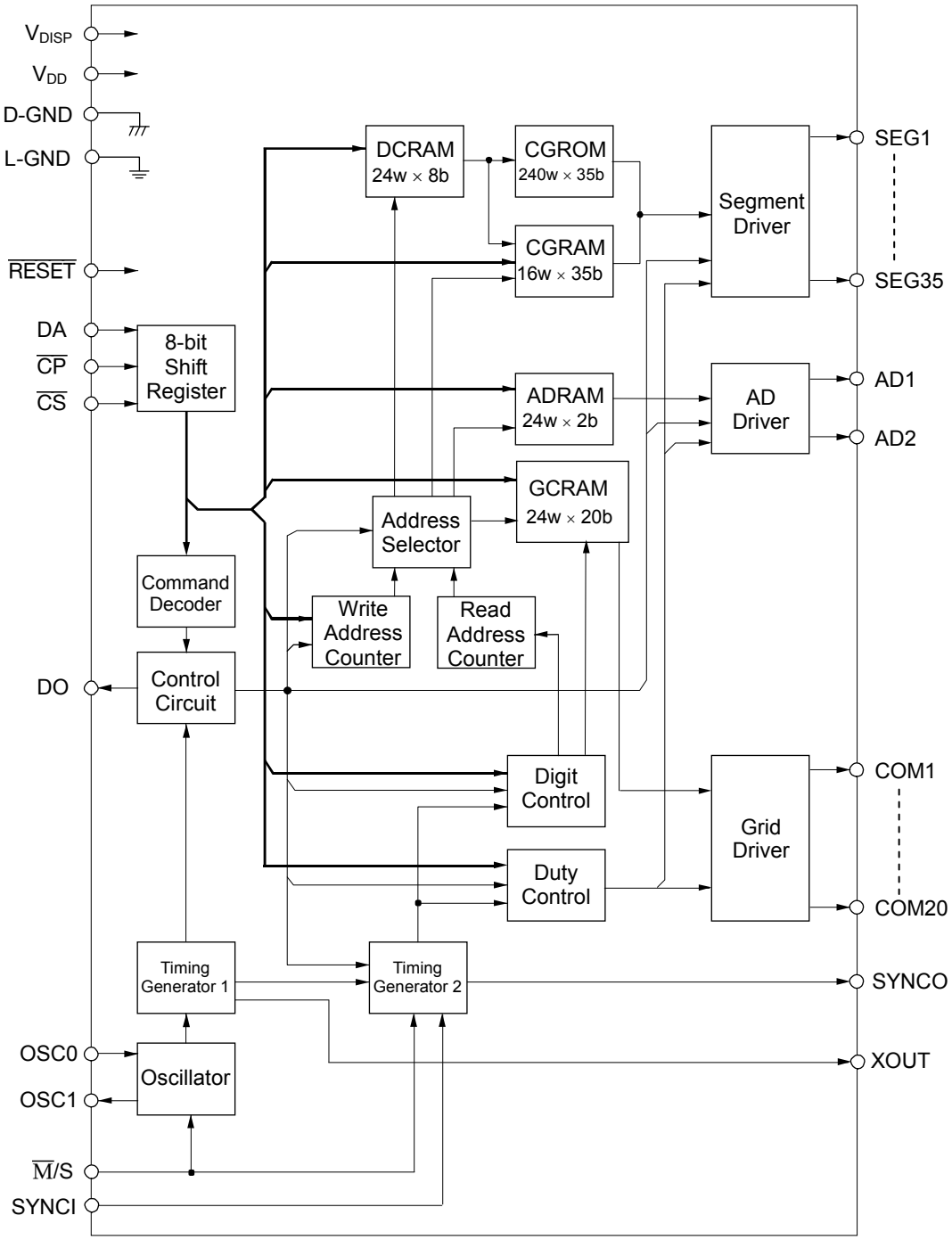
GENERAL DESCRIPTION

The ML9286-xx is a 5 × 7 dot matrix type vacuum fluorescent display (VFD) tube controller driver IC which displays characters, numerics and symbols of a maximum of 20digits × 1 line.
Dot matrix VFD tube drive signals are generated by serial data sent from a micro-controller. A display system is easily realized by internal ROM and RAM for character display.

FEATURES

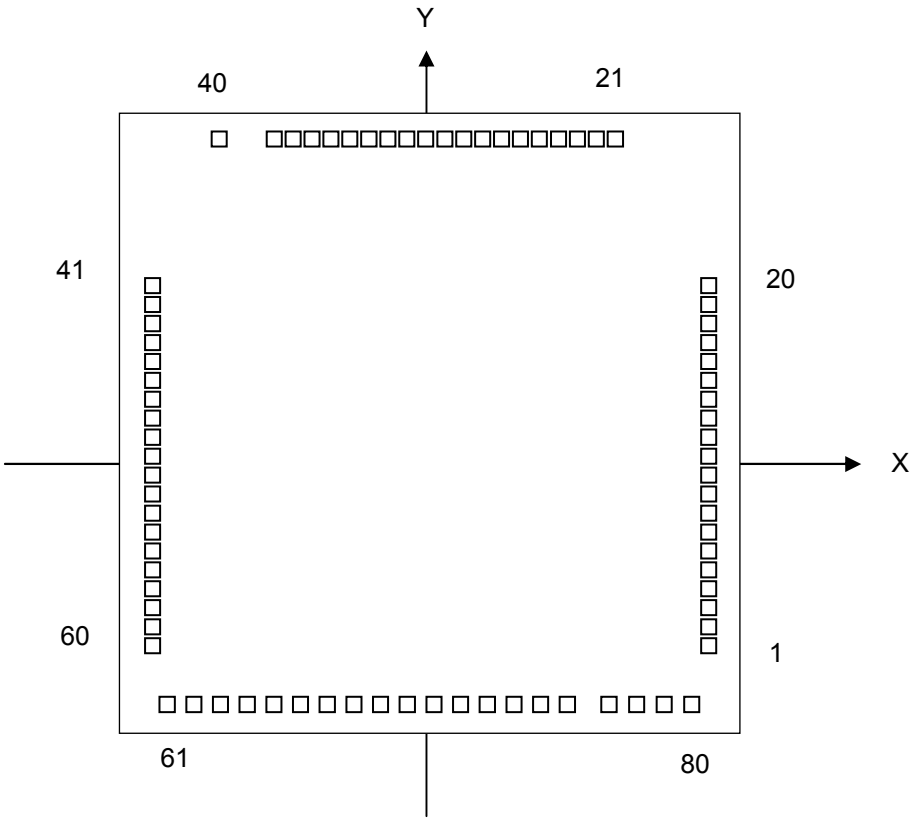
- Logic power supply (V_{DD}) : 3.0V to 3.6V or 4.5V to 5.5V
- VFD tube drive power supply (V_{DISP}) : 20V to 80V
- VFD driver output current
  (VFD driver output can be connected directly to the VFD tube. No pull-down resistor is required.)
  - Segment driver (SEG1 to SEG35) : –5 mA (V_{DISP} = 80 V)
  - Segment driver (AD1 to AD2) : –10 mA (V_{DISP} = 80 V)
  - Grid driver (COM1 to COM20) : –30 mA (V_{DISP} = 80 V)
- Content of display
  - CGROM : 5 × 7 dots 240 types (character data)
  - CGRAM : 5 × 7 dots 16 types (character data)
  - ADRAM : 24 (display timing) × 2 bits (symbol data)
  - DCRAM : 24 (display timing) × 8 bits (register for character data display)
- Display control function
  - Display digit : 9 to 20 digits
  - GCRAM (Grid control RAM) : The display timing from T9 to T24 can be set.
    Built-in multi grid function
  - Display duty (brightness adjustment) : 256 stages
  - All lights ON/OFF
- 4 interfaces with micro-controller : DA, $\overline{CS}$, $\overline{CP}$, $\overline{RESET}$
- 1-byte instruction execution (excluding data write to RAM and Display duty set)
- Built-in oscillation circuit
- Crystal oscillation or ceramic oscillation
- Package options
  AL-Pad Chip (ML9286-xxWA)
  80-pin plastic TQFP (TQFP80-P-1212-0.50-K) (ML9286-xxTB)

BLOCK DIAGRAM



PIN CONFIGURATION

PAD LAYOUT

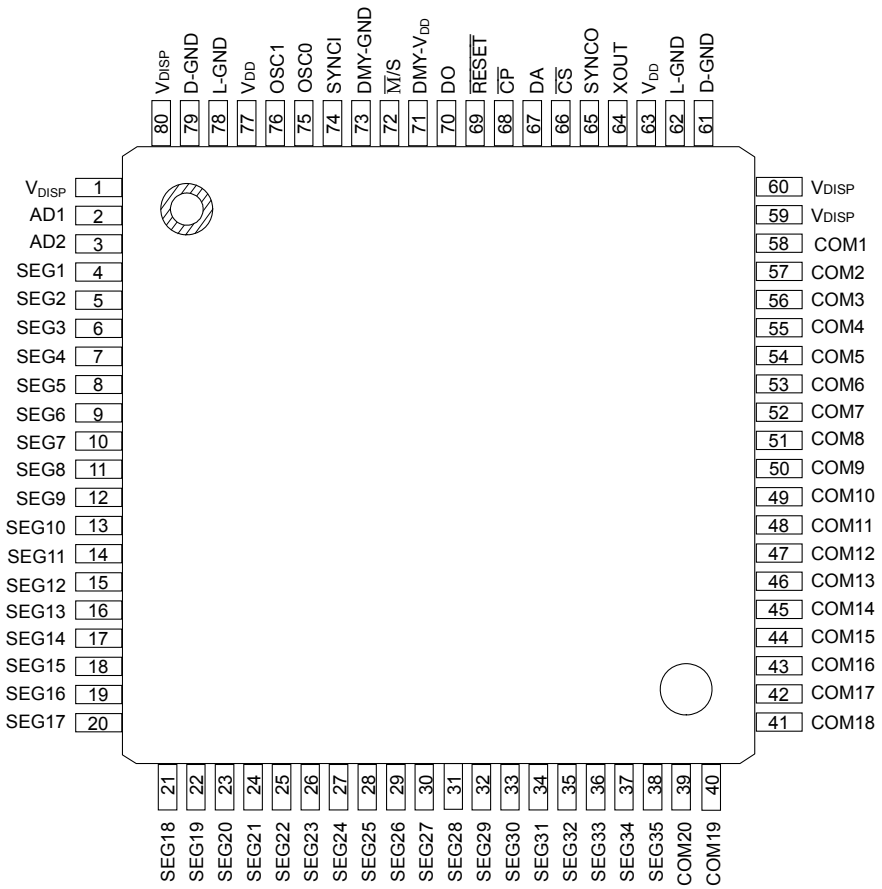


Chip Size : X : 3.79 mm × Y : 3.89 mm
Chip Thickness : 280 µm
PAD Size : 90µm × 90µm(Metal) 80µm × 80µm(PV Pad hole)

PAD COORDINATES

PAD No	PAD Name	X [µm]	Y [µm]	PAD No	PAD Name	X [µm]	Y [µm]
1	V_{DISP}	1760	-1347	41	COM18	-1760	743
2	AD1	1760	-1237	42	COM17	-1760	633
3	AD2	1760	-1127	43	COM16	-1760	523
4	SEG1	1760	-1017	44	COM15	-1760	413
5	SEG2	1760	-907	45	COM14	-1760	303
6	SEG3	1760	-797	46	COM13	-1760	193
7	SEG4	1760	-687	47	COM12	-1760	83
8	SEG5	1760	-577	48	COM11	-1760	-27
9	SEG6	1760	-467	49	COM10	-1760	-137
10	SEG7	1760	-357	50	COM9	-1760	-247
11	SEG8	1760	-247	51	COM8	-1760	-357
12	SEG9	1760	-137	52	COM7	-1760	-467
13	SEG10	1760	-27	53	COM6	-1760	-577
14	SEG11	1760	83	54	COM5	-1760	-687
15	SEG12	1760	193	55	COM4	-1760	-797
16	SEG13	1760	303	56	COM3	-1760	-907
17	SEG14	1760	413	57	COM2	-1760	-1017
18	SEG15	1760	523	58	COM1	-1760	-1127
19	SEG16	1760	633	59	V_{DISP}	-1760	-1237
20	SEG17	1760	743	60	V_{DISP}	-1760	-1347
21	SEG18	1063	1810	61	D-GND	-1553	-1810
22	SEG19	953	1810	62	L-GND	-1381	-1810
23	SEG20	843	1810	63	V_{DD}	-1211	-1810
24	SEG21	733	1810	64	XOUT	-1061	-1810
25	SEG22	623	1810	65	SYNCO	-931	-1810
26	SEG23	513	1810	66	$\overline{CS}$	-776	-1810
27	SEG24	403	1810	67	DA	-602	-1810
28	SEG25	293	1810	68	$\overline{CP}$	-428	-1810
29	SEG26	183	1810	69	$\overline{RESET}$	-254	-1810
30	SEG27	73	1810	70	DO	-105	-1810
31	SEG28	-37	1810	71	DMY-VDD	25	-1810
32	SEG29	-147	1810	72	$\overline{M}$/S	180	-1810
33	SEG30	-257	1810	73	DMY-GND	319	-1810
34	SEG31	-367	1810	74	SYNCI	464	-1810
35	SEG32	-477	1810	75	OSC0	641	-1810
36	SEG33	-587	1810	76	OSC1	886	-1810
37	SEG34	-697	1810	77	V_{DD}	1060	-1810
38	SEG35	-807	1810	78	L-GND	1230	-1810
39	COM20	-943	1810	79	D-GND	1402	-1810
40	COM19	-1273	1810	80	V_{DISP}	1589	-1810

PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic TQFP

PIN DESCRIPTION

PAD No	Symbol	Type	Connects to	Description
4～38	SEG1 to 35	O	VFD tube anode electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –5.0 mA
39～58	COM1 to 20	O	VFD tube grid electrode	Fluorescent display tube grid electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –30.0 mA
2, 3	AD1, AD2	O	VFD tube anode electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH} > –10.0 mA
63,77	V_{DD}	—	Power supply	Power supply pin for internal logic.
1, 59, 60,80	V_{DISP}	—	Power supply	Power supply pin for driving fluorescent tubes.
61, 79	D-GND	—	Power supply	D-GND pin for driver circuits of a VFD tube. Connect this pin to the external L-GND.
62, 78	L-GND	—	Power supply	L-GND pin for logic circuits. Connect this pin to the external D-GND.
67	DA	I	Micro controller	Serial data input. (Built-in Schmitt Circuit) Input from LSB. (positive logic)
68	$\overline{CP}$	I	Micro controller	Shift clock input. (Built-in Schmitt Circuit) Serial data is shifted on the rising edge of $\overline{CP}$.
66	$\overline{CS}$	I	Micro controller	Chip select input. (Built-in Schmitt Circuit) Serial data transfer is disabled when $\overline{CS}$ pin is "H" level.
69	$\overline{RESET}$	I	Micro controller	Reset input. (Built-in Schmitt Circuit)"Low" initializes all the functions. For initial status see Reset Function.
75	OSC0	I	Crystal or ceramic resonator	Pins for self-oscillation. Connect these pins to the crystal and capacitors or to the ceramic resonator and capacitors. The target oscillation frequency is 4.0 MHz. (Note that the device includes the feed back resistor. See Application Circuit.)
76	OSC1	O		
70	DO	O	—	Serial data output pin for test mode. (positive logic) Do not use in normal operation. (DO outputs “L” level in normal operation.)
64	XOUT	O	Cascade connection	Generate output 1/4 clock for OSC0. The main usage is to connect this pin to the OSC0 pin of the adjacent IC when the ML9286 is cascaded.
65	SYNCO	O	Cascade connection	Frame sync signal output pin. A synchronous pulse is output from this pin immediately before the start of the frame.
74	SYNCI	I	Cascade connection	Frame sync signal input pin. A synchronous pulse is input from this pin immediately before the start of the frame.
72	$\overline{M}$/S	—	Cascade connection	This pin is used for setting the master or salve. When $\overline{M}$/S = Low, the ML9286 is master mode. When $\overline{M}$/S = High, the ML9286 is slave mode.
73	DMY-GND	O	—	The output pin to fix the adjacent input pin to the GND level. Use this pin only for this purpose.
71	DMY-V_{DD}	O	—	The output pin to fix the adjacent input pin to the V_{DD} level. Use this pin only for this purpose.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	—	–0.3 to +6.5	V
Supply Voltage (2)	V_{DISP}	—	–0.3 to +85	V
Input Voltage	V_{IN}	—	–0.3 to V_{DD}+0.3	V
Operating Temperature	Tj	—	–40 to +125	°C
Output Current	I_{O1}	COM1 to COM20	–40.0 to 2.0	mA
	I_{O2}	AD1, AD2	–20.0 to 2.0	
	I_{O3}	SEG1 to SEG35	–10.0 to 2.0	
	I_{O4}	DO	–2.0 to 2.0	
Power Dissipation	P_D	Ta ≥ 25°C 80-pin plastic TQFP	400	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

GND = 0 V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	3.3V unit power supply used	3.0	3.3	3.6	V
		5.0V unit power supply used	4.5	5.0	5.5	V
Supply Voltage (2)	V_{DISP}	—	20	—	80	V
$\overline{CP}$ Frequency	f_C	—	—	—	2.0	MHz
Oscillation Frequency	f_{OSC}	Self-oscillation	3.5	4.0	4.5	MHz
Frame Frequency	f_{FR}	DIGIT = 1 to 20, Self-oscillation	171	195	220	Hz
Operating Temperature	T_j	AL-Pad Chip	–40	—	+125	°C
	Ta	80-pin plastic TQFP	–40	—	+105	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 3.0 to 3.6V or 4.5 to 5.5V, V_{DISP} = 20 to 80 V, Ta = –40 to +105°C)

Parameter	Symbol	Applied pin	Condition	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	*1	V_{DD}= 3.0 to 3.6 V	0.8 V_{DD}	—	—	V
			V_{DD}= 4.5 to 5.5 V	0.7 V_{DD}	—	—	
Low Level Input Voltage	V_{IL}	*1	V_{DD}= 3.0 to 3.6 V	—	—	0.2 V_{DD}	V
			V_{DD}= 4.5 to 5.5 V	—	—	0.3 V_{DD}	
High Level Input Current	I_{IH}	*1	V_{IN} = V_{DD}	–2.0	—	+2.0	μA
Low Level Input Current	I_{IL}	*1	V_{IN} = 0 V	–2.0	—	+2.0	μA
High Level Output Voltage	V_{OH1}	COM1 to 20	V_{DISP} = 80 V, I_{OH1} = –30 mA	V_{DISP} –4.0	—	—	V
	V_{OH2}	AD1, AD2	V_{DISP} = 80 V, I_{OH2} = –10 mA	V_{DISP} –4.0	—	—	V
	V_{OH3}	SEG1 to 35	V_{DISP} = 80 V, I_{OH3} = –5 mA	V_{DISP} –4.0	—	—	V
	V_{OH4}	DO,XOUT, SYNCO	I_{OH4} = –400 μA	V_{DD} –0.3	—	—	V
Low Level Output Voltage	V_{OL1}	*2	V_{DISP} = 80 V,I_{OL1} = 1 mA	—	—	1.0	V
	V_{OL2}	DO,XOUT, SYNCO	I_{OL2} = 400 μA	—	—	0.3	V
Current Consumption (1)	I_{DD1}	V_{DD}	V_{DD} = 3.6V,f_{OSC} = 4.0MHz, no load, Duty=240/256, Digit =1 to 20, All lights ON mode	—	—	3	mA
		V_{DISP}		—	—	2	
	I_{DD2}	V_{DD}	V_{DD} = 3.6V,f_{OSC} = 4.0MHz, no load, Duty=0/256, Digit =1 to 9, All lights OFF mode	—	—	3	mA
		V_{DISP}		—	—	1	
	I_{DD3}	V_{DD}	V_{DD} = 5.5V,f_{OSC} = 4.0MHz, no load, Duty=240/256, Digit =1 to 20, All lights ON mode	—	—	4	mA
		V_{DISP}		—	—	2	
	I_{DD4}	V_{DD}	V_{DD} = 5.5V,f_{OSC} = 4.0MHz, no load, Duty=0/256, Digit =1 to9, All lights OFF mode	—	—	4	mA
		V_{DISP}		—	—	1	
Current Consumption (2)	I_{DDS}	V_{DD}	No clock supply. Ta=85°C Tj=85°C	—	—	20	μA
	I_{DISPS}	V_{DISP}		—	—	20	μA

*1) $\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$,SYNCI
*2) COM1 to 20, SEG1 to 35, AD1, AD2

AC Characteristics

(V_{DD} = 3.0 to 3.6V or 4.5 to 5.5V, V_{DISP} = 20 to 80 V, Ta = –40 to +105°C)

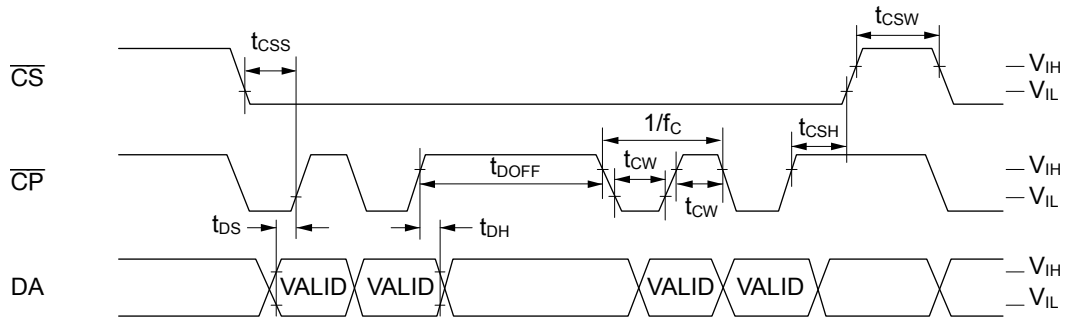
Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	2.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		200	—	ns
DA Setup Time	t_{DS}	—		200	—	ns
DA Hold Time	t_{DH}	—		200	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		250	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	Self-oscillation		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		350	—	ns
Data Processing Time	t_{DOFF}	Self-oscillation		8	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input from microcontroller, etc. externally		350	—	ns
$\overline{RESET}$ Time	t_{RSON}	—		t_{OSCON}	—	ns
DA Wait Time	t_{RSOFF}	—		250	—	ns
All Output Slew Rate	t_R	C_I = 100 pF	t_R = 20% to 80%	—	2.0	µs
	t_F		t_F = 80% to 20%	—	2.0	µs
Oscillation Start-up time	t_{OSCON}	—		*1		

*1 t_{OSCON} depends on the type of crystal or resonator.
Refer to characteristic data of crystal or resonator used.

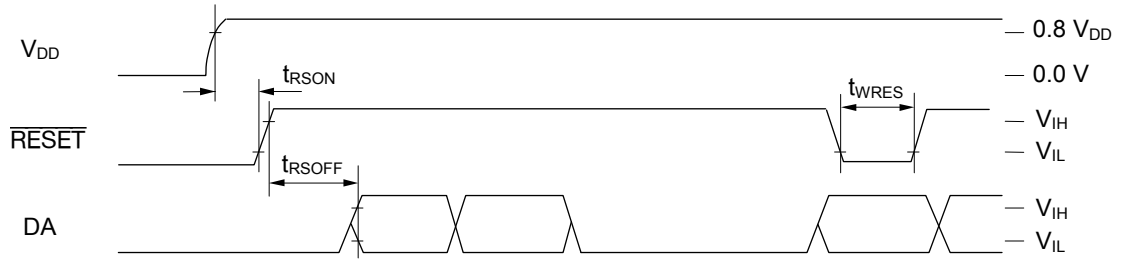
Timing Diagram

Symbol	V_{DD} = 3.0 to 3.6V	V_{DD} = 4.5V to 5.5V
V_{IH}	0.8 V_{DD}	0.7 V_{DD}
V_{IL}	0.2 V_{DD}	0.3 V_{DD}

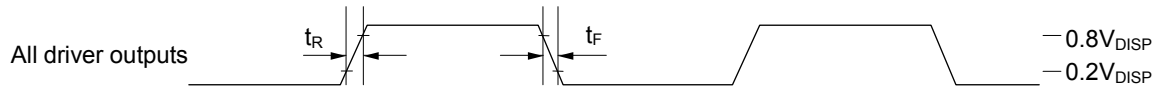
Data Timing



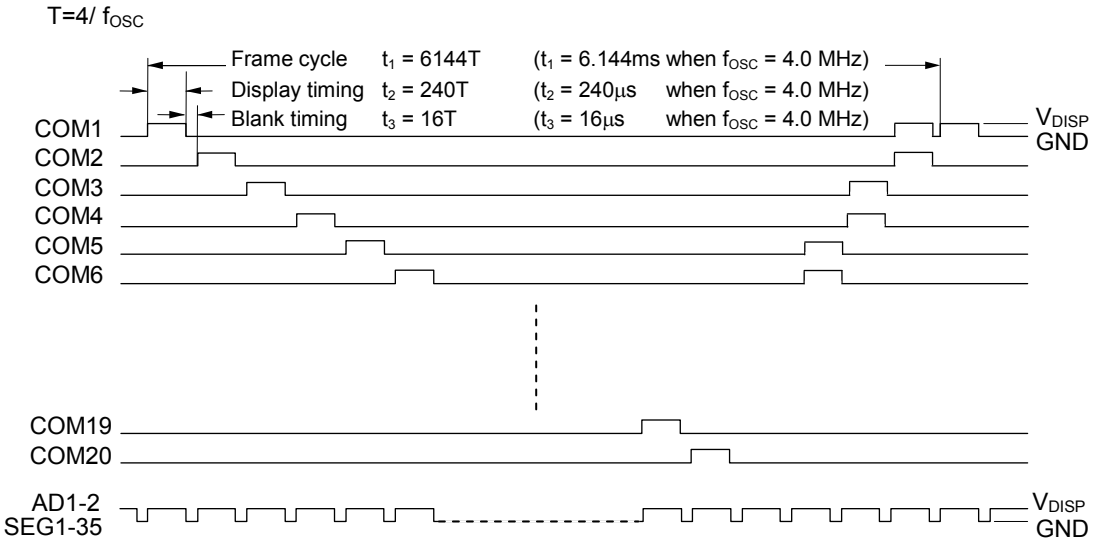
Reset Timing



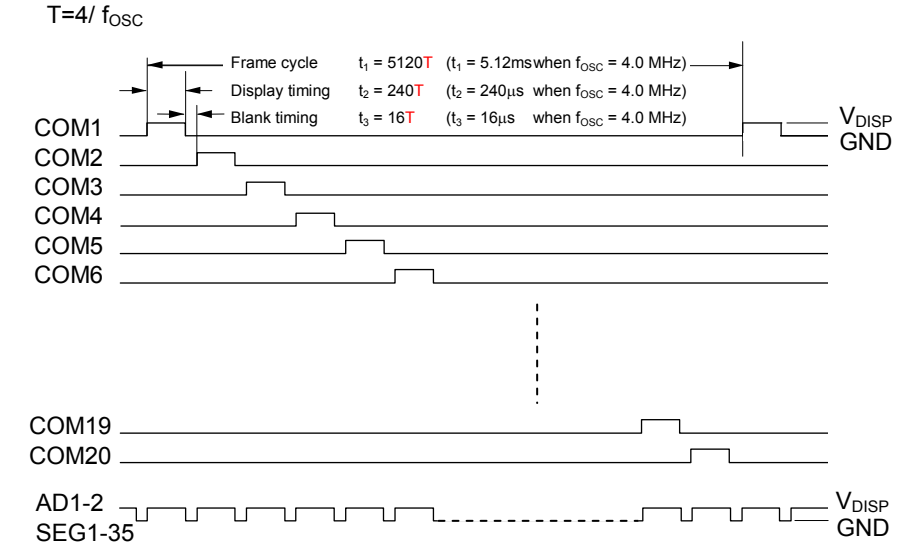
Output Timing



Digit Output Timing (for T24 timing set, at a duty of 240/256)



Digit Output Timing (for T20 timing set, at a duty of 240/256)



FUNCTIONAL DESCRIPTION

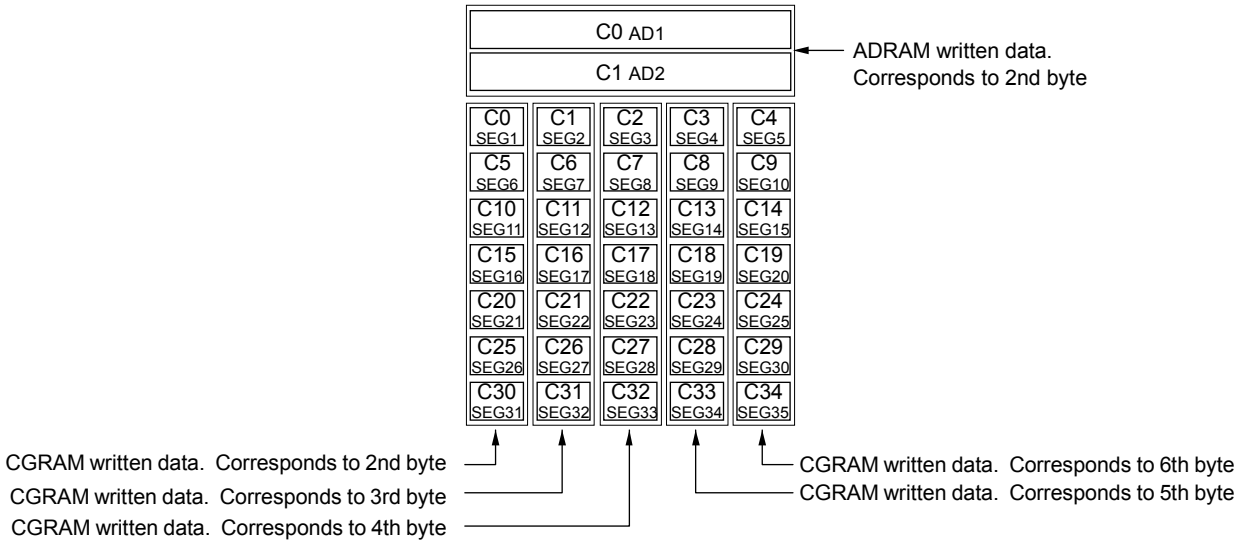
Commands List

No	Command	LSB			1st byte				MSB	LSB			2nd byte				MSB
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
1	DCRAM data write	X0	X1	X2	X3	X4	1	0	0	C0	C1	C2	C3	C4	C5	C6	C7
2	CGRAM data write	X0	X1	X2	X3	*	0	1	0	C0	C5	C10	C15	C20	C25	C30	*
										C1	C6	C11	C16	C21	C26	C31	*
										C2	C7	C12	C17	C22	C27	C32	*
										C3	C8	C13	C18	C23	C28	C33	*
										C4	C9	C14	C19	C24	C29	C34	*
3	ADRAM data write	X0	X1	X2	X3	X4	1	1	0	C0	C1	*	*	*	*	*	*
4	GCRAM data write	*	*	*	*	*	0	0	1	C0	C1	C2	C3	C4	C5	C6	C7
										C8	C9	C10	C11	C12	C13	C14	C15
										C16	C17	C18	C19	*	*	*	*
5	Display duty set	*	*	*	*	*	1	0	1	D0	D1	D2	D3	D4	D5	D6	D7
6	Number of timing set	K0	K1	K2	K3	*	0	1	1								
7	All lights ON/OFF	L	H	*	*	*	1	1	1								
8	Test mode	T0	T1	T2	T3	1	0	0	0								

* : Don't care
Xn : Address specification for each RAM
Cn : Character code specification for each RAM
Dn : Display duty specification
Kn : Number of display timing specification
H : All lights ON instruction
L : All lights OFF instruction
Tn : Test mode specification

Note 1: When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically. Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.
Note 2: The test mode is used for inspection before shipment. It is not a user function.

Positional Relationship Between SEGn and ADn (one digit)

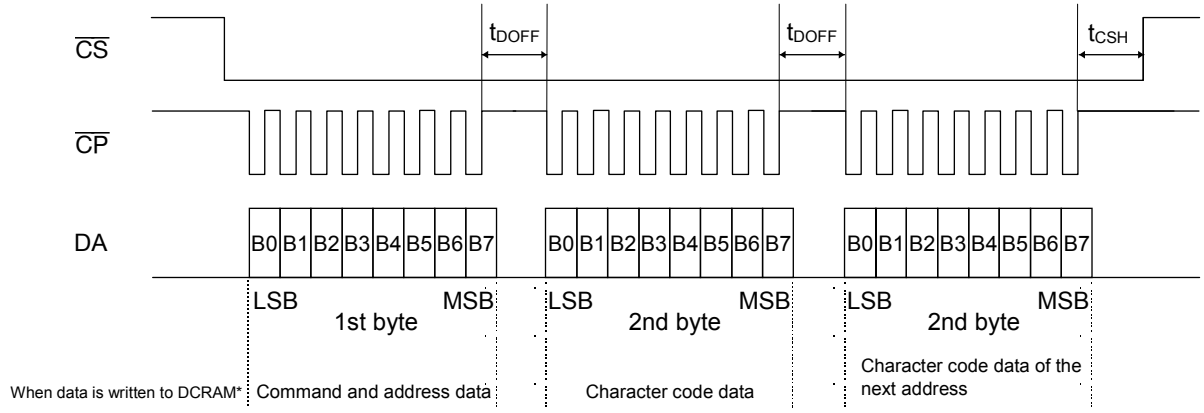


Data Transfer Method and Command Write Method

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the $\overline{CS}$ pin to "Low" level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the $\overline{CP}$ pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the $\overline{CS}$ pin to "High" disables data transfer. Data input from the point when the $\overline{CS}$ pin changes from "High" to "Low" is recognized in 8-bit units.



* When data is written to RAM (DCRAM, ADRAM, CGRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Reset Function

Reset is executed when the $\overline{RESET}$ pin is set to "L", (when turning power on, for example) and initializes all functions.
Initial status is as follows:

- Address of each RAM ..... address "00"H
- Data of each RAM ..... All contents are undefined
- Display timing ..... T1 to T24
- Brightness adjustment..... 0/256
- All display lights ON or OFF ..... OFF mode
- Segment output ..... All segment outputs (SEG1 to SEG35) go "Low"
- Common output ..... All common outputs (COM1 to COM20) go "Low"
- AD output ..... All AD outputs (AD1 and AD2) go "Low"

Please set the functions again according to "Setting Flowchart" after reset.

DESCRIPTION OF COMMANDS AND FUNCTIONS

1. DCRAM data write

(Specifies the addresses 00H to 1FH of DCRAM and writes the character codes of CGROM and CGRAM.)

DCRAM (Data Control RAM) has a 5-bit address to store the character codes of CGROM and CGRAM.
The character code specified by DCRAM is converted to a 5 × 7 dot matrix character pattern via CGROM or CGRAM.
(The DCRAM can store 24 timing.)

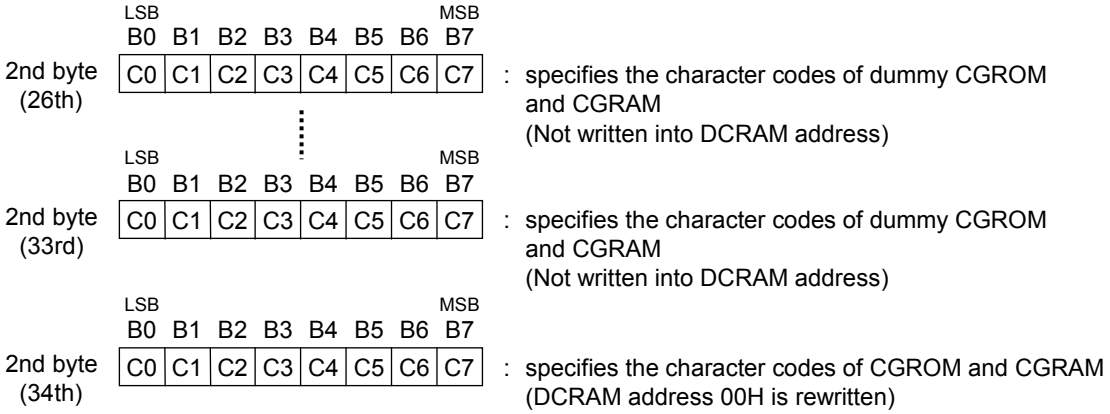
[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
1st byte (1st)	X0	X1	X2	X3	X4	1	0	0	:	selects DCRAM data write mode and specifies DCRAM address (Ex: Specifies DCRAM address 00H.)
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	:	specifies the character codes of CGROM and CGRAM (written into DCRAM address 00H)

To specify the character code of CGROM and CGRAM continuously to the next address, specify only character codes as follows.
The addresses of DCRAM are automatically incremented. Specification of an address is unnecessary.

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
2nd byte (3rd)	C0	C1	C2	C3	C4	C5	C6	C7	:	specifies the character codes of CGROM and CGRAM (written into DCRAM address 01H)
2nd byte (4th)	C0	C1	C2	C3	C4	C5	C6	C7	:	specifies the character codes of CGROM and CGRAM (written into DCRAM address 02H)
⋮										
2nd byte (25th)	C0	C1	C2	C3	C4	C5	C6	C7	:	specifies the character codes of CGROM and CGRAM (written into DCRAM address 17H)

After the character code setting up to 24 timing is completed, to set a character code from DCRAM address 00H continuously, set a dummy character code to DCRAM addresses between 18H and 1FH.
(DCRAM address is incremented automatically up to 1FH and after return to 00H)



X0 (LSB) to X4 (MSB): DCRAM addresses (5 bits: 24 timing)
C0 (LSB) to C7 (MSB): Character codes of CGROM and CGRAM (8 bits: 256 characters)

[Timing setting positions and set DCRAM addresses]

HEX	X0	X1	X2	X3	X4	Timing setting	HEX	X0	X1	X2	X3	X4	Timing setting
00	0	0	0	0	0	T1	10	0	0	0	0	1	T17
01	1	0	0	0	0	T2	11	1	0	0	0	1	T18
02	0	1	0	0	0	T3	12	0	1	0	0	1	T19
03	1	1	0	0	0	T4	13	1	1	0	0	1	T20
04	0	0	1	0	0	T5	14	0	0	1	0	1	T21
05	1	0	1	0	0	T6	15	1	0	1	0	1	T22
06	0	1	1	0	0	T7	16	0	1	1	0	1	T23
07	1	1	1	0	0	T8	17	1	1	1	0	1	T24
08	0	0	0	1	0	T9	18	0	0	0	1	1	—
09	1	0	0	1	0	T10	19	1	0	0	1	1	—
0A	0	1	0	1	0	T11	1A	0	1	0	1	1	—
0B	1	1	0	1	0	T12	1B	1	1	0	1	1	—
0C	0	0	1	1	0	T13	1C	0	0	1	1	1	—
0D	1	0	1	1	0	T14	1D	1	0	1	1	1	—
0E	0	1	1	1	0	T15	1E	0	1	1	1	1	—
0F	1	1	1	1	0	T16	1F	1	1	1	1	1	—

2. CGRAM data write

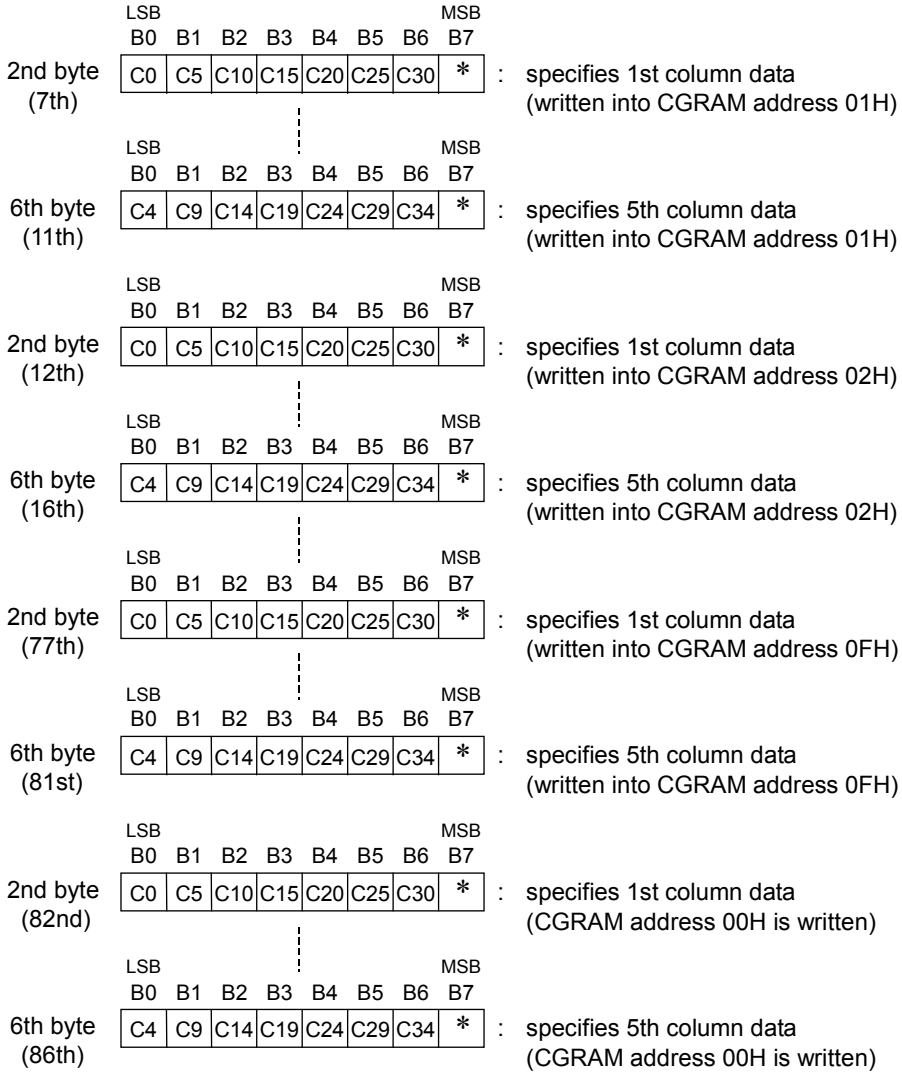
(Specifies the addresses of CGRAM and writes character pattern data.)

CGRAM (Character Generator RAM) has a 4-bit address to store 5 × 7 dot matrix character patterns.
A character pattern stored in CGRAM can be displayed by specifying the character code (address) by DCRAM.
The address of CGRAM is assigned to 00H to 0FH. (All the other addresses are the CGROM addresses.)
(The CGRAM can store 16 types of character patterns.)

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
1st byte (1st)	X0	X1	X2	X3	*	0	1	0	:	selects CGRAM data write mode and specifies CGRAM address. (Ex: Specifies CGRAM address 00H.)
2nd byte (2nd)	C0	C5	C10	C15	C20	C25	C30	*	:	specifies 1st column data (written into CGRAM address 00H)
3rd byte (3rd)	C1	C6	C11	C16	C21	C26	C31	*	:	specifies 2nd column data (written into CGRAM address 00H)
4th byte (4th)	C2	C7	C12	C17	C22	C27	C32	*	:	specifies 3rd column data (written into CGRAM address 00H)
5th byte (5th)	C3	C8	C13	C18	C23	C28	C33	*	:	specifies 4th column data (written into CGRAM address 00H)
6th byte (6th)	C4	C9	C14	C19	C24	C29	C34	*	:	specifies 5th column data (written into CGRAM address 00H)

To specify character pattern data continuously to the next address, specify only character pattern data as follows.
The addresses of CGRAM are automatically incremented. Specification of an address is therefore unnecessary.
The 2nd to 6th byte (character pattern data) are regarded as one data item, so 200 ns is sufficient for t_{DOFF} time between bytes.



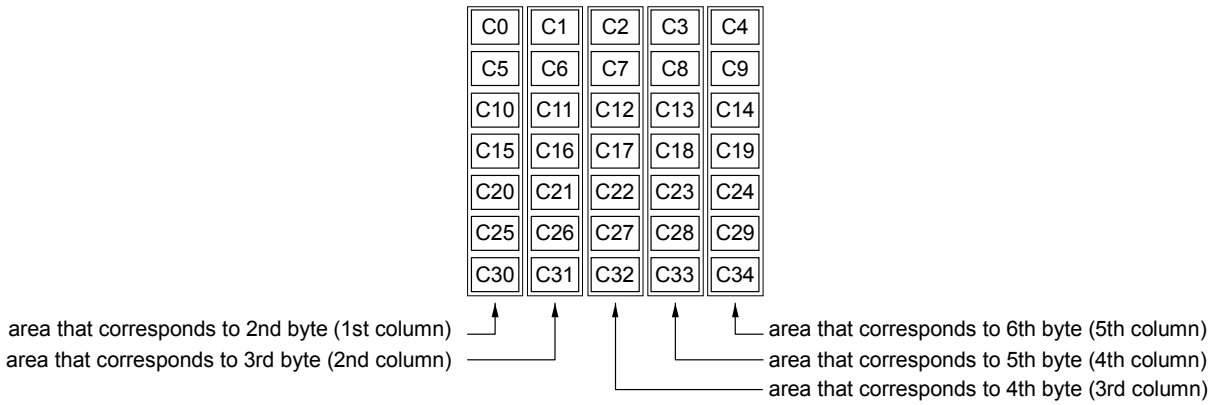
X0 (LSB) to X3 (MSB) : CGRAM addresses (4 bits: 16 characters)
C0 (LSB) to C34 (MSB) : Character pattern data (35 bits: 35 outputs per digit)
* : Don't care

[CGROM addresses and set CGRAM addresses]

Refer to ROMCODE table

HEX	X0	X1	X2	X3	CGROM address	HEX	X0	X1	X2	X3	CGROM address
00	0	0	0	0	RAM00(00000000B)	08	0	0	0	1	RAM08(00001000B)
01	1	0	0	0	RAM01(00000001B)	09	1	0	0	1	RAM09(00001001B)
02	0	1	0	0	RAM02(00000010B)	0A	0	1	0	1	RAM0A(00001010B)
03	1	1	0	0	RAM03(00000011B)	0B	1	1	0	1	RAM0B(00001011B)
04	0	0	1	0	RAM04(00000100B)	0C	0	0	1	1	RAM0C(00001100B)
05	1	0	1	0	RAM05(00000101B)	0D	1	0	1	1	RAM0D(00001101B)
06	0	1	1	0	RAM06(00000110B)	0E	0	1	1	1	RAM0E(00001110B)
07	1	1	1	0	RAM07(00000111B)	0F	1	1	1	1	RAM0F(00001111B)

Positional relationship between the output area of CGROM and that of CGRAM



Note: CGROM (Character Generator ROM) has an 8-bit address to generate 5 × 7 dot matrix character patterns.
CGRAM can store 240 types of character patterns.

3. ADRAM data write

(Specifies the addresses 00H to 1FH of ADRAM and writes symbol data.)

ADRAM (Additional Data RAM) has a 5-bit address to store symbol data.
Symbol data specified by ADRAM is directly output without CGROM and CGRAM.
(The ADRAM can store 2 types of symbol patterns for each digit.)
The terminal to which the contents of ADRAM are output can be used as a cursor.

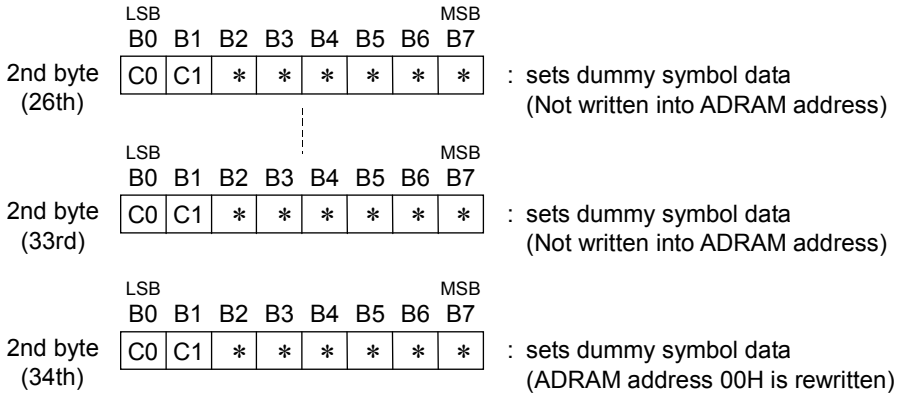
[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	X0	X1	X2	X3	X4	1	1	0	: selects ADRAM data write mode and specifies ADRAM address (Ex: Specifies ADRAM address 00H.)
2nd byte (2nd)	C0	C1	*	*	*	*	*	*	: sets symbol data (written into ADRAM address 00H.)

To specify symbol data continuously to the next address, specify only symbol data as follows.
The address of ADRAM is automatically incremented. Specification of addresses is therefore unnecessary.

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (3rd)	C0	C1	*	*	*	*	*	*	: sets symbol data (written into ADRAM address 01H)
2nd byte (4th)	C0	C1	*	*	*	*	*	*	: sets symbol data (written into ADRAM address 02H)
	⋮								
2nd byte (25th)	C0	C1	*	*	*	*	*	*	: sets symbol data (written into ADRAM address 17H)

After the symbol data setting up to 24 timing is completed, to set a symbol data from ADRAM address 00H continuously, set a dummy symbol data to ADRAM addresses between 18H and 1FH.
(ADRAM address is incremented automatically up to 1FH and after return to 00H)



X0 (LSB) to X4 (MSB) : ADRAM addresses (5 bits: 24 characters)
C0 (LSB) to C1 (MSB) : Symbol data (2 bits: 2-symbol data per digit)

* : Don't care

[Timing setting and ADRAM addresses]

HEX	X0	X1	X2	X3	X4	Timing setting	HEX	X0	X1	X2	X3	X4	Timing setting
00	0	0	0	0	0	T1	10	0	0	0	0	1	T17
01	1	0	0	0	0	T2	11	1	0	0	0	1	T18
02	0	1	0	0	0	T3	12	0	1	0	0	1	T19
03	1	1	0	0	0	T4	13	1	1	0	0	1	T20
04	0	0	1	0	0	T5	14	0	0	1	0	1	T21
05	1	0	1	0	0	T6	15	1	0	1	0	1	T22
06	0	1	1	0	0	T7	16	0	1	1	0	1	T23
07	1	1	1	0	0	T8	17	1	1	1	0	1	T24
08	0	0	0	1	0	T9	18	0	0	0	1	1	—
09	1	0	0	1	0	T10	19	1	0	0	1	1	—
0A	0	1	0	1	0	T11	1A	0	1	0	1	1	—
0B	1	1	0	1	0	T12	1B	1	1	0	1	1	—
0C	0	0	1	1	0	T13	1C	0	0	1	1	1	—
0D	1	0	1	1	0	T14	1D	1	0	1	1	1	—
0E	0	1	1	1	0	T15	1E	0	1	1	1	1	—
0F	1	1	1	1	0	T16	1F	1	1	1	1	1	—

4. GCRAM data write (Multi Grid Function)
(writes data by the number of COM outputs for digits)

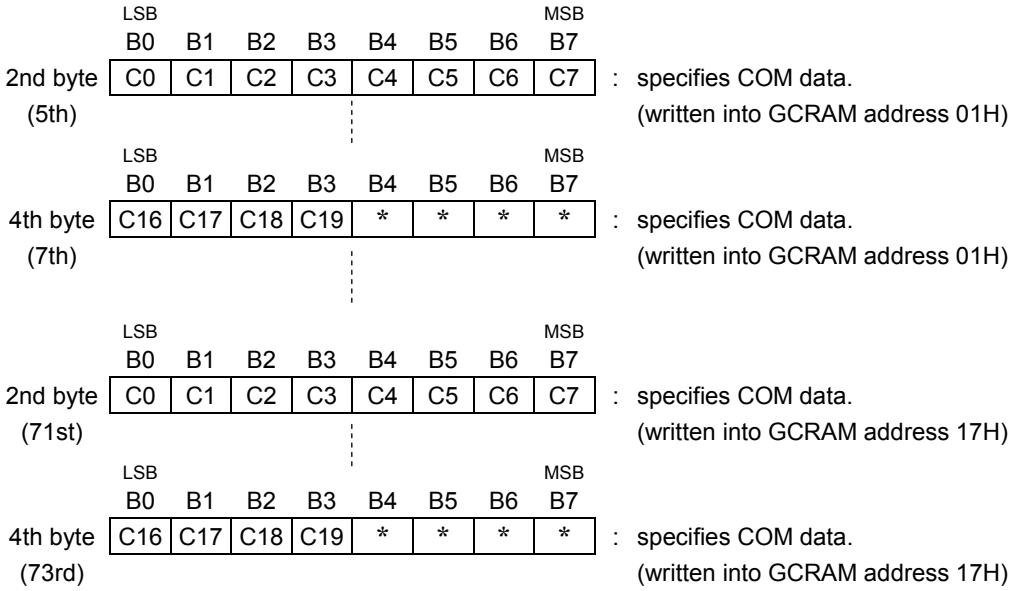
GCRAM (Grid Control RAM) has a 5-bit address to control the number of COM outputs for digits.
GCRAM outputs specified data directly to COMn, allowing COM outputs to be controlled arbitrarily.
It is also possible to supply a large current by connecting a plurality of COMs outside the ML9286.
For example, when COM19 and COM20 are connected, the ML9286 has 19 display digits. In this case, the user specifies "19" as the number of display digits.
Write grid data at GCRAM addresses 00H and later.
Carry out this mode before putting-out-lights mode release.
Refer to a「setting operation flow chart」about the details of a setup.
Write COM data"0" in the GCRAM address which is not used for incorrect display prevention.
Moreover, this setting can set COM of three a timing or less.
When four or more setting, any COM is not set. (The COM outputs are all "L")

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
1st byte (1st)	*	*	*	*	*	0	0	1	:	selects a GCRAM data write mode.
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	:	specifies COM data. (written into GCRAM address 00H)
3rd byte (3rd)	C8	C9	C10	C11	C12	C13	C14	C15	:	specifies COM data. (written into GCRAM address 00H)
4th byte (4th)	C16	C17	C18	C19	*	*	*	*	:	specifies COM data. (written into GCRAM address 00H)

C0 (LSB) to C19 (MSB): Grid control data (20 bits)
*: Don't Care

Note: To specify additional grid control data, specify the grid control data as shown below. The GCRAM addresses are automatically incremented.
The second byte to the fourth byte (for grid data) are treated as a single piece of element and the byte-byte t_{DOFF} can be 200 ns.



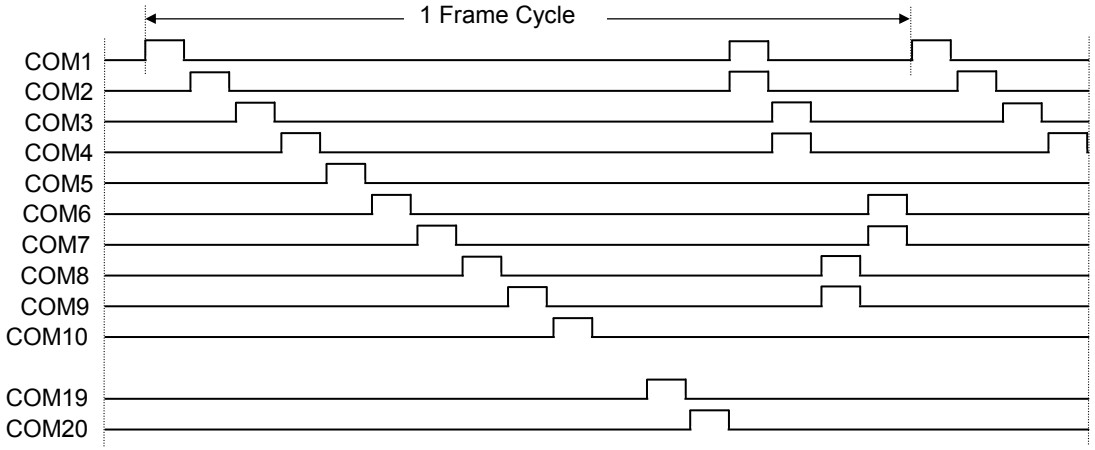
With the above operations, COM data of up to 24 digits are set. To set other COM data at GCRAM addresses 00H and later, specify dummy symbol data at GCRAM addresses 18H to 1FH (to automatically increment the GCRAM address and set the GCRAM address to 00H).

[GCRAM addresses (digit positions) and COM positions]

GCRAM address (HEX)	T1 (00)	T2 (01)	T3 (02)		T22 (15)	T23 (16)	T24 (17)
COM1	C0	C0	C0		C0	C0	C0
COM2	C1	C1	C1		C1	C1	C1
COM3	C2	C2	C2		C2	C2	C2
COM4	C3	C3	C3		C3	C3	C3
COM5	C4	C4	C4	.....	C4	C4	C4
COM16	C15	C15	C15		C15	C15	C15
COM17	C16	C16	C16		C16	C16	C16
COM18	C17	C17	C17		C17	C17	C17
COM19	C18	C18	C18		C18	C18	C18
COM20	C19	C19	C19		C19	C19	C19

[GCRAM output example]
1. When 20-digit display of multi grid.
<Setup>
Number setup of timing set : T24
* Write "0" also in the beam which is not used.

GCRAM Address (HEX)	T1 (00)	T2 (01)	T3 (02)	T4 (03)	T5 (04)	T6 (05)	T7 (06)	T8 (07)	T9 (08)	T10 (09)	..	T19 (12)	T20 (13)	T21 (14)	T22 (15)	T23 (16)	T24 (17)
COM1	1	0	0	0	0	0	0	0	0	0		0	0	1	0	0	0
COM2	0	1	0	0	0	0	0	0	0	0		0	0	1	0	0	0
COM3	0	0	1	0	0	0	0	0	0	0		0	0	0	1	0	0
COM4	0	0	0	1	0	0	0	0	0	0		0	0	0	1	0	0
COM5	0	0	0	0	1	0	0	0	0	0		0	0	0	0	0	0
COM6	0	0	0	0	0	1	0	0	0	0		0	0	0	0	0	1
COM7	0	0	0	0	0	0	1	0	0	0		0	0	0	0	0	1
COM8	0	0	0	0	0	0	0	1	0	0		0	0	0	0	1	0
COM9	0	0	0	0	0	0	0	0	1	0		0	0	0	0	1	0
COM10	0	0	0	0	0	0	0	0	0	1		0	0	0	0	0	0
:																	
COM19	0	0	0	0	0	0	0	0	0	0		1	0	0	0	0	0
COM20	0	0	0	0	0	0	0	0	0	0		0	1	0	0	0	0



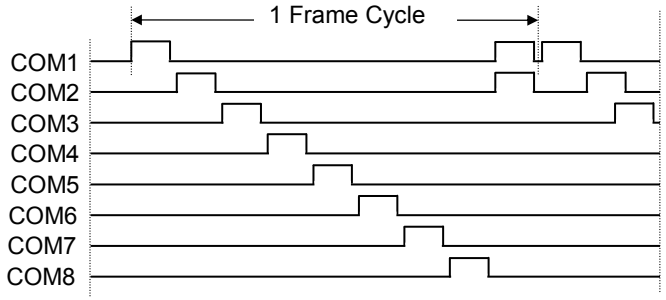
2. When 8-digit display of multi grid.

<Setup>

Number setup of timing set : T9

* Write "0" also in the beam which is not used.

GCRAM アドレス (HEX)	T1 (00)	T2 (01)	T3 (02)	T4 (03)	T5 (04)	T6 (05)	T7 (06)	T8 (07)	T9 (08)	T10 (09)	T11 (0A)	..	T20 (13)	T21 (14)	T22 (15)	T23 (16)	T24 (17)
COM1	1	0	0	0	0	0	0	0	1	0	0		0	0	0	0	0
COM2	0	1	0	0	0	0	0	0	1	0	0		0	0	0	0	0
COM3	0	0	1	0	0	0	0	0	0	0	0		0	0	0	0	0
COM4	0	0	0	1	0	0	0	0	0	0	0		0	0	0	0	0
COM5	0	0	0	0	1	0	0	0	0	0	0		0	0	0	0	0
COM6	0	0	0	0	0	1	0	0	0	0	0		0	0	0	0	0
COM7	0	0	0	0	0	0	1	0	0	0	0		0	0	0	0	0
COM8	0	0	0	0	0	0	0	1	0	0	0		0	0	0	0	0
COM9	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
COM10	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
:																	
COM19	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
COM20	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0



5. Display duty set

(Writes a display duty value to the duty cycle register.)

Display duty adjusts brightness in 256 stages (0/256 to 240/256) using 8-bit data.
When the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". (see "Reset Function") Always execute this instruction before turning the display on, then set a desired duty value.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	*	*	*	*	*	1	0	1	: Selects display duty set.

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (2nd)	D0	D1	D2	D3	D4	D5	D6	D7	: Sets duty value set.

D0 (LSB) to D7 (MSB) : display duty data (8 bits: 0/256 to 240/256 stages)
* : Don't care

[Relation between setup data and controlled COM/AD/SEG duty]

HEX	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	COM/AD/SEG duty
00	0	0	0	0	0	0	0	0	0	0	0/256
01	1	0	0	0	0	0	0	0	0	0	1/256
02	0	1	0	0	0	0	0	0	0	0	2/256
⋮											⋮
EF	1	1	1	1	1	1	0	1	1	1	239/256
F0	0	0	0	0	0	0	1	1	1	1	240/256
⋮											⋮
FE	0	1	1	1	1	1	1	1	1	1	240/256
FF	1	1	1	1	1	1	1	1	1	1	240/256

← The state when $\overline{\text{RESET}}$ signal is input.

6. Number of timing set

(Writes the number of display timing to the display timing register.)

The number of timing set can T9 to T24 display timing using 4-bit data.
When the $\overline{\text{RESET}}$ signal is input, the number of timing register value is "0". (see "Reset Function") Always execute this instruction to change the number of timings before turning the display on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	K0	K1	K2	K3	*	0	1	1	: selects the number of timing set mode

K0 (LSB) to K3 (MSB) : number of timing data (4 bits)
* : Don't care

[Relation between setup data and timing set]

HEX	K0	K1	K2	K3	Timing Setting	HEX	K0	K1	K2	K3	Timing Setting
0	0	0	0	0	T1 to T24	8	0	0	0	1	T1 to T16
1	1	0	0	0	T1 to T9	9	1	0	0	1	T1 to T17
2	0	1	0	0	T1 to T10	A	0	1	0	1	T1 to T18
3	1	1	0	0	T1 to T11	B	1	1	0	1	T1 to T19
4	0	0	1	0	T1 to T12	C	0	0	1	1	T1 to T20
5	1	0	1	0	T1 to T13	D	1	0	1	1	T1 to T21
6	0	1	1	0	T1 to T14	E	0	1	1	1	T1 to T22
7	1	1	1	0	T1 to T15	F	1	1	1	1	T1 to T23

* The state when $\overline{\text{RESET}}$ signal is input.

7. All display lights ON/OFF set

(Turns all display lights ON or OFF.)

When the $\overline{\text{RESET}}$ signal is input, All display lights OFF mode is set. (see "Reset Function")
All display lights ON mode is used primarily for display testing.
All display lights OFF mode is primarily used for display blink and to prevent malfunction when power is turned on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	L	H	*	*	*	1	1	1	: selects all display lights ON or OFF mode and specifies display operation

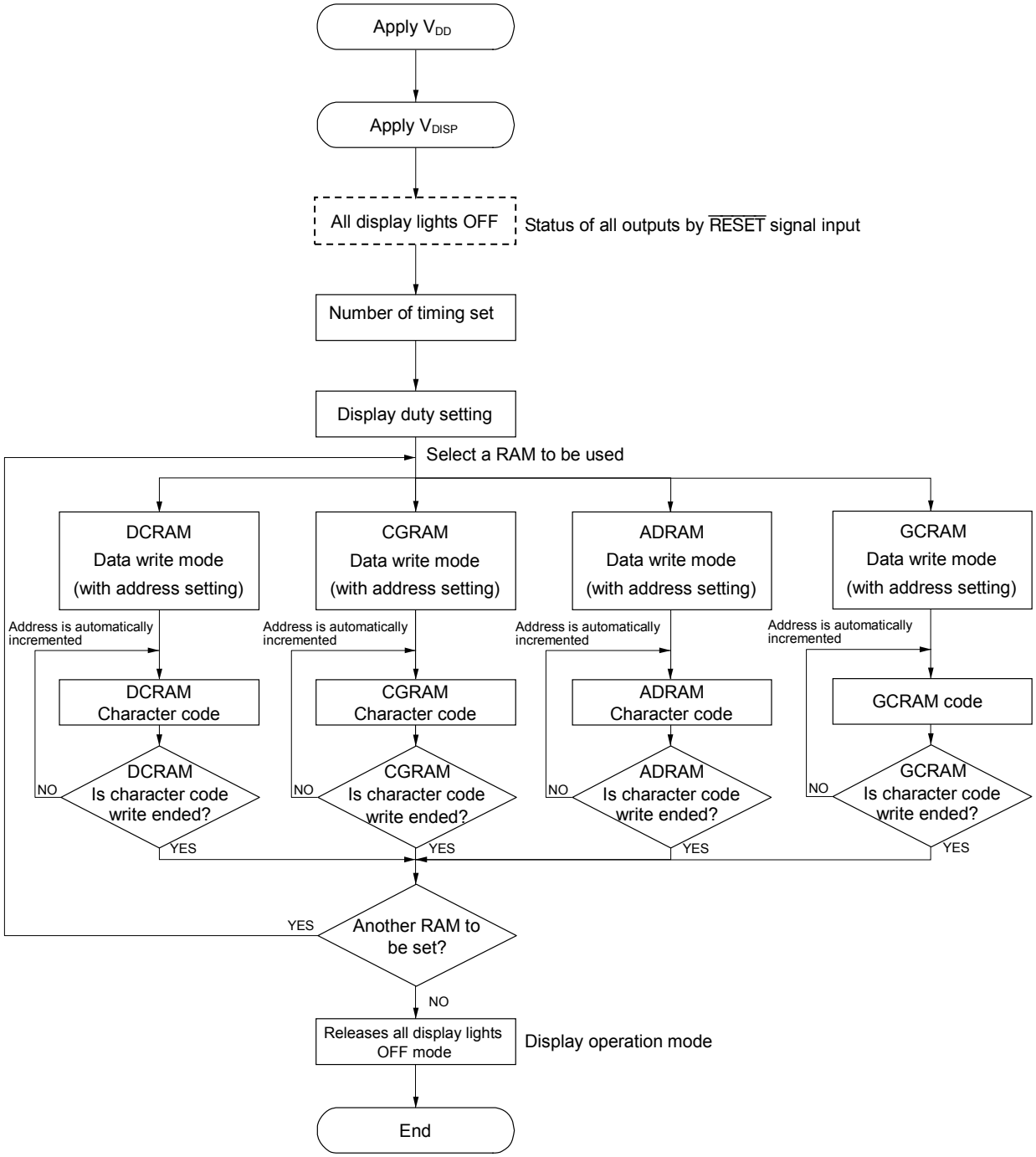
L and H: display operation data
*: Don't care

[Set data and display state of SEG and AD]

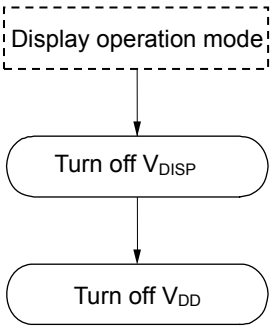
L	H	Display state of SEG and AD	
0	0	Normal display	
1	0	Sets all outputs to Low	(The state when $\overline{\text{RESET}}$ signal is input.)
0	1	Sets all outputs to High	
1	1	Sets all outputs to High	

SETTING FLOWCHART

(Power applying included)



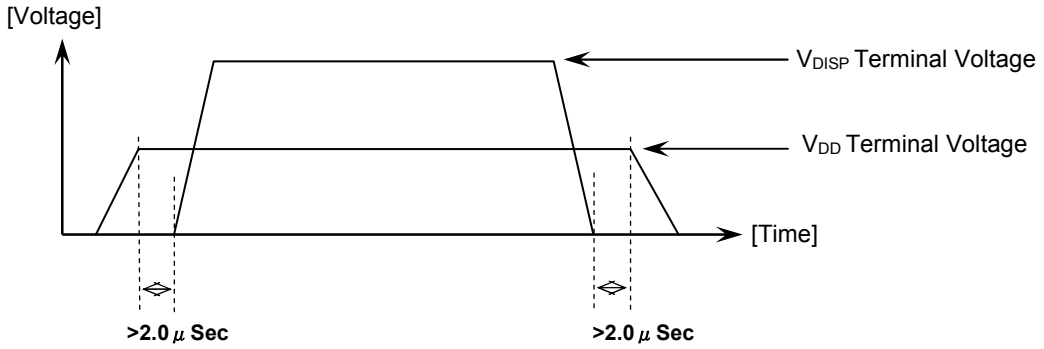
POWER-OFF FLOWCHART



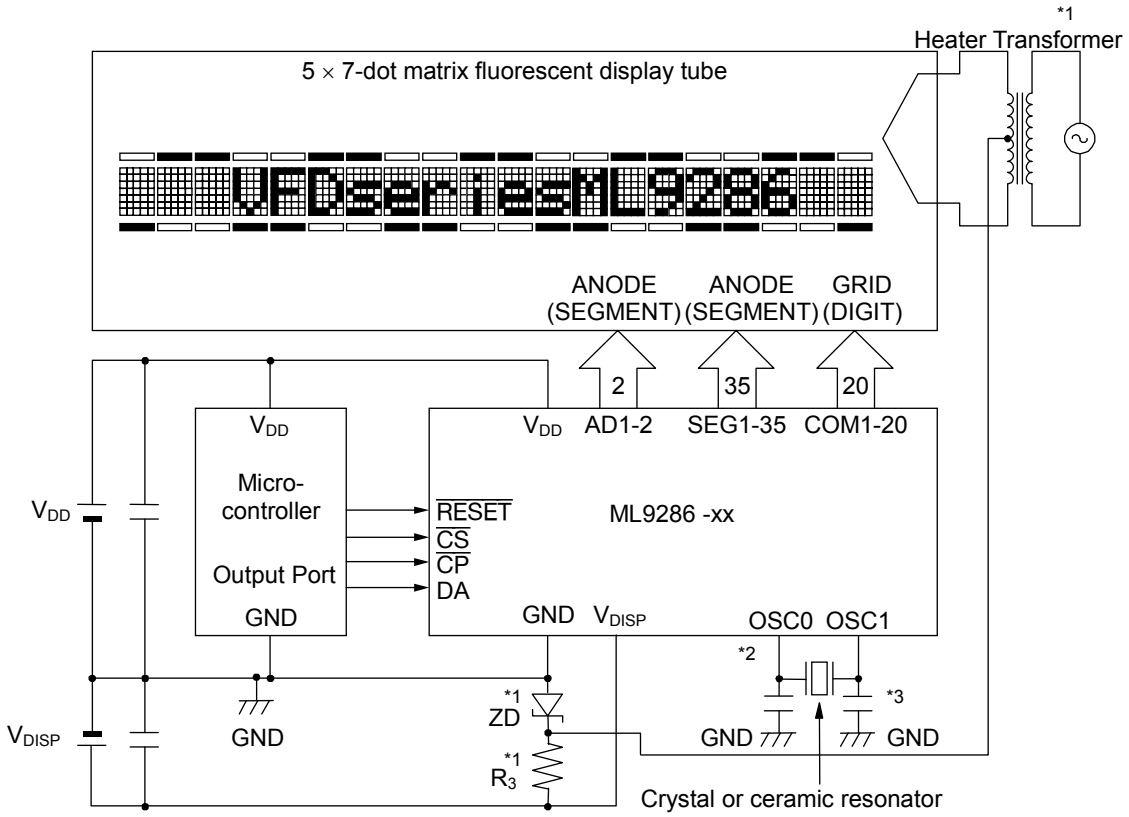
CAUTION FOR POWER-ON SEQUENCE

Set V_{DD} and V_{DISP} as the same voltage and connect them at the outside of IC.

To prevent the mulfunction, turn on the driver power supply V_{DISP} after the logic power supply V_{DD} is turned on at Power-on sequence. And also, turn off the driver power supply V_{DISP} before the logic power supply V_{DD} is turned off at Power-off sequence.



APPLICATION CIRCUIT

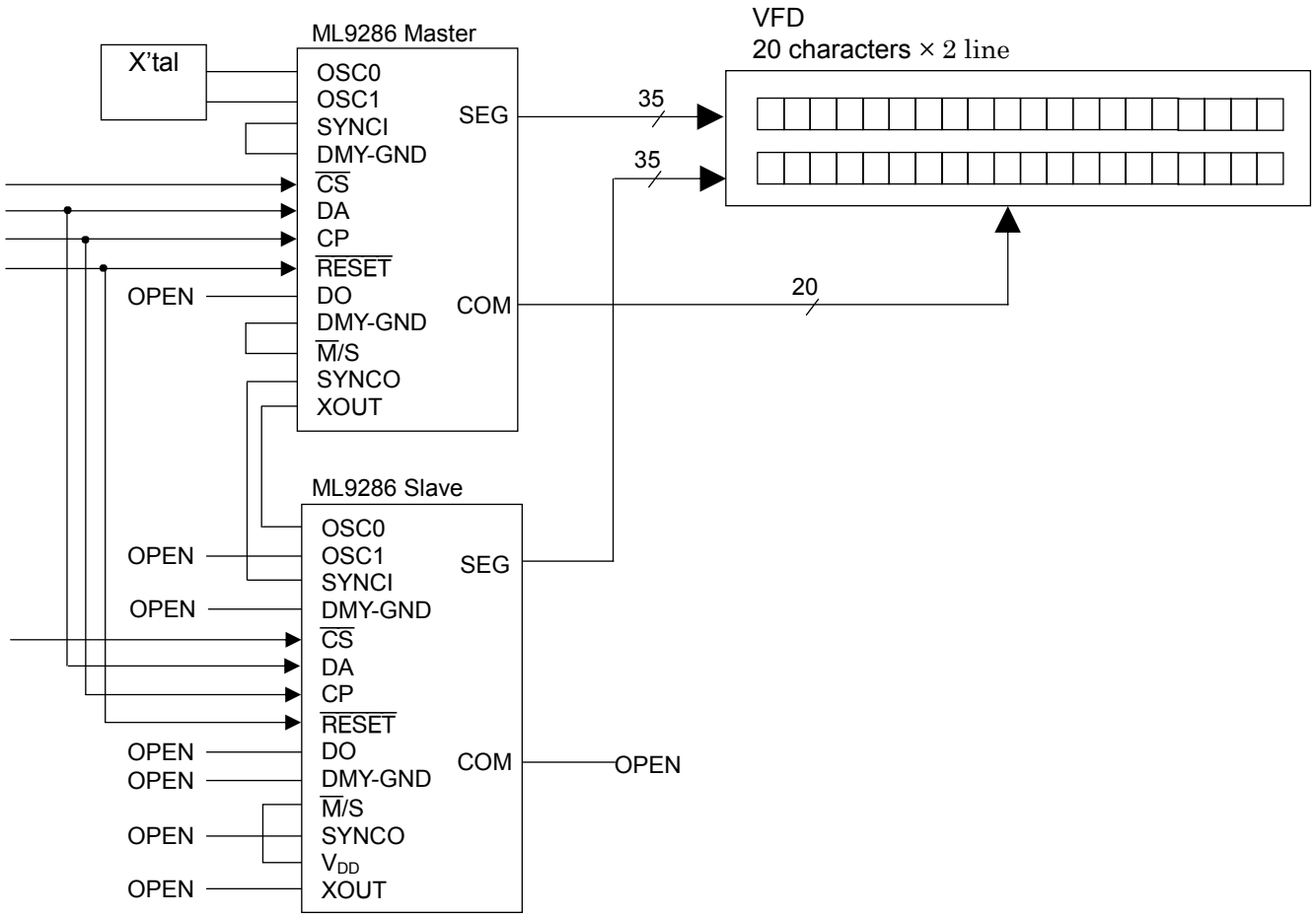


Notes: *1. The application circuit indicates a circuit by which fluorescent display tube filaments are ac driven using a heater transformer. Contact fluorescent display tube manufacturers for the methods and circuits of driving fluorescent display tube filaments.

*2. Keep the wires between the OSC0 pin and the crystal or ceramic resonator as short as possible to avoid generating noise.

*3 For oscillation capacitor values, refer to data of the crystal or ceramic resonator used.

APPLICATION CIRCUIT (CASCADE CONNECTION)

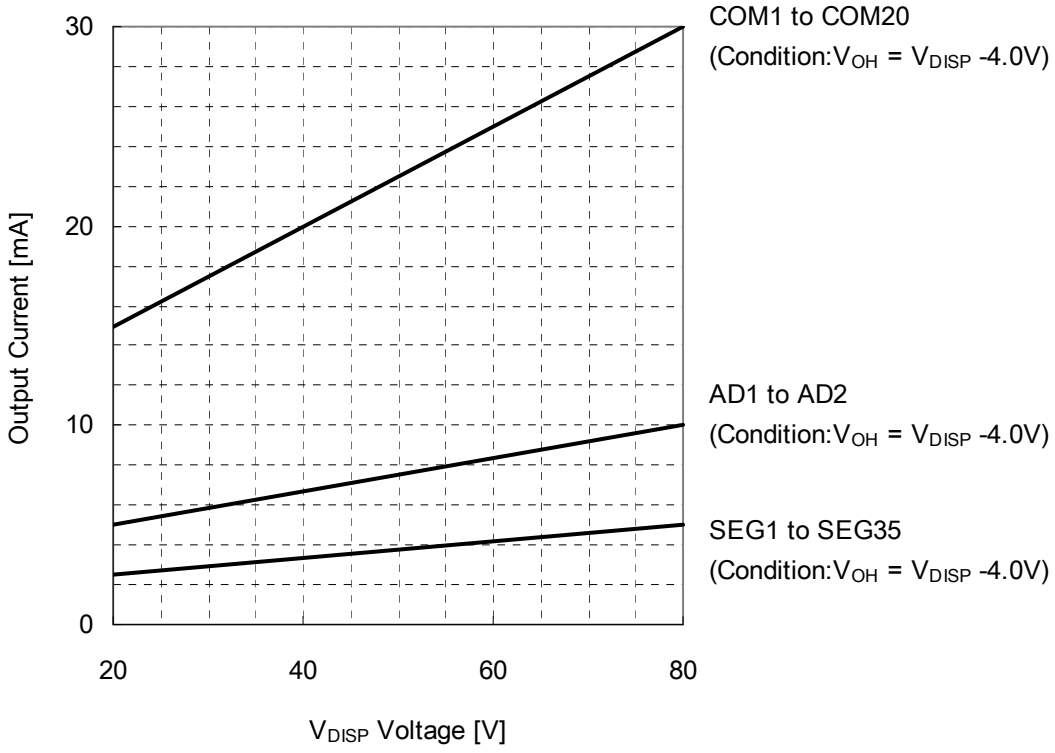


Notes: *1. Please set the display timing register of Master IC and Slave IC to the same value.

REFERENCE DATA

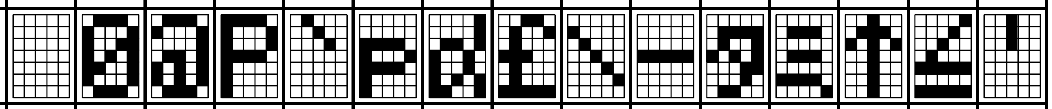
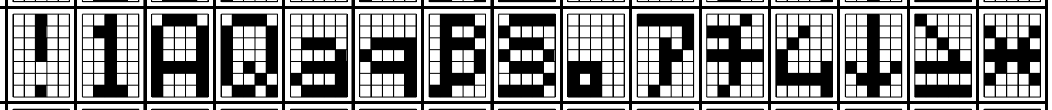
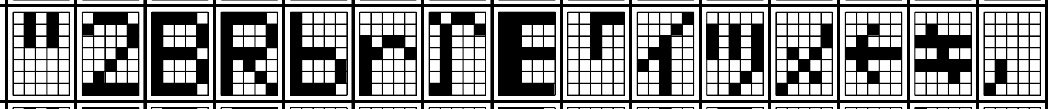
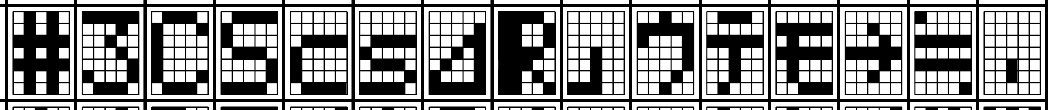
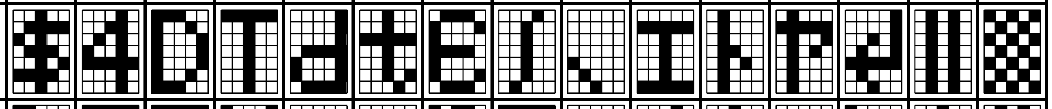
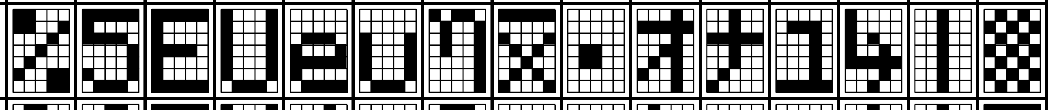
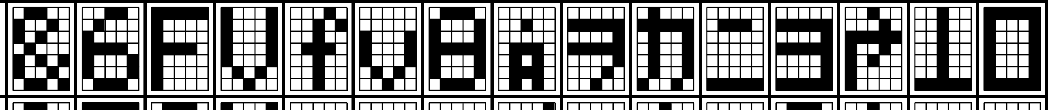
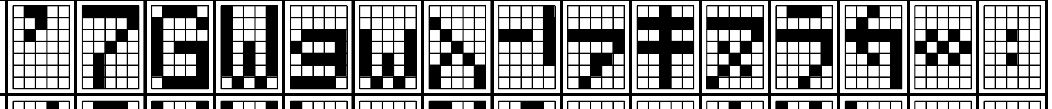
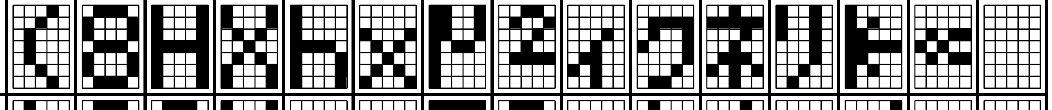
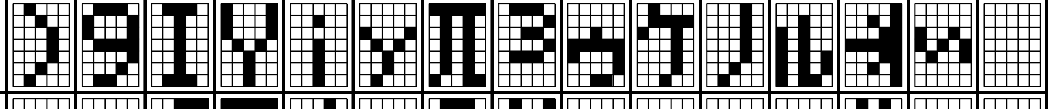
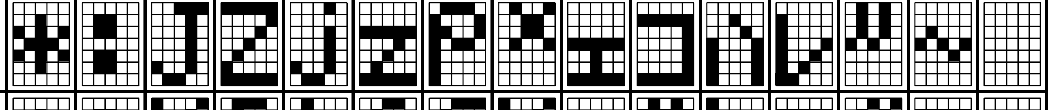
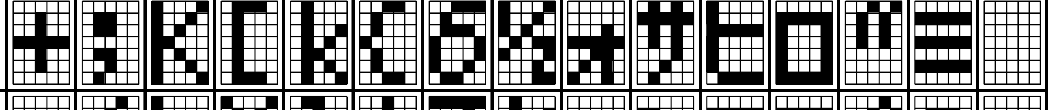
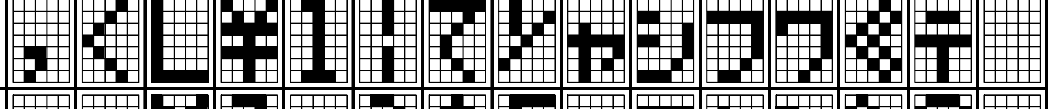
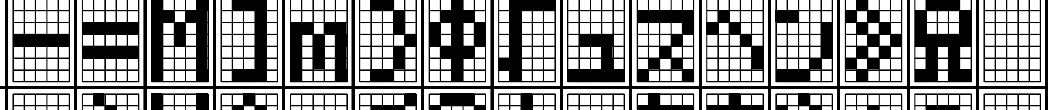
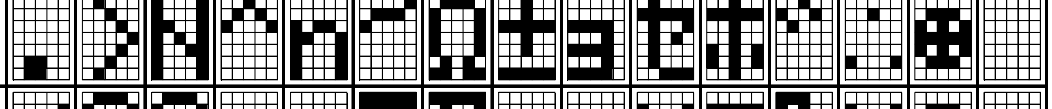
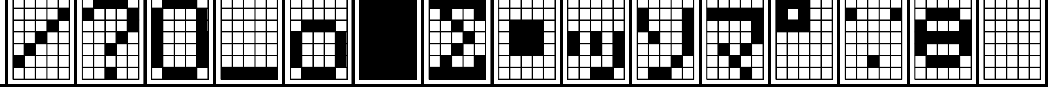
Graphs illustrating the V_{DISP} versus driver output current capability relationship are shown below.
Care must be taken not to use the total power in excess of allowable power dissipation.

V_{DISP} Voltage vs Output Current of Each Driver



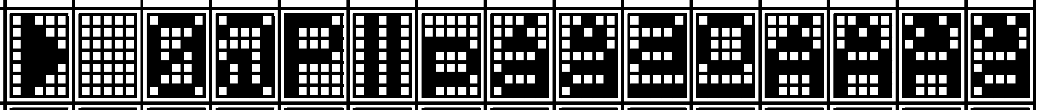
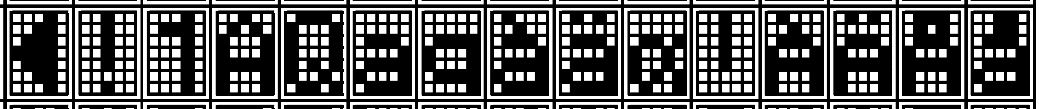
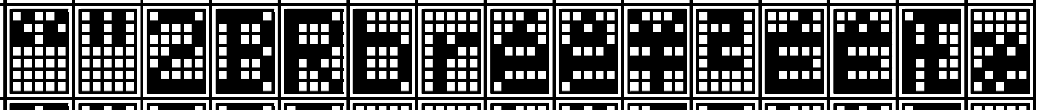
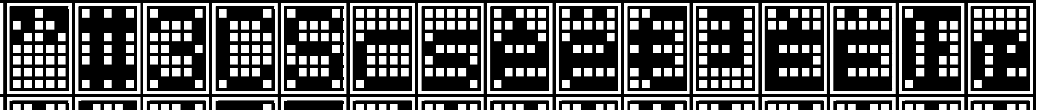
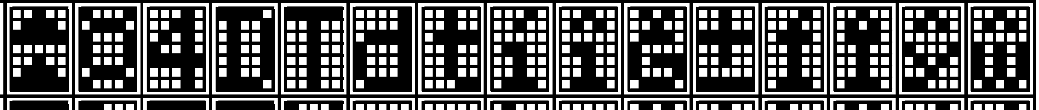
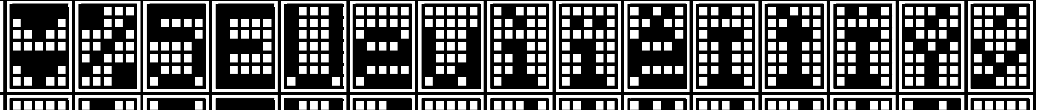
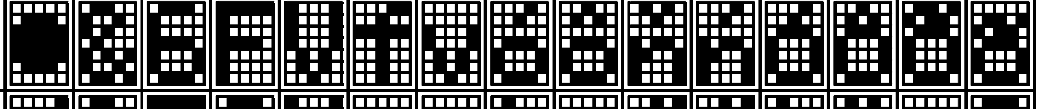
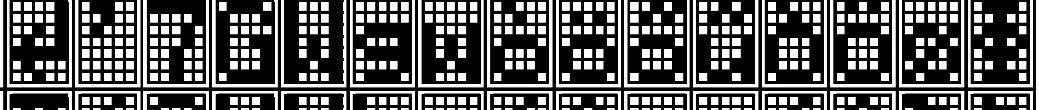
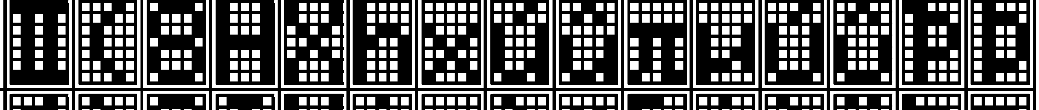
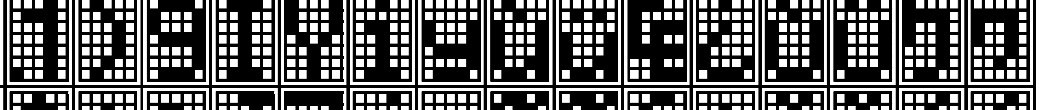
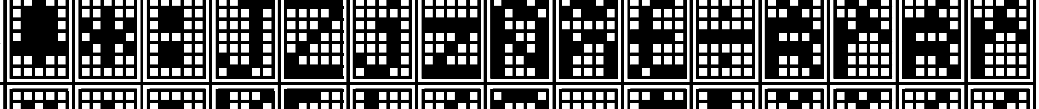
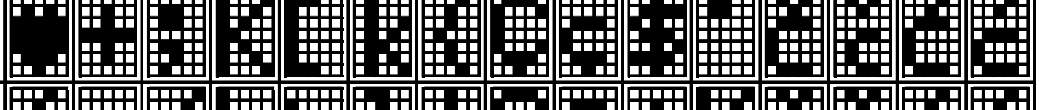
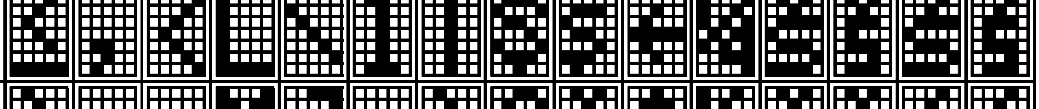
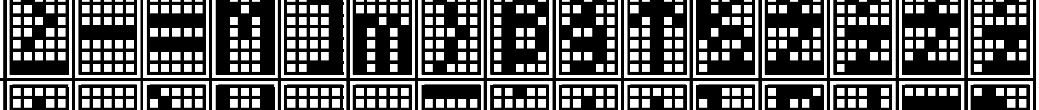
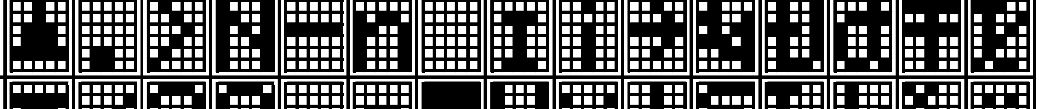
ML9286-01 ROM CODE

*ROM CODE is the character set for SEG1 to SEG35.
00000000b(00h) to 00001111b(0Fh) are the CGRAM addresses

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0															
0001	RAM1															
0010	RAM2															
0011	RAM3															
0100	RAM4															
0101	RAM5															
0110	RAM6															
0111	RAM7															
1000	RAM8															
1001	RAM9															
1010	RAMA															
1011	RAMB															
1100	RAMC															
1101	RAMD															
1110	RAME															
1111	RAMF															

ML9286-02 ROM CODE

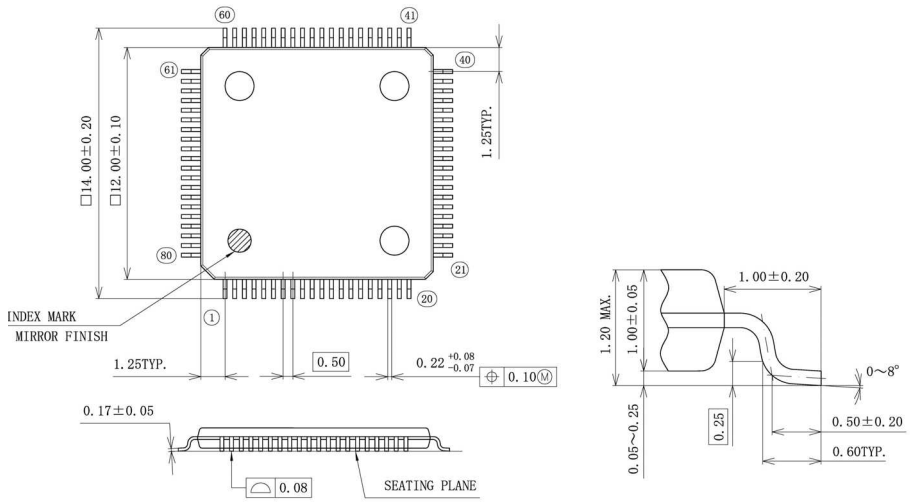
*ROM CODE is the character set for SEG1 to SEG35.
00000000b(00h) to 00001111b(0Fh) are the CGRAM addresses

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0															
0001	RAM1															
0010	RAM2															
0011	RAM3															
0100	RAM4															
0101	RAM5															
0110	RAM6															
0111	RAM7															
1000	RAM8															
1001	RAM9															
1010	RAMA															
1011	RAMB															
1100	RAMC															
1101	RAMD															
1110	RAME															
1111	RAMF															

PACKAGE DIMENSIONS

(Unit: mm)

TQFP80-P-1212-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Plating (≥5μm)
Package weight (g)	0.40 TYP.
Rev. No./Last Revised	1/Feb. 1, 2008

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9286-01	Mar. 1, 2010	—	—	Final edition 1

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