International IⓇR Rectifier

IRF7832Z

HEXFET® Power MOSFET

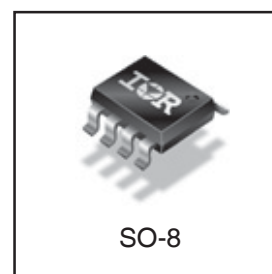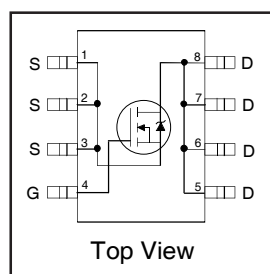| V_{DSS}	$R_{DS(on)}$ max	Qg
30V	3.8mΩ@V_{GS} = 10V	30nC

Applications
- Synchronous MOSFET for Notebook Processor Power
- Synchronous Rectifier MOSFET for Isolated DC-DC Converters

Benefits
- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- 20V V_{GS} Max. Gate Rating
- 100% tested for Rg

Top View

SO-8

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	21	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	17	A
I_{DM}	Pulsed Drain Current ①	160	
P_D @T_A = 25°C	Power Dissipation	2.5	W
P_D @T_A = 70°C	Power Dissipation	1.6	
	Linear Derating Factor	0.02	W/°C
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	——	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	——	50	

Notes ① through ⑤ are on page 10

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Static @ T$_J$ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV$_{DSS}$	Drain-to-Source Breakdown Voltage	30	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔBV$_{DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	0.023	——	V/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.1	3.8	mΩ	V$_{GS}$ = 10V, I$_D$ = 20A ③
		——	3.7	4.5		V$_{GS}$ = 4.5V, I$_D$ = 16A ③
V$_{GS(th)}$	Gate Threshold Voltage	1.35	——	2.35	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 250µA
ΔV$_{GS(th)}$	Gate Threshold Voltage Coefficient	——	-5.5	——	mV/°C	
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	1.0	µA	V$_{DS}$ = 24V, V$_{GS}$ = 0V
		——	——	150		V$_{DS}$ = 24V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	100	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V$_{GS}$ = -20V
gfs	Forward Transconductance	80	——	——	S	V$_{DS}$ = 15V, I$_D$ = 16A
Q$_g$	Total Gate Charge	——	30	45	nC	V$_{DS}$ = 15V
Q$_{gs1}$	Pre-Vth Gate-to-Source Charge	——	7.9	——		V$_{GS}$ = 4.5V
Q$_{gs2}$	Post-Vth Gate-to-Source Charge	——	2.6	——		I$_D$ = 16A
Q$_{gd}$	Gate-to-Drain Charge	——	11	——		See Fig. 16
Q$_{godr}$	Gate Charge Overdrive	——	8.5	——		
Q$_{sw}$	Switch Charge (Q$_{gs2}$ + Q$_{gd}$)	——	13.6	——		
Q$_{oss}$	Output Charge	——	19	——	nC	V$_{DS}$ = 16V, V$_{GS}$ = 0V
R$_g$	Gate Resistance	——	1.2	1.9	Ω	
t$_{d(on)}$	Turn-On Delay Time	——	14	——	ns	V$_{DD}$ = 15V, V$_{GS}$ = 4.5V
t$_r$	Rise Time	——	15	——		I$_D$ = 16A
t$_{d(off)}$	Turn-Off Delay Time	——	18	——		Clamped Inductive Load
t$_f$	Fall Time	——	5.6	——		
C$_{iss}$	Input Capacitance	——	3860	——	pF	V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	840	——		V$_{DS}$ = 15V
C$_{rss}$	Reverse Transfer Capacitance	——	370	——		ƒ = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E$_{AS}$	Single Pulse Avalanche Energy ②	——	350	mJ
I$_{AR}$	Avalanche Current ①	——	16	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①	——	——	160		
V$_{SD}$	Diode Forward Voltage	——	——	1.0	V	T$_J$ = 25°C, I$_S$ = 16A, V$_{GS}$ = 0V ③
t$_{rr}$	Reverse Recovery Time	——	16	24	ns	T$_J$ = 25°C, I$_F$ = 16A, V$_{DD}$ = 15V
Q$_{rr}$	Reverse Recovery Charge	——	29	44	nC	di/dt = 500A/µs ③
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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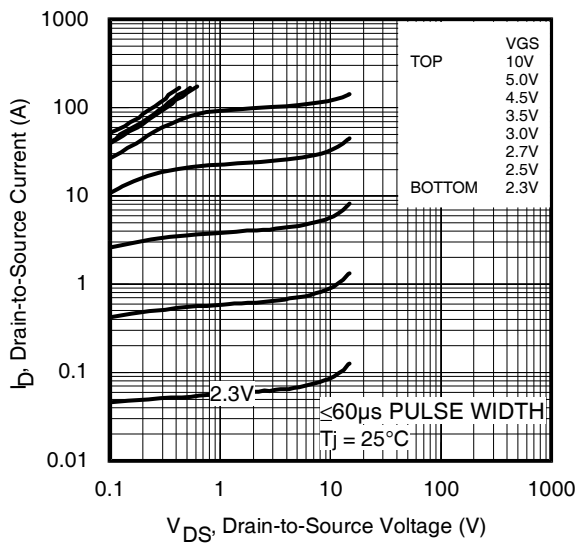# International IOR Rectifier

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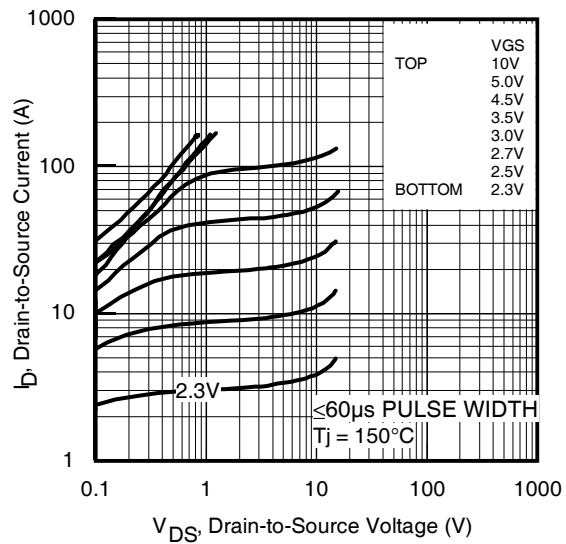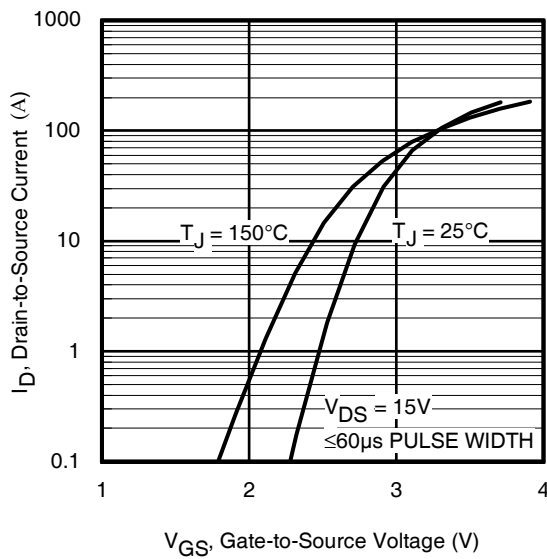

Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics
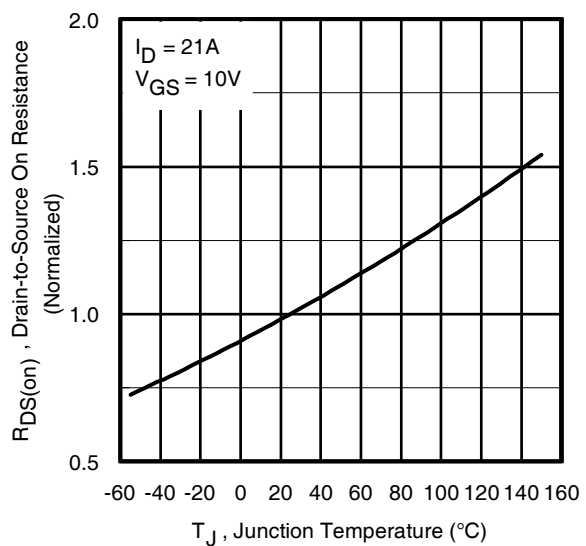
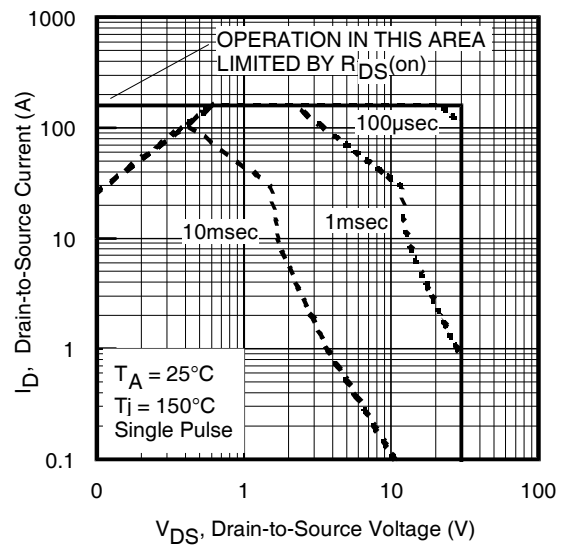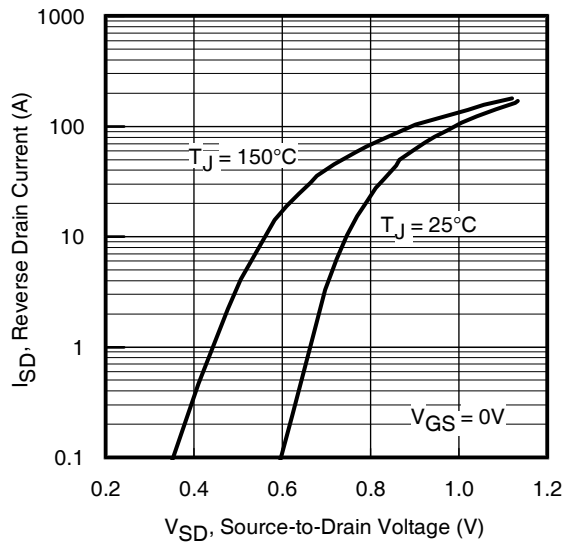**Fig 4.** Normalized On-Resistance vs. Temperature

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Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

Fig 7. Typical Source-Drain Diode
Forward Voltage

Fig 8. Maximum Safe Operating Area

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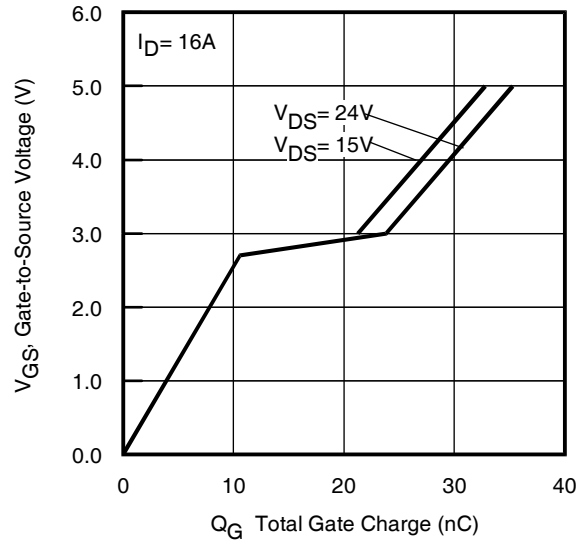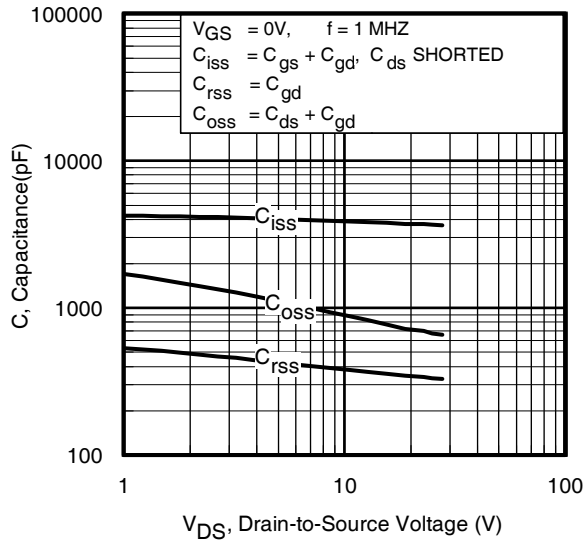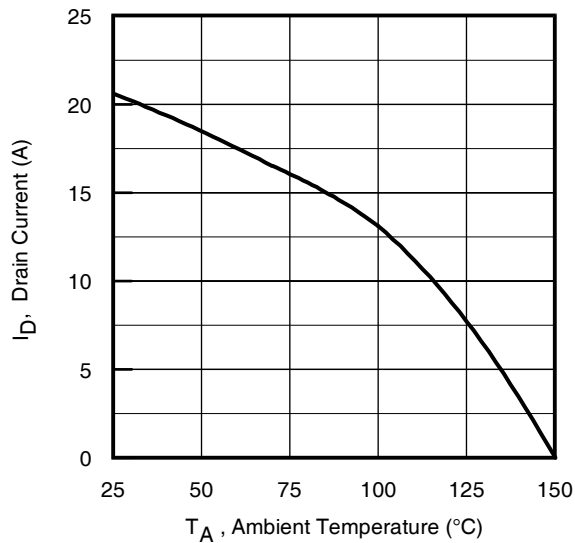
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Fig 9. Maximum Drain Current vs. Case Temperature
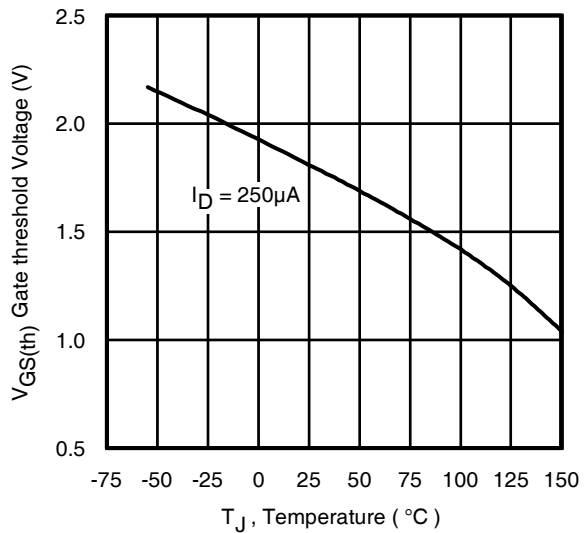
Fig 10. Threshold Voltage vs. Temperature

Ri (°C/W)	τi (sec)
5.6971	0.015296
28.314	1.214900
16	40.40000

Notes:
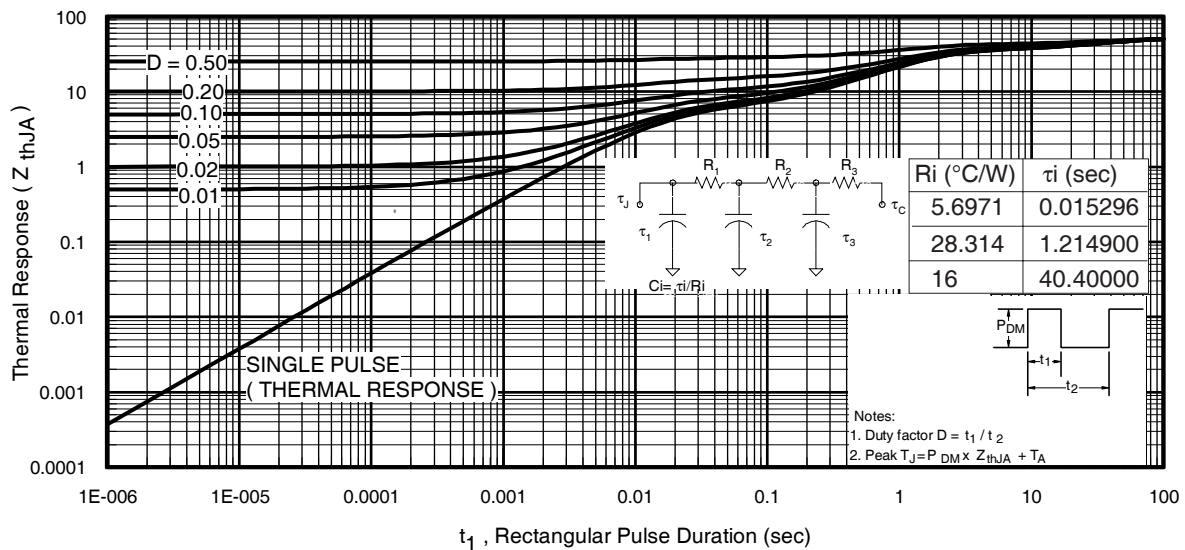1. Duty factor $D = t_1 / t_2$
2. Peak $T_J = P_{DM} \times Z_{thJA} + T_A$

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient
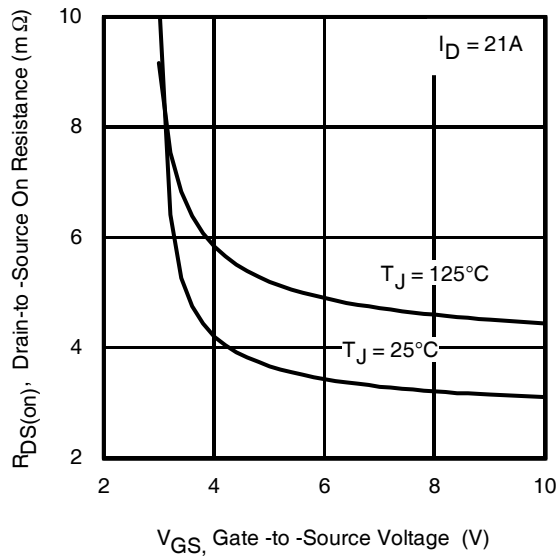
IRF7832Z

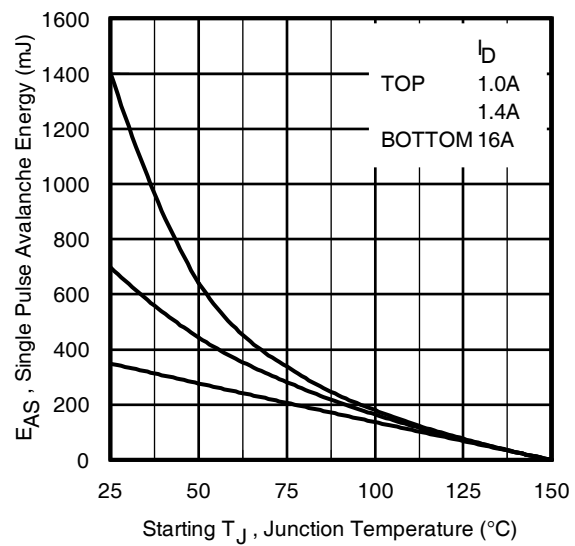
Fig 12. On-Resistance vs. Gate Voltage

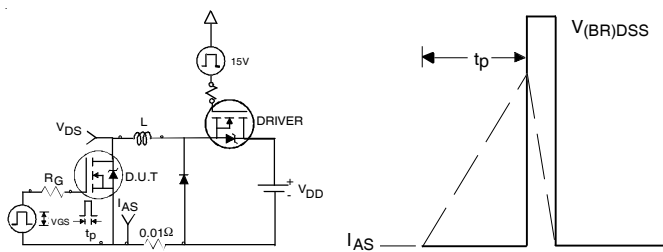Fig 13. Maximum Avalanche Energy vs. Drain Current
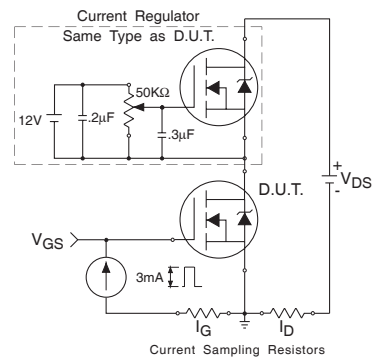

Fig 14. Unclamped Inductive Test Circuit and Waveform

Fig 15. Gate Charge Test Circuit

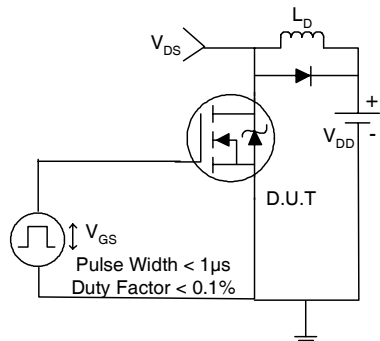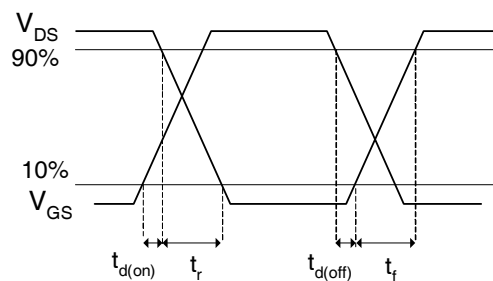
Fig 16. Switching Time Test Circuit

Fig 17. Switching Time Waveforms

D.U.T

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

V_{DD}

R_G

① Driver Gate Drive

P.W.　Period　$D = \dfrac{P.W.}{Period}$

$V_{GS}=10V$ *

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current
di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 18. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Id

Vds

Vgs
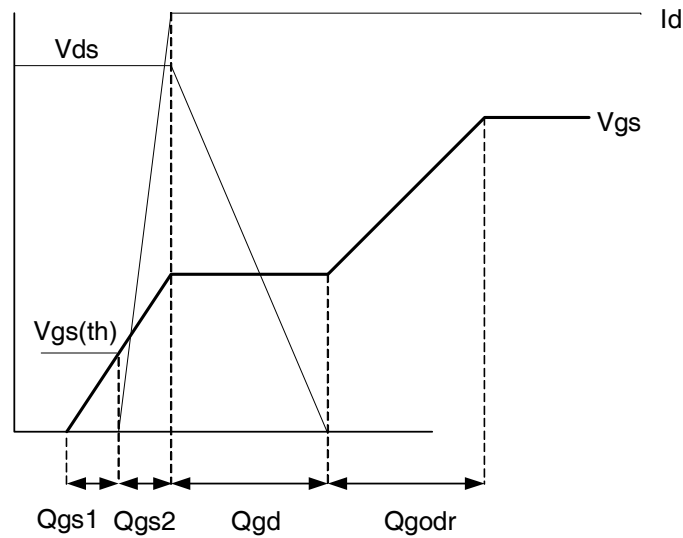
Vgs(th)

Qgs1　Qgs2　Qgd　Qgodr

Fig 19. Gate Charge Waveform

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Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^{2} \times R_{ds(on)} \right)$$
$$+ \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^{*}$$
$$P_{loss} = \left(I_{rms}^{2} \times R_{ds(on)} \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left(Q_{rr} \times V_{in} \times f \right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.
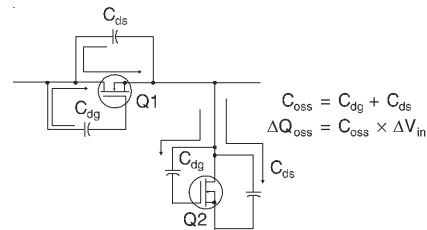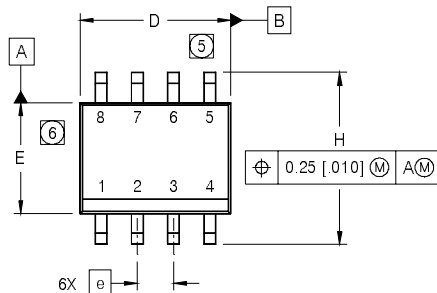

Figure A: Q_{oss} Characteristic

$$C_{oss} = C_{dg} + C_{ds}$$
$$\Delta Q_{oss} = C_{oss} \times \Delta V_{in}$$

SO-8 Package Outline (Dimensions are shown in millimeters (inches)

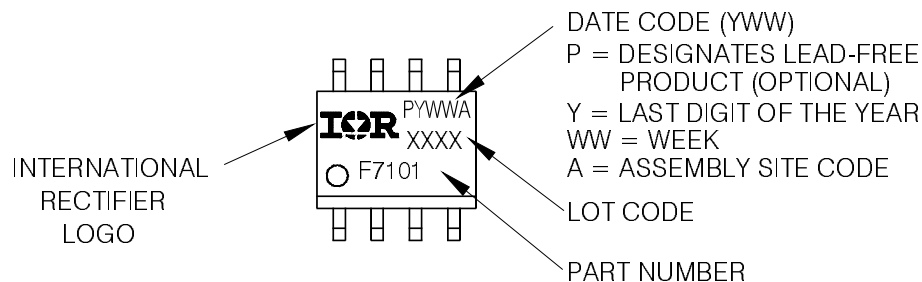| DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°
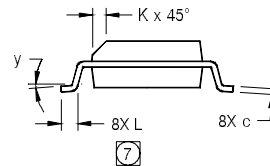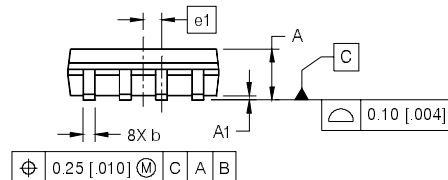
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
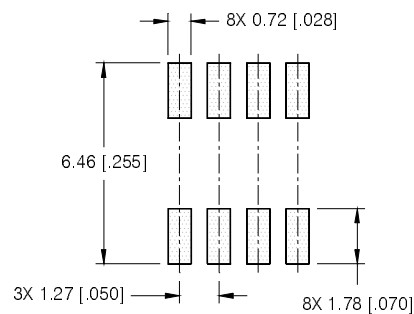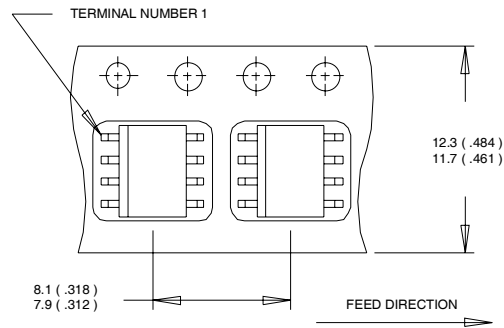
SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

INTERNATIONAL RECTIFIER LOGO

DATE CODE (YWW)
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
Y = LAST DIGIT OF THE YEAR
WW = WEEK
A = ASSEMBLY SITE CODE

LOT CODE

PART NUMBER

IRF7832Z

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)

TERMINAL NUMBER 1

12.3 (.484)
11.7 (.461)

8.1 (.318)
7.9 (.312)

FEED DIRECTION

NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

$\varnothing$ 330.00
(12.992)
MAX.

14.40 (.566)
12.40 (.488)
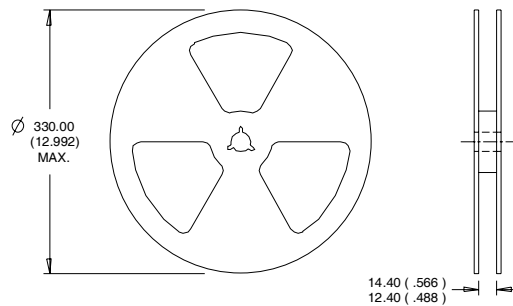
NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 2.7mH, R_G = 25Ω, I_{AS} = 16A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

⑤ R_θ is measured at T_J of approximately 90°C.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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