STK5F1U3C3D-E

Inverter Power IPM for 3-phase Motor Drive

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Overview

This "Inverter Power IPM" is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single DIP module (Dual-In line Package). Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers
- Built-in cross conduction prevention
- Externally accessible embedded thermistor for substrate temperature measurement
- The level of the over-current protection current is adjustable with the external resistor, "RSD"
- Low switching noise by optimized the gate resistor

Certification

- UL1557 (File Number: E339285)

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Remarks	Ratings	Unit
Supply voltage	V_{CC}	P to N, surge < 500V *1	450	V
Collector-emitter voltage	V_{CE}	P to U,V,W or U,V,W to N	600	V
Output current	Io	P, N, U, V, W terminal current	±30	A
		P, N, U, V, W terminal current, Tc=100°C	±15	
Output peak current	Iop	P, N, U, V, W terminal current, PW=1ms	±49	A
Pre-driver supply voltage	VD1,2,3,4	VB1 to VS1,VB2 to VS2,VB3 to VS3,V_{DD} to V_{SS} *2	20	V
Input signal voltage	VIN	HIN1, 2, 3, LIN1, 2, 3	–0.3 to V_{DD}	V
FAULT terminal voltage	VFAULT	FAULT terminal	–0.3 to V_{DD}	V
Maximum loss	Pd	IGBT per channel	56.8	W
Junction temperature	Tj	IGBT,FRD	150	°C
Storage temperature	Tstg		–40 to +125	°C
Operating temperature	Tc	HIC case	–20 to +100	°C
Tightening torque	MT	A screw part at use M4 type screw *3	1.17	Nm
Withstand voltage	Vis	50Hz sine wave AC 1 minute *4	2000	VRMS

Reference voltage is N terminal = V_{SS} terminal voltage unless otherwise specified.

*1: Surge voltage developed by the switching operation due to the wiring inductance between the P and N terminals.

*2: Terminal voltage: VD1=VB1–VS1, VD2=VB2–VS2, VD3=VB3–VS3, VD4=V_{DD}–V_{SS}.

*3: Flatness of the heat-sink should be 0.25mm and below.

*4: Test conditions: AC 2500V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4=15V

Parameter	Symbol	Conditions		Test circuit	Ratings Min.	Ratings Typ.	Ratings Max.	Unit
Power output section								
Collector to emitter cut-off current	I_{CE}	V_{CE}=600V		Fig.1	-	-	100	μA
Bootstrap diode reverse current	IR(BD)	VR(BD)=600V			-	-	100	μA
Collector to emitter saturation voltage	V_{CE}(sat)	Ic=30A	Upper side	Fig.2	-	1.7	2.5	V
			Lower side		-	2.2	3.1	
		Ic=15A, Tj=100°C	Upper side		-	1.4	-	
			Lower side		-	1.7	-	
Diode forward voltage	VF	IF=30A	Upper side	Fig.3	-	1.8	2.7	V
			Lower side		-	2.3	3.1	
		IF=15A, Tj=100°C	Upper side		-	1.45	-	
			Lower side		-	1.7	-	
Junction to case thermal resistance	θj-c(T)	IGBT		-	-	1.8	-	°C/W
	θj-c(D)	FWD		-	-	2.3	-	°C/W
Control (Pre-driver) section								
Pre-drive power supply consumption current	ID	VD1, 2, 3=15V		Fig.4	-	0.05	0.4	mA
		VD4=15V			-	1.0	4.0	
High level input voltage	Vin H	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 to V_{SS}		-	2.5	-	-	V
Low level input voltage	Vin L			-	-	-	0.8	V
Logic 1 input leakage current	I_{IN+}	VIN=+3.3V		-	-	100	195	μA
Logic 0 input leakage current	I_{IN-}	VIN=0V		-	-	-	1	μA
Bootstrap limiting resistor	RBoot			-	-	39	-	Ω
Gate resistor	Rb			-	-	30	-	Ω
	Rg			-	-	47	-	Ω
Protection section								
Over-current protection current	ISD	PW=100μs,RSD=0Ω		Fig.5	37	-	49	A
Over-current protection noise filter time constant	ISDNF			-	-	2.0	-	us
V_{dd} and V_{Bx} supply undervoltage positive going input threshold	V_{ddUV+} V_{BxUV+}			-	10.6	11.1	11.6	V
V_{dd} and V_{Bx} supply undervoltage negative going input threshold	V_{ddUV-} V_{BxUV-}			-	10.4	10.9	11.4	V
V_{dd} and V_{Bx} supply undervoltage $I_{lockout}$ hysteresis	V_{ddUVH} V_{BxUVH}			-	-	0.2	-	V
FAULT terminal sink current	IOSD	VFAULT=0.1V		-	1	1.5	-	mA
FAULT clearance delay time	FLTCLR	From time fault condition clear		-	1.3	1.65	2.5	ms
Switching character								
Switching time	tON	Io=30A, Inductive load		Fig.6	-	0.8	1.5	μs
	tOFF				-	1.0	2.0	μs
Turn-on switching loss	Eon	Io=30A, V_{CC}=300V, VD=15V, L=690μH			-	1070	-	μJ
Turn-off switching loss	Eoff				-	890	-	μJ
Total switching loss	Etot				-	1960	-	μJ
Turn-on switching loss	Eon	Io=15A, V_{CC}=300V, VD=15V, L=690μH, Tc=100°C			-	590	-	μJ
Turn-off switching loss	Eoff				-	590	-	μJ
Total switching loss	Etot				-	1180	-	μJ
Diode reverse recovery energy	Erec	Io=15A, V_{CC}=300V, VD=15V, L=690μH, Tc=100°C		-	-	95	-	μJ
Diode reverse recovery time	Trr				-	145	-	ns
Reverse bias safe operating area	RBSOA	Io = 49A, V_{CE}=450V		-	Full square			
Short circuit safe operating area	SCSOA	V_{CE}=400V, Tc=100°C		-	4	-	-	μs
Electric current output signal level	ISO	Io=30A		-	0.384	0.405	0.427	V

Reference voltage is V_{SS} terminal voltage unless otherwise specified.

*1: The lower side's V_{CE}(sat) and VF include a loss by the shunt resistance.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Notes

1. When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch.After protection operation ends,it returns automatically within about 18ms to 80ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once.However, the operation of pre-drive power supply low voltage protection (UVLO:with hysteresis about 0.2V) is as follows.

   Upper side:
   The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn ‘low’.

   Lower side:
   The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

2. When assembling the IPM on the heat sink with M4 type screw, tightening torque range is 0.79 Nm to 1.17 Nm.

3. The pre-drive low voltage protection is the feature to protect devices when the pre-driver supply voltage falls due to an operating malfunction.

Pin Assignment

Pin No.	Name	Description	Pin No.	Name	Description
1	VB1	High side floating supply voltage 1	44	P	Positive bus input voltage
2	VS1	High side floating supply offset voltage	43	P	Positive bus input voltage
3	-	Without pin	42	P	Positive bus input voltage
4	VB2	High side floating supply voltage 2	41	-	Without pin
5	VS2	High side floating supply offset voltage	40	N	Negative bus input voltage
6	-	Without pin	39	N	Negative bus input voltage
7	VB3	High side floating supply voltage 3	38	N	Negative bus input voltage
8	VS3	High side floating supply offset voltage	37	-	Without pin
9	-	Without pin	36	U	U-phase output
10	HIN1	Logic input high side driver-Phase1	35	U	U-phase output
11	HIN2	Logic input high side driver-Phase2	34	U	U-phase output
12	HIN3	Logic input high side driver-Phase3	33	-	Without pin
13	LIN1	Logic input low side driver-Phase1	32	V	V-phase output
14	LIN2	Logic input low side driver-Phase2	31	V	V-phase output
15	LIN3	Logic input low side driver-Phase3	30	V	V-phase output
16	FAULT	Fault out (open drain)	29	-	Without pin
17	ISO	Current monitor pin	28	W	W-phase output
18	TH	Thermistor out	27	W	W-phase output
19	VDD	+15V main supply	26	W	W-phase output
20	VSS	Negative main supply	25	-	Without pin
21	ISD	Over-current protection level setting pin	24	NC	-
22	NC	-	23	NC	-

Test Circuit

(The tested phase: U+ shows the upper side of the U phase and U− shows the lower side of the U phase.)

■ **ICE / IR(BD)**

	U+	V+	W+	U-	V-	W-
M	42	42	42	34	30	26
N	34	30	26	38	38	38

	U(BD)	V(BD)	W(BD)
M	1	4	7
N	20	20	20

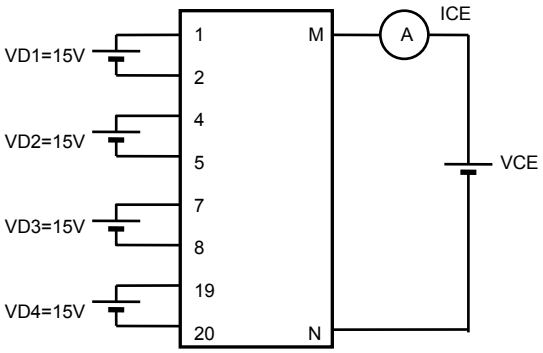


Fig.1

■ **VCE(SAT) (Test by pulse)**

	U+	V+	W+	U-	V-	W-
M	42	42	42	34	30	26
N	34	30	26	17	19	21
m	10	11	12	13	14	15

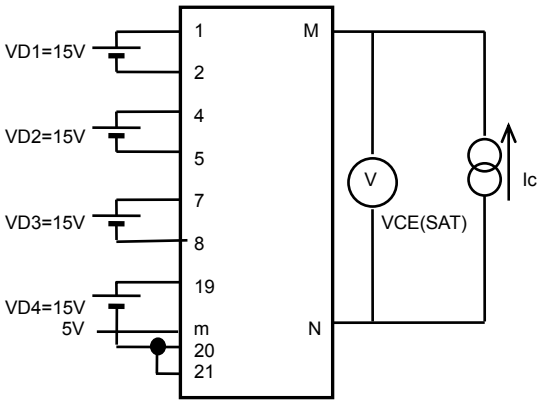


Fig.2

■ **VF (Test by pulse)**

	U+	V+	W+	U-	V-	W-
M	42	42	42	34	30	26
N	34	30	26	38	38	38

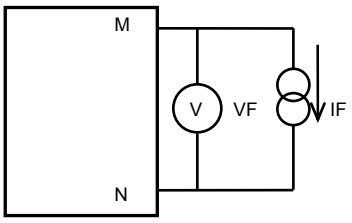


Fig.3

■ **ID**

	VD1	VD2	VD3	VD4
M	1	4	7	19
N	2	5	8	20

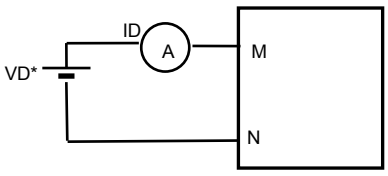
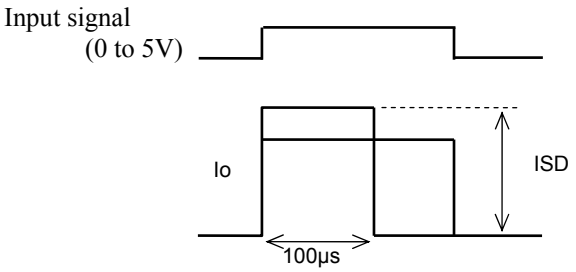


Fig.4

■ **ISD**



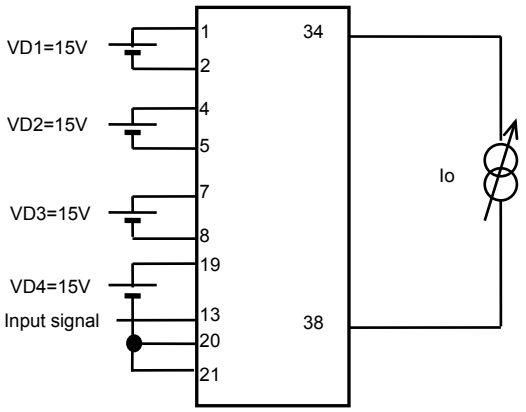
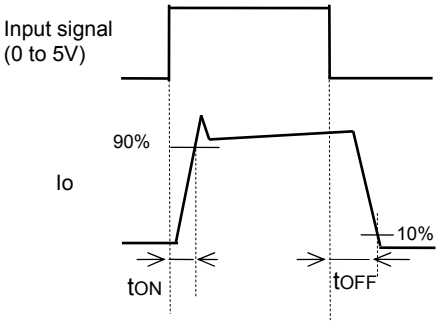


Fig.5

■ **Switching time (The circuit is a representative example of the lower side U phase.)**



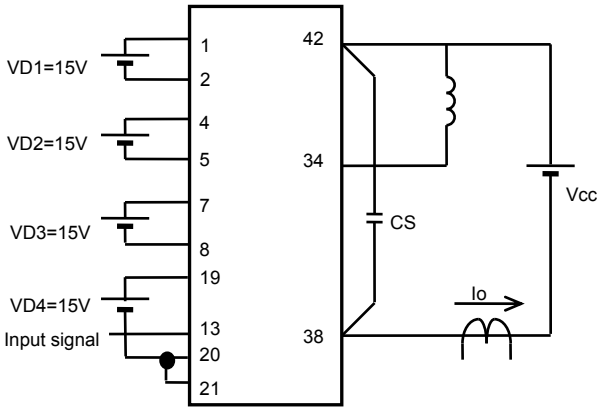
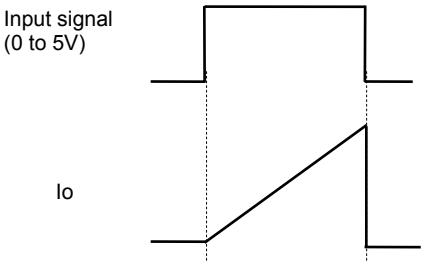


Fig.6

■ **RB-SOA (The circuit is a representative example of the lower side U phase.)**



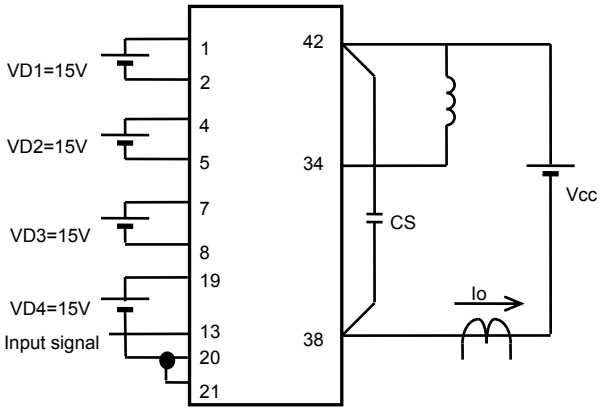


Fig.7

Logic Timing Chart

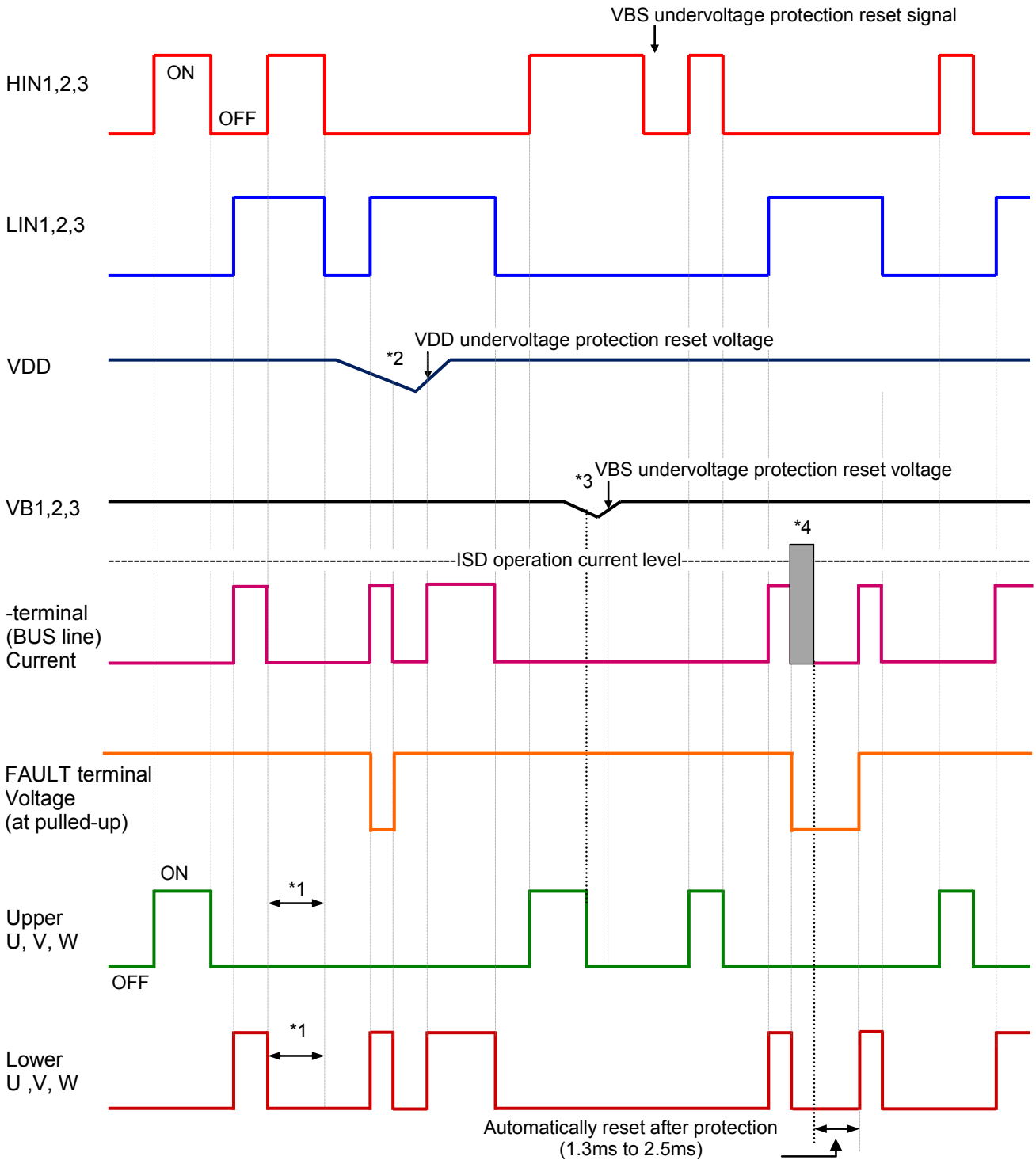


Fig. 8

Notes

*1 : Diagram shows the prevention of shoot-through via control logic. More dead time to account for switching delay needs to be added externally.

*2 : When V_{DD} decreases all gate output signals will go low and cut off all of 6 IGBT outputs. part. When V_{DD} rises the operation will resume immediately.

*3 : When the upper side gate voltage at VB1, VB2 and VB3 drops only, the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gat voltage rises.

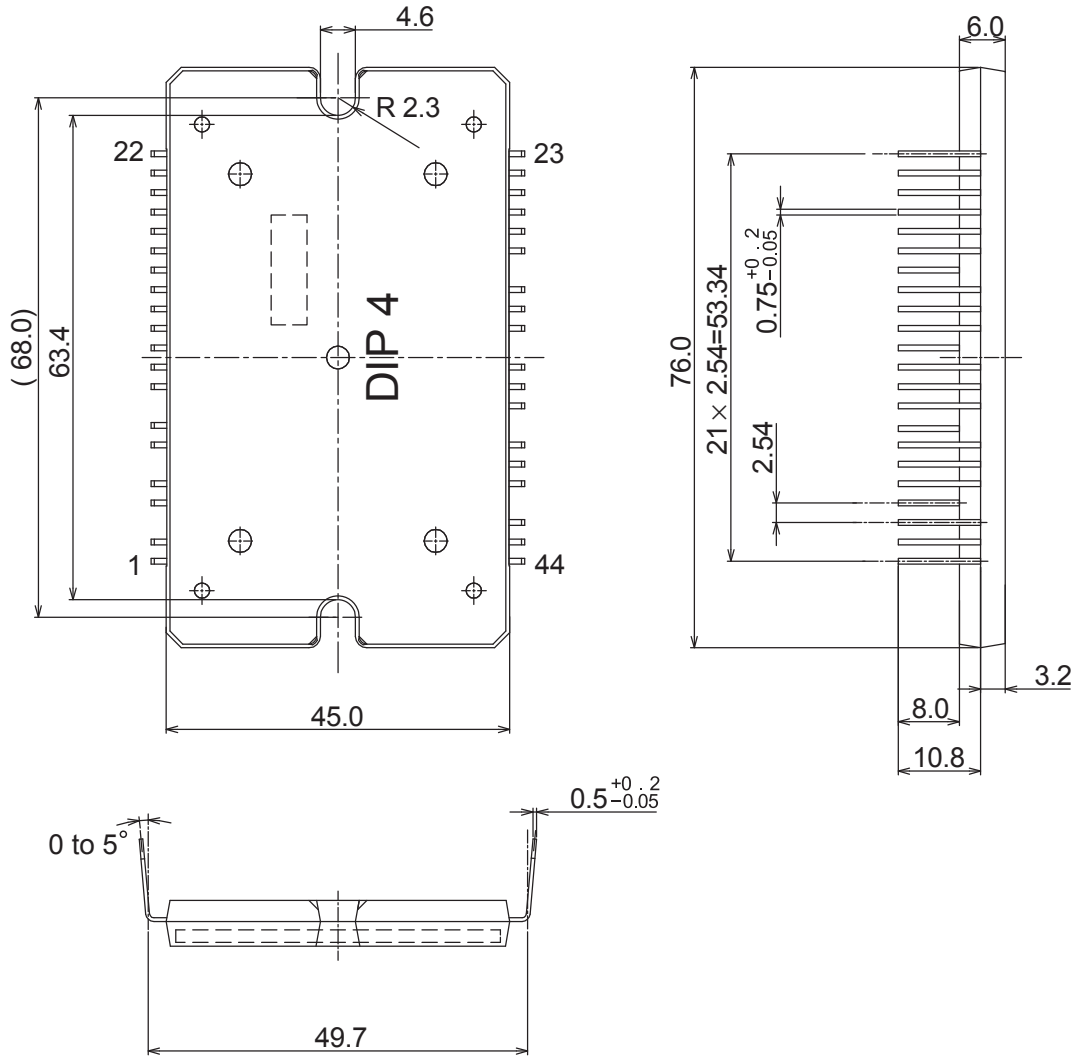
*4 : In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 1.3 to 2.5ms after the over current condition is removed.

Package Dimensions

unit : mm

HYBRID INTEGRATED MODULE
CASE MODAW
ISSUE O

Missing Pin : 3, 6, 9, 29, 33, 37, 41



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5F1U3C3D-E	MODAW, 610AC-DIP4-UL (Pb-Free)	6 / Tube