

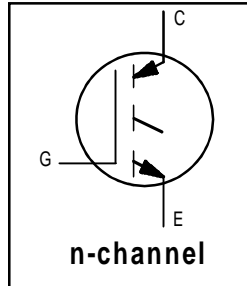
## IRG4BC30U-S

INSULATED GATE BIPOLAR TRANSISTOR

UltraFast Speed IGBT

### Features

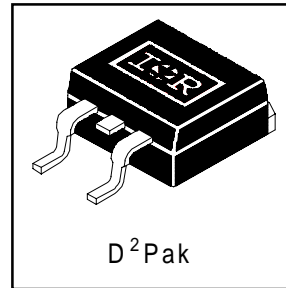
- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200 kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- Industry standard D<sup>2</sup>Pak package



$V_{CES} = 600V$
$V_{CE(on)} \text{ typ.} = 1.95V$
@ $V_{GE} = 15V, I_C = 12A$

### Benefits

- Generation 4 IGBT's offer highest efficiency available
- IGBT's optimized for specified application conditions
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBT's



### Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{CES}$	Collector-to-Emitter Breakdown Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	23	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	12	
$I_{CM}$	Pulsed Collector Current ①	92	
$I_{LM}$	Clamped Inductive Load Current ②	92	
$V_{GE}$	Gate-to-Emitter Voltage	$\pm 20$	V
$E_{ARV}$	Reverse Voltage Avalanche Energy ③	10	mJ
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	100	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	42	
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient, ( PCB Mounted, steady-state)*	—	40	

\* When mounted on 1" square PCB (FR-4 or G-10 Material ). For recommended footprint and soldering techniques refer to application note #AN-994.

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

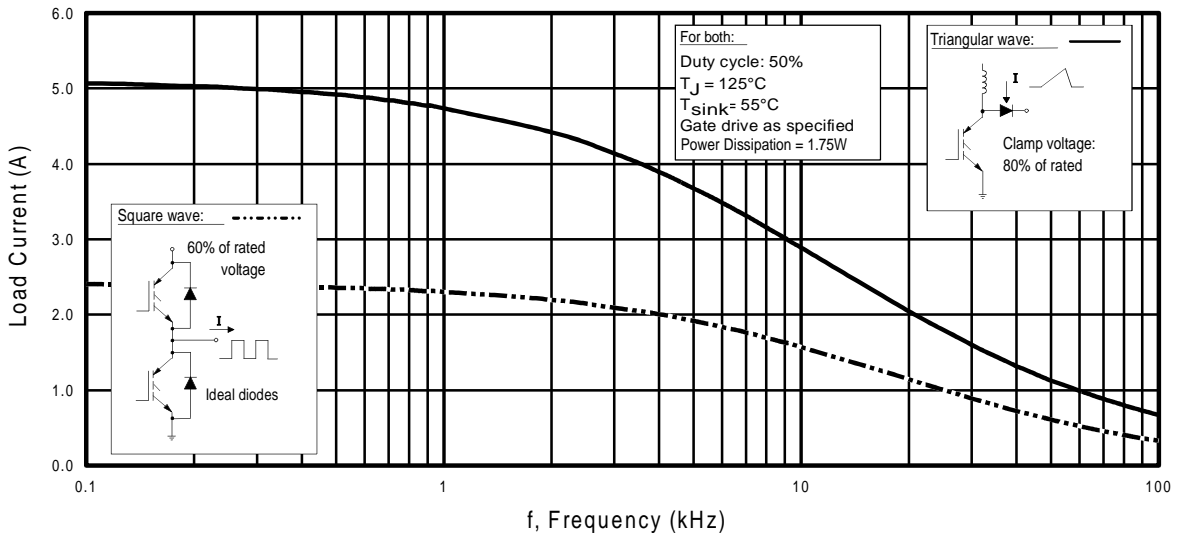
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu\text{A}$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage <sup>④</sup>	18	—	—	V	$V_{GE} = 0V, I_C = 1.0A$
$DV_{(BR)CES/DT_J}$	Temperature Coeff. of Breakdown Voltage	—	0.63	—	V/ $^\circ\text{C}$	$V_{GE} = 0V, I_C = 1.0mA$
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.95	2.1	V	$I_C = 12A$ $V_{GE} = 15V$ See Fig.2, 5
		—	2.52	—		
		—	2.09	—		
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu\text{A}$
$DV_{GE(th)/DT_J}$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/ $^\circ\text{C}$	$V_{CE} = V_{GE}, I_C = 250\mu\text{A}$
$g_{fe}$	Forward Transconductance <sup>⑤</sup>	3.1	8.6	—	S	$V_{CE} = 100V, I_C = 12A$
$I_{CES}$	Zero Gate Voltage Collector Current	—	—	250	$\mu\text{A}$	$V_{GE} = 0V, V_{CE} = 600V$
		—	—	2.0		$V_{GE} = 0V, V_{CE} = 10V, T_J = 25^\circ\text{C}$
		—	—	1000		$V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$
$I_{GES}$	Gate-to-Emitter Leakage Current	—	—	$\pm 100$	nA	$V_{GE} = \pm 20V$

## Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

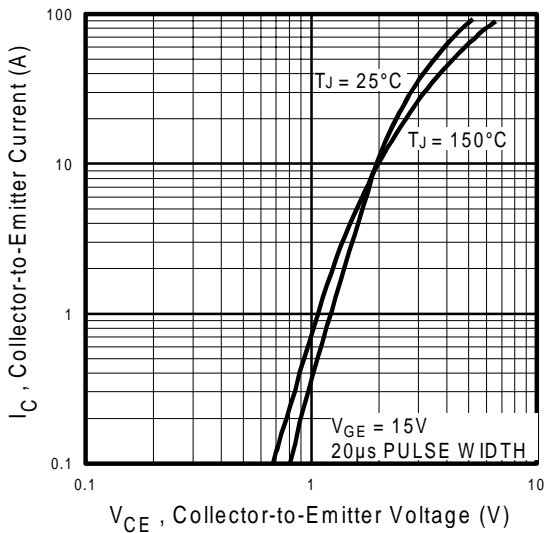
	Parameter	Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge (turn-on)	—	50	75	nC	$I_C = 12A$ $V_{CC} = 400V$ See Fig.8 $V_{GE} = 15V$
$Q_{ge}$	Gate - Emitter Charge (turn-on)	—	8.1	12		
$Q_{gc}$	Gate - Collector Charge (turn-on)	—	18	27		
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$T_J = 25^\circ\text{C}$ $I_C = 12A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 23\Omega$ Energy losses include "tail" See Fig. 10, 11, 13, 14
$t_r$	Rise Time	—	9.6	—		
$t_{d(off)}$	Turn-Off Delay Time	—	78	120		
$t_f$	Fall Time	—	97	150	mJ	See Fig. 13, 14
$E_{on}$	Turn-On Switching Loss	—	0.16	—		
$E_{off}$	Turn-Off Switching Loss	—	0.20	—		
$E_{ts}$	Total Switching Loss	—	0.36	0.50	ns	$T_J = 150^\circ\text{C},$ $I_C = 12A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 23\Omega$ Energy losses include "tail"
$t_{d(on)}$	Turn-On Delay Time	—	20	—		
$t_r$	Rise Time	—	13	—		
$t_{d(off)}$	Turn-Off Delay Time	—	180	—	mJ	See Fig. 13, 14
$t_f$	Fall Time	—	140	—		
$E_{ts}$	Total Switching Loss	—	0.73	—		
$L_E$	Internal Source Inductance	—	7.5	—	nH	Measured 5mm from package
$C_{ies}$	Input Capacitance	—	1100	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ See Fig.7 $f = 1.0\text{MHz}$
$C_{oes}$	Output Capacitance	—	73	—		
$C_{res}$	Reverse Transfer Capacitance	—	14	—		

### Notes:

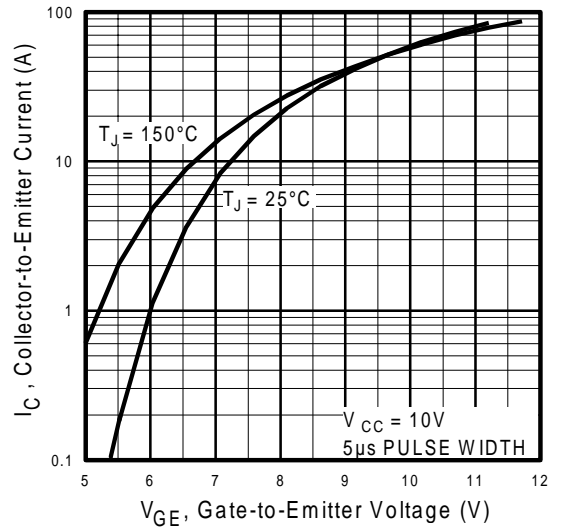
- ① Repetitive rating;  $V_{GE} = 20V$ , pulse width limited by max. junction temperature. ( See fig. 13b )
- ②  $V_{CC} = 80\%(V_{CES}), V_{GE} = 20V, L = 10\mu\text{H}, R_G = 23\Omega,$  (See fig. 13a)
- ③ Repetitive rating; pulse width limited by maximum junction temperature.
- ④ Pulse width  $\leq 80\mu\text{s}$ ; duty factor  $\leq 0.1\%$ .
- ⑤ Pulse width  $5.0\mu\text{s}$ , single shot.



**Fig. 1 - Typical Load Current vs. Frequency**  
(For square wave,  $I = I_{\text{RMS}}$  of fundamental; for triangular wave,  $I = I_{\text{PK}}$ )



**Fig. 2 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**

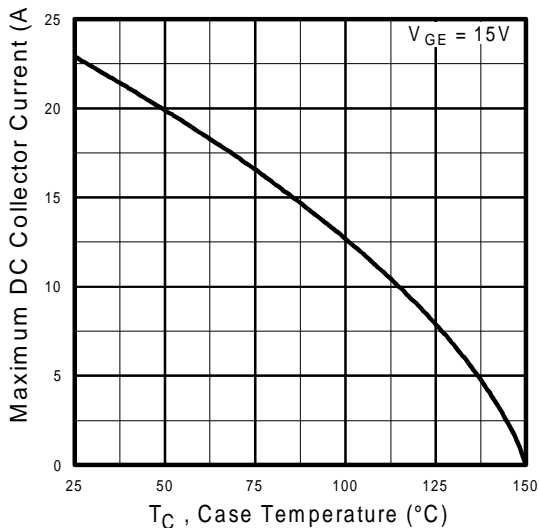


Fig. 4 - Maximum Collector Current vs. Case Temperature

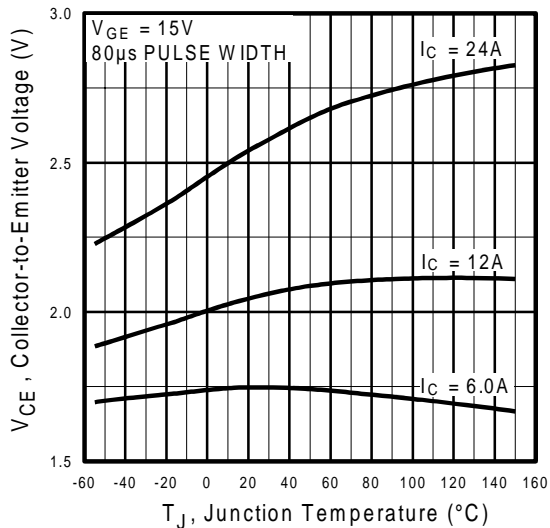


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

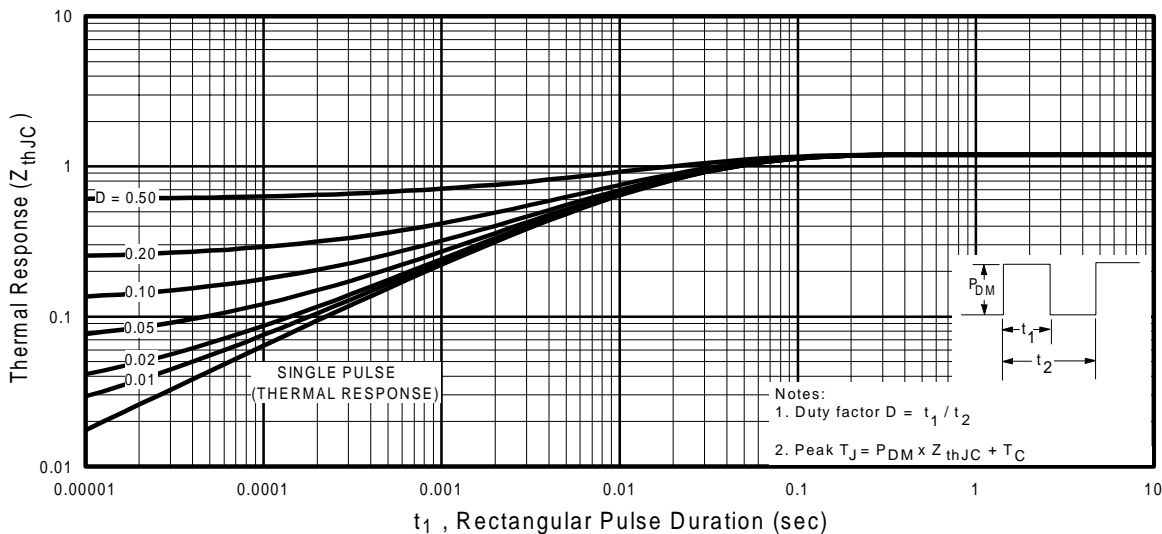
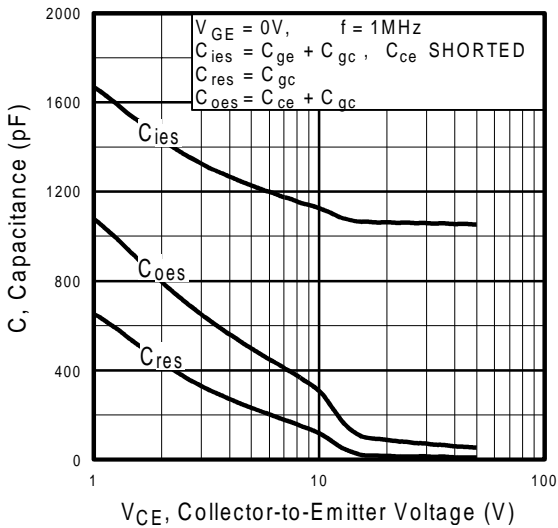
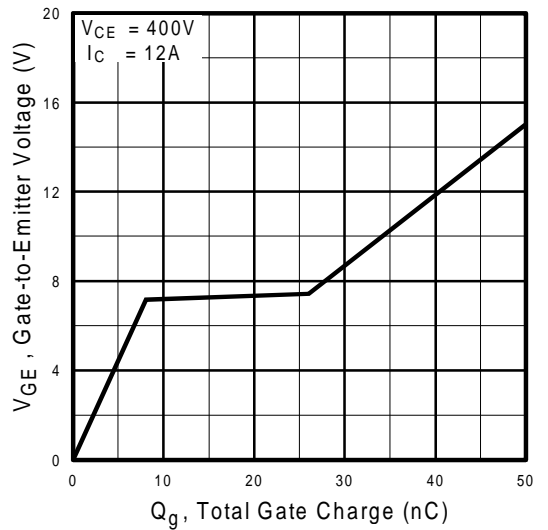


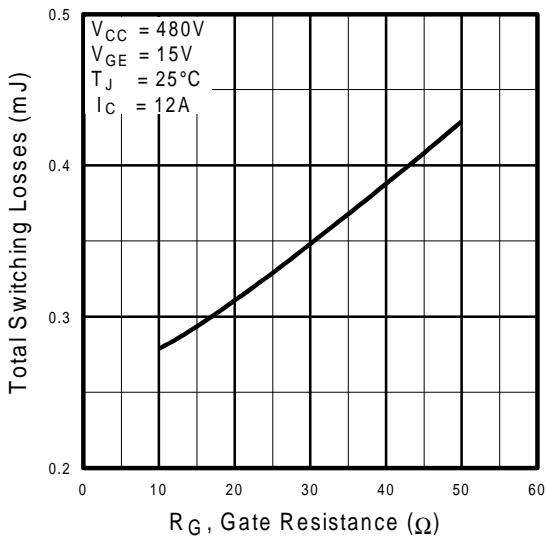
Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



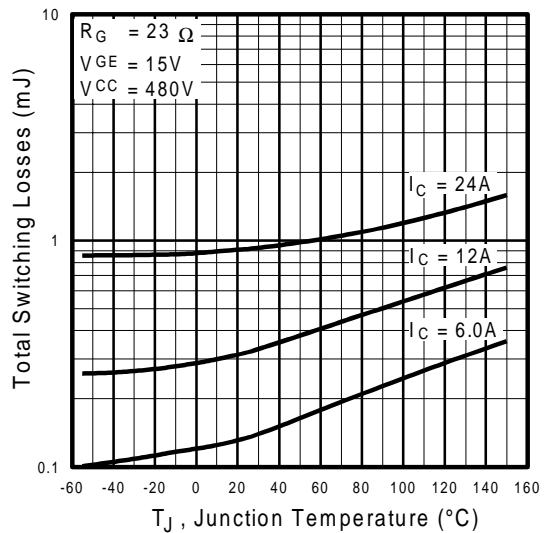
**Fig. 7** - Typical Capacitance vs. Collector-to-Emitter Voltage



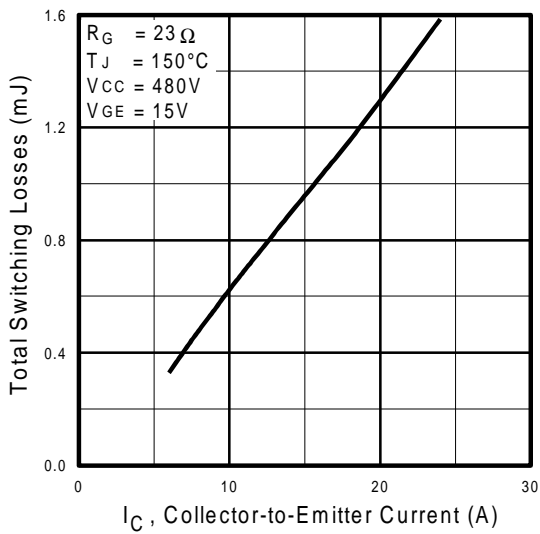
**Fig. 8** - Typical Gate Charge vs. Gate-to-Emitter Voltage



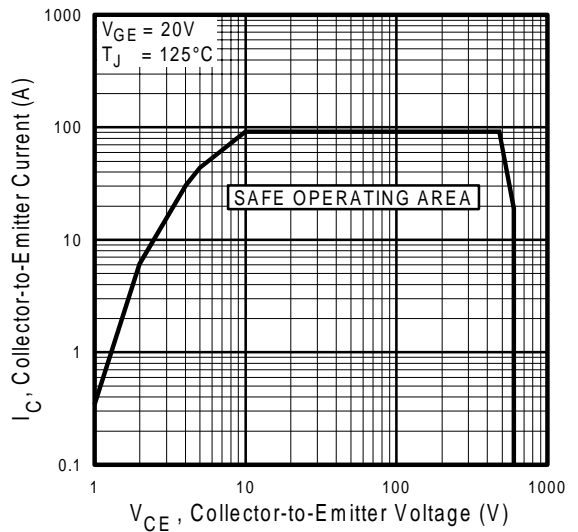
**Fig. 9** - Typical Switching Losses vs. Gate Resistance



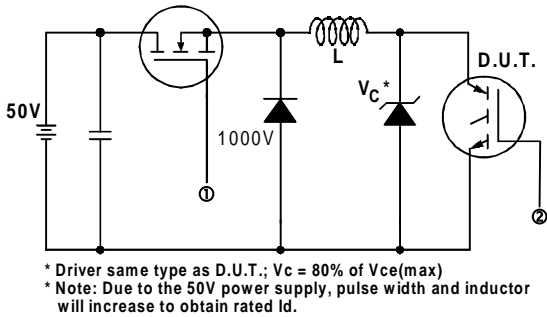
**Fig. 10** - Typical Switching Losses vs. Junction Temperature



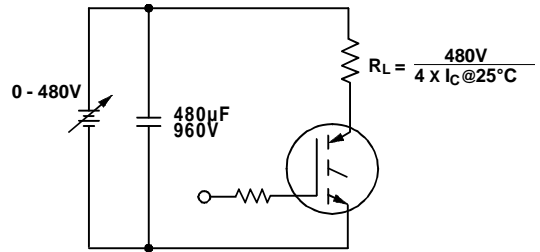
**Fig. 11** - Typical Switching Losses vs. Collector-to-Emitter Current



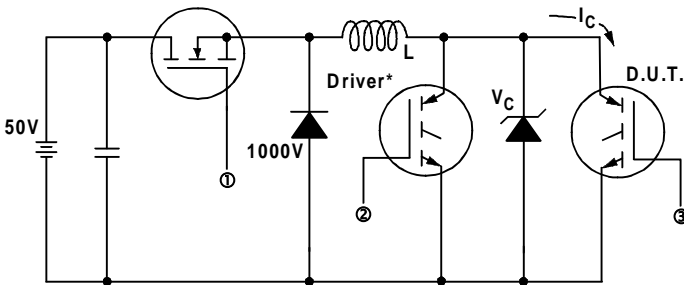
**Fig. 12** - Turn-Off SOA



**Fig. 13a** - Clamped Inductive Load Test Circuit

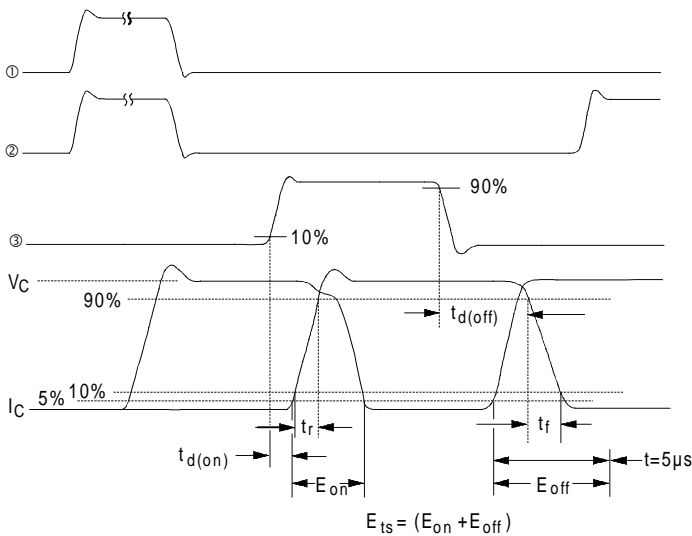


**Fig. 13b** - Pulsed Collector Current Test Circuit



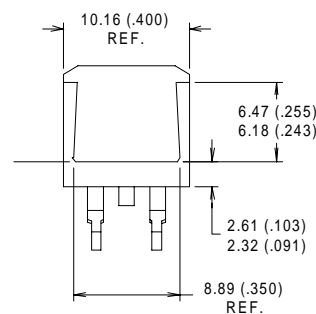
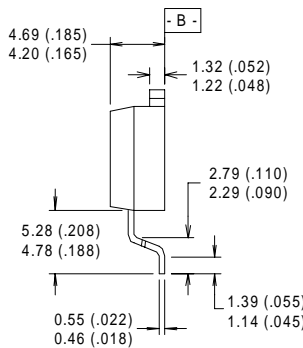
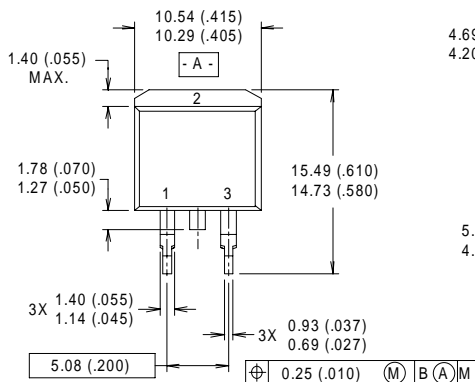
**Fig. 14a** - Switching Loss Test Circuit

\* Driver same type as D.U.T.,  $V_C = 480V$

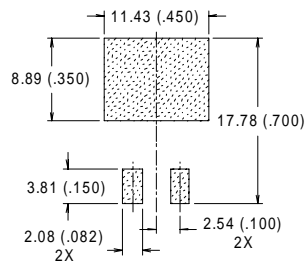


**Fig. 14b** - Switching Loss Waveforms

**D<sup>2</sup>Pak Package Outline**



**MINIMUM RECOMMENDED FOOTPRINT**



**NOTES:**

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

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Note: For the most current drawings please refer to the IR website at:  
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