

REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS SURFACE MOUNT (LCC-18)

IRFE9210 200V, P-CHANNEL

Product Summary

Part Number	BVDSS	RDS(on)	Id
IRFE9210	-200V	3.0Ω	-1.3A

The leadless chip carrier (LCC) package represents the logical next step in the continual evolution of surface mount technology. Designed to be a close replacement for the TO-39 package, the LCC will give designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the LCC package to meet the specific needs of the power market by increasing the size of the bottom source pad, thereby enhancing the thermal and electrical performance. The lid of the package is grounded to the source to reduce RF interference.



LCC-18

Features:

- Surface Mount
- Small Footprint
- Alternative to TO-39 Package
- Hermetically Sealed
- Dynamic dv/dt Rating
- Avalanche Energy Rating
- Simple Drive Requirements
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
I_D @ $V_{GS} = -10V, T_C = 25^\circ C$	Continuous Drain Current	-1.3	A
I_D @ $V_{GS} = -10V, T_C = 100^\circ C$	Continuous Drain Current	-0.84	
I_{DM}	Pulsed Drain Current ①	-5.2	
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	11	W
	Linear Derating Factor	0.09	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	72	mJ
I_{AR}	Avalanche Current ①	-	A
E_{AR}	Repetitive Avalanche Energy ①	-	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J	Operating Junction	-55 to 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5 S)	
	Weight	0.42(typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _j	Temperature Coefficient of Breakdown Voltage	—	-0.22	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DSON}	Static Drain-to-Source On-State Resistance	—	—	3.0	Ω	V _{GS} = -10V, I _D = -0.84A④
		—	—	3.45		V _{GS} = -10V, I _D = -1.3A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	0.7	—	—	S (Ω)	V _{DS} > -15V, I _{DS} = -0.84A④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V _{DS} = -160V, V _{GS} = 0V
		—	—	-250		V _{DS} = -160V V _{GS} = 0V, T _j = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 20V
Q _g	Total Gate Charge	—	—	8.9	nC	V _{GS} = -10V, I _D = -1.3A V _{DS} = -100V
Q _{gs}	Gate-to-Source Charge	—	—	2.1		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	3.9		
t _{d(on)}	Turn-On Delay Time	—	—	15	ns	V _{DD} = -100V, I _D = -1.3A, R _G = 7.5Ω
t _r	Rise Time	—	—	25		
t _{d(off)}	Turn-Off Delay Time	—	—	40		
t _f	Fall Time	—	—	15		
L _S + L _D	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	170	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz
C _{oss}	Output Capacitance	—	54	—		
C _{rss}	Reverse Transfer Capacitance	—	17	—		

Source-Drain Diode Ratings and Characteristics**Thermal Resistance**

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction to Case	—	—	11	°C/W	
R _{thJ-PCB}	Junction to PC Board	—	—	27		Soldered to a copper clad PC board

For footnotes refer to the last page

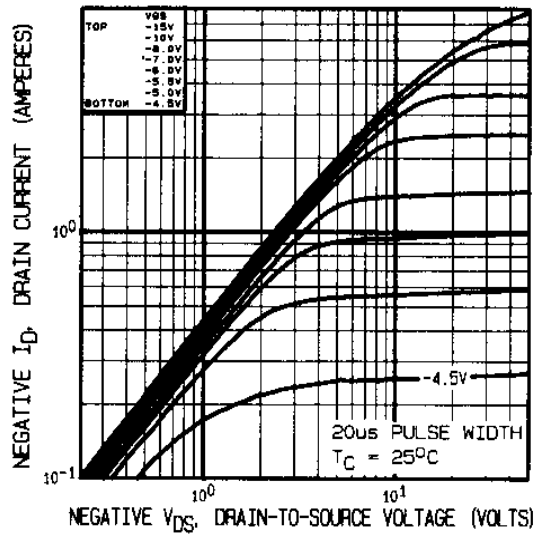


Fig 1. Typical Output Characteristics

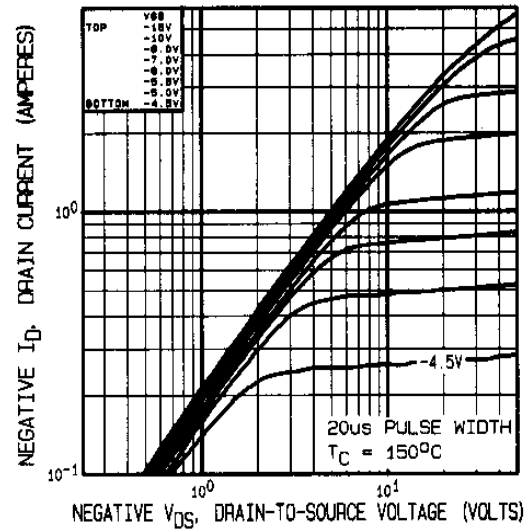


Fig 2. Typical Output Characteristics

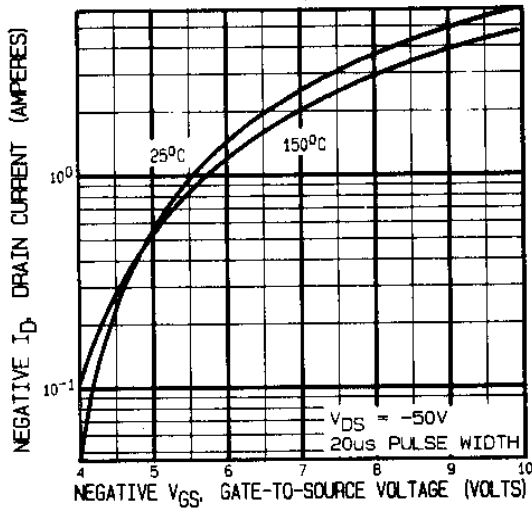


Fig 3. Typical Transfer Characteristics

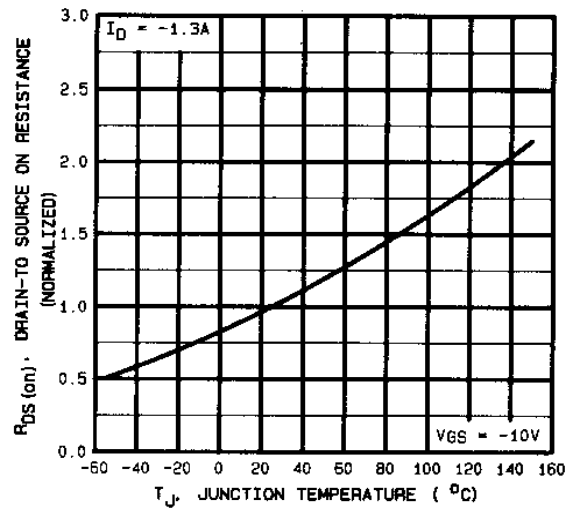


Fig 4. Normalized On-Resistance
Vs. Temperature

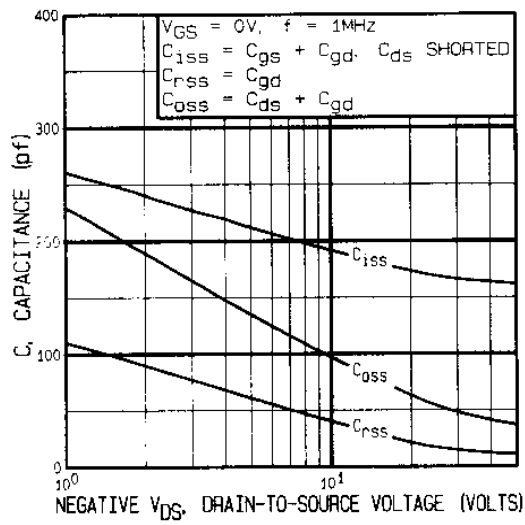


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

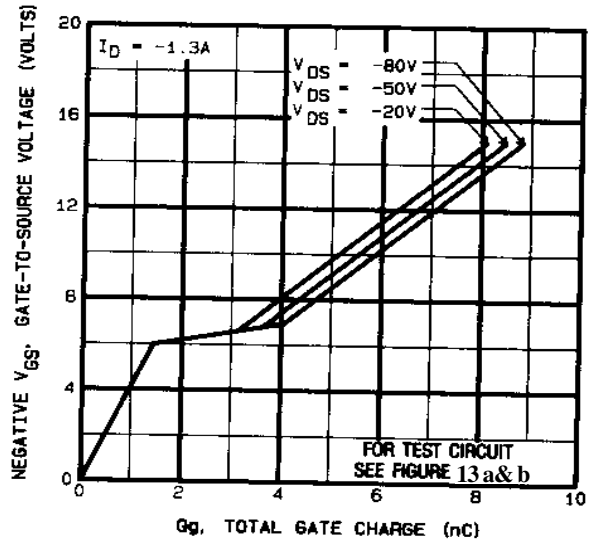


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

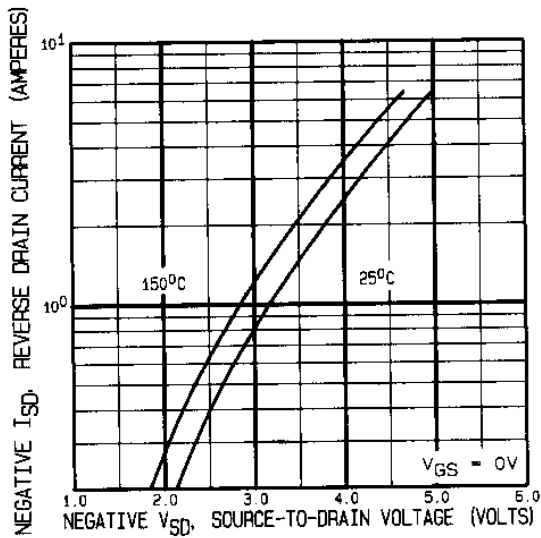


Fig 7. Typical Source-Drain Diode Forward Voltage

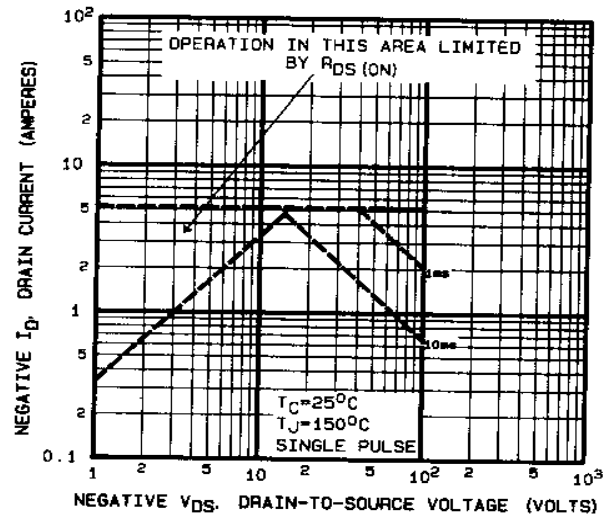


Fig 8. Maximum Safe Operating Area

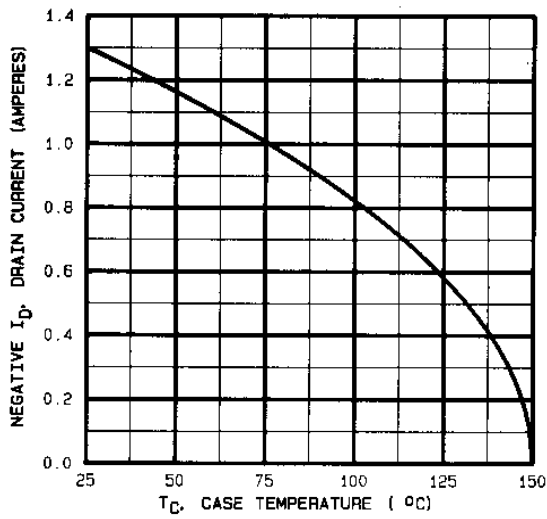


Fig 9. Maximum Drain Current Vs. Case Temperature

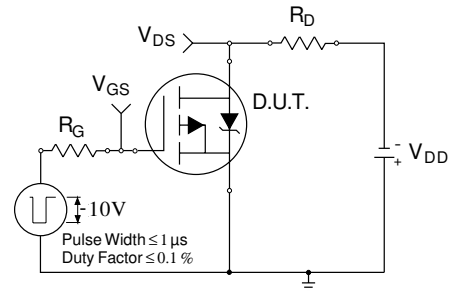


Fig 10a. Switching Time Test Circuit

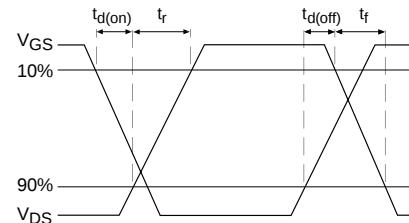


Fig 10b. Switching Time Waveforms

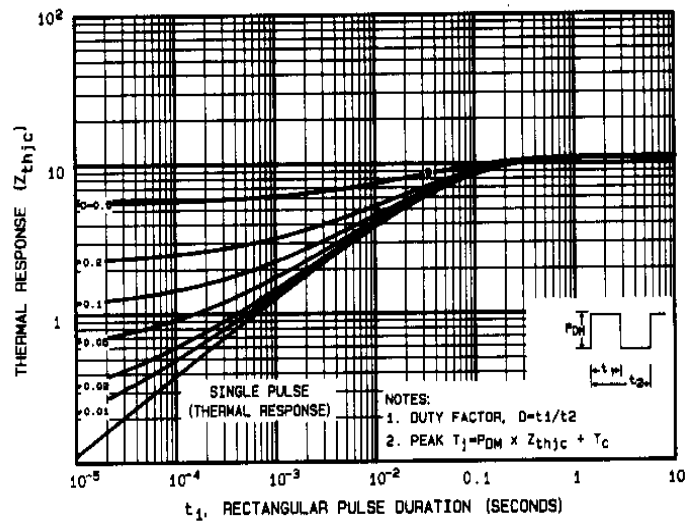


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

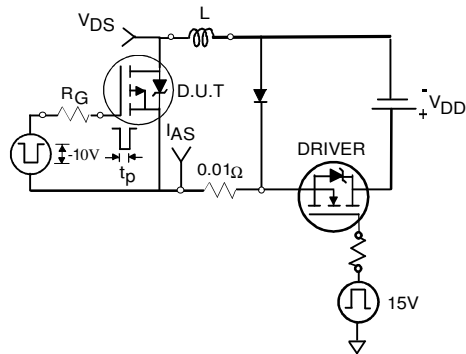


Fig 12a. Unclamped Inductive Test Circuit

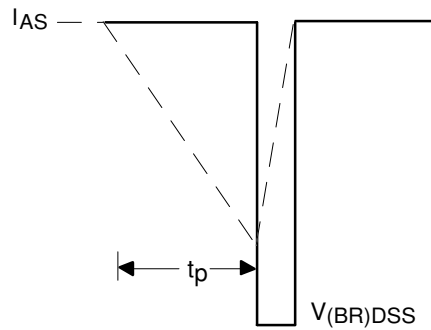


Fig 12b. Unclamped Inductive Waveforms

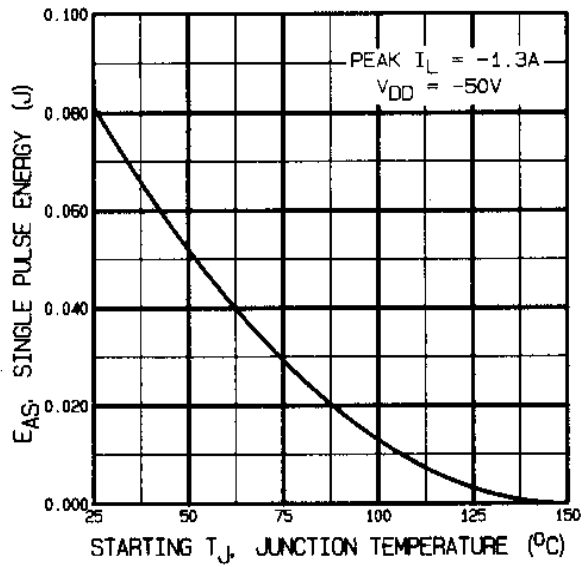
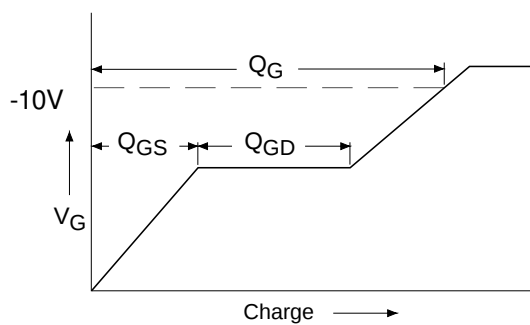
Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

Fig 13a. Basic Gate Charge Waveform

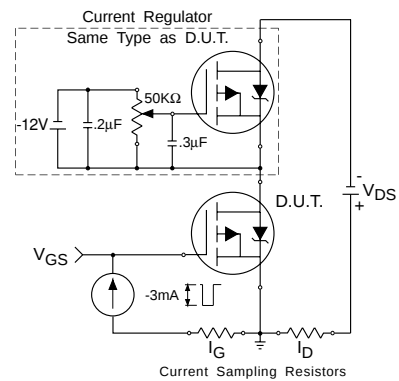
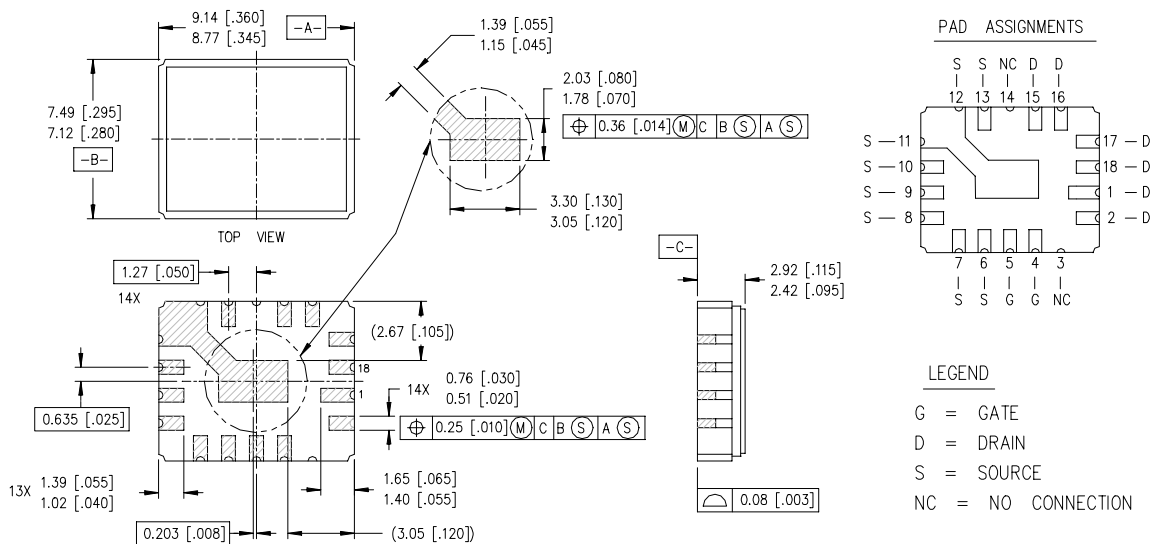


Fig 13b. Gate Charge Test Circuit

Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -50V$, starting $T_J = 25^\circ C$,
Peak $I_L = -1.3A$,
- ③ $I_{SD} \leq -1.3A$, $di/dt \leq -70A/\mu s$,
 $V_{DD} \leq -200V$, $T_J \leq 150^\circ C$
Suggested $R_G = 7.5 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — LCC-18



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].