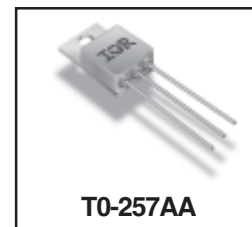


**RADIATION HARDENED
POWER MOSFET
THRU-HOLE (TO-257AA)**

**IRHY57133CMSE
JANSR2N7488T3
130V, N-CHANNEL
REF: MIL-PRF-19500/705
R5 TECHNOLOGY**

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number
IRHY57133CMSE	100K Rads (Si)	0.09 Ω	18A*	JANSR2N7488T3



International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Ultra Low $R_{DS(on)}$
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Eyelets
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ $V_{GS} = 12V$, $T_C = 25^\circ C$	Continuous Drain Current	18*	A
I_D @ $V_{GS} = 12V$, $T_C = 100^\circ C$	Continuous Drain Current	12	
I_{DM}	Pulsed Drain Current ①	72	
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
EAS	Single Pulse Avalanche Energy ②	80	mJ
I_{AR}	Avalanche Current ①	18	A
EAR	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	8.0	V/ns
T_J	Operating Junction	-55 to 150	°C
T_{STG}	Storage Temperature Range		
	Lead Temperature	300 (0.063in./1.6mm from case for 10sec)	
	Weight	4.3(Typical)	g

* Current is limited by package

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	130	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.16	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.09	Ω	V _{GS} = 12V, I _D = 12A ④
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
g _{fs}	Forward Transconductance	8.5	—	—	S (r)	V _{DS} ≥ 15V, I _{DS} = 12A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 104V, V _{GS} = 0V
		—	—	25		V _{DS} = 104V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	48	nC	V _{GS} = 12V, I _D = 18A V _{DS} = 65V
Q _{gs}	Gate-to-Source Charge	—	—	16		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	18		
t _{d(on)}	Turn-On Delay Time	—	—	20	ns	V _{DD} = 65V, I _D = 18A, V _{GS} = 12V, R _G = 7.5Ω
t _r	Rise Time	—	—	70		
t _{d(off)}	Turn-Off Delay Time	—	—	25		
t _f	Fall Time	—	—	35		
L _S + L _D	Total Inductance	—	6.8	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C _{iss}	Input Capacitance	—	965	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	300	—		
C _{rss}	Reverse Transfer Capacitance	—	20	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	18*	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	72		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 18A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	200	nS	T _J = 25°C, I _F = 18A, di/dt ≤ 100A/μs V _{DD} ≤ 25V ④
Q _{RR}	Reverse Recovery Charge	—	—	1.5	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

* Current is limited by package

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	1.67	°C/W	
R _{thJA}	Junction-to-Ambient	—	—	80		Typical Socket Mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

Radiation Characteristics

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International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ $T_j = 25^\circ\text{C}$, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads (Si)		Units	Test Conditions ⑧
		Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	130	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5		$V_{GS} = V_{DS}, I_D = 1.0mA$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	10	μA	$V_{DS} = 104V, V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.09	Ω	$V_{GS} = 12V, I_D = 12A$
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-257AA)	—	0.09	Ω	$V_{GS} = 12V, I_D = 12A$
V_{SD}	Diode Forward Voltage ④	—	1.2	V	$V_{GS} = 0V, I_D = 18A$

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V_{DS} (V)				
				@ $V_{GS} = 0V$	@ $V_{GS} = -5V$	@ $V_{GS} = -10V$	@ $V_{GS} = -15V$	@ $V_{GS} = -20V$
Br	36.7	309	39.5	130	130	130	130	130
I	59.8	341	32.5	130	130	130	100	50
Au	82.3	350	28.4	130	120	30	—	—

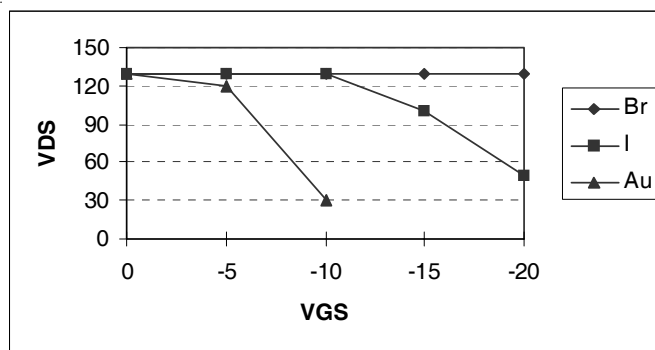


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

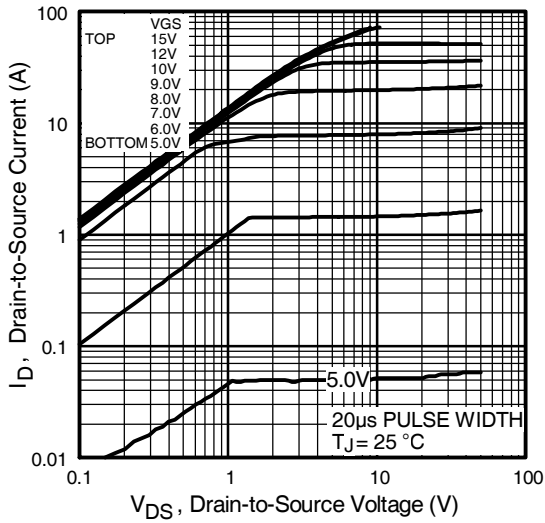


Fig 1. Typical Output Characteristics

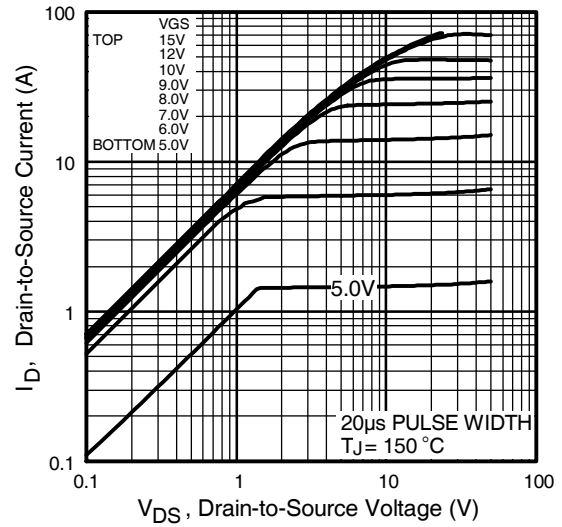


Fig 2. Typical Output Characteristics

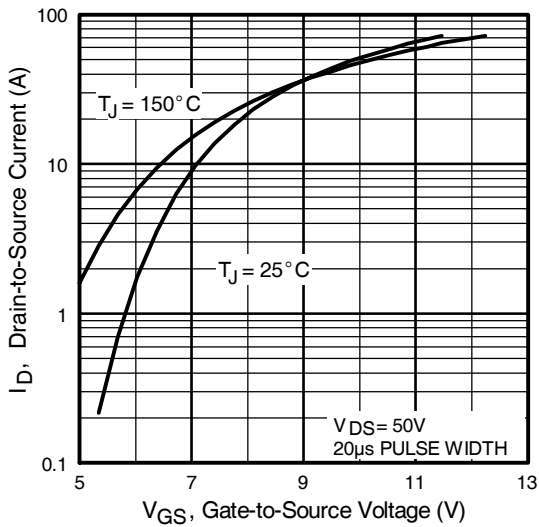


Fig 3. Typical Transfer Characteristics

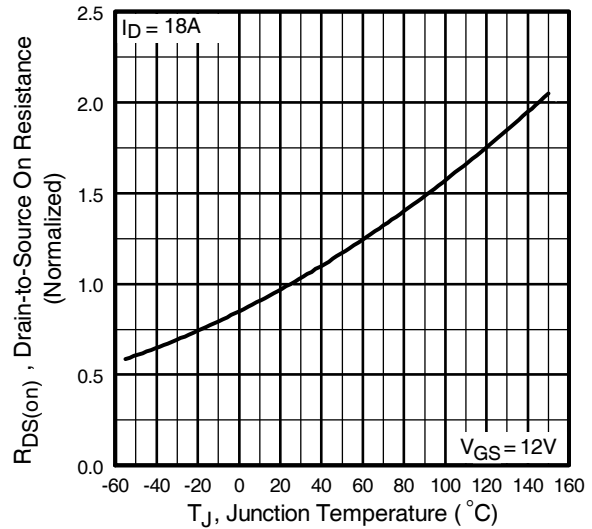


Fig 4. Normalized On-Resistance Vs. Temperature

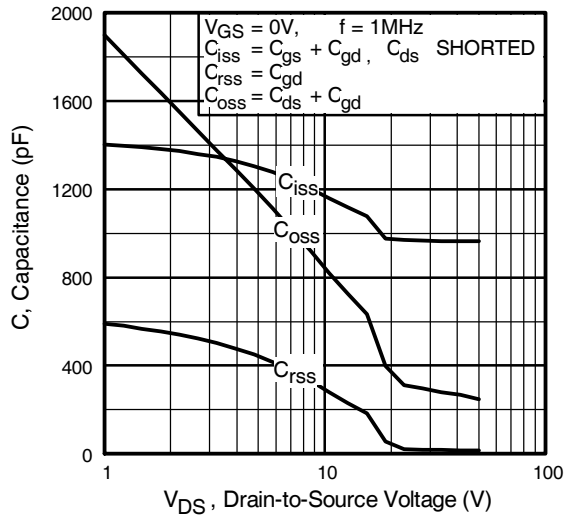


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

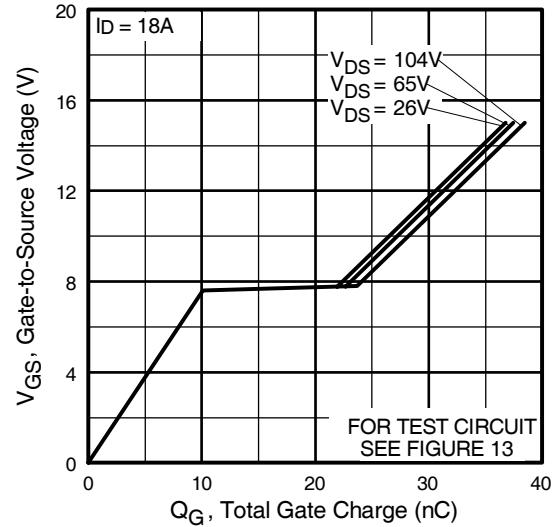


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

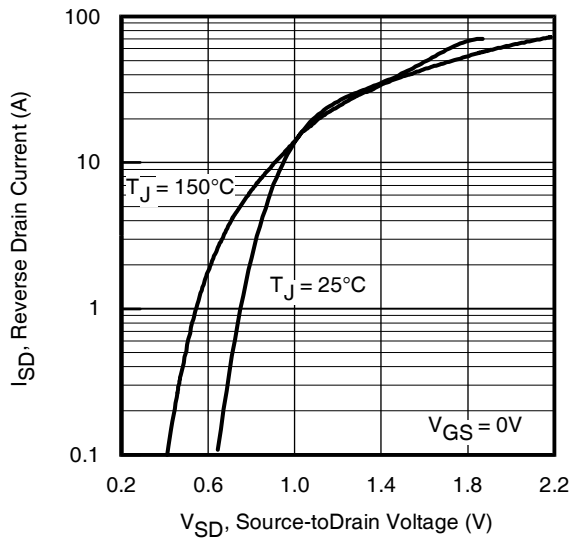


Fig 7. Typical Source-Drain Diode Forward Voltage

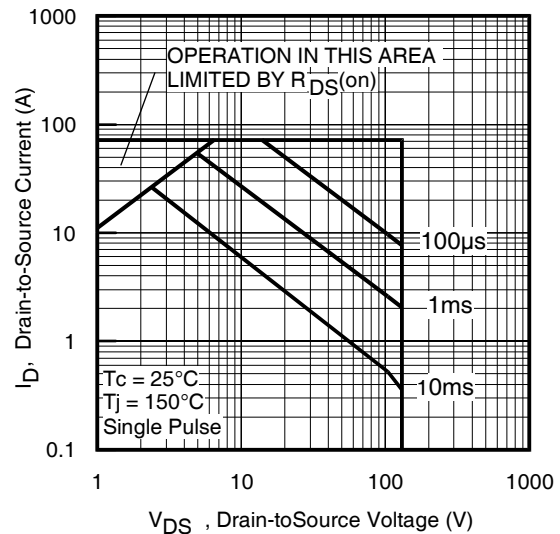


Fig 8. Maximum Safe Operating Area

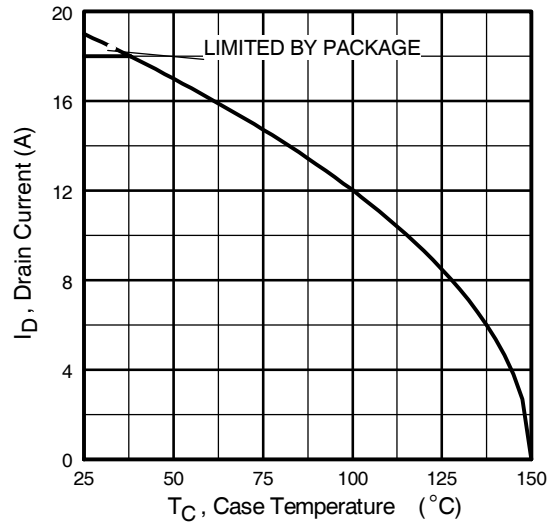


Fig 9. Maximum Drain Current Vs. Case Temperature

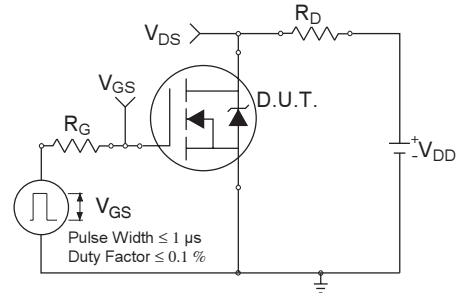


Fig 10a. Switching Time Test Circuit

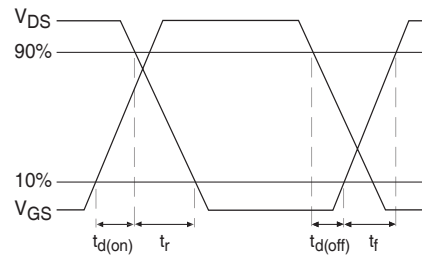


Fig 10b. Switching Time Waveforms

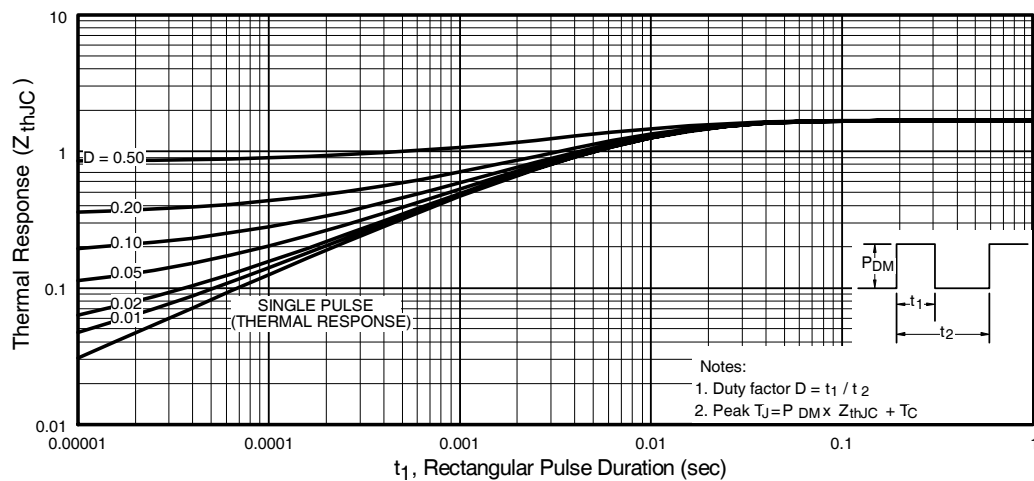


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Pre-Irradiation

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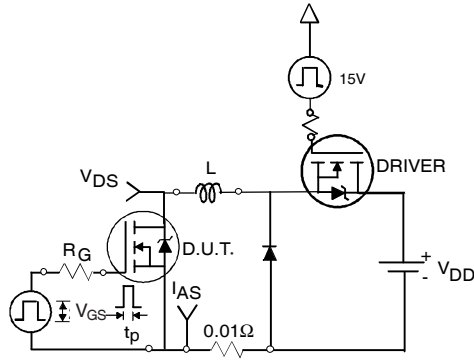


Fig 12a. Unclamped Inductive Test Circuit

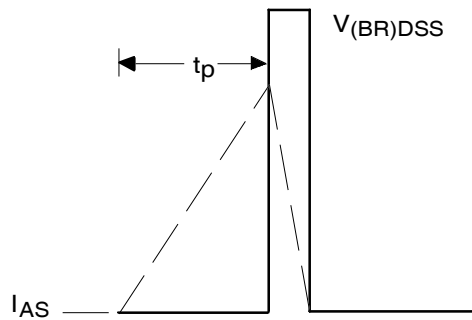


Fig 12b. Unclamped Inductive Waveforms

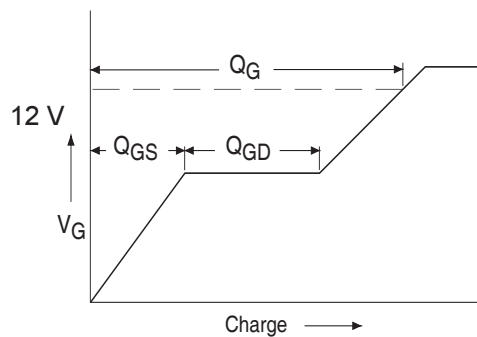


Fig 13a. Basic Gate Charge Waveform

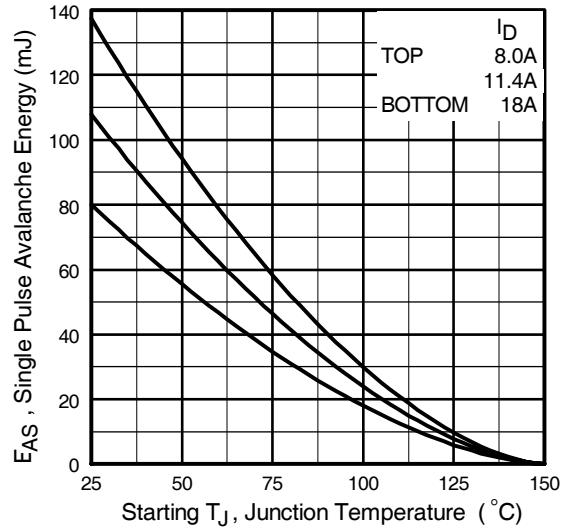


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

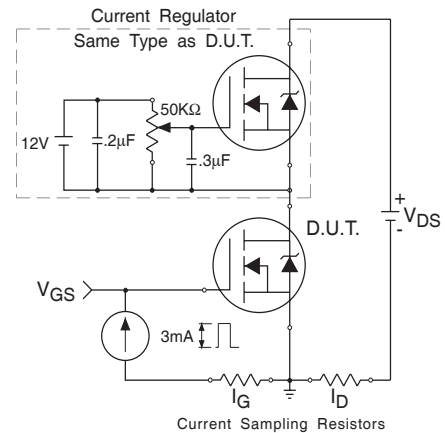
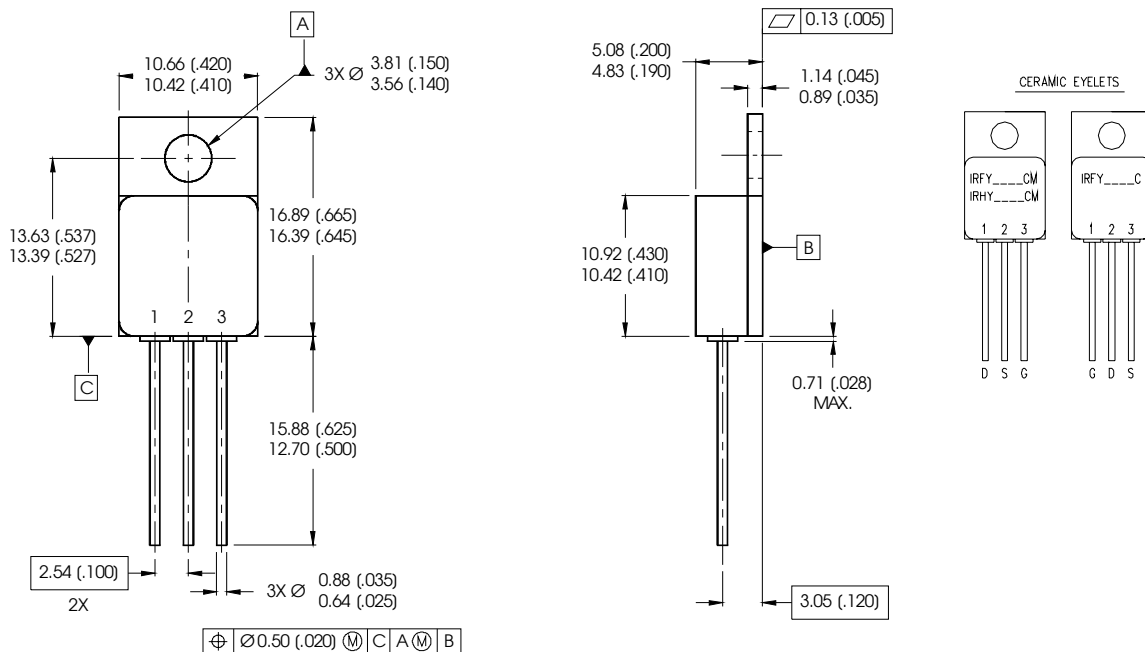


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 0.5\text{ mH}$
Peak $I_L = 18A$, $V_{GS} = 12V$
- ③ $I_{SD} \leq 18A$, $di/dt \leq 280A/\mu s$,
 $V_{DD} \leq 130V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300\text{ }\mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
104 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — TO-257AA**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

LEGEND

- 1 = DRAIN
2 = SOURCE
3 = GATE

International
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Data and specifications subject to change without notice. 06/2004