

**RADIATION HARDENED
POWER MOSFET
SURFACE MOUNT (SMD-0.2)**

**IRHNM597110
JANSR2N7506U8
100V, P-CHANNEL
REF: MIL-PRF-19500/749**



Product Summary

Part Number	Radiation Level	RDS(on)	ID	QPL Part Number
IRHNM597110	100K Rads (Si)	1.2Ω	-3.1A	JANSR2N7506U8
IRHNM593110	300K Rads (Si)	1.2Ω	-3.1A	JANSF2N7506U8

**Refer to Page 10 for 1 Additional Part Number -
IRHNM597110 (Ceramic Lid)**



International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight
- Complimentary N-Channel Available - IRHNM57110, IRHNM57110

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = -12V, TC = 25°C	Continuous Drain Current	-3.1	A
ID @ VGS = -12V, TC = 100°C	Continuous Drain Current	-2.0	
IDM	Pulsed Drain Current ①	-12.4	
PD @ TC = 25°C	Max. Power Dissipation	23	W
	Linear Derating Factor	0.18	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	28	mJ
IAR	Avalanche Current ①	-3.1	A
EAR	Repetitive Avalanche Energy ①	2.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-21	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (for 5s)	
	Weight	0.25 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.13	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	1.2	Ω	V _{GS} = -12V, I _D = -2.0A ^④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -1.0mA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	4.88	—	mV/°C	
g _{fs}	Forward Transconductance	1.9	—	—	S	V _{DS} = -15V, I _{DS} = -2.0A ^④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-10	μA	V _{DS} = -80V, V _{GS} = 0V
		—	—	-25		V _{DS} = -80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 20V
Q _g	Total Gate Charge	—	—	11	nC	V _{GS} = -12V, I _D = -3.1A V _{DS} = -50V
Q _{gs}	Gate-to-Source Charge	—	—	5.0		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	4.0		
t _{d(on)}	Turn-On Delay Time	—	—	18	ns	V _{DD} = -50V, I _D = -3.1A, V _{GS} = -12V, R _G = 7.5Ω
t _r	Rise Time	—	—	26		
t _{d(off)}	Turn-Off Delay Time	—	—	24		
t _f	Fall Time	—	—	85		
L _S + L _D	Total Inductance	—	6.8	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	379	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 100KHz
C _{oss}	Output Capacitance	—	98	—		
C _{rss}	Reverse Transfer Capacitance	—	9.5	—		
R _g	Gate Resistance	—	24	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
IS	Continuous Source Current (Body Diode)	—	—	-3.1	A	
ISM	Pulse Source Current (Body Diode)①	—	—	-12.4		
VSD	Diode Forward Voltage	—	—	-5.0	V	Tj = 25°C, IS = -3.1A, VGS = 0V ④
trr	Reverse Recovery Time	—	—	100	ns	Tj = 25°C, IF = -3.1A, di/dt ≤ -100A/μs VDD ≤ -50V ④
QRR	Reverse Recovery Charge	—	—	271	nC	
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	5.4	°C/W	

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

Radiation Characteristics

IRHNM597110, JANSR2N7506U8

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ $T_j = 25^\circ\text{C}$, Post Total Dose Irradiation ⑤ ⑥

	Parameter	Up to 300K Rads (Si) ¹		Units	Test Conditions
		Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	V	$V_{GS} = 0V, I_D = -1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0		$V_{GS} = V_{DS}, I_D = -1.0mA$
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	$V_{GS} = -20V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	100		$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	μA	$V_{DS} = -80V, V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source ^② On-State Resistance (TO-3)	—	0.916	Ω	$V_{GS} = -12V, I_D = -2.0A$
$R_{DS(on)}$	Static Drain-to-Source On-state ^④ Resistance (SMD-0.2)	—	1.2	Ω	$V_{GS} = -12V, I_D = -2.0A$
V_{SD}	Diode Forward Voltage ^④	—	-5.0	V	$V_{GS} = 0V, I_D = -3.1A$

1. Part Number IRHNM597110, IRHNM593110 and additional part numbers listed on page 10.

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)				
			@VGS = 0V	@VGS = 5V	@VGS = 10V	@VGS = 15V	@VGS = 20V
$38 \pm 5\%$	$270 \pm 7.5\%$	$35 \pm 7.5\%$	-100	-100	-100	-100	-100
$61 \pm 5\%$	$330 \pm 7.5\%$	$30 \pm 7.5\%$	-100	-100	-100	-100	-25
$84 \pm 5\%$	$350 \pm 7.5\%$	$28 \pm 7.5\%$	-100	-100	-100	-30	-

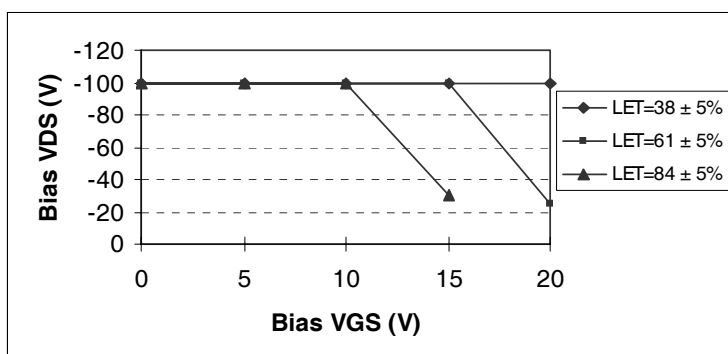


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

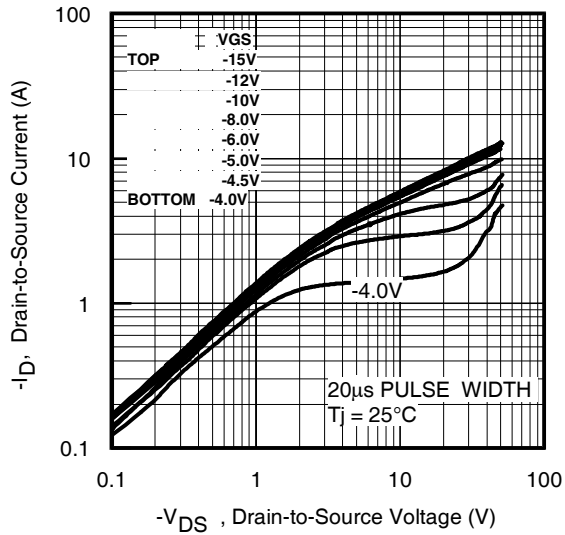


Fig 1. Typical Output Characteristics

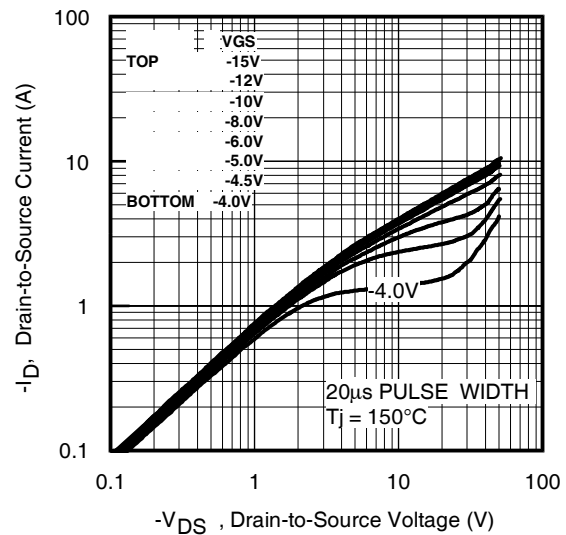


Fig 2. Typical Output Characteristics

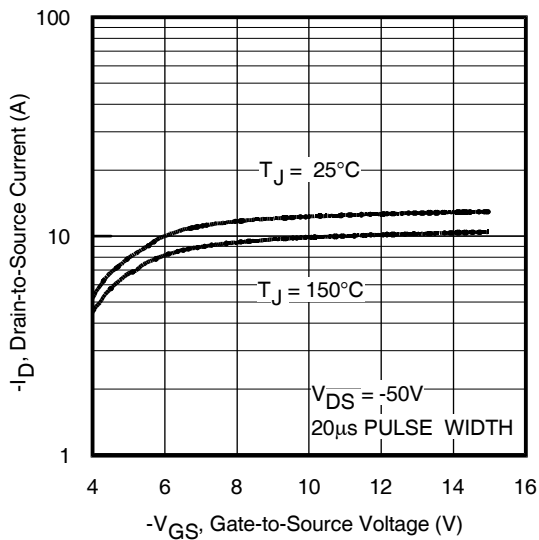
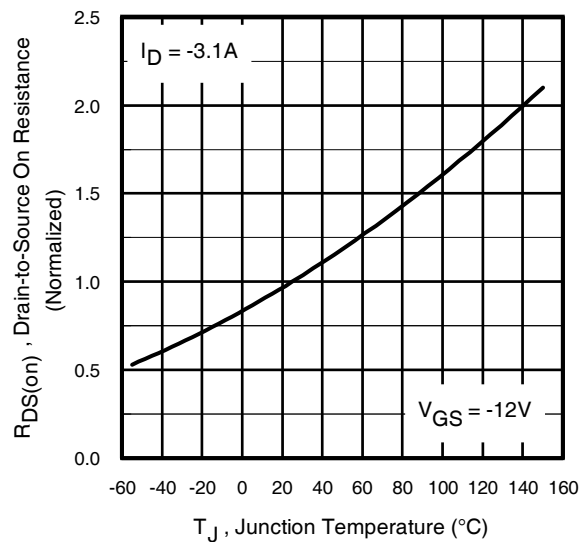


Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance
Vs. Temperature

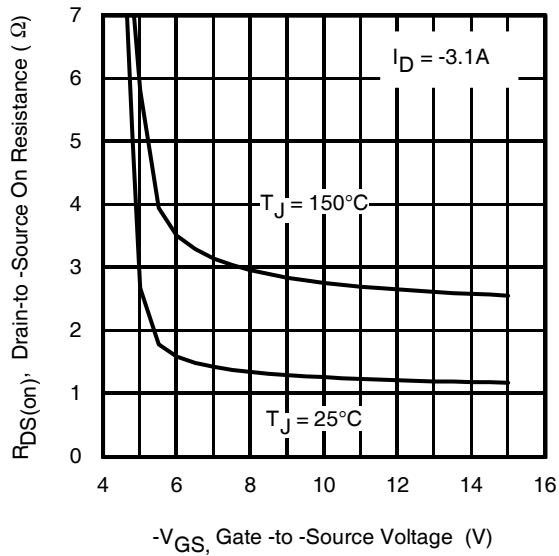


Fig 5. Typical On-Resistance Vs Gate Voltage

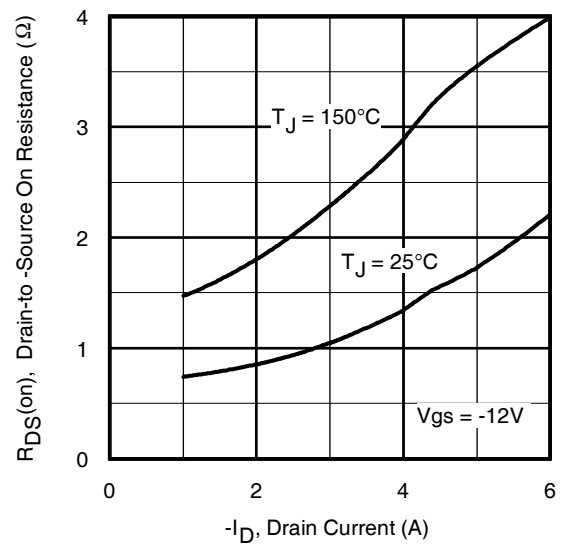


Fig 6. Typical On-Resistance Vs Drain Current

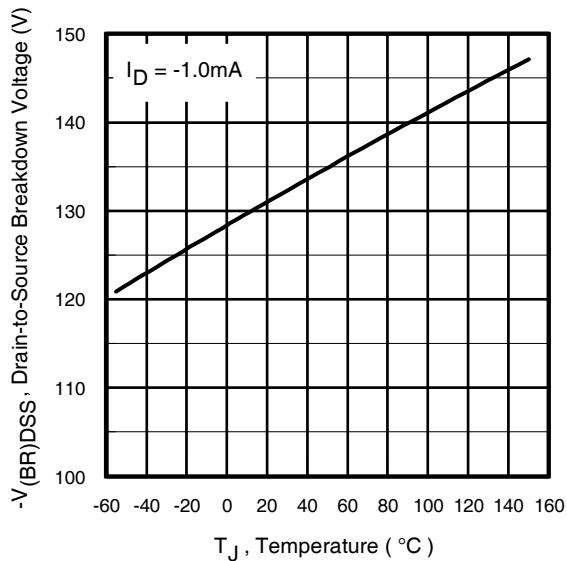


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

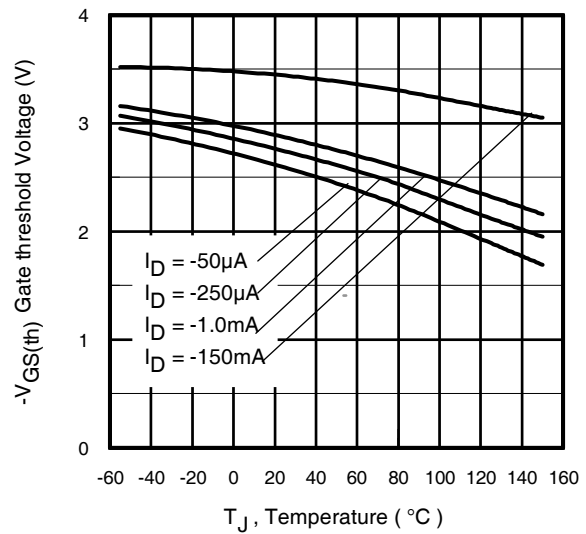


Fig 8. Typical Threshold Voltage Vs Temperature

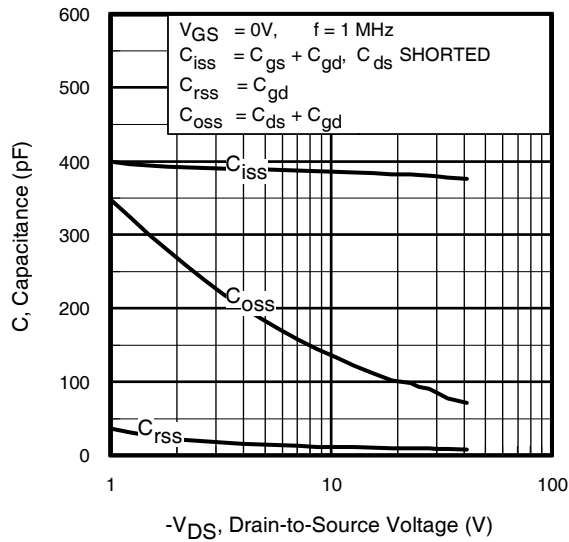


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

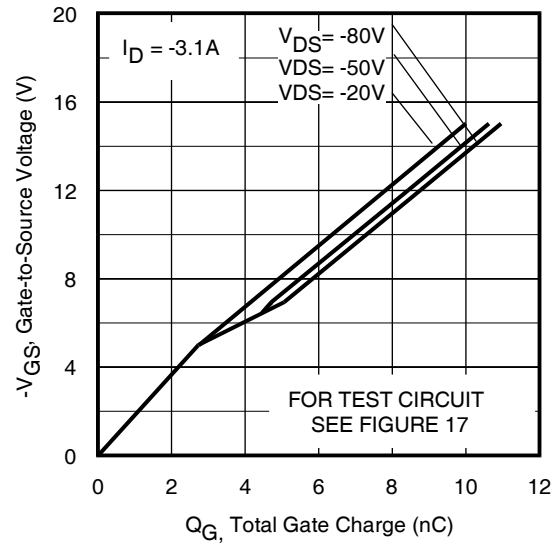


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

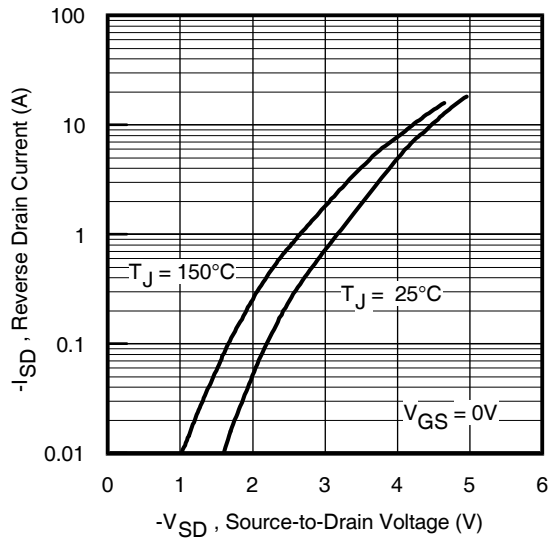


Fig 11. Typical Source-Drain Diode Forward Voltage

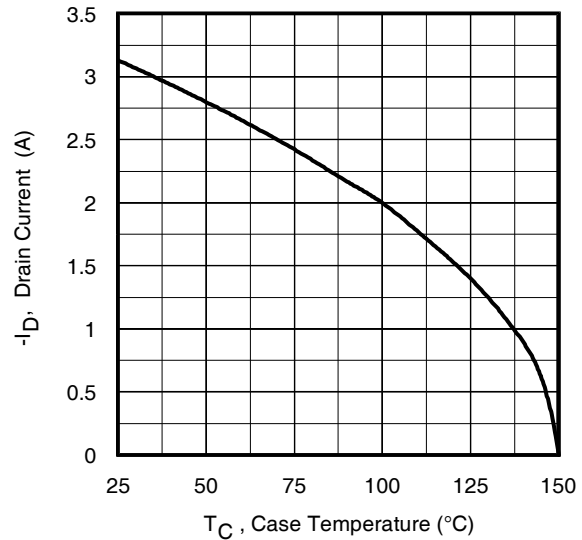


Fig 12. Maximum Drain Current Vs. Case Temperature

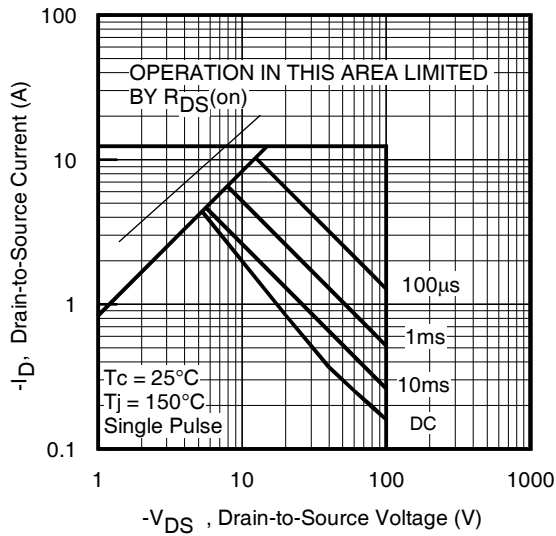


Fig 13. Maximum Safe Operating Area

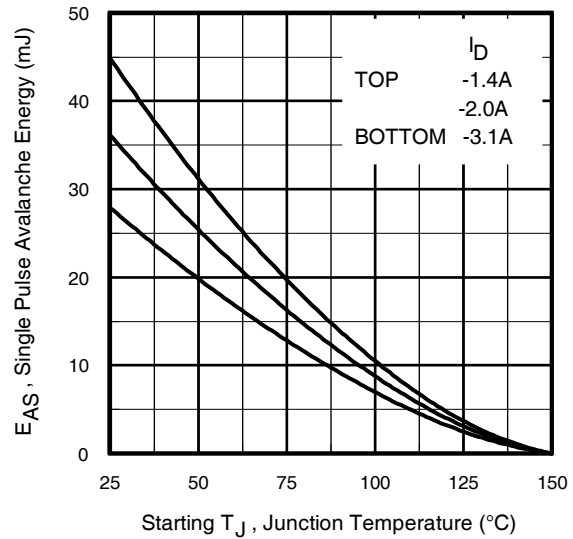


Fig 14. Maximum Avalanche Energy Vs. Drain Current

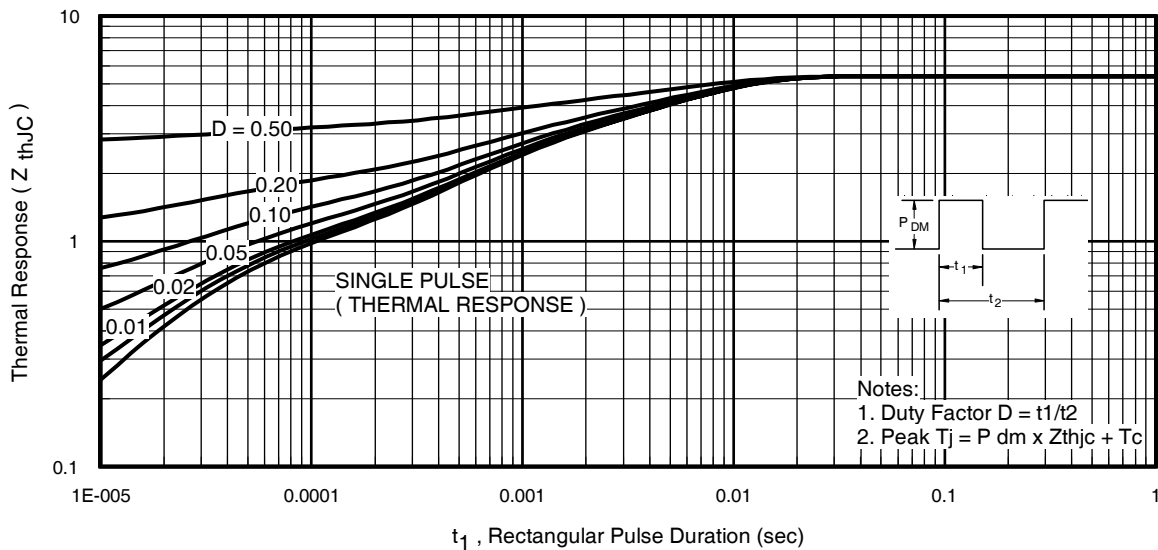


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

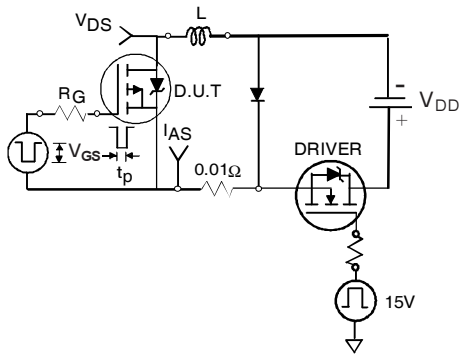


Fig 16a. Unclamped Inductive Test Circuit

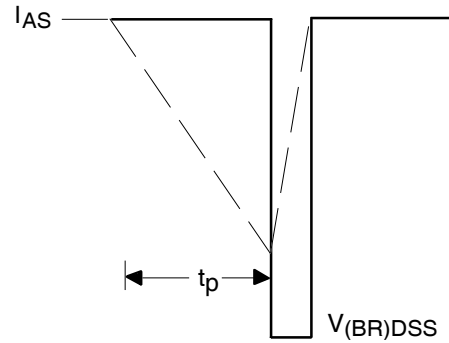


Fig 16b. Unclamped Inductive Waveforms

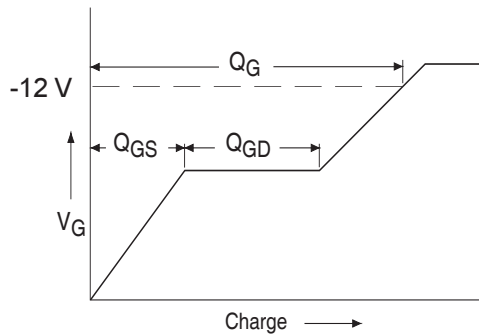


Fig 17a. Basic Gate Charge Waveform

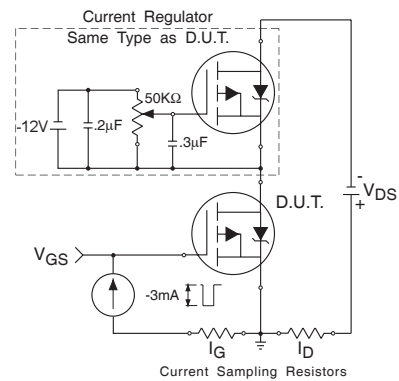


Fig 17b. Gate Charge Test Circuit

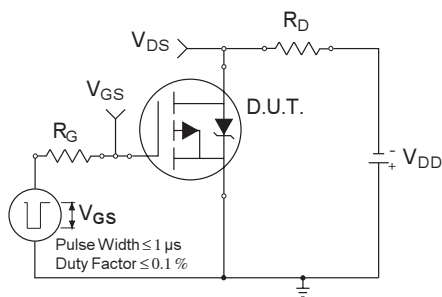


Fig 18a. Switching Time Test Circuit

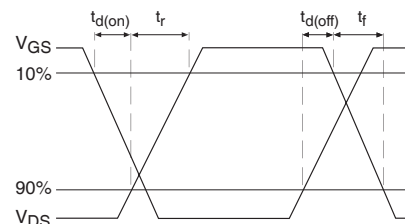
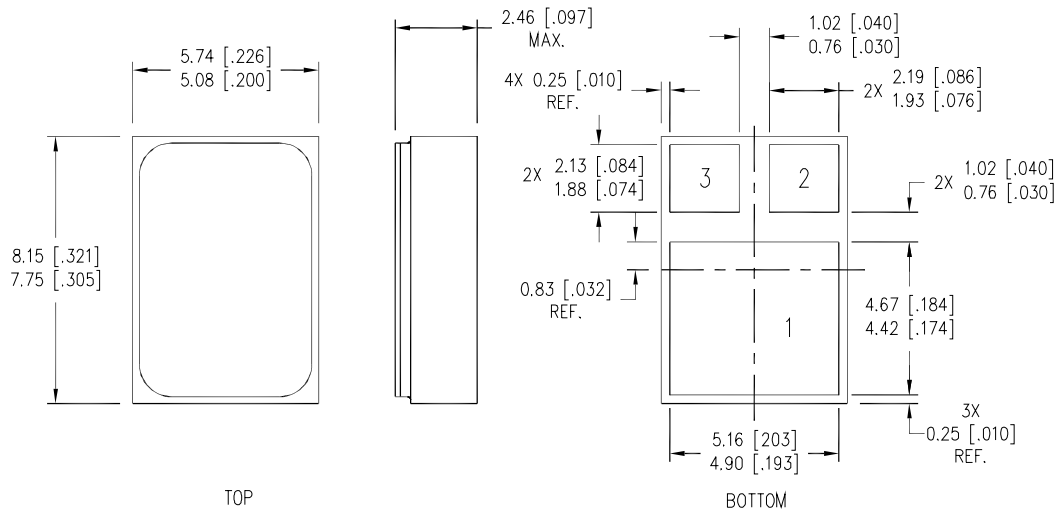


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions — SMD-0.2 (Metal Lid)



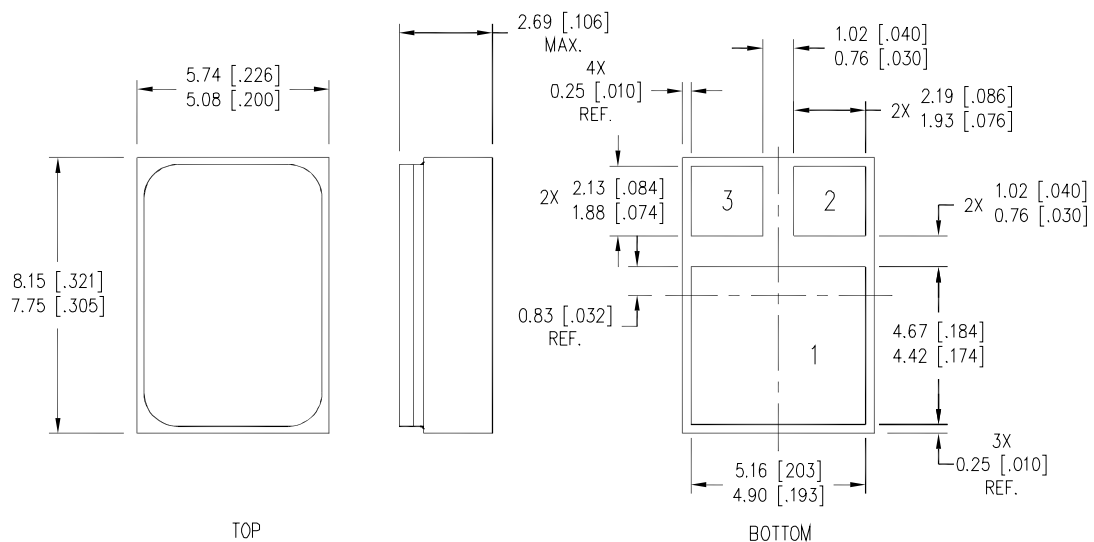
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

PAD ASSIGNMENT

- 1 = DRAIN
2 = GATE
3 = SOURCE

Case Outline and Dimensions — SMD-0.2 (Ceramic Lid)



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
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Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -50V$, starting $T_J = 25^\circ C$, $L = 5.8mH$
Peak $I_L = -3.1A$, $V_{GS} = -12V$
- ③ $I_{SD} \leq -3.1A$, $di/dt \leq -544A/\mu s$,
 $V_{DD} \leq -100V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with VGS Bias.**
-12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with VDS Bias.**
-80 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Additional Product Summary (continued from page 1 and 3)**Product Summary**

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number	 SMD-0.2 (CERAMIC LID)
IRHNMC597110	100K Rads (Si)	1.2Ω	-3.1A	JANSR2N7506U8C	
IRHNMC593110	300K Rads (Si)	1.2Ω	-3.1A	JANSF2N7506U8C	

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Visit us at www.irf.com for sales contact information.

Data and specifications subject to change without notice. 09/2010