

HYBRID-HIGH RELIABILITY DC/DC CONVERTER

AHV28XX SERIES 28V Input, Single, Dual and Triple Output

Description

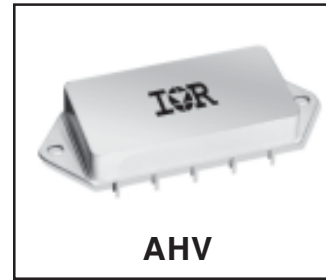
The AHV Series of DC/DC converters are designed to replace the AHE/ATO family of converters in applications requiring compliance to MIL-STD-704A through E, in particular the input surge requirement of 80V specified to withstand transient input voltage of 80V. No input voltage or output power derating is necessary over the full military temperature range.

These converters are packaged in an extremely rugged, low profile package that meets all requirements of MIL-STD-883 and MIL-PRF-38534. Parallel seam weld sealing and the use of ceramic pin feed thru seals assure long term hermeticity after exposure to extended temperature cycling.

The basic circuit is a push-pull forward topology using power MOSFET switches. The nominal switching frequency is 500KHz. A unique current injection circuit assures current balancing in the power switches. All AHV series converters use a single stage LC input filter to attenuate input ripple current. A low power 11.5V series regulator provides power to an epitaxial CMOS custom pulse width modulator integrated circuit. This single integrated circuit provides all PWM primary circuit functions. Power is transferred from primary to secondary through a ferrite core power transformer. An error voltage signal is generated by comparing a highly stable reference voltage with the converter output voltage and drives the PWM through a unique wideband magnetic feedback circuit. This proprietary feedback circuit provides an extremely wide bandwidth, high gain control loop, with high phase margin. The feedback control loop gain is insensitive to temperature, radiation, aging, and variations in manufacturing. The transfer function of the feedback circuit is a function of the feedback transformer turns ratio which cannot change when subjected to environmental extremes.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are fabricated utilizing DSCC qualified processes. For available screening options, refer to device screening table in the data sheet. Variations in electrical, mechanical and screening can be accommodated. Contact IR Santa Clara for special requirements.

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Features

- 80V Transient Input (100 msec max.)
- 50V DC Input (Continuous)
- 16V to 40V DC Input Range
- Single, Dual and Triple Outputs
- 15W Output Power
(No Temperature Derating)
- Low Input / Output Noise
- Full Military Temperature Range
- Wideband PWM Control Loop
- Magnetic Feedback
- Low Profile Hermetic Package (0.405")
- Short Circuit and Overload Protection
- Constant Switching Frequency (500KHz)
- True Hermetic Package (Parallel Seam Welded, Ceramic Pin Feedthru)
- Standard Microcircuit Drawings Available

AHV28XX Series

Specifications (Single Output Models)

International
IRF Rectifier

$T_{CASE} = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = +28\text{V} \pm 5\%$ unless otherwise specified

Absolute Maximum Ratings	
Input voltage	-0.5V to +50VDC (Continuous), 80V (100 msec)
Power output	Internally limited, 17.5W typical
Soldering temperature	300°C for 10 seconds (1 pin at a time)
Operating case temperature	-55°C to +125°C
Storage case temperature	-65°C to +135°C

TEST	SYMBOL	Condition -55°C ≤ T _C ≤ +125°C, V _{IN} = 28 VDC ±5%, C _L =0, unless otherwise specified	Group A Subgroups	AHV2805S		AHV2812S		AHV2815S		Units
				Min	Max	Min	Max	Min	Max	
STATIC CHARACTERISTICS OUTPUT	V _{OUT}	V _{IN} = 16, 28, and 40 VDC I _{OUT} = 0	1 2,3	4.95 4.90	5.05 5.10	11.88 11.76	12.12 12.24	14.85 14.70	15.15 15.30	V V
	I _{OUT}	V _{IN} = 16, 28, and 40 VDC	1,2,3	0.0	3.00	0.0	1.25	0.0	1.00	A
	V _{RIP}	V _{IN} = 16, 28, and 40 VDC BW = DC to 1 MHz	1,2,3		60		60		60	mVp-p
Power REGULATION	P _{OUT}	V _{IN} = 16, 28, and 40 VDC	1,2,3	15		15		15		W
REGULATION	Line	V _{IN} = 16, 28, and 40 VDC I _{OUT} = 0, half load and full load	1 2,3		5.0 25		30 60		35 75	mV
	Load	V _{IN} = 16, 28, and 40 VDC I _{OUT} = 0, half load and full load	1,2,3		50		120		150	
INPUT	Current	I _{OUT} = 0, Inhibit (pin 2) = 0	1,2,3		18		18		18	mA
	Ripple Current	I _{OUT} = 0, Inhibit (pin 2) = Open I _{OUT} = Full load	1,2,3		50 50		50 50		50 50	mA mAp-p
EFFICIENCY	E _{FF}	I _{OUT} = Full Load T _C = +25°C	1	72		72		72		%
ISOLATION	ISO	Input to output or any pin to case (except pin 8) at 500 VDC T _C = +25°C	1	100		100		100		MΩ
Capacitive Load ^{2,3}	C _L	No effect on DC performance T _C = +25°C	4		500		200		200	μF
Load Fault Power Dissipation	P _D	Overload, T _C = +25°C ⁴ Short Circuit, T _C = +25°C	1		8.5 8.5		8.5 8.5		8.5 8.5	W
Switching Frequency	F _S	I _{OUT} = Full Load	4	450	550	450	550	450	550	KHz
DYNAMIC CHARACTERISTICS Step Load Changes Output Transient ⁵ Recovery ^{5,6}	VOT _{LOAD}	50% Load ₁₃₅ 100% Load	4	-300	+300	-300	+300	-300	+300	mVpk
	TT _{LOAD}	No Load ₁₃₅ 50%	4	-500	+500	-750	+750	-750	+750	mVpk
		50% Load ₁₃₅ 100%	4		70		70		70	μs
		No Load ₃₃₅ 50% Load	4		200		1500		1500	μs
		50% Load ₃₃₅ No ILoad	4		5.0		5.0		5.0	ms
Step Line Changes Output Transient	VOT _{LINE}	Input step 16 to 40 VDC ^{3,7} Input step 40 to 16 VDC ^{3,7}	4 4		300 -1000		500 -1500		500 -1500	mVpk mVpk
Recovery	TT _{LINE}	Input step 16 to 40 VDC ^{3,6,7} Input step 40 to 16 VDC ^{3,6,7}	4 4		800 800		800 800		800 800	μs μs
TURN-ON Overshoot Delay	V _{TonOS} T _{on D}	I _{OUT} = OA and Full Load I _{OUT} = O and Full Load ⁸	4,5,6 4,5,6		550 10		750 10		750 10	mVpk ms
Load Fault Recovery	TR _{LF}	V _{IN} = 16 to 40 VDC	4,5,6		10		10		10	ms

Notes to Specifications (Single Output Models)

- Bandwidth guaranteed by design. Tested for 20KHz to 2MHz.
- Capacitive load may be any value from 0 to the maximum limit without affecting dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but will interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn-on.
- Parameter shall be tested as part of design characterization and after design or process changes. Thereafter shall be guaranteed to the limits specified.
- An overload is that condition with a load in excess of the rated load but less than necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
- Load step transition time between 2μs to 10μs.
- Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of V_{OUT} at 50% load.
- Input step transition time between 2μs and 10μs.
- Turn on delay time measurement is for either a step application of power at input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input. Above 125°C case temperature, derate output power linearly to 0 at 135°C case.

Specifications (Dual Output Models)

$T_{CASE} = -55^{\circ}C$ to $+125^{\circ}C$, $V_{IN} = +28V \pm 5\%$ unless otherwise specified

Absolute Maximum Ratings	
Input voltage	-0.5V to +50VDC (Continuous), 80V (100 msec)
Power output	Internally limited, 17.5W typical
Soldering temperature	300°C for 10 seconds (1 pin at a time)
Operating case temperature	-55°C to +125°C
Storage case temperature	-65°C to +135°C

TEST	SYMBOL	Condition -55°C ≤ T _C ≤ +125°C, V _{IN} = 28 VDC ±5%, C _L =0, unless otherwise specified	Group A Subgroups	AHV2805D		AHV2812		AHV281D		Units	
				Min	Max	Min	Max	Min	Max		
STATIC CHARACTERISTICS OUTPUT	Voltage ¹	I _{OUT} = 0	1	±4.95	±5.05	±11.88	±12.12	±14.85	±15.15	V	
	Current ^{1,2}	V _{IN} = 16, 28, and 40 VDC	2,3	±4.90	±5.10	±11.76	±12.24	±14.70	±15.30	V	
	Ripple Voltage ^{1,3}	V _{IN} = 16, 28, and 40 VDC BW = DC to 2 MHz	1,2,3	0.0	±1500	0.0	±625	0.0	±500	mVp-p	
	Power ^{1,2,4}	V _{IN} = 16, 28, and 40 VDC	1,2,3	15		15		15		W	
REGULATION Line ^{1,5}	VR _{LINE}	V _{IN} = 16, 28, and 40 VDC	1		30		30		35	mV	
	I _{OUT} VR _{LOAD}	I _{OUT} = 0, half load and full load V _{IN} = 16, 28, and 40 VDC I _{OUT} = 0, half load and full load	2,3 1,2,3		60 120		60 120		75 150		
INPUT Current	I _{IN}	I _{OUT} = 0, Inhibit (pin 2) Tied to input return (pin 10)	1,2,3		18		18		18	mA	
	Ripple Current ³	I _{OUT} = 0, Inhibit (pin 2) = Open I _{OUT} = Full load BW = DC to 2MHz	1,2,3		65 50		65 50		65 50		
EFFICIENCY	E _{EFF}	I _{OUT} = Full Load T _C = +25°C	1	72		72		72		%	
ISOLATION	ISO	Input to output or any pin to case (except pin 8) at 500 VDC, T _C = +25°C	1	100		100		100		MΩ	
Capacitive Load ^{6,7}	C _L	No effect on DC performance T _C = +25°C	4		200		200		200	μF	
Load Fault Power Dissipation	P _D	Overload, T _C = +25°C ⁸ Short Circuit, T _C = +25°C	1		8.5 8.5		8.5 8.5		8.5 8.5	W	
Switching Frequency	F _S	I _{OUT} = Full Load	4	450	550	450	550	450	550	KHz	
DYNAMIC CHARACTERISTICS Step Load Changes Output Transient ⁹	VOT _{LOAD}	50% Load ₁₃₅ 100% Load No Load ₁₃₅ 50%	4	-300	+300	-300	+300	-300	+300	mVpk	
	Recovery ^{9,10}	TT _{LOAD}	50% Load ₁₃₅ 100% No Load ₃₃₅ 50% Load 50% Load ₃₃₅ No Load	4	-500	+500	-500	+500	-500	+500	mVpk
				4		70		70		70	μs
				4		200		1500		1500	μs
		4		5.0		5.0		5.0	ms		
Step Line Changes Output Transient ^{7,11}	VOT _{LINE}	Input step 16 to 40 VDC	4		300		1200		1500	mVpk	
	Recovery ^{7,10,11}	TT _{LINE}	Input step 40 to 16 VDC	4		1000		-1500		-1500	mVpk
			Input step 16 to 40 VDC	4		4800		4.0		4.0	μs
			Input step 40 to 16 VDC	4		4800		4.0		4.0	μs
TURN-ON Overshoot ¹	VTON _{OS}	I _{OUT} = 0 and Full Load	4,5,6		550		600		600	mVpk	
Delay ^{1,12}	T _{on D}	I _{OUT} = 0 and Full Load	4,5,6		10		10		10	ms	
Load Fault Recovery ⁷	TR _{LF}		4,5,6		10		10		10	ms	

For Notes to Specifications, refer to page 5

Specifications (Triple Output Models)

T_{CASE} = -55°C to +125°C, V_{IN} = +28V ± 5% unless otherwise specified

Absolute Maximum Ratings	
Input voltage	-0.5V to +50VDC (Continuous), 80V (100 msec)
Power output	Internally limited, 17.5W typical
Soldering temperature	300°C for 10 seconds (1 pin at a time)
Operating case temperature	-55°C to +125°C
Storage case temperature	-65°C to +135°C

TEST	SYMBOL	Condition -55°C ≤ T _C ≤ +125°C, V _{IN} = 28 VDC ±5%, C _L =0, unless otherwise specified	Group A Subgroups	AHV2812T		AHV2815T		Units	
				Min	Max	Min	Max		
STATIC CHARACTERISTICS OUTPUT Voltage ¹	V _{OUT}	I _{OUT} = 0 (main)	1	4.95	5.05	4.95	5.05	V	
		I _{OUT} = 0 (dual) ¹	2,3	4.90	5.10	4.90	5.10	V	
	Current ^{1,2,3}	I _{OUT}	V _{IN} = 16, 28, and 40 VDC (main)	1	±11.88	±12.12	±14.85	±15.15	V
			V _{IN} = 16, 28, and 40 VDC (dual) ¹	2,3	±11.76	±12.24	±14.70	±15.30	V
Ripple Voltage ^{1,4}	V _{RIP}	V _{IN} = 16, 28, and 40 VDC BW = DC to 2 MHz (main)	1,2,3	0.0	2000	0.0	2000	mA	
		V _{IN} = 16, 28, and 40 VDC BW = DC to 2 MHz (main)	1,2,3	0.0	±208	0.0	±167	mA	
Power ^{1,2,3}	P _{OUT}	V _{IN} = 16, 28, and 40 VDC (main)	1,2,3		80		80	mVp-p	
		(+dual)	1,2,3	10		10		W	
		(-dual)	1,2,3	2.5		2.5		W	
		(total)	1,2,3	2.5		2.5		W	
REGULATION Line ^{1,3}	VR _{LINE}	V _{IN} = 16, 28, and 40 VDC I _{OUT} = 0, 50%, and 100% load (main)	1,2,3		25		25	mV	
Load ^{1,3}	VR _{LOAD}	I _{OUT} = 0, 50%, and 100% load (dual) V _{IN} = 16, 28, and 40 VDC I _{OUT} = 0, 50%, and 100% load (main)			±60		±75		
		I _{OUT} = 0, 50%, and 100% load (dual)			50		50		
		I _{OUT} = 0, 50%, and 100% load (dual)			±60		±75		
INPUT Current	I _{IN}	I _{OUT} = 0, Inhibit (pin 8) Tied to input return (pin 10)	1,2,3		15		15	mA	
		I _{OUT} = 0	1,2,3		50		50	mA	
Ripple Current ⁴	I _{RIP}	Inhibit (pin 2) = open I _{OUT} = 2000 mA (main) I _{OUT} = ±208mA (±12V) I _{OUT} = ±167mA (±15V) BW = DC to 2MHz	1,2,3		50		50	mAp-p	
EFFICIENCY	E _{FF}	I _{OUT} = 2000mA (main) I _{OUT} = ±208mA (±12V) I _{OUT} = ±167mA (±15V)	1	72		72		%	
ISOLATION	ISO	Input to output or any pin to case (except pin 7) at 500 VDC, TC = +25°C	1	100		100		MΩ	
Capacitive Load ^{6,7}	C _L	No effect on DC performance TC = +25°C (main) (dual)	4		500 200		500 200	μF	
Load Fault Power Dissipation ³	P _D	Overload, TC = +25°C ⁵ Short Circuit, TC = +25°C	1		8.5 8.5		8.5 8.5	W	
Switching Frequency ¹	F _S	I _{OUT} = 2000mA (main) I _{OUT} = ±208mA (±12V) I _{OUT} = ±167mA (±15V)	4	450	550	450	550	KHz	

For Notes to Specifications, refer to page 5

Specifications (Triple Output Models) - continued

TEST	SYMBOL	Condition -55°C ≤ TC ≤ +125°C, VIN = 28 VDC ±5%, CL=0, unless otherwise specified	Group A Subgroups	AHV2812T		AHV2815T		Units
				Min	Max	Min	Max	
DYNAMIC CHARACTERISTICS Step Load Changes Output Transient ⁹ Recovery ^{9,10}	VOT _{LOAD}	50% Load ₁₃₅ 100% Load	4	-300	+300	-300	+300	mVpk
	TT _{LOAD}	No Load ₁₃₅ 50%	4	-400	+400	-400	+400	mVpk
		50% Load ₁₃₅ 100%	4		100		100	µs
		No Load ₃₃₅ 50% Load	4		2000		2000	µs
		50% Load ₃₃₅ No ILoad	4		5.0		5.0	ms
Step Line Changes Output Transient Recovery ^{7,10,11}	VOT _{LINE}	Input step 16 to 40 VDC	4		1200		1200	mVpk
	TT _{LINE}	Input step 40 to 16 VDC	4		-1500		-1500	mVpk
		Input step 16 to 40 VDC	4		4.0		4.0	µs
		Input step 40 to 16 VDC	4		4.0		4.0	µs
TURN-ON Overshoot ¹ Delay ^{1,12}	VT _{onOS} T on D	I _{OUT} = 0 and ±625mA	4		750		750	mVpk
		I _{OUT} = 0 and ±625mA	4		15		15	ms
Load Fault Recovery ⁷	TR _{LF}		4		15		15	ms

Notes to Specifications (Triple Output Models)

1. Tested at each output.
2. Parameter guaranteed by line and load regulation tests.
3. At least 25% of the total power should be taken from the (+5V) main output.
4. Bandwidth guaranteed by design. Tested for 20KHz to 2MHz.
5. An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
6. Capacitive load may be any value from 0 to the maximum limit without affecting dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn-on.
7. Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified.
8. Above 125°C case temperature, derate output power linearly to 0 at 135°C case.
9. Load step transition time between 2µs and 10µs.
10. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of V_{OUT} at 50% load.
11. Input step transition time between 2µs and 10µs.
12. Turn on delay time measurement is for either a step application of power at input or the removal of a ground signal from the inhibit pin (pin 8) while power is applied to the input.

Notes to Specifications (Dual Output Models)

1. Tested at each output.
2. Parameter guaranteed by line and load regulation tests.
3. Bandwidth guaranteed by design. Tested for 20KHz to 2MHz.
4. Total power at both outputs.
5. When operating with unbalanced loads, at least 25% of the load must be on the positive output to maintain regulation.
6. Capacitive load may be any value from 0 to the maximum limit without affecting dc performance. A capacitive load in excess of the maximum limit will not disturb loop stability but may interfere with the operation of the load fault detection circuitry, appearing as a short circuit during turn-on.
7. Parameter shall be tested as part of design characterization and after design or process changes. Thereafter parameters shall be guaranteed to the limits specified.
8. An overload is that condition with a load in excess of the rated load but less than that necessary to trigger the short circuit protection and is the condition of maximum power dissipation.
9. Load step transition time between 2µs and 10µs.
10. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of V_{OUT} at 50% load.
11. Input step transition time between 2µs and 10µs.
12. Turn on delay time measurement is for either a step application of power at input or the removal of a ground signal from the inhibit pin (pin 2) while power is applied to the input.
13. Above 125°C case temperature, derate output power linearly to 0 at 135°C.

Application Information

Inhibit Function

Connecting the inhibit pin (Pin 2 of single and dual models, pin 8 of triple models) to the input return (pin 10) will cause the converter to shutdown and operate in a low power standby mode. Power consumption in this mode is calculated by multiplying V_{in} times the input current inhibited, typically 225mW at V_{in} equal to 28V. The input current inhibited is relatively constant with changes in V_{in} . The open circuit inhibit pin voltage is typically 11.5V and can be conveniently driven by an open collector driver. An internal pull-up resistor enables the user to leave this pin floating if the inhibit function is not used in their particular application. All models use identical inhibit internal circuits. Forcing inhibit pin to any voltage between 0V and 6V will assure the converter is inhibited. The input current to this pin is 500 μ A maximum at $V_{pin2} = 0V$. The converter can be turned on by opening Pin 2 or forcing a voltage from 10V to 50V. Inhibit pin current from 10V to 50V is less than $\pm 50\mu$ A.

EMI Filter

An optional EMI filter (AFC461) will reduce the input ripple current to levels below the limits imposed by MIL-STD-461 CEO3.

The output voltage of the AHV28XXS can be adjusted upward by connecting a resistor between the Output Adjust (Pin 3) and the Output Common (Pin 4) as shown in Table 1.

Table 1: Output Adjustment Resistor Values

* Resistance (Ohms) Pin 3 to 4	Output Voltage Increase (%)		
	5V	12V	15V
None	0	0	0
390 K	+1.0%	+1.6%	+1.7%
145 K	+2.0%	+3.2%	+3.4%
63 K	+3.1%	+4.9%	+5.1%
22 K	+4.1%	+6.5%	+6.8%
0	+5.0%	+7.9%	+8.3%

* Output Adjust (Single Output Models Only)

Standard Microcircuit Drawing Equivalence Table

Standard Microcircuit Drawing Number	Vendor Cage Code	IR Standard Part Number
5962-91773	52467	AHV2805S
5962-92112	52467	AHV2812S
5962-92113	52467	AHV2815S
5962-92114	52467	AHV2812D
5962-92115	52467	AHV2812T
5962-92116	52467	AHV2815T

Figure 1. (Single Output) Block Diagram

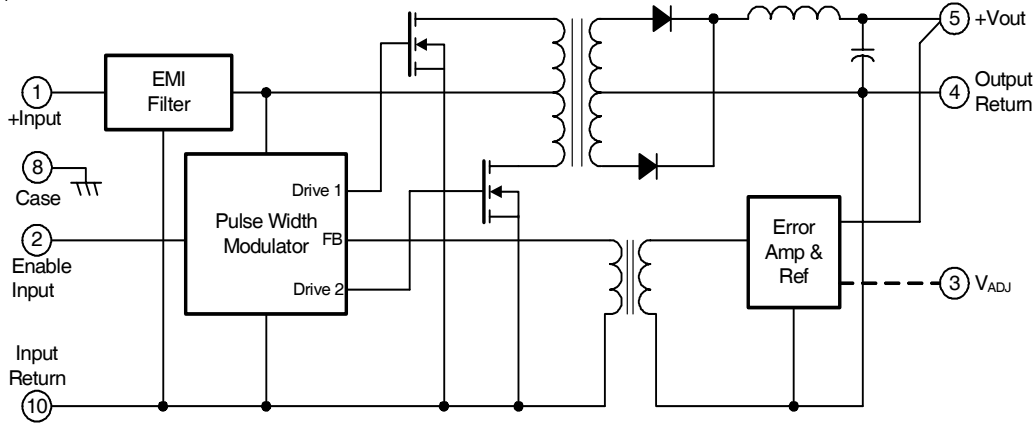


Figure 2. (Dual Output) Block Diagram

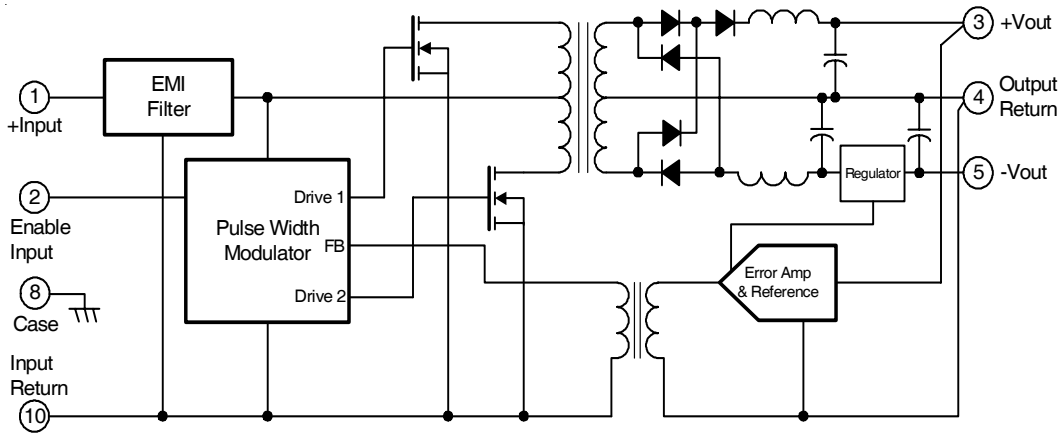
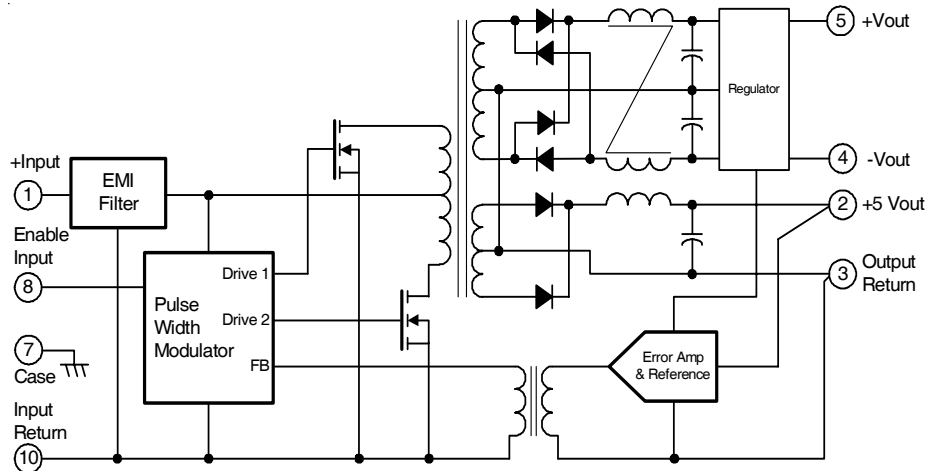
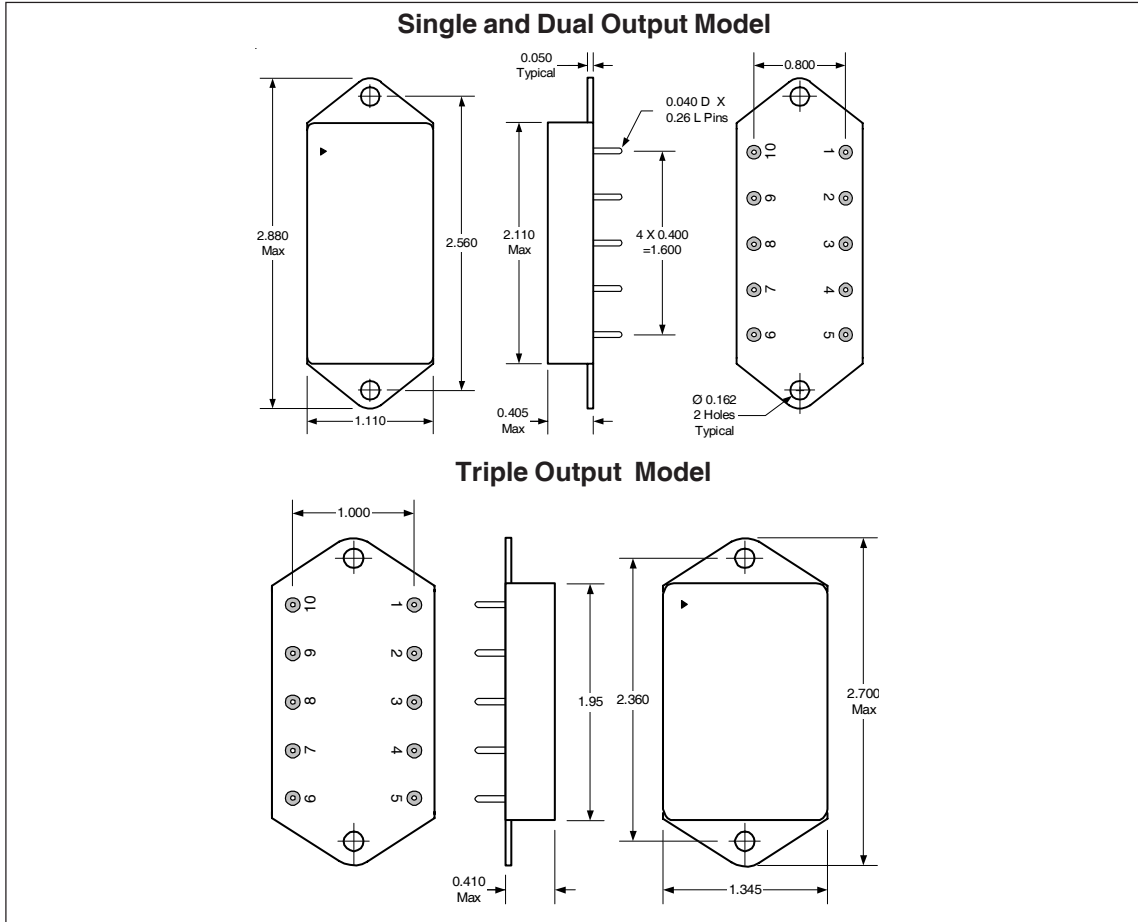


Figure 3. (Triple Output) Block Diagram



Mechanical Outlines



Pin Designation

Pin #	Single Output	Dual Output	Triple Output
1	+ Input	+ Input	+ Input
2	Enable Input	Enable Input	+ 5VDC Output
3	Output Adjust *	+ Output	Output Return
4	Output Return	Output Return	- Dual Output (12/15VDC)
5	+ Output	- Output	+ Dual Output (12/15VDC)
6	NC	NC	NC
7	NC	NC	Case Ground
8	Case Ground	Case Ground	Enable Input
9	NC	NC	NC
10	Input Return	Input Return	Input Return

* Output Adjust (Single Output Models Only)

Device Screening

Requirement	MIL-STD-883 Method	No Suffix	ES ②	HB	CH
Temperature Range	—	-20°C to +85°C	-55°C to +125°C ③	-55°C to +125°C	-55°C to +125°C
Element Evaluation	MIL-PRF-38534	N/A	N/A	N/A	Class H
Non-Destructive Bond Pull	2023	N/A	N/A	N/A	N/A
Internal Visual	2017	①	Yes	Yes	Yes
Temperature Cycle	1010	N/A	Cond B	Cond C	Cond C
Constant Acceleration	2001, Y1 Axis	N/A	500 Gs	3000 Gs	3000 Gs
PIND	2020	N/A	N/A	N/A	N/A
Burn-In	1015	N/A	48 hrs@hi temp	160 hrs@125°C	160 hrs@125°C
Final Electrical (Group A)	MIL-PRF-38534 & Specification	25°C	25°C ②	-55°C, +25°C, +125°C	-55°C, +25°C, +125°C
PDA	MIL-PRF-38534	N/A	N/A	N/A	10%
Seal, Fine and Gross	1014	Cond A	Cond A, C	Cond A, C	Cond A, C
Radiographic	2012	N/A	N/A	N/A	N/A
External Visual	2009	①	Yes	Yes	Yes

Notes:

- ① Best commercial practice
- ② Sample tests at low and high temperatures
- ③ -55°C to +105°C for AHE, ATO, ATW

