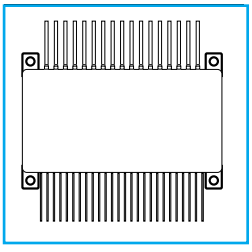
FULL-FEATURED POWER MODULE FOR DIRECT DRIVE OF 3-PHASE BRUSHLESS DC MOTORS



25 Amp. Push-Pull 3-Phase Brushless DC Motor Controller/Driver Module in a Power Flatpack

FEATURES

- Fully integrated 3-Phase Brushless DC Motor Control Subsystem includes power stage, non-isolated driver stage, and controller stage
- MOSFET Output Stage
- 25A Average Phase Current with 48V Maximum Bus Voltage
- Internal Precision Current Sense Resistor (6W max. dissipation)
- Speed and Direction Control of Motor
- Brake Input for Dynamic Braking of Motor
- Overvoltage/Coast Input for Shutdown of All Power Switches
- Soft Start for Safe Motor Starting
- Unique Hermetic or Plastic Ring Frame Power Flatpacks
  - Hermetic (3.10" x 2.10" x 0.385")
  - Plastic Ring Frame (4.13" x 2.00" x 0.49")

APPLICATIONS

- Fans and Pumps
- Hoists
- Actuator Systems

DESCRIPTION

The OM9371 is one of a series of versatile, integrated three-phase brushless DC motor controller/driver subsystems housed in a 43 pin power flatpack. The OM9371 is best used as a two quadrant speed controller for controlling/driving fans, pumps, and motors in applications which require small size. Many integral control features provide the user much flexibility in adapting the OM9371 to specific system requirements.

The small size of the complete subsystem is ideal for aerospace, military, and high-end industrial applications. Two package types provide a broad range of cost and screening options to fit any application.

8 10 R2
Supersedes 6 11 R1

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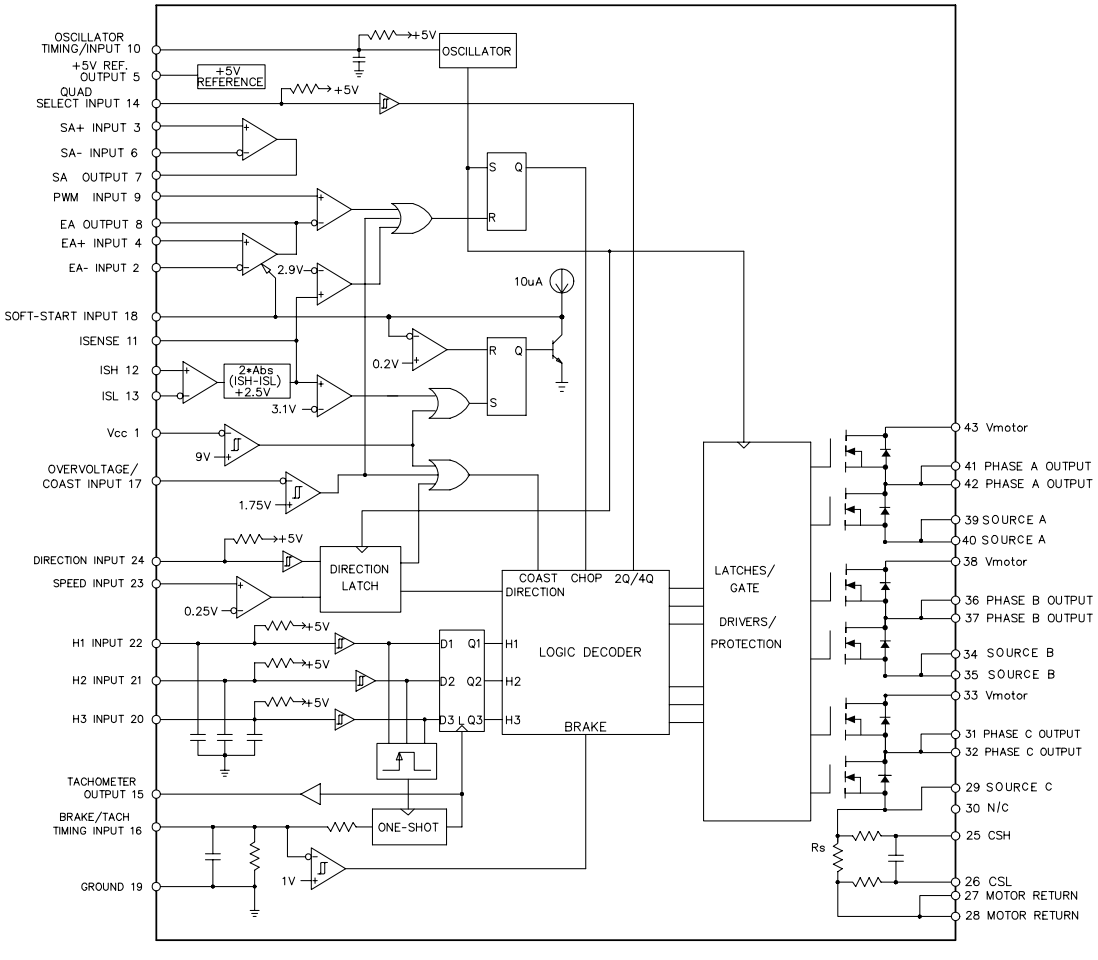
SIMPLIFIED BLOCK DIAGRAM



COMMUTATION TRUTH TABLE

This table shows the Phase Output state versus the state of the Hall-Effect and Direction Inputs. Please note that the OM9371 Hall-Effect Inputs are Grey-encoded; that is, only one input is allowed to change from one input state to another at a time.

The commutation coding shown reflects Hall-Effect sensors that are spaced at 120° mechanical increments. Also, internal protection logic disables all three Phase Outputs when the Hall-Effect Inputs are set to an illegal condition (i.e. all logic low or all logic high).

DIGITAL INPUTS				PHASE OUTPUTS		
Dir	H1	H2	H3	A	B	C
1	0	0	1	Hi-Z	Sink	Source
1	0	1	1	Sink	Hi-Z	Source
1	0	1	0	Sink	Source	Hi-Z
1	1	1	0	Hi-Z	Source	Sink
1	1	0	0	Source	Hi-Z	Sink
1	1	0	1	Source	Sink	Hi-Z
0	1	0	1	Sink	Source	Hi-Z
0	1	0	0	Sink	Hi-Z	Source
0	1	1	0	Hi-Z	Sink	Source
0	0	1	0	Source	Sink	Hi-Z
0	0	1	1	Source	Hi-Z	Sink
0	0	0	1	Hi-Z	Source	Sink
X	0	0	0	Hi-Z	Hi-Z	Hi-Z
X	1	1	1	Hi-Z	Hi-Z	Hi-Z

ABSOLUTE MAXIMUM RATINGS

Motor Supply Voltage, V_m . . . . . 48 Vdc
Peak Motor Supply Voltage $V_{m\ pK}$ . . . . . 60 Vdc
Average Phase Output Current, I_o . . . . . 25 Amperes DC*
Peak Phase Output Current, I_{om} . . . . . 50 Amperes Peak**
Control Supply Voltage, V_{cc} . . . . . +18 V
Logic Input Voltage (Note 1) . . . . . -0.3 V to +8 V
Reference Source Current . . . . . -30 mAdc
Error Amplifier Input Voltage Range, (EA1+/EA1-) . . . . . -0.3 Vdc to 10 Vdc
Error Amplifier Output Current . . . . . ±8 mAdc
Spare Amplifier Input Voltage (EA2+/EA2-) . . . . . -0.3 Vdc to 10 Vdc
Spare Amplifier Output Current . . . . . ±8 mAdc
Current Sense Amplifier Input Voltage (ISH/ISL) . . . . . -0.3 V to +6 Vdc
Current Sense Amplifier Output Current . . . . . ±10 mAdc
Tachometer Output Current . . . . . ±10 mAdc
PWM Input Voltage . . . . . - 0.3 Vdc to +6 Vdc
Operating Junction Temperature . . . . . -55°C to +150° C
Storage Temperature Range . . . . . -65° C to +150° C
Power Switch Junction-to-Case Thermal Resistance, $R\theta_{jc}$ . . . . . 0.55°C/W
Package Isolation Voltage . . . . . 600 Vrms
Lead Soldering Temperature . . . . . 300°C, 10 seconds maximum, 0.125” from case
* Tcase = 25° C
** Tcase = 25° C, Maximum pulse width = 10mSec

RECOMMENDED OPERATING CONDITIONS (Tcase = 25° C)

Motor Power Supply Voltage, V_m . . . . . + 2 8 Vdc
Average Phase Output Current, I_O
With Internal Current Sense Resistor (Note 2)
Each Power Switch . . . . . 25 A
Control Supply Voltage, V_{cc} . . . . . 15Vdc ±10%
Logic Low Input Voltage, V_{il} . . . . . 0.8 Vdc (max)
Logic High Input Voltage, V_{ih} . . . . . 2.0 Vdc (min)

Note 1: Logic Inputs: Direction, Hall Inputs (H1...H3) Overvoltage - Coast, Speed, and Quad Select.

Note 2: The internal 5mΩ current sense resistor is limited to 6 Wdc power dissipation. Other values are available. Please contact the factory for more information.

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	MIN.	TYP.	MAX.	UNITS
Power Output Section						
Zero Gate Voltage Drain Current	**I_{dss}**	Vds = 60Vdc V_{gs} = 0V			250	uA
Drain-to-Source On-Resistance	**Rds(on)**	Id =37.5 A V_{gs} = 10V (Note 4)			0.016	Ohms
Gate Body Leakage Current	I_{gssr}	V_{gs} = 20 Vdc, Vds = 0V			100	nA
Diode Forward Voltage	**V_f**	I_S = 37.5 A			0.9	V
Diode Reverse Recovery Time	trr	I_S = 75A, di/dt = -100A/usec, Vgs = 0V		56		nSec
Control Section						
Control Supply Current	**Icc**	Vcc over operating range			100	mA
Control Turn-On Threshold	Vcc(+)	Tc over operating range	9.45			V
Driver Turn-On Threshold	**Vcc(+)**	Tc over operating range	13.0			V
Reference Section						
Output Voltage	**Vr_{ef}**		4.9	5.0	5.1	V
Output Voltage	**Vr_{ef}**	Tc over operating range	4.7	5.0	5.3	V
Output Current	Io		---	---	30	mA
Load Regulation		Iload = 0mA to -20mA	-40	-5		mV
Short Circuit Current	Isc	Tc over operating range	50	100	150	mA
Error Amplifier / Spare Amplifier Sections						
EA1 / EA2 Input Offset Current	Ios	V(pin 2) = V(pin 4) = 0V V(pin 3) = V(pin 6) = 0V	-30	-3	0	nA
EA1 / EA2 Input Bias Current	Iin	V(pin 2) = V(pin 4) = 0V V(pin 3) = V(pin 6) = 0V	-50	-45	0	nA
Input Offset Voltage	Vos	0V < Vcommon-mode < 3V			7	mV
Amplifier Output Voltage Range	--		0		6	V
PWM Comparator Section						
PWM Input Current	Iin	V(pin 9) = 2.5V	0	3.0	30	uA
Current-Sense Amplifier Section						
ISH / ISL Input Current	Iin	V(pin 12) = V(pin 13) = 0V	-850	-320	0	uA
Input Offset Current	Ios	V(pin 12) = V(pin 13) = 0V		+/-2	+/-12	uA
Peak Current Threshold Voltage	**Vpk**	V(pin 12) = 0V, V(pin 13) Varied to Threshold	0.14	0.20	0.26	V
Over Current Threshold Voltage	**Voc**	V(pin 12) = 0V, V(pin 13) Varied to Threshold	0.26	0.30	0.36	V
ISH / ISL Input Voltage Range	--	(Note 2)	-1		2	V
Amplifier Voltage Gain	Av	V(pin 12) = 0.3V, V(pin 13) = 0.5V to 0.7V	1.75	1.95	2.15	V/V
Amplifier Level Shift	**--**	V(pin 12) = V(pin13) = 0.3V	2.4	2.5	2.65	V
Logic Input Section						
H1, H2, H3 Low Voltage Threshold	Vil	Tc over operating range	0.8	1.0	1.2	V
H1, H2, H3 High Voltage Threshold	Vih	Tc over operating range	1.6	1.9	2.0	V
H1, H2, H3 Input Current	Iin	Tc over operating range, V(pin 20, 21 or 22) = 0Vdc	-400	-250	-120	uA
Quad Select / Direction Threshold Voltage	Vth	Tc over operating range	0.8	1.4	2.0	V
Quad Select Voltage Hysteresis	Vh			70		mV
Direction Voltage Hysteresis	Vh			0.6		V
Quad Select Input Current	Iin		-30	50	150	uA
Direction Input Current	Iin		-30	-1	30	uA
Overvoltage / Coast Input Section						
Overvoltage / Coast Inhibit Threshold Voltage	**Vth**	Tc over operating range	1.65	1.75	1.85	V
Overvoltage / Coast Restart Threshold Voltage	**Vth**	Tc over operating range	1.55	1.65	1.75	V
Overvoltage / Coast Hysteresis Voltage	Vh		0.05	0.10	0.15	V
Overvoltage / Coast Input Current	Iin		-10	-1	0	uA

Parameter	Symbol	Conditions (Note 1)	MIN.	TYP.	MAX.	Units
Soft-Start Section						
Soft-Start Pull-Up Current	Ip	V(pin) 18) = 0V	-16	-10	-5	uA
Soft-Start Discharge Current	Id	V(pin 18) = 2.5V	0.1	0.4	3.0	mA
Soft-Start Reset Threshold Voltage	**Vth**		0.1	0.2	0.3	V
Tachometer/Brake Section						
Tachometer Output High Level	**Voh**	Tc over operating range (Pin 15) 10kΩ to 2.5 V	4.7	5.0	5.3	V
Tachometer Output Low Level	**Vol**	Tc over operating range (Pin 15) 10kΩ to 2.5 V			0.2	V
Tachometer On-Time	**ton**		85	100	140	us
Tachometer On-Time Variation	--	Tc over operating range		0.1		%
Brake/Tach Timing Input Current	Iin	V (pin 16) = 0V	-4.0	-1.9		mA
Brake/Tach Timing Threshold Voltage	**Vth**	Tc over operating range	0.8	1.0	1.2	V
Brake/Tach Timing Voltage Hysteresis	Vh			0.09		V
Speed Input Threshold Voltage	**Vth**	Tc over operating range	220	257	290	mV
Speed Input Current	Iin		-30	-5	30	uA
Oscillator Section						
Oscillator Frequency	**fo**	Measured at pin 10	13.5	14.8	20.0	kHz

SPECIFICATION NOTES:

1. All parameters specified for Ta = 25°C, Vcc = 15Vdc, Rosc = 75KΩ (to Vref), Cosc = 1800 pF, and all Phase Outputs unloaded (Ta ~ Tj). All negative currents shown are sourced by (flow from) the pin under test.

2. Either ISH or ISL may be driven over the range shown.

3. Bold parameters tested at -55°C, 25°C, 125°C for SFB.

4. Pulse Test: Pulse Width ≤ 300 μSec, Duty Cycle ≤ 2%.

PINOUT

PIN#	NAME	PIN#	NAME
1	VCC	23	Speed Input
2	EA1 "-" Input	24	Direction Input
3	EA2 "+" Input	25	CSH
4	EA1 "+" Input	26	CSL
5	+5V Reference Output	27	Motor Return
6	EA2 "-" Input	28	Motor Return
7	EA2 Output	29	Source C
8	EA1 Output	30	(No Connection)
9	PWM Input	31	Phase C Output
10	Oscillator Timing Input	32	Phase C Output
11	Isense	33	Vmotor
12	ISH	34	Source B
13	ISL	35	Source B
14	Quad Select Input	36	Phase B Output
15	Tachometer Output	37	Phase B Output
16	Brake/Tach Timing Input	38	Vmotor
17	Overvoltage/Coast Input	39	Source A
18	Soft-Start Input	40	Source A
19	Ground	41	Phase A Output
20	H3 Input	42	Phase A Output
21	H2 Input	43	Vmotor
22	H1 Input	(Case)	(No Connection)

PIN DESCRIPTIONS / FUNCTIONALITY

VCC (Pin 1) -- The Vcc Supply input provides bias voltage to all of the internal control electronics within the OM9371, and should be connected to a nominal +15Vdc power source. High frequency bypass capacitors (10uF polarized in parallel with 0.1uF ceramic are recommended) should be connected as close as possible to pin 1 and Ground (pin 19).

ERROR AMPLIFIER (EA1- Input, Pin 2; EA1+ Input, Pin 4; EA1 Output, Pin 8) -- The Error Amplifier is an uncommitted LM158-type operational amplifier, providing the user with many external control loop compensation options. This amplifier is compensated for unity gain stability, so it can be used as a unity gain input buffer to the internal PWM comparator when pin 2 is connected to pin 8. The output of the Error Amplifier is internally connected to the PWM comparator's "-" input, simplifying external layout connections.

+5V REFERENCE OUTPUT (Pin 5) -- This output provides a temperature-compensated, regulated voltage reference for critical external loads. It is recommended that this pin be used to power the external Hall-effect motor position sensors. By design, the +5V reference must be in regulation before the remainder of the control circuitry is activated. This feature allows the Hall-effect sensors to become powered and enabled before any Phase Output is enabled in the OM9371, preventing damage at turn-on. High-frequency bypass capacitors (10uF polarized in parallel with 0.1uF ceramic are recommended) should be connected as close as possible to pin 5 and Ground (pin 19).

SPARE AMPLIFIER (EA2- Input, Pin 6; EA2+ Input, Pin 3; EA2 Output, Pin 7) -- The Spare Amplifier is an uncommitted LM158-type operational amplifier, and in addition to the internal error amplifier, provides the user with additional external control loop compensation options. This amplifier is also compensated for unity gain stability and it can be used as a unity gain input buffer when pin 6 is connected to pin 7. If the Spare Amplifier is unused, pin 3 should be connected to Ground, and pin 6 should be connected to pin 7.

PWM INPUT (Pin 9) -- This pin is connected to the "+" input of the internal PWM comparator. The PWM output clears the internal PWM latch, which in turn commands the Phase Outputs to chop. For voltage-mode control systems, pin 9 may be connected to the Oscillator Timing Input, pin 10.

OSCILLATOR TIMING INPUT (Pin 10) -- The Oscillator Timing Input sets a fixed PWM chopping frequency by means of an internal resistor (Rosc), whose value is set to 75kΩ, connected from pin 10 to the +5V Reference Output, and an internal capacitor (Cosc), whose value is 1800pF, connected from pin 10 to Ground. In custom applications, the recommended range of values for Rosc is 10kΩ to 100kΩ, and for Cosc is 0.001uF to 0.01uF, and the maximum operating frequency should be kept below 20kHz. The approximate oscillator frequency is:

$$fo = \frac{2}{(Rosc \times Cosc)} \quad [Hz]$$

The voltage waveform on pin 10 is a ramp whose magnitude is approximately 1.2Vp-p, centered at approximately 1.6Vdc. In addition to the voltage-mode PWM control, pin 10 may be used for slope compensation in current-mode control applications.

ISENSE (Pin 11) -- This pin is connected to the output of the internal current-sense amplifier. It drives a peak-current (cycle-by-cycle) comparator which controls Phase Output chopping, and a fail-safe current comparator which, in the event of an output overcurrent condition, activates the soft-start feature and disables the Phase Outputs until the overcurrent condition is removed. The magnitude of the voltage appearing at pin 11 is dependent upon the voltages present at the current-sense amplifier inputs, ISH and ISL:

$$V(Isense) = 2.5V + [2 \times ABS (ISH - ISL)] \quad [Volts]$$

CURRENT SENSE INPUTS (ISH, Pin 12; ISL, pin 13) -- These inputs to the current-sense amplifier are interchangeable and they can be used as differential inputs. The differential voltage applied between pins 12 and 13 should be kept below +/-0.5Vdc to avoid saturation.

QUAD SELECT INPUT (Pin 14) -- This input is used to set the OM9371 in a half control or full control chopping regime. When driven with a logic low level, the OM9371 is in the half control mode, whereby only the three lower (pull-down) power switches associated with the Phase Outputs are allowed to chop. Alternately, when driven with a logic high level, the OM9371 is in the full control mode, where all six power switches (pull-up and pull-down) associated with the Phase Outputs are chopped by the PWM. During motor braking, changing the logic state of the Quad Select Input has no effect on the operation of the OM9371.

TACHOMETER OUTPUT (Pin 15) -- This output provides a fixed width 5V pulse when any Hall-effect Input (1, 2 or 3) changes state. The pulse width of the Tachometer Output is set internally in the OM9371 to 113µs (nominal). The average value of the output voltage on pin 15 is directly proportional to the motor's speed, so this output may be used (with an external averaging filter) as a true tachometer output, and fed back to the Speed Input (pin 23) to sense the actual motor speed.

Note: Whenever pin 15 is high, the internal Hall-effect position latches are inhibited (i.e. "latched"), to reject noise during the chopping portion of the commutation cycle, and this makes additional commutations impossible. This means that in order to prevent false commutation at a speed less than the desired maximum speed, the highest speed as observed at the Tachometer Output should be set above the expected maximum value.

BRAKE / TACH TIMING INPUT (Pin 16) -- The Brake/Tach Timing Input is a dual-purpose input. Internal to the OM9371 are timing components tied from pin 16 to Ground (a 51kΩ resistor and a 3300pF capacitor). These components set the minimum pulse width of the Tachometer Output to 113µs, and this time may be adjusted using external components, according to the equation:

$$T(tach) = 0.67 \times (C_t + 3300pf) \times \left(\frac{Rt \times 51k\Omega}{Rt + 51k\Omega}\right) (\mu s)$$

The recommended range of external resistance (to Ground) is 15kΩ to ∞, and the range of external capacitance (to Ground) is 0pF to 0.01uF. With each Tachometer Output pulse, the capacitor tied to pin 16 is discharged from approximately 3.33V to approximately 1.67V by an internal timing resistor. The Brake / Tach Timing Input has another function. If this pin is pulled below the brake threshold voltage, the OM9371 will enter the brake mode. The brake mode is defined as the disabling of all three high-side (pull-up) drivers associated with the Phase Outputs, and the enabling of all three low-side (pull-down) drivers.

OVERVOLTAGE / COAST INPUT (Pin 17) -- This input may be used as a shutdown or an enable/disable input to the OM9371. Also, since the switching inhibit threshold is so tightly defined, this input can be directly interfaced with a resistive divider which senses the voltage of the motor supply, Vm, for overvoltage conditions. A high level (greater than the inhibit threshold) on pin 17 causes the coast condition to occur, whereby all Phase Outputs revert to a Hi-Z state and any motor current which flowed prior to the Overvoltage / Coast command is commutated via the power "catch" rectifiers associated with each Phase Output.

SOFT-START INPUT (Pin 18) -- The Soft-Start input is internally connected to a 10µA (nominal) current source, the collector of an NPN clamp/discharge transistor, and a voltage comparator whose soft-start/restart threshold is 0.2Vdc (nominal). An external capacitor is connected from this pin to Ground (pin 19). Whenever the Vcc supply input drops below the turn-on threshold, approximately 9Vdc, or the sensed current exceeds the over-current threshold, approximately 0.3V at the current sense amplifier, the soft-start latch is set. This drives the NPN clamp transistor which discharges the external soft-start capacitor. When the capacitor voltage drops below the soft-start/restart threshold and a fault condition does not exist, the soft-start latch is cleared; the soft-start capacitor charges via the internal current source.

In addition to discharging the soft-start capacitor, the clamp transistor also clamps the output of the error amplifier internal to the controller IC, not allowing the voltage at the output of the error amplifier to exceed the voltage at pin 18, regardless of the inputs to the amplifier. This action provides for an orderly motor start-up either at start-up or when recovering from a fault condition.

GROUND (Pin 19) -- The voltages that control the OM9371 are referenced with respect to this pin. All bypass capacitors, timing resistors and capacitors, loop compensation components, and the Hall-effect filter capacitors must be referenced as close as possible to pin 19 for proper circuit operation. Additionally, pin 19 must be connected as close as physically possible to the Motor Return, pins 27 and 28.

HALL-EFFECT INPUTS (H1, Pin 22; H2, Pin 21; H3, Pin 20) -- Each input has an internal pull-up resistor to the +5V Reference. Each input also has an internal 180pF noise filter capacitor to Ground. In order to minimize the noise which may be coupled from the motor commutation action to these inputs, it is strongly recommended that additional external filter capacitors, whose value is in the range of 2200pF, be connected from each Hall-Effect Input pin to Ground. Whatever capacitor value is used, the rise/fall times of each input must be guaranteed to be less than 20us for proper tachometer action to occur. Motors with 60 degree position sensing may be used if one or two of the Hall-effect sensor signals is inverted prior to connection to the Hall-Effect Inputs.

SPEED INPUT (Pin 23) - This pin is connected to the "+" input of a voltage comparator, whose threshold is 0.25Vdc. As long as the Speed Input is less than 0.25V, the direction latch is transparent. When the Speed Input is greater than 0.25V, then the direction latch inhibits all changes in direction. It is recommended, especially while operating in the half control mode, that the Tachometer Output is connected to the Speed Input via a low-pass filter, **such that the direction latch is transparent only when the motor is spinning very slowly**. In this case, the motor has too little stored energy to damage the power devices during direction reversal.

DIRECTION INPUT (Pin 24) - This input is used to select the motor direction. This input has an internal protection feature: the logic-level present on the Direction Input is first loaded into a direction latch, then shifted through a two-bit shift register before interfacing with the internal output phase driver logic decoder. Also, protection circuitry detects when the input and the output of the direction latch or the 2-bit shift register are different, and inhibits the Phase Outputs (i.e. Hi-Z) during those times. This feature may be used to allow the motor to coast to a safe speed before a direction reversal takes place. Power stage cross-conduction (current "shoot-through" from Vmotor to Ground through simultaneously enabled pull-up and pull-down drivers) is prevented by the shift register as it is clocked by the PWM oscillator, so that a fixed delay of between one and two PWM oscillator clock cycles occurs. This delay or "dead-time" guarantees that power-stage cross-conduction will not occur.

CURRENT SENSE OUTPUTS (CSH, Pin 25; CSL, Pin 26) - The Current Sense Outputs produce a differential voltage equal to the motor current times the sense resistance value (5mΩ nominal). There is an internal .018μF filter capacitor across pins 25 and 26, and two 100Ω series resistors, one between each pin and each end of the current sense resistor. To configure the current sense amplifier for cycle-by-cycle current limiting and/or overcurrent protection, connect pin 25 to pin 12 (ISH) and pin 26 to pin 13 (ISL).

MOTOR RETURN (Pins 27 and 28) - These pins are connected to the most negative terminal of the motor supply (Vm-). This connection is electrically isolated from the logic Ground internal to the OM9371 package to minimize, if not eliminate, noise on the logic ground. The connection to the logic ground is made by the user external to the package (refer to Ground (pin 19)). In order to minimize packaging losses and parasitic effects, it is essential that both of these pins be firmly connected to the motor supply Ground, with as short a connection as physically possible.

SOURCE (Pins 29, 34, 35, 39 and 40) -- The source pins form the low-side connection of the pull-down switches associated with each Phase Output. Because of the switching current capability of the OM9371, all 6 pins should be externally connected together with a low impedance bus to minimize losses and voltage differentials. Also, due to layout design considerations, pin 29 is internally connected to the "top" of the internal current-sense resistor.

PHASE OUTPUTS (Phase A, Pins 41 and 42; Phase B, Pins 36 and 37; Phase C, Pins 31 and 32) -- These outputs are connected to either Vmotor via the pull-up driver or Source via the pull-down driver, depending upon the Hall-Effect and Direction Inputs (see Commutation Truth Table). The two pins associated with each Phase Output must be connected to one of the three phases of the motor driven by the OM9371.

V_{MOTOR} (Pins 33, 38, and 43) - These pins are connected to the most positive terminal of the motor supply (Vm+). For proper operation, all three pins must be connected together externally with a low impedance power bus. The V_{motor} power bus should be bypassed with an adequately voltage-rated ceramic capacitor, 0.1μF (typical), and a low-ESR electrolytic capacitor, whose capacitance value can be selected by the following: 10μF-per-Ampere of average motor current from V_{motor} to Motor Return.

Note: All connections, including the power bus capacitor connections, must be made as close as possible to the V_{motor} and Motor Return pins to minimize parasitic effects.

PACKAGE AND SCREENING OPTIONS

The OM9371 is offered in a hermetic flatpack package as well as a plastic ring frame, low profile flatpack package. The hermetic package, F-43, is shown in Figure 1. The plastic ring frame, low profile package, MP3-43L, has slightly larger dimensions and is shown in Figure 2.

The hermetic version is offered in two standard screening levels: a full military temperature range of -55°C to +125°C with limited screening and with MIL-STD-883 screening. The plastic ring frame version is offered in an industrial temperature range of -40°C to +85°C with limited screening.

The screening levels for the SFB, SF and SPP versions are listed in the table below. All tests and inspections are in accordance with those listed in MIL-STD-883.

Test/Inspection	SFB	SF	SPP
Precap Visual Inspection	100%	100%	100%
Temperature Cycle	100%	N.A.	N.A.
Mechanical Shock	100%	N.A.	N.A.
Hermeticity (Fine and Gross Leak)	100%	100%	N.A.
Pre Burn-In Electrical	100%	N.A.	N.A.
Burn-In (160 hours)	100%	N.A.	N.A.
Final Electrical Test	-55°C, +25°C, +125°C	+25°C	+25°C
Group A Testing	100%	N.A.	N.A.
Final Visual Inspection	100%	100%	100%

APPLICATIONS

Start-Up Conditions

The OM9371 3-phase brushless DC motor controller/driver is designed to drive fractional to integral horsepower motors. To ensure proper operation, it is necessary to ensure that the high-side bootstrap capacitors are charged during initial start-up. However, the method(s) used to ensure this may be dependent upon the application. For example, some applications may only require that OV_COAST (pin 17) be connected to ground, either via a hardwire connection or via a switch (Enable/Disable), before applying Vcc. When Vcc is applied, the controller/driver is forced into brake mode for approximately 200μsec (all high-side drivers are disabled and all low-side drivers are enabled).

This may not be adequate for other applications; RC_BRAKE (pin 16) may have to be momentarily connected to ground via a switch, either manually or electronically (ref. Figure 3). Note that with the component values shown in Figure 3, RC_BRAKE is pulled low for approximately 300 mSec after applying Vcc at pin1.

Modes of Operation

Figures 4 and 5, shown on the following pages, provide schematic representations of typical voltage-mode and current-mode applications for the OM9371 controller/driver.

Figure 4 represents the implementation of a typical voltage-mode controller for velocity control. A voltage or speed command is applied to the noninverting input of the error amplifier which is configured as a voltage follower. The output of the error amplifier is compared to a pulse width modulated ramp, and since motor speed is nearly proportional to the average phase output voltage, the speed is controlled via duty cycle control. If a speed feedback loop is required, the tachometer output can be connected to the inverting input of the error amplifier via a loop compensation network.

Figure 4 also shows the implementation of the cycle-by-cycle current limit/overcurrent protection feature of the OM9371. The load current is monitored via the controller's internal sense resistor. The current sense signal is filtered and fed into the current sense amplifier where the absolute value of ISH-ISL is multiplied by two and biased up by 2.5 volts. The output of the current sense amplifier is compared to a fixed reference, thus providing cycle-by-cycle current limiting and/or overcurrent protection as necessary. The typical peak current threshold (ISH-ISL) is 0.20 volts; the typical over current threshold (ISH-ISL) is 0.30 volts.

Figure 5 represents the implementation of a typical current-mode controller for torque control. The load current is monitored via the controller's internal sense resistor. The current sense signal is filtered and fed into the current sense amplifier where the absolute value of ISH-ISL is multiplied by two and biased up by 2.5 volts. Besides the implementation of the cycle-by-cycle current limit/overcurrent protection feature of the OM9371 discussed in the preceding paragraph, the output of the current sense amplifier is fed into the error amplifier which is configured as a differential amplifier. An error signal representing the difference between the current command input and the value of the amplified current sense signal is produced. Then it is compared to a pulse width modulated ramp and since torque is nearly proportional to the average phase output current, the torque is controlled via duty cycle control.

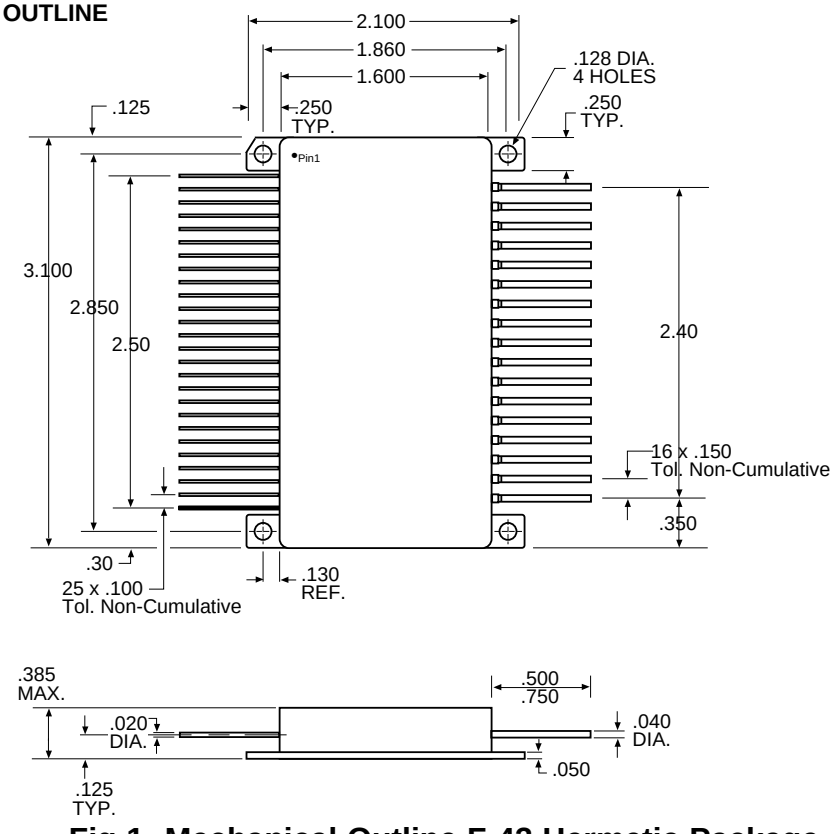


Fig 1: Mechanical Outline F-43 Hermetic Package

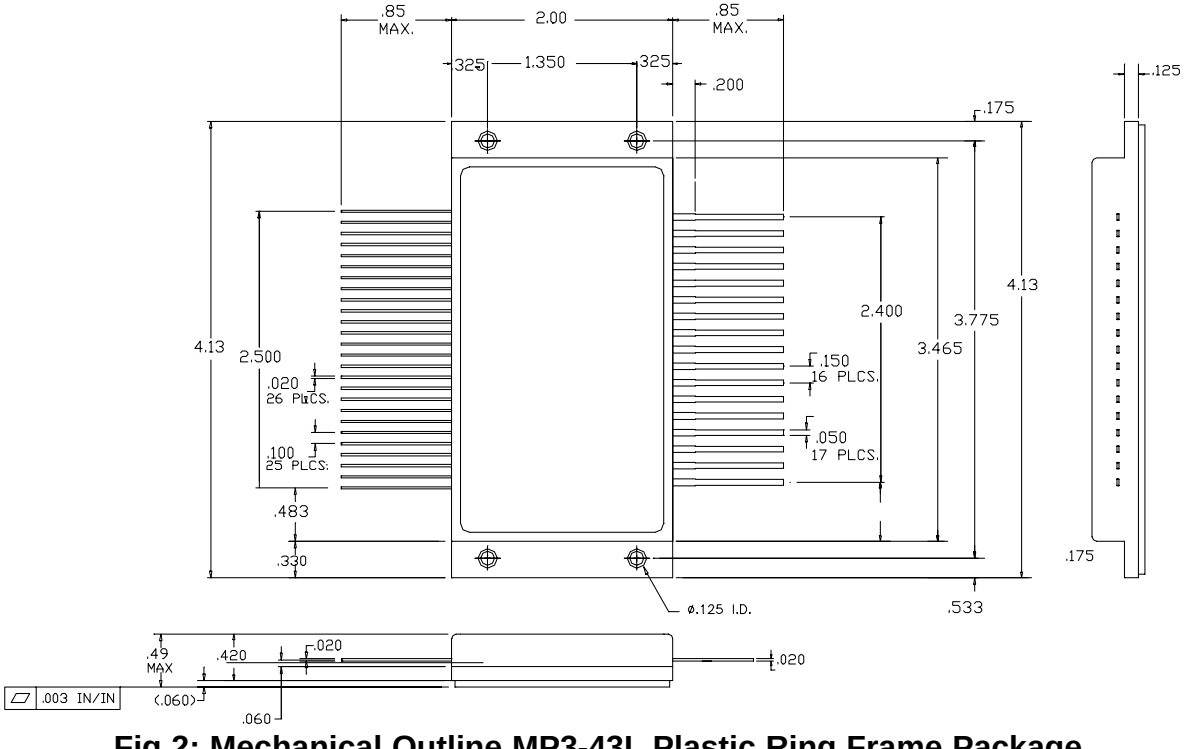


Fig 2: Mechanical Outline MP3-43L Plastic Ring Frame Package

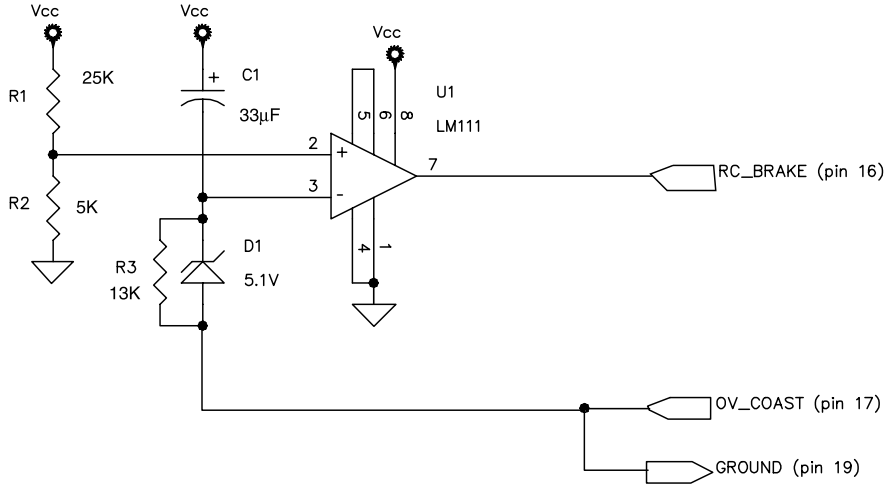


Fig 3: Optional Start-Up Circuit

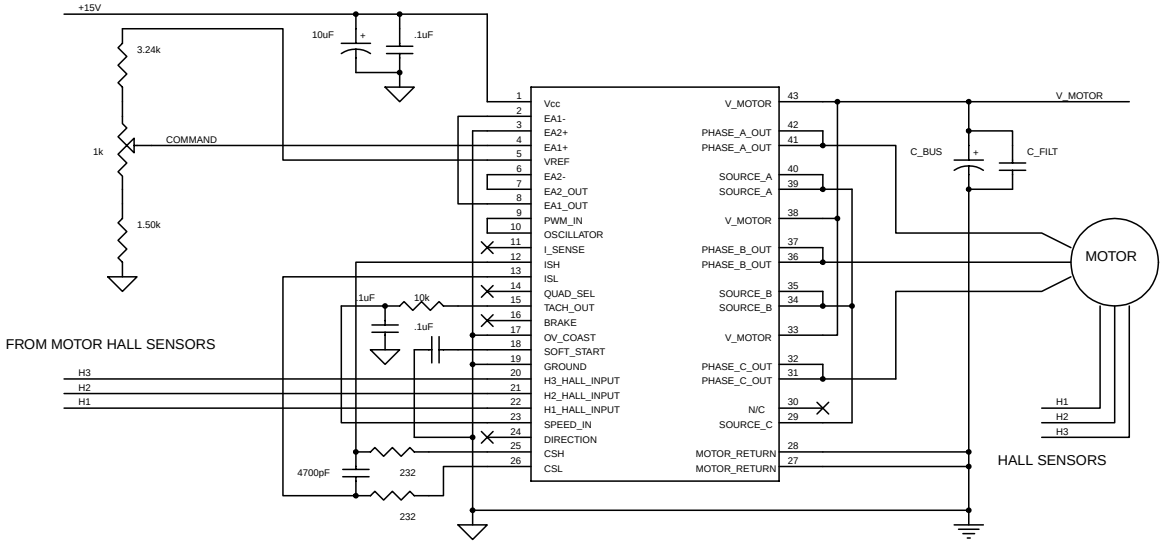


Fig 4: Implementation of a Voltage-Mode Controller

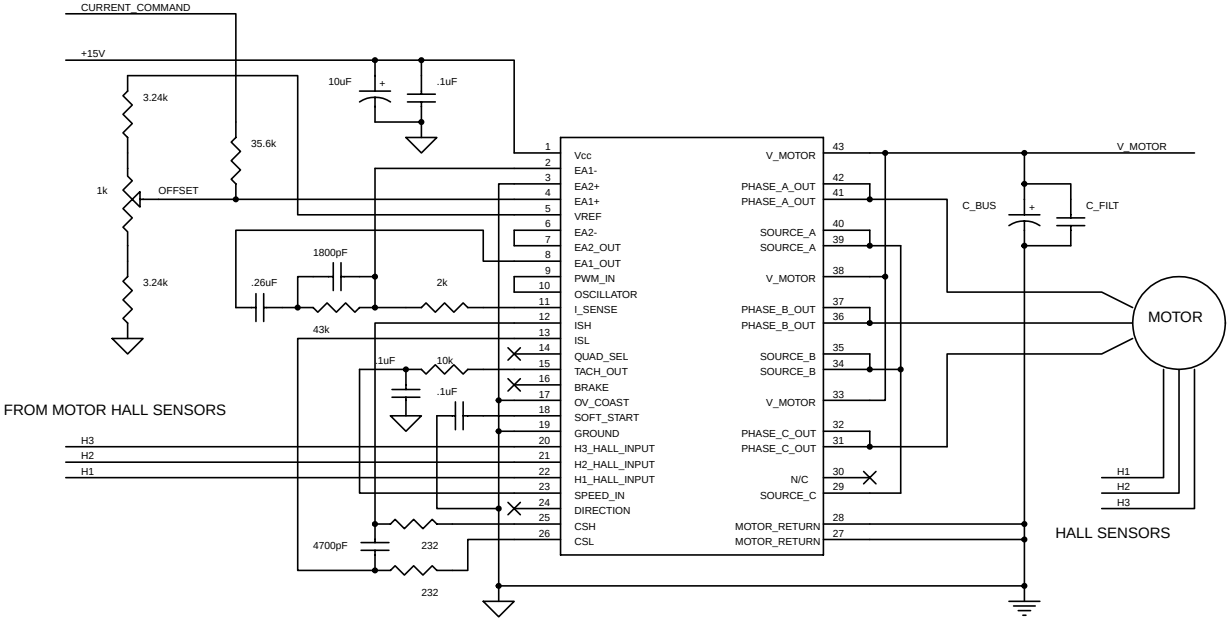


Fig 5: Implementation of a Current-Mode Controller