International
IOR Rectifier

Data Sheet No. PD60244A

IRS26094DSPbF

HALF BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to 600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Under-Voltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Separate logic and power grounds
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal 540 ns dead-time, programmable up to 4.2 µs with external resistor
- Lower di/dt gate driver for better noise immunity
- High side output in phase with IN input
- Shutdown input turns off both channels
- Integrated bootstrap diode
- Suitable for both trapezoidal and sinusoidal motor control
- RoHS compliant

Typical Applications

- Motor Control
- Air Conditioners
- General Purpose Inverters
- Micro/Mini Inverter Drivers

Product Summary

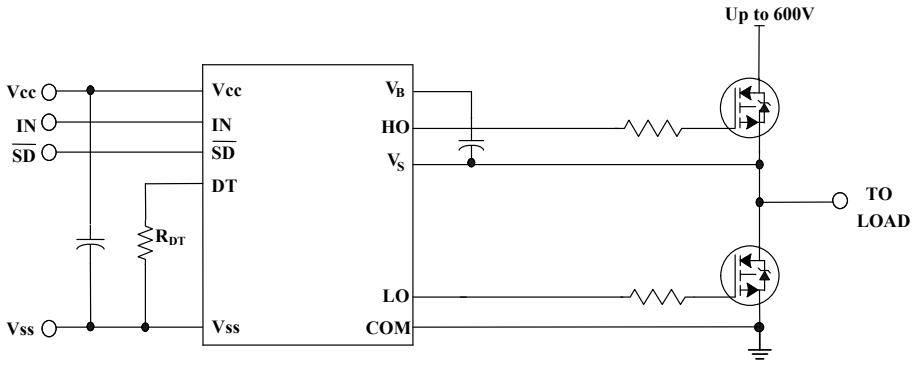
Topology	Half bridge driver
V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typ.)	120 mA & 250 mA
t_{ON} & t_{OFF} (typ.)	750 ns & 200 ns
Dead-time (typ.)	540 ns, programmable up to 4.2 µs

Package Options

14-Lead SOIC

14-Lead PDIP

Typical Connection Diagram



IRS26094D

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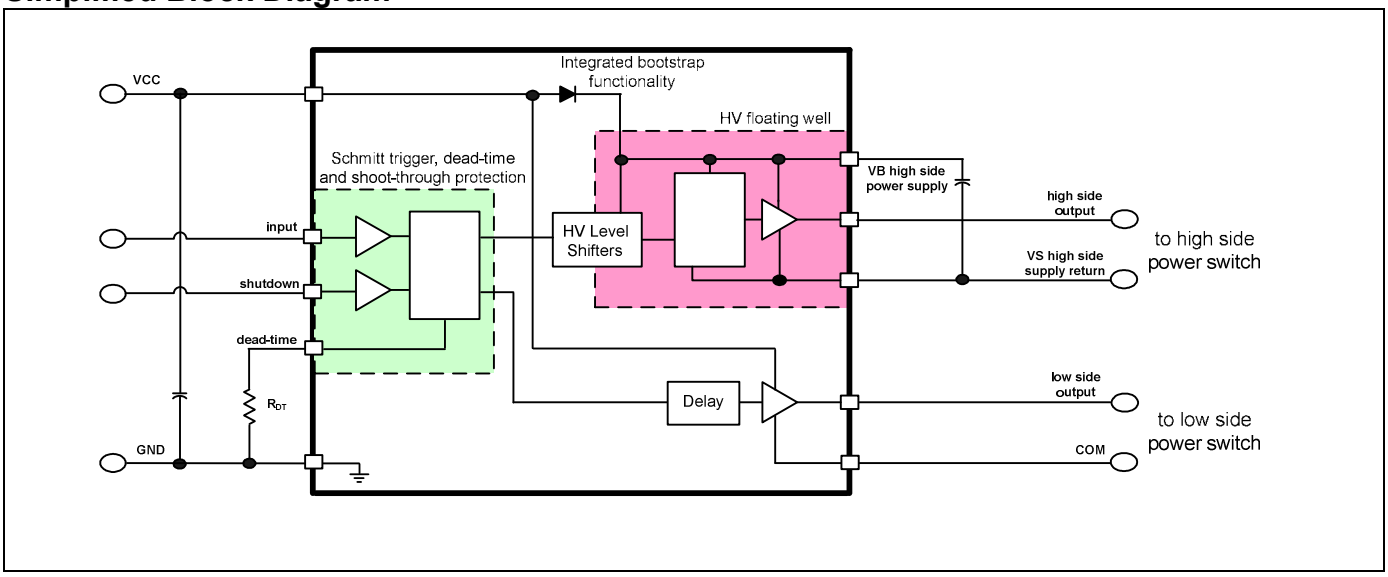
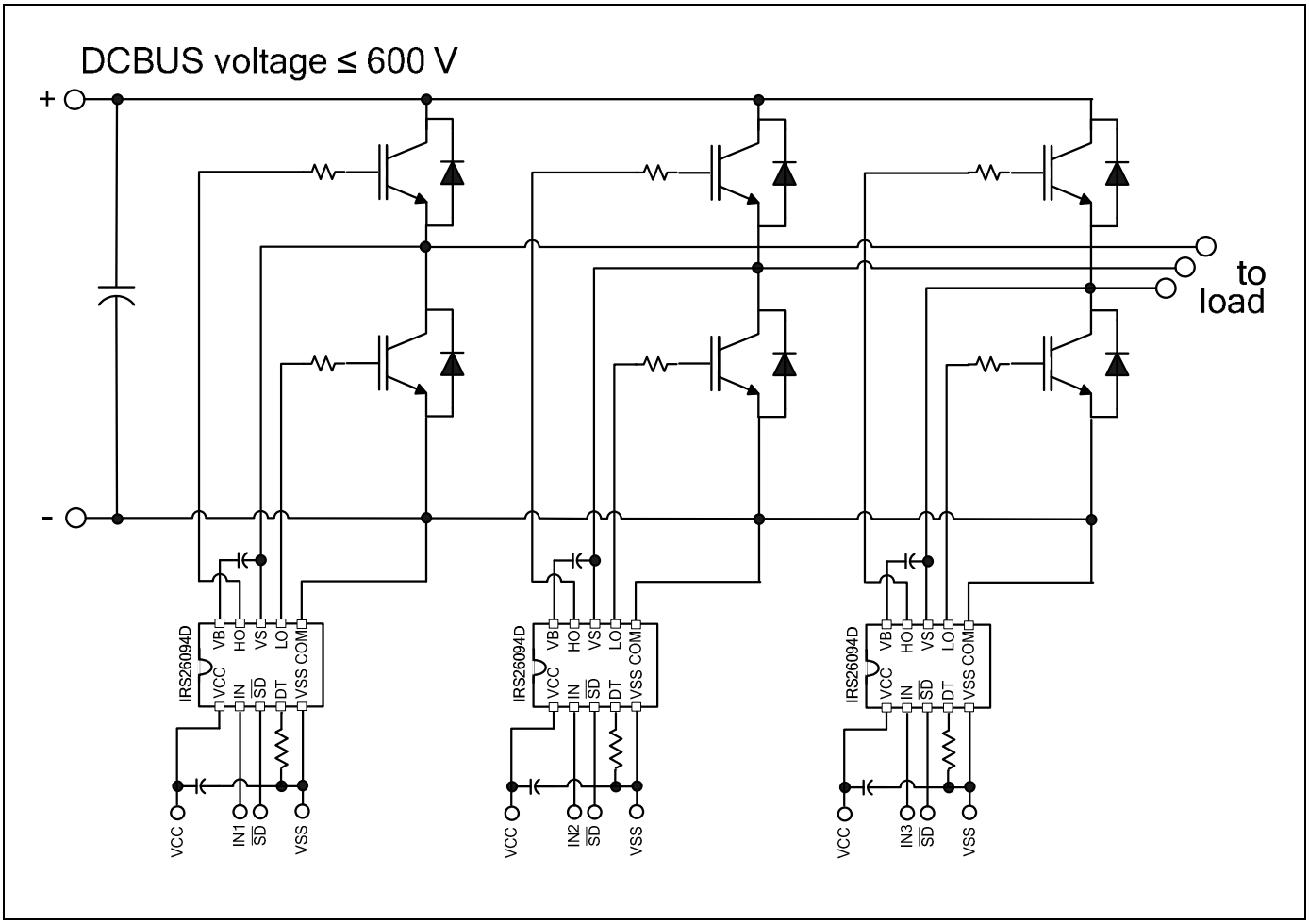
Description

The IRS26094D is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. Between the turn-off of an output driver and the turn-on of the other a minimum dead-time interval is inserted, which can be optionally programmed with an external resistor for greater design flexibility. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration up to 600 V.

Simplified Block Diagram



Typical Application Diagram



Qualification Information†

Qualification Level		Industrial††
		Comments: This IC has passed JEDEC industrial qualification. IR consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2 , 260°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise specified. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	620	V
V_S	High side floating supply offset voltage		V_B - 20†	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	20†	
COM	Low side power ground		V_{CC}-25†	V_{CC}+0.3	
V_{LO}	Low side output voltage		COM-0.3	V_{CC} + 0.3	
V_{DT}	Programmable dead-time input voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltages		-0.3	V_{CC} + 0.3	
PW_{IN}	Input pulse width		500	—	ns
dVS/dt	Allowable offset supply voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25°C	14 lead SOIC	—	1.0	W
		14 lead PDIP		1.6	
Rth_{JA}	Thermal resistance, junction to ambient	14 lead SOIC	—	120	°C/W
		14 lead PDIP		75	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

† All supplies are fully tested at 25 V. An internal clamp exists for each supply: a 25 V clamp between Vcc and COM, while a 20 V clamp for each other supply.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise specified. The V_S offset ratings are tested with all supplies biased at 15 V.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +10	V_S + 20	V
V_S	Static high side floating supply offset voltage†	COM-8	600	
$V_S(t)$	Transient high side floating supply offset voltage††	COM-50	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
COM	Low side power ground	-5	5	
V_{LO}	Low side output voltage	COM	V_{CC}	
V_{DT}	Programmable dead-time input voltage	0	V_{CC}	
V_{IN}	Logic input voltages	0	V_{CC}	
R_{DT}	External dead-time pulldown resistor	0	200	kΩ
T_A	Ambient temperature	-40	125	°C

† Logic operation for V_S of –8 V to 600 V. Logic state held for V_S of –8 V to $–V_{BS}$.

†† Operational for transient negative V_S of COM - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

Dynamic Electrical Characteristics

$V_{CC} = V_B$ = 15 V, V_S = COM = V_{SS}, T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	470	750	1100	ns	V_{IN} = 0 V and 5 V, R_{DT} = 0 Ω
t_{off}	Turn-off propagation delay	120	220	300		V_{IN} = 0 V and 5 V
t_r	Turn-on rise time	—	150	220		
t_f	Turn-off fall time	—	50	80		
t_{SD}	Shutdown propagation delay	—	220	300		
t_{DT}	Dead-time	350	530	800		R_{DT} = 0 Ω
		3400	4200	5400		R_{DT} = 200 kΩ
MDT	Dead-time matching†	—	—	60		R_{DT} = 0 Ω
		—	—	600		R_{DT} = 200 kΩ
MT	ton, toff propagation delay matching time	—	—	50		

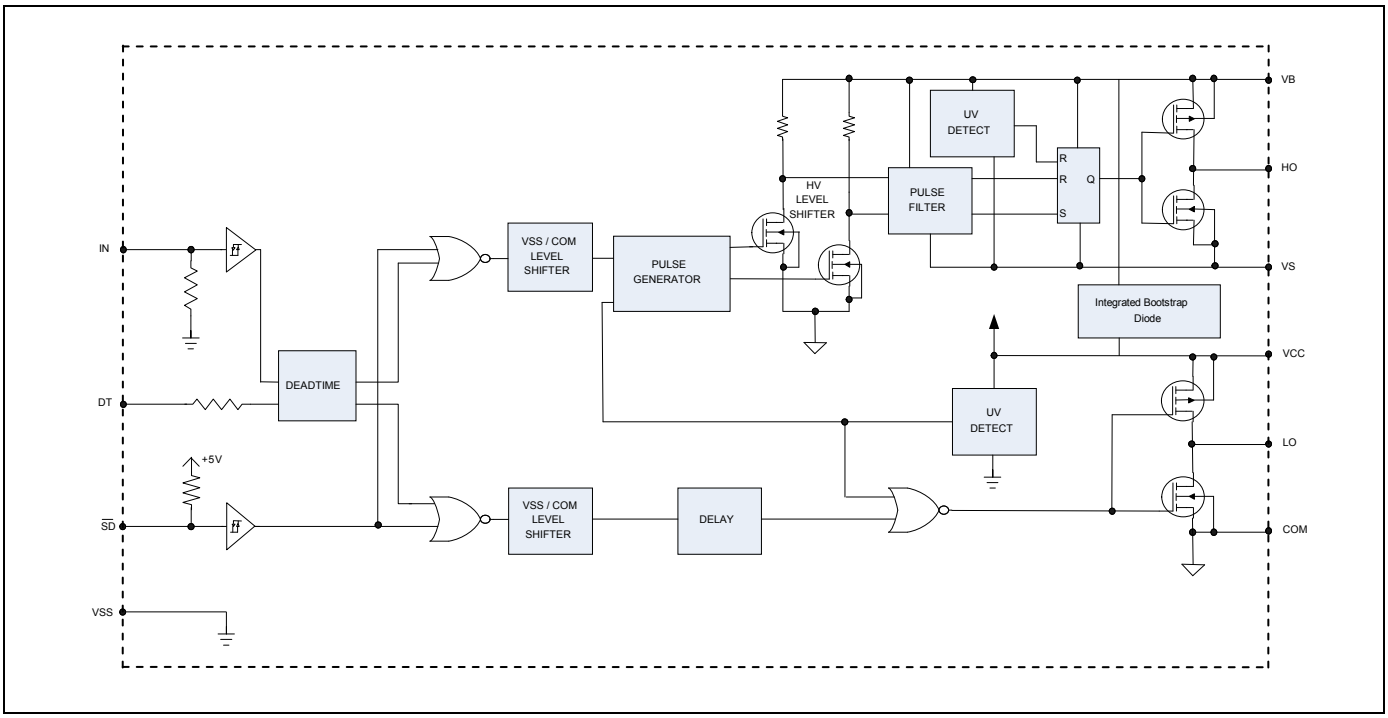
† Please see the application section for more details.

Static Electrical Characteristics

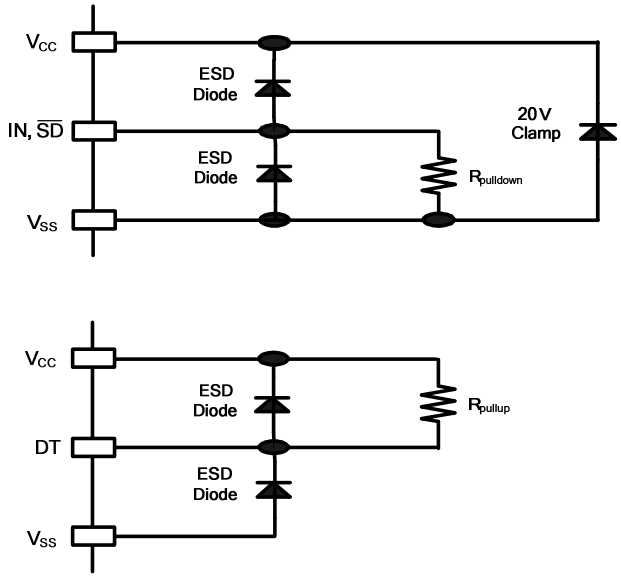
(V_{CC}-COM) = (V_B-V_S) = 15 V and T_A = 25 °C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS}. The V_O and I_O parameters are referenced to COM and V_S and are applicable to the output leads LO and HO respectively. The V_{CCUV} and V_{BSUV} parameters are referenced to COM and V_S respectively.

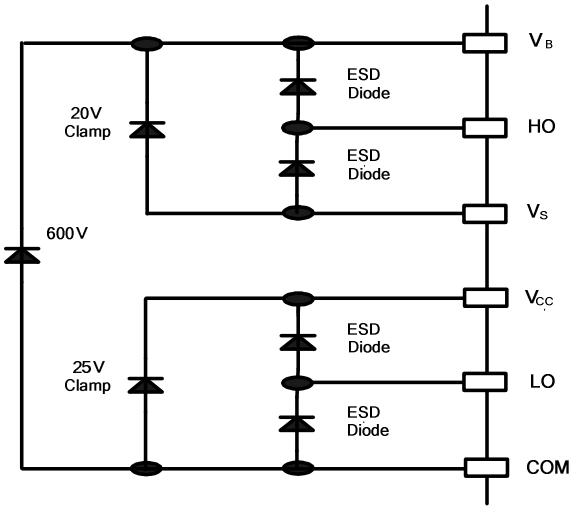
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO, logic "0" for LO	2.5	—	—	V	
V_{IL}	Logic "0" input voltage for HO, logic "1" for LO	—	—	0.8		
$V_{IN,TH+}$	Input positive going threshold	—	1.9	—		
$V_{IN,TH-}$	Input negative going threshold	—	1	—		
V_{OH}	High level output voltage	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage	—	0.2	0.6		
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply under-voltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply under-voltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply under-voltage hysteresis	0.4	0.7	—		
I_{LK}	Offset supply leakage current	—	1	50	µA	V_B =V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	45	70		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	—	1.1	1.8	mA	V_{IN} = 0 V or 5 V, R_{DT} = 0 Ω
I_{IN+}	Logic "1" input bias current	—	5	20	µA	V_{IN} = 5 V
I_{IN-}	Logic "0" input bias current	—	—	2		V_{IN} = 0 V
I_{o+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0 V or 15 V PW ≤ 10 µs
I_{o-}	Output low short circuit pulsed current	250	350	—		
$V_{SD,TH+}$	Shutdown inactive going threshold	2.5	—	—	V	
$V_{SD,TH-}$	Shutdown active going threshold	—	—	0.8		
I_{SD+}	Shutdown inactive input bias current	—	120	165	µA	SD = 5 V
I_{SD-}	Shutdown active input bias current	—	—	1		SD = 0 V
$V_{DT,TH+}$	Dead-time activating shutdown threshold	—	V_{CC}-2	—	V	
I_{SD+}	Dead-time input bias current	—	750		µA	DT = 0 V
I_{SD-}	Dead-time activating shutdown input bias current	—	—	1		DT = V_{CC}
R_{BS}	Bootstrap resistance	—	200	—	Ω	

Functional Block Diagram



Input/Output Pin Equivalent Circuit Diagrams



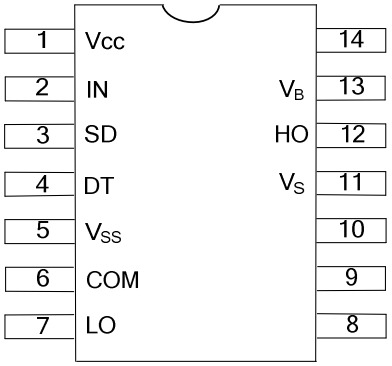


Lead Definitions

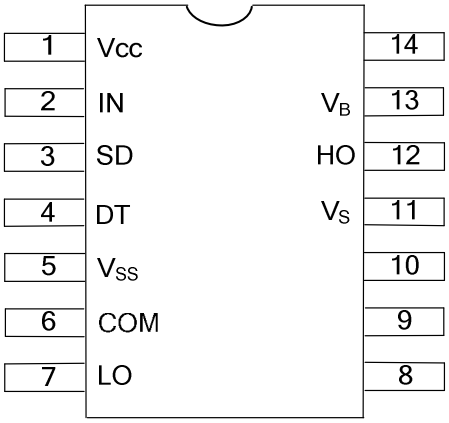
Symbol	Description
VCC	Low side and logic power supply
VSS	Logic supply return
VB	High side floating power supply
VS	High side floating supply return
IN	Logic input for high and low side gate driver outputs HO and LO, input is in-phase with HO output and out-of-phase with LO output
/SD	Logic input for shutdown, turns off both channels, active low
DT	Programmable dead-time input
HO	High side gate driver output
LO	Low side gate driver output
COM	Low side supply return

Lead Assignments

14 lead SOIC



14 lead PDIP



Application Information and Additional Details

IGBT/MOSFET Gate Drive

The IRS26094D HVIC is designed to drive high side and low side MOSFET or IGBT power devices. Figures 1 and 2 show the definition of some of the relevant parameters associated with the gate driver output functionality. The output current that drives the gate of the external power switches is defined as I_O. The output voltage that drives the gate of the external power switches is defined as V_{HO} for the high side and V_{LO} for the low side; this parameter is sometimes generically called V_{OUT} and in this case the high side and low side output voltages are not differentiated.

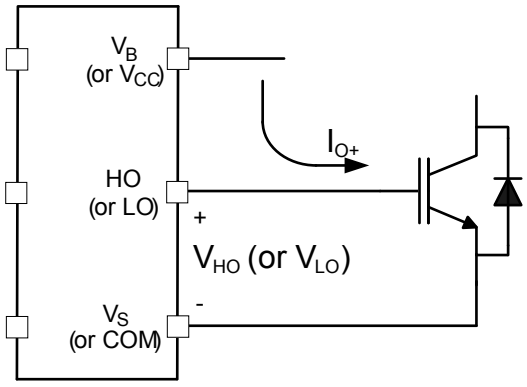


Figure 1: HVIC sourcing current

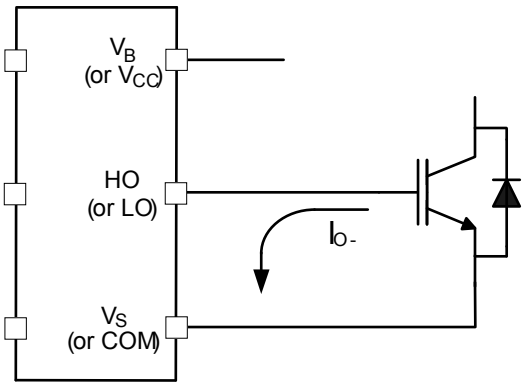


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationship between the input and output signals of the IRS26094D HVIC is shown in Figure 3. The definitions of some of the relevant parameters associated with the gate driver input to output transmission are given.

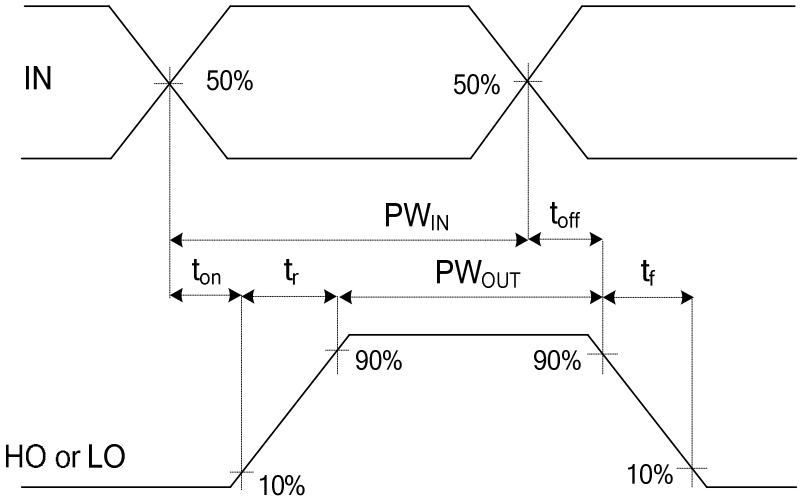


Figure 3: Switching time waveforms

During interval A of Figure 4 the HVIC receives the IN command to turn on the high side switch; correspondingly, the high side signal HO turns on and the low side signal LO turns off simultaneously. Vice versa, during interval B the HVIC receives the IN command to turn off the high side switch; correspondingly, the high side signal HO turns off and the low side signal LO turns on simultaneously.

During intervals C the shutdown signal /SD is activated low; correspondingly, both the high and the low side signals HO and LO turn off, regardless of the IN signal received.

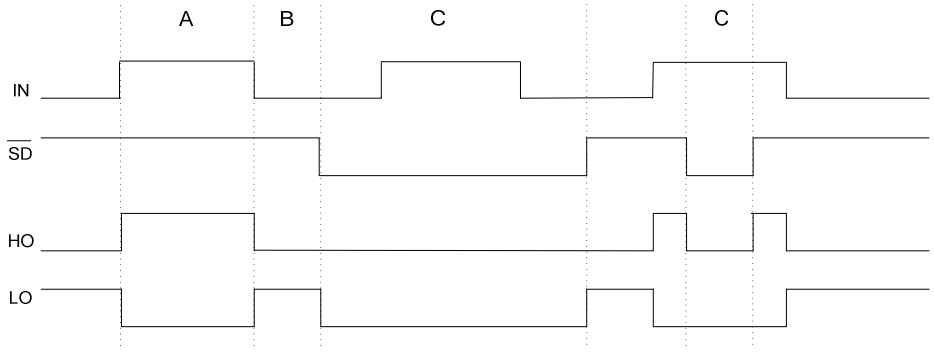


Figure 4: Input/output timing diagram

Dead-time and Programmability

The IRS26094D HVIC provides an internal dead-time protection, by automatically inserting a time interval between the turn-ons of the gate driver outputs LO and HO; to ensure that the power switch being turned off has fully turned off before the other power switch is turned on. Figure 5 illustrates the relationship between the output gate signals and defines the two dead-time parameters $t_{DTLO-HO}$ and $t_{DTHO-LO}$. These parameters distinguish between the commutation from HO turning off to LO turning on, and vice versa. Their maximum difference $|t_{DTLO-HO} - t_{DTHO-LO}|$ is defined as the dead-time matching parameter MDT.

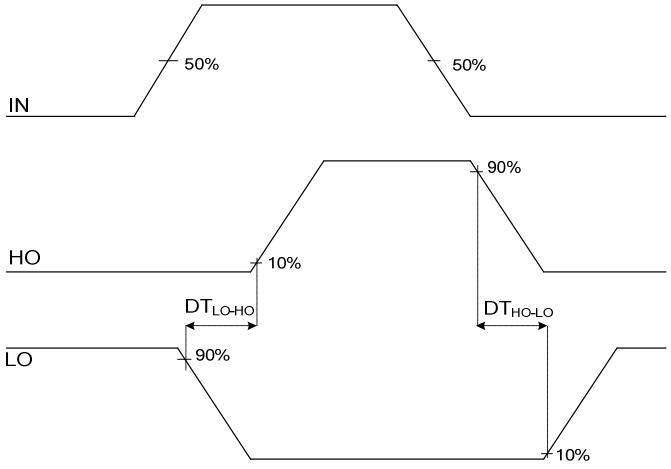


Figure 5: Dead-time definition

For the minimum dead-time interval to be automatically inserted, the DT input pin must be tied to V_{SS}, as shown in Figure 6.

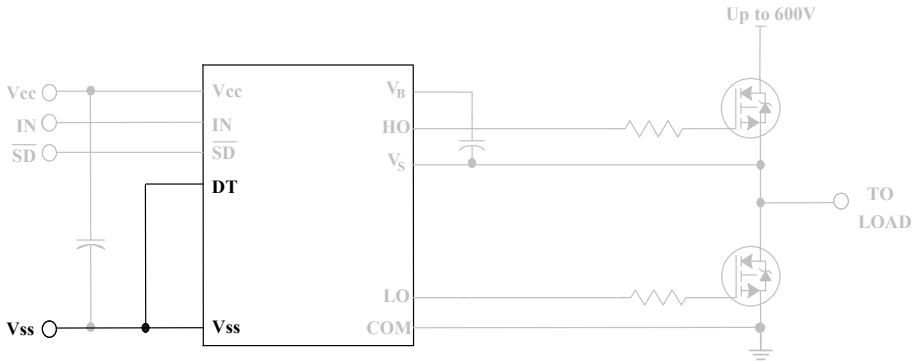


Figure 6: Minimum dead-time configuration

The dead-time interval to be automatically inserted can be optionally programmed with an external R_{DT} resistor connected between DT and V_{SS}, and increased up to the value of 4.2 µs, for greater design flexibility, as shown in Figure 7.

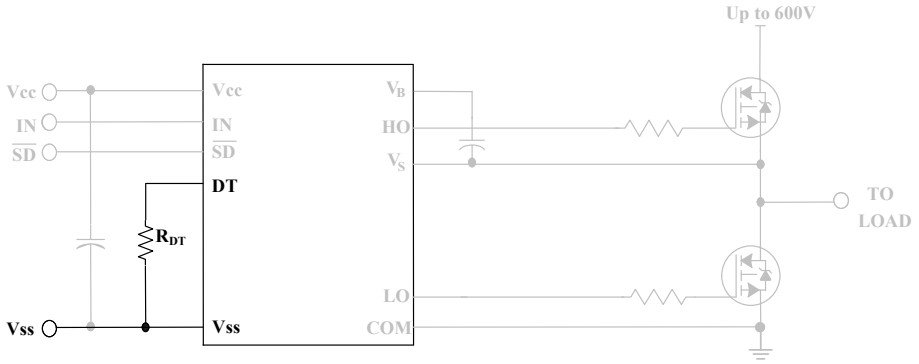


Figure 7: Optional programmable dead-time configuration

Thanks to the internal pull-up acting on DT, a protection feature enables the detection of open circuits occurring on the wire connecting the DT pin: whenever the voltage on DT exceed the $V_{DT,TH+}$ threshold, an open circuit is assumed and shutdown of the high and low side signals HO and LO is commanded. For this reason, R_{DT} must not exceed the maximum value recommended.

Matched Propagation Delays

The IRS26094D HVIC is designed for propagation delay matching. With this feature, the input to output propagation delays t_{ON}, t_{OFF} are the same for the low side and the high side channels; the maximum difference being specified by the delay matching parameter MT as defined in Figure 8.

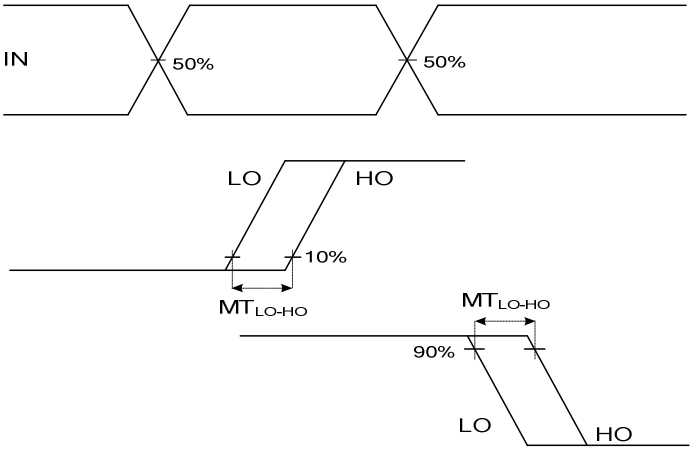


Figure 8: Delay matching waveform definition

Input Logic Compatibility

The IRS26094D HVIC is designed with inputs compatible with standard CMOS and TTL outputs with 3.3 V, 5 V and 15 V logic level signals. Figure 9 shows how an input signal is logically interpreted.

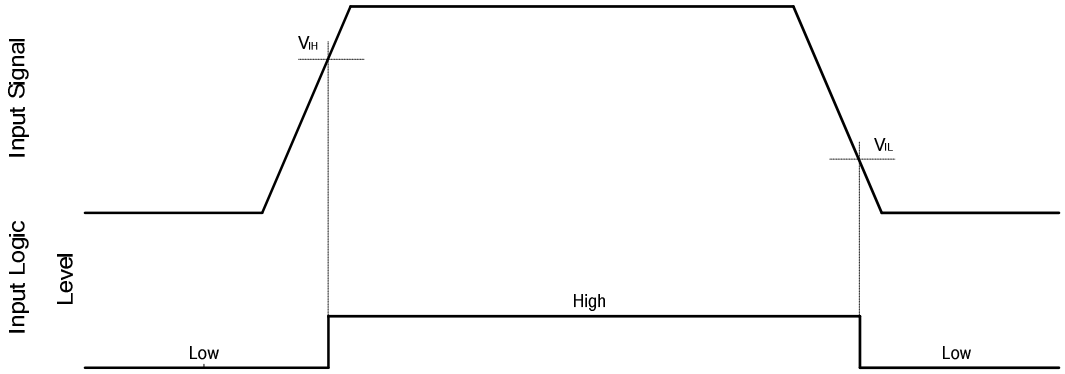


Figure 9: IN and /SD input thresholds

Shoot-Through Protection

The IRS26094D presents a shoot-through protection circuit which prevents cross-conduction of the power switches. Table 1 shows the input to output relationship in the form of a truth table.

IN	HO	LO
0	0	1
1	1	0

Table 1: Input/output truth table

Under-Voltage Lockout Protection

The IRS26094D HVIC provides under-voltage lockout protection on both the V_{CC} low side and logic fixed power supply and the V_{BS} high side floating power supply. Figure 10 illustrates this concept by considering the V_{CC} (or V_{BS}) plotted over time: as the waveform crosses the UVLO threshold, the under-voltage protection is entered or exited.

Upon power up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the gate driver outputs LO and HO will remain disabled. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during normal operation, the under-voltage lockout circuitry will shutdown the gate driver outputs LO and HO.

Upon power up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the gate driver output HO will remain disabled. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during normal operation, the under-voltage lockout circuitry will shutdown the high side gate driver output HO.

The UVLO protection ensures that the HVIC drives external power devices only with a gate supply voltage sufficient to fully enhance them. Without this protection, the gates of the external power switches could be driven with a low voltage, which would result in power switches conducting current while with a high channel impedance, which would produce very high conduction losses possibly leading to power device failure.

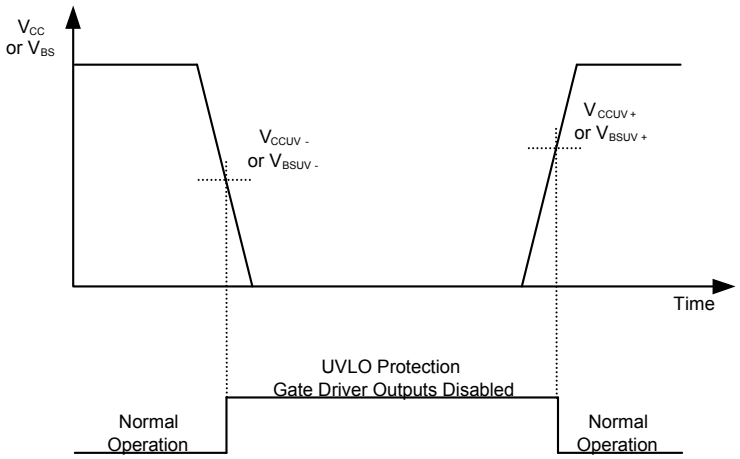


Figure 10: UVLO protection

Shutdown Input

The relationship between the shutdown input and the output signals of the IRS26094D HVIC is shown in Figure 11.

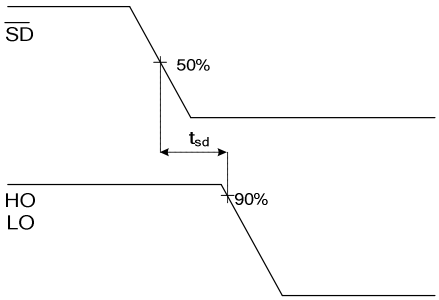


Figure 11: Shutdown waveforms definition

The shutdown functionality allows the µcontroller to shutdown or enable the gate driver outputs LO and HO: when the /SD pin is high the HVIC is able to operate normally (assuming no under-voltage condition occurs on V_{CC}), while when the /SD pin goes low, the gate drive outputs LO and HO are pulled low until the shutdown condition is ceased.
Table 2 gives a summary of the shutdown functionality.

/SD pin: shutdown functionality	
Shutdown input high	Outputs enabled*
Shutdown input low	Outputs disabled

Table 2: Shutdown functionality truth table
(*assuming no under-voltage condition occurs on V_{CC})

Truth Table: Under-Voltage lockout, Shutdown

Table 3 provides the truth table for the IRS26094D HVIC.

The 1st line shows that for V_{CC} below the UVLO threshold both the gate driver outputs LO and HO are disabled. After V_{CC} returns above V_{CCUV}, the gate driver outputs return functional.

The 2nd line shows that for V_{BS} below the UVLO threshold, the gate driver output HO is disabled. After V_{BS} returns above V_{BSUV}, HO remains low until a new rising transition of HIN is received.

The 3rd line shows that when a shutdown command is received through the /SD pin, both the gate driver outputs LO and HO are disabled. This condition is not latched.

The last line shows the normal operation of the HVIC.

	VCC	VBS	/SD	outputs	
				LO	HO
UVLO V_{CC}	$<V_{CCUV}$			0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$		-(IN)	0
Shutdown command	15 V	15 V	low	0	0
Normal operation	15 V	15 V	high	-(IN)	IN

Table 3: UVLO and shutdown truth table

Integrated Bootstrap Functionality

The IRS26094D HVIC embeds an integrated bootstrap FET that eliminates the need of external bootstrap diodes and resistors allowing an alternative drive of the bootstrap supply for a wide range of applications.
A bootstrap FET is connected between the high side floating power supply V_B and the low side and logic fixed power supply V_{CC}, as represented in Figure 12.

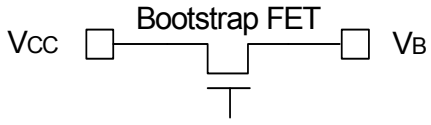


Figure 12: Simplified bootstrap FET connection

The bootstrap FET is suitable for most PWM modulation schemes, including trapezoidal control, and can be used either in parallel with the external bootstrap network (diode and resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations in the following situations:

- when the motor runs at a very low current (so that the negative phase voltage decay can be longer than 20us) and complementary PWM is not used;
- at very high PWM duty cycle, corresponding to very short LIN pulses, due to the bootstrap FET equivalent resistance R_{BS}.

The bootstrap FET is conditioned as follows:

- bootstrap turns-off (immediately) or stays off when either:
  - /SD goes/stays low;
  - V_B goes/ stays high (> 1.1*V_{CC});
  - IN goes/stays high (after the deadtime interval has elapsed);
- bootstrap turns-on when:
  - /SD is high AND IN goes/stays low AND V_B is low (<1.1*V_{CC});
  - /SD is high AND IN goes high, during the deadtime interval after the transition of LO from high to low, AND V_B is low (<1.1*V_{CC}).

In Figure 13 the BootFET timing diagram details are represented.

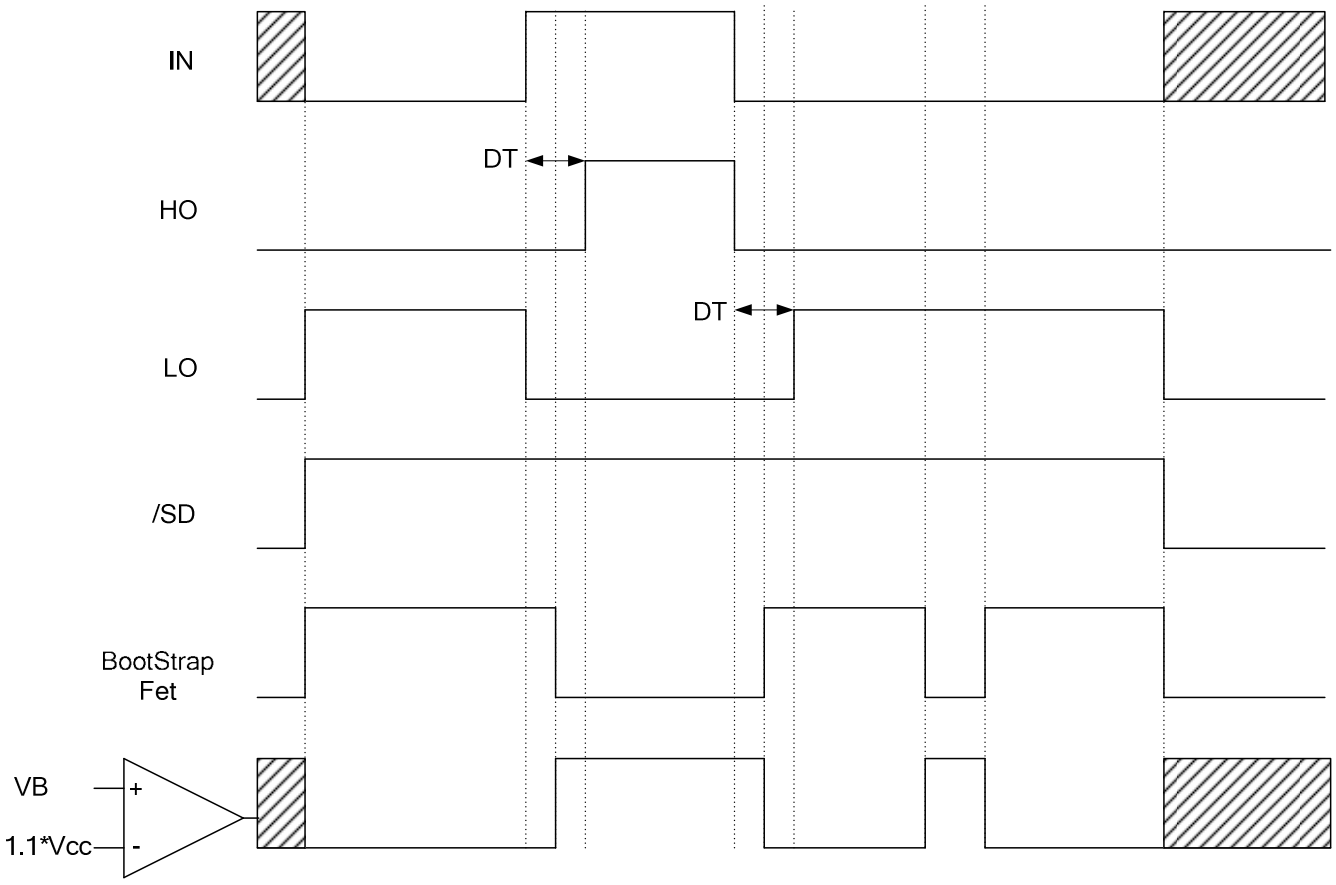


Figure 13: BootFET timing diagram

Bootstrap Power Supply Design

For information related to the design of the bootstrap power supply while using the integrated bootstrap functionality of the IRS26094D, please refer to Application Note 1123 (AN-1123) entitled "Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality." This application note is available at www.irf.com.

For information related to the design of a standard bootstrap power supply (i.e., using an external discrete diode) please refer to Design Tip 04-4 (DT04-4) entitled "Using Monolithic High Voltage Gate Drivers." This design tip is available at www.irf.com.

Tolerant to Negative VS Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power devices switch on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 14; where we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 15 and 16) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

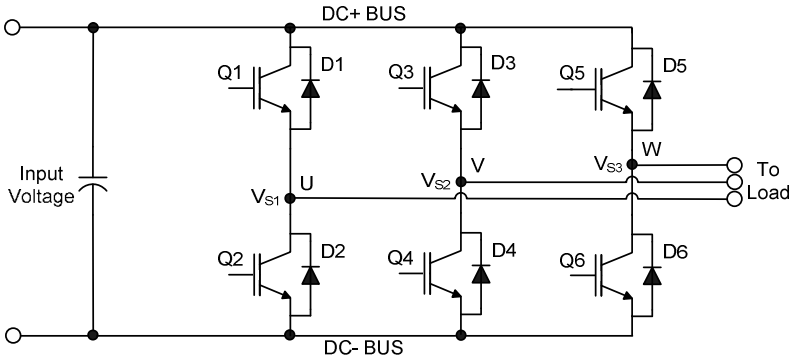


Figure 14: Three phase inverter

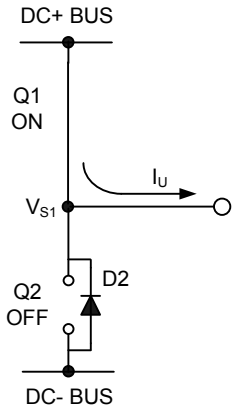


Figure 15: Q1 conducting

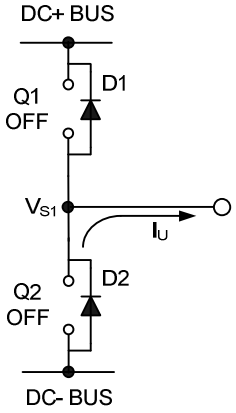


Figure 16: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 17 and 18), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

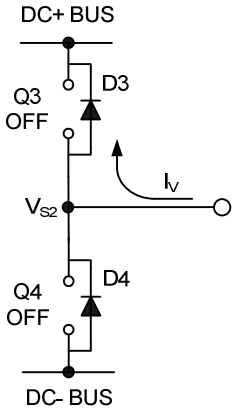


Figure 17: D3 conducting

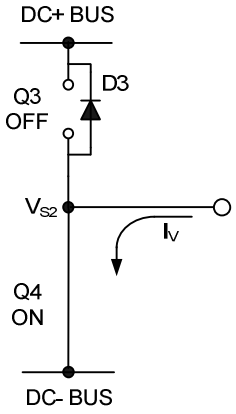


Figure 18: Q4 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient".

The circuit shown in Figure 19 depicts one leg of the three phase inverter; Figures 20 and 21 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

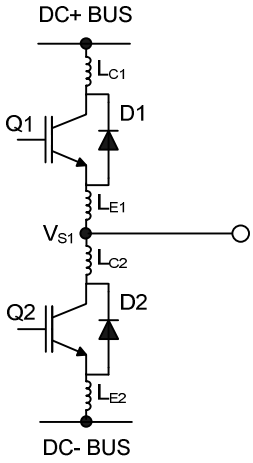


Figure 19: Parasitic elements

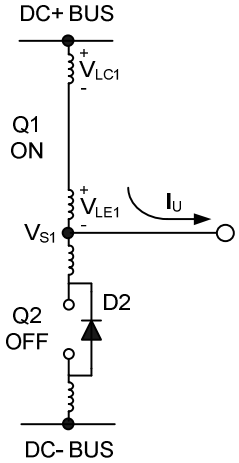


Figure 20: VS positive

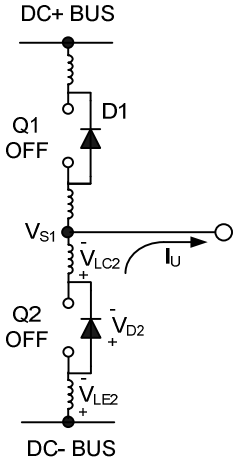


Figure 21: VS negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the IRS26094D's robustness can be seen in Figure 22, where there is represented the IRS26094D Safe Operating Area at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; vice versa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.

At V_{BS}=15V in case of -V_S transients greater than -16.5 V for a period of time greater than 50 ns; the HVIC will hold by design the high-side outputs in the off state for 4.5 µs.

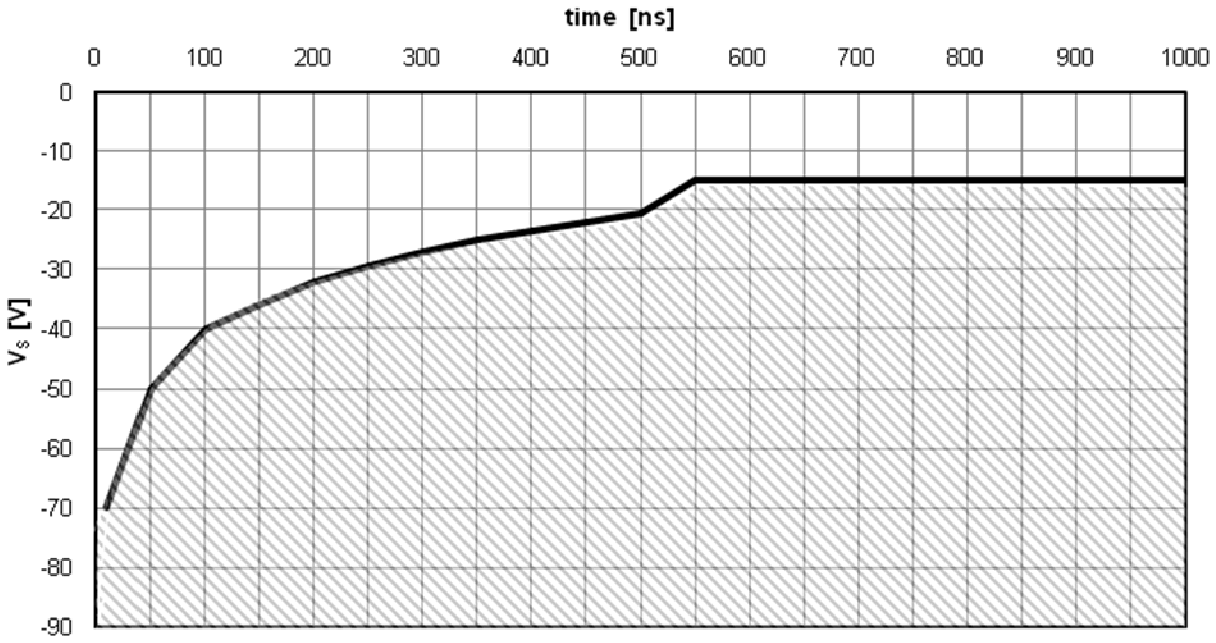


Figure 22: Negative VS transient SOA @ VBS=15V

Even though the IRS26094D has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 23). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

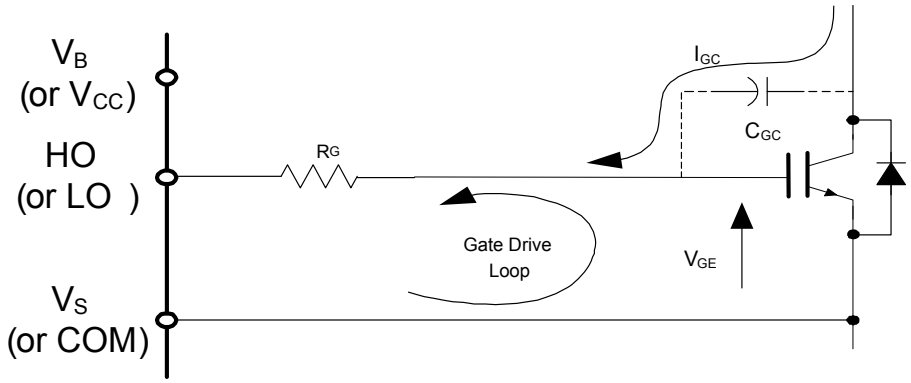


Figure 23: Antenna loops

Supply Capacitor: It is recommended to place a bypass capacitor between the V_{CC} and V_{SS} pins. This connection is shown in Figure 24. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

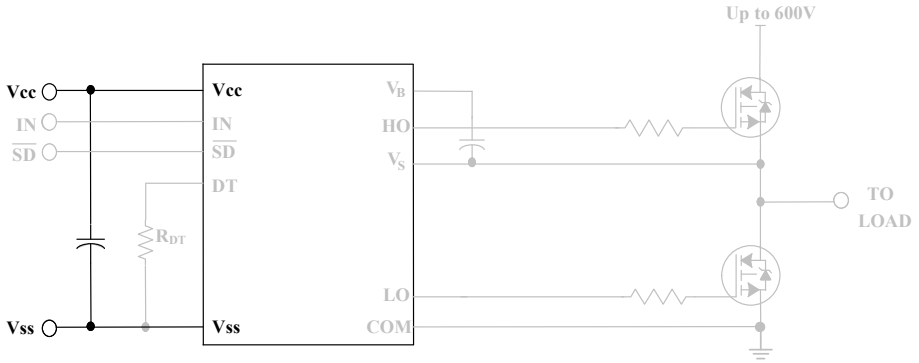


Figure 24: Supply capacitor

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side source to low-side collector distance, and 2) minimize

the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 25), and in some cases using a clamping diode between COM and V_S (see Figure 26). See DT04-4 at www.irf.com for more detailed information.

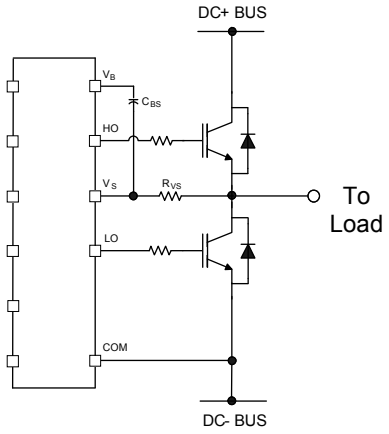


Figure 25: VS resistor

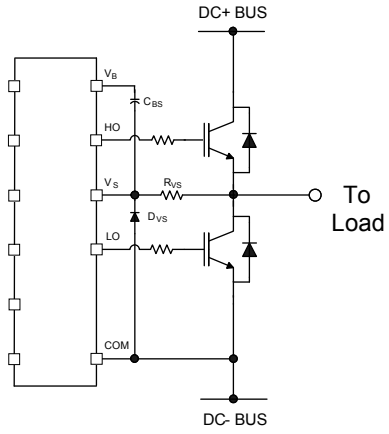


Figure 26: VS clamping diode

Integrated Bootstrap FET limitation

The integrated Bootstrap FET functionality has an operational limitation under the following bias conditions applied to the HVIC:

- **VCC pin voltage = 0V AND**
- **VS or VB pin voltage > 0**

In the absence of a VCC bias, the integrated bootstrap FET voltage blocking capability is compromised and a current conduction path is created between VCC & VB pins, as illustrated in Fig.27 below, resulting in power loss and possible damage to the HVIC.

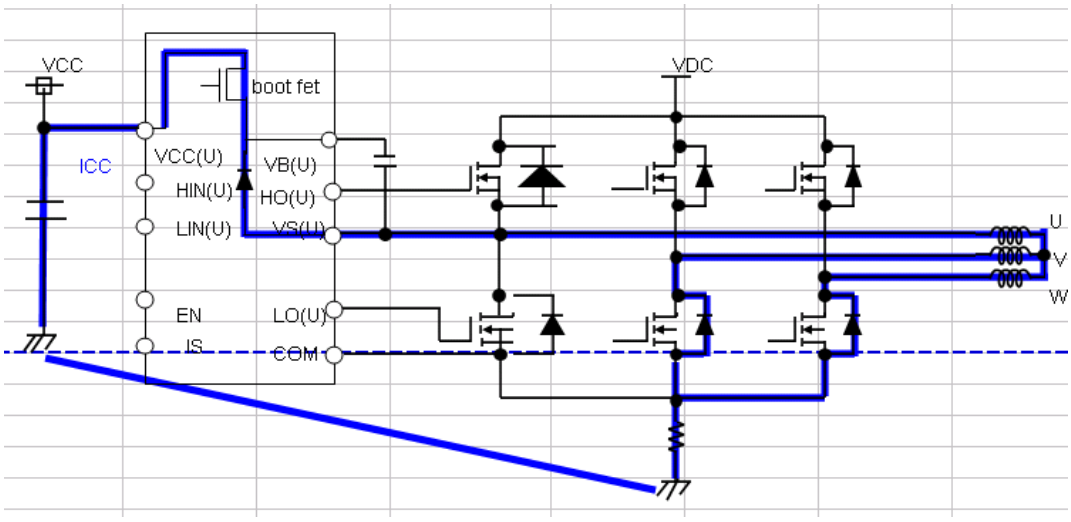


Figure 27: Current conduction path between VCC and VB pin

Relevant Application Situations:

The above mentioned bias condition may be encountered under the following situations:

- In a motor control application, a permanent magnet motor naturally rotating while VCC power is OFF. In this condition, Back EMF is generated at a motor terminal which causes high voltage bias on VS nodes resulting unwanted current flow to VCC.

- Potential situations in other applications where VS/VB node voltage potential increases before the VCC voltage is available (for example due to sequencing delays in SMPS supplying VCC bias)

Application Workaround:

Insertion of a standard p-n junction diode between VCC pin of IC and positive terminal of VCC capacitors (as illustrated in Fig.28) prevents current conduction "out-of" VCC pin of gate driver IC. It is important not to connect the VCC capacitor directly to pin of IC. Diode selection is based on 25V rating or above & current capability aligned to ICC consumption of IC - 100mA should cover most application situations. As an example, Part number # LL4154 from Diodes Inc (25V/150mA standard diode) can be used.

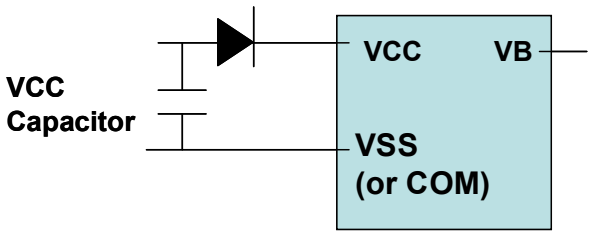


Figure 28: Diode insertion between VCC pin and VCC capacitor

Note that the forward voltage drop on the diode (V_F) must be taken into account when biasing the VCC pin of the IC to meet UVLO requirements. *VCC pin Bias = VCC Supply Voltage – V_F of Diode*.

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Parameter Temperature Trends

Figures 29-52 provide information on the experimental performance of the IRS26094D HVIC. The line plotted in each figure is generated from actual experimental data. A small number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood temperature trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

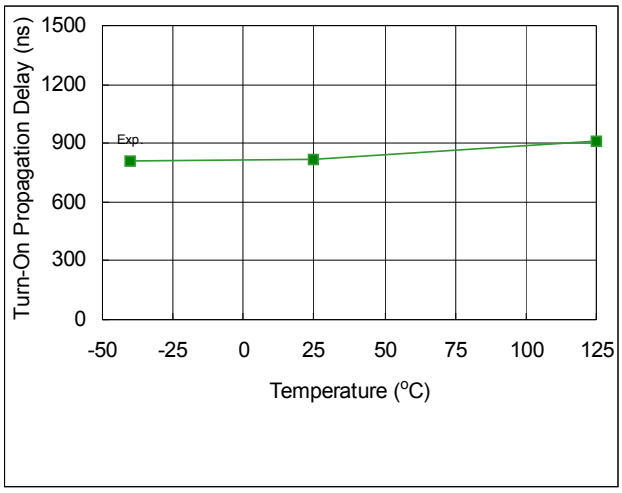


Fig. 29. Turn-on propagation delay vs. temperature

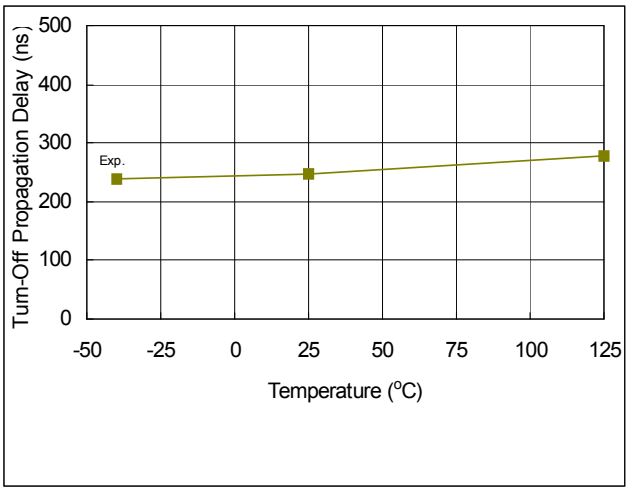


Fig. 30. Turn-off propagation delay vs. temperature

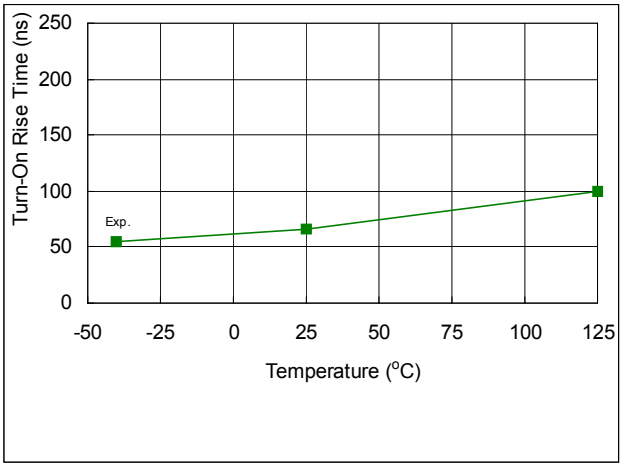


Fig. 31. Turn-on rise time vs. temperature

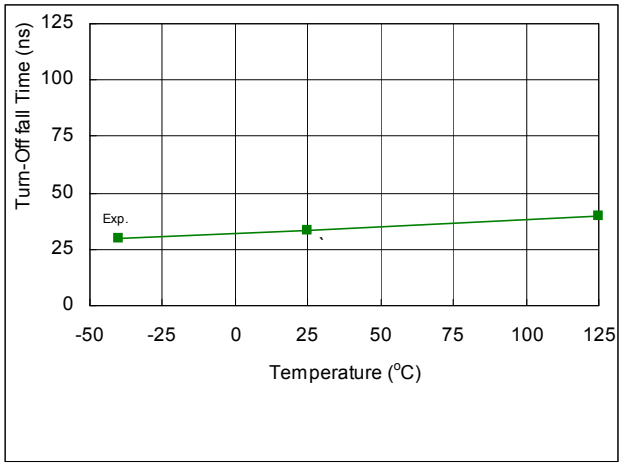


Fig.32. Turn-off fall time vs. temperature

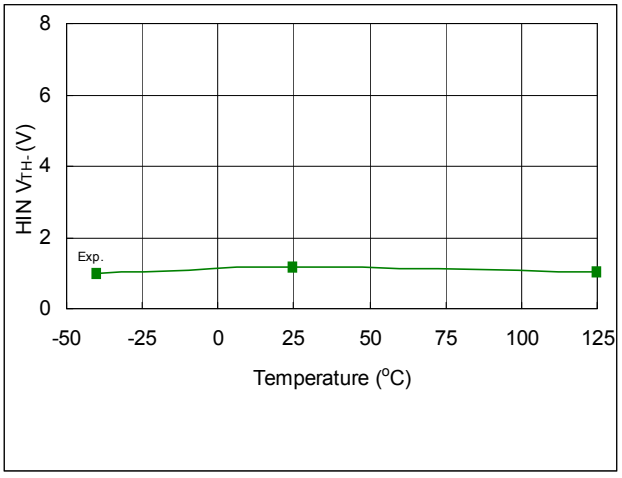


Fig. 33. Input negative going threshold vs. temperature

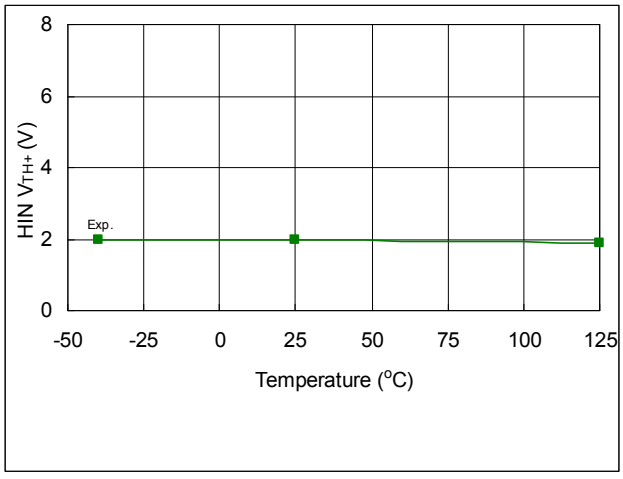


Fig. 34. Input positive going threshold vs. temperature

3

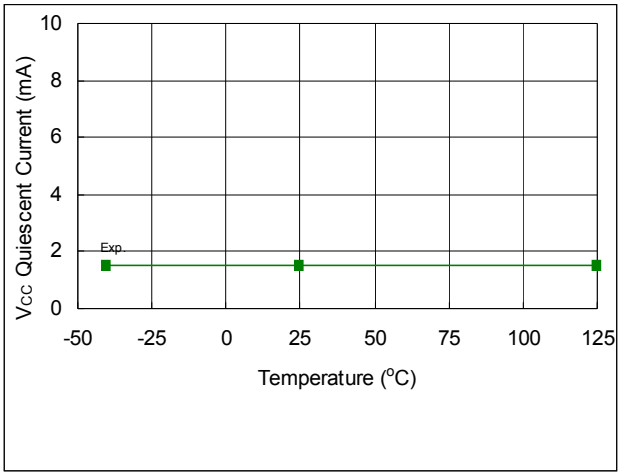


Fig. 33. Quiescent VCC supply current vs. temperature

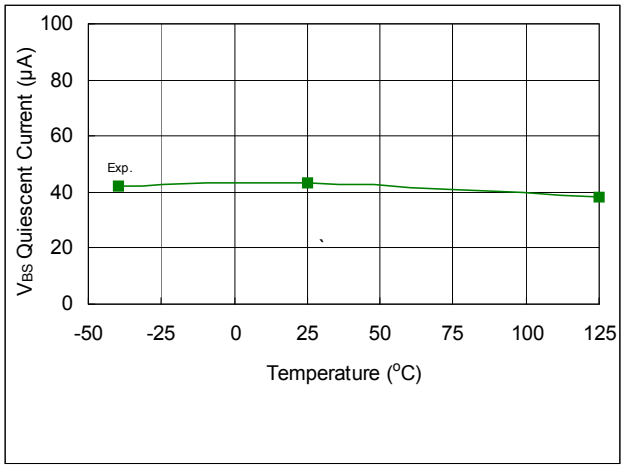


Fig. 34. Quiescent VBS supply current vs. temperature

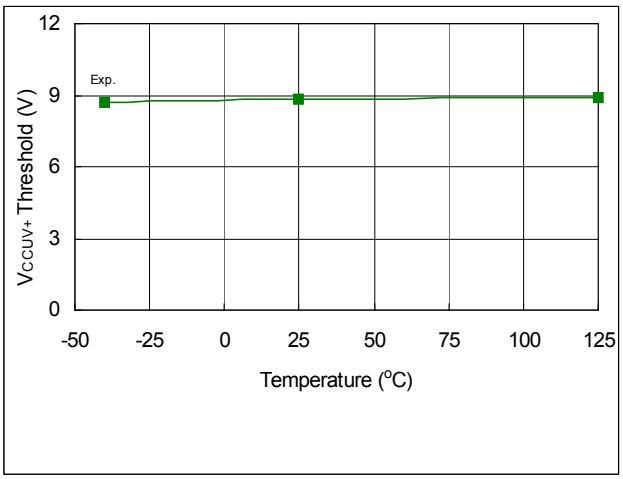


Fig. 35. VCC supply under-voltage positive going threshold vs. temperature

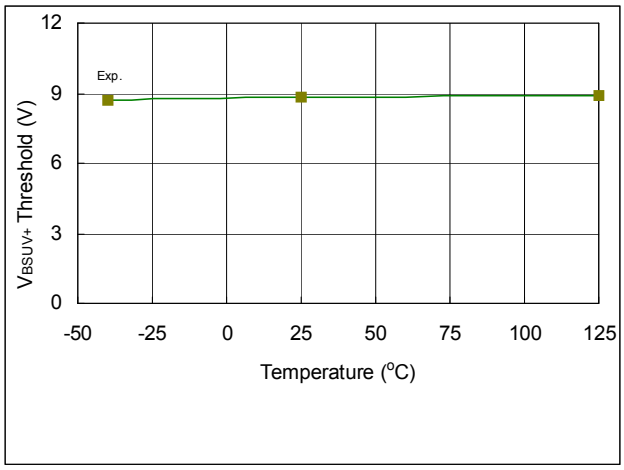


Fig. 36. VBS supply under-voltage positive going threshold vs. temperature

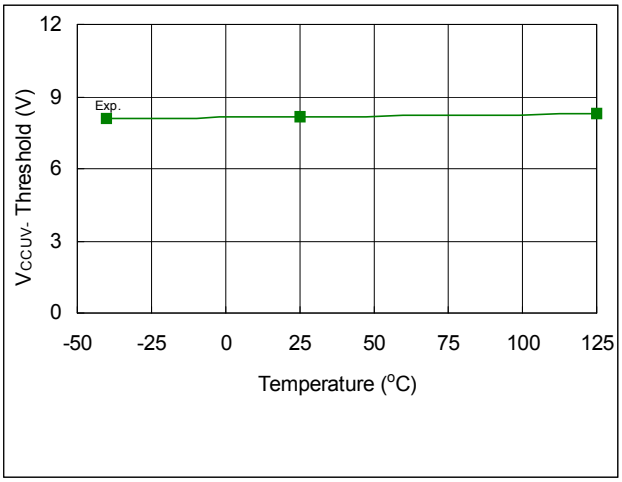


Fig. 37. VCC supply under-voltage negative going threshold vs. temperature

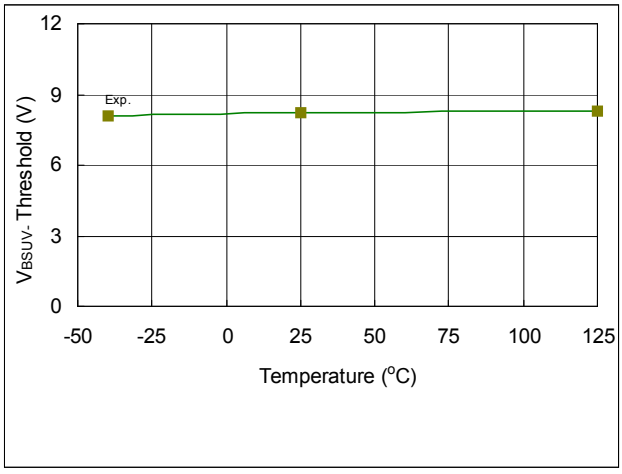


Fig. 38. VBS supply under-voltage negative going threshold vs. temperature

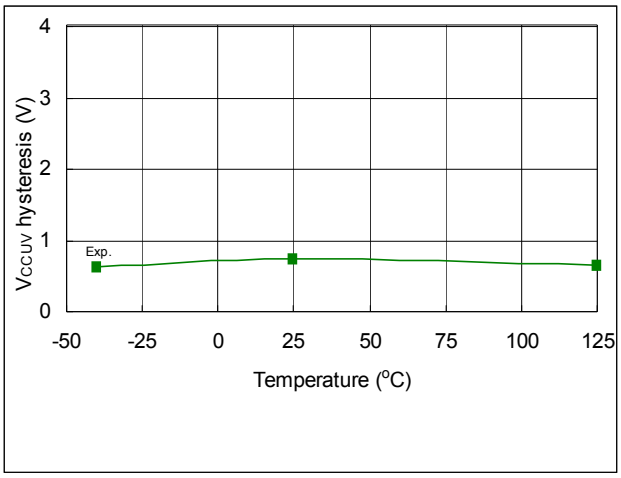


Fig. 39. VCC supply under-voltage hysteresis vs. temperature

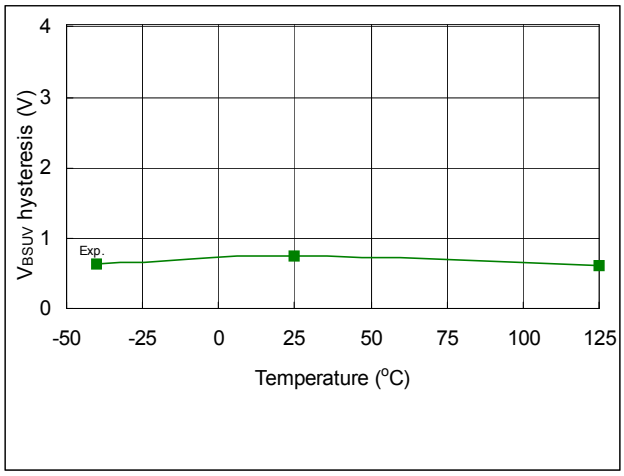


Fig. 40. VBS supply under-voltage hysteresis vs. temperature

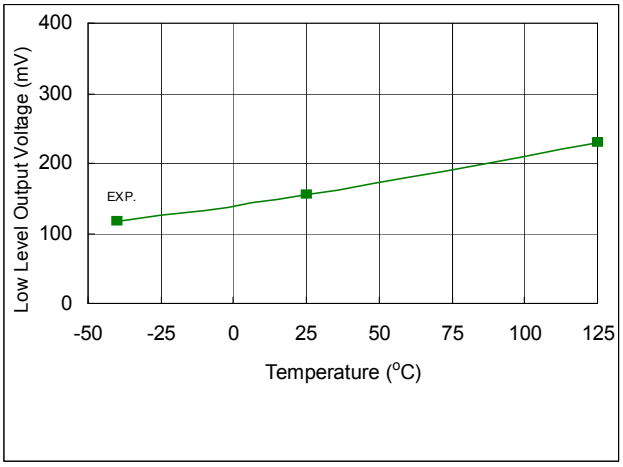


Fig. 41. Low level output voltage vs. temperature

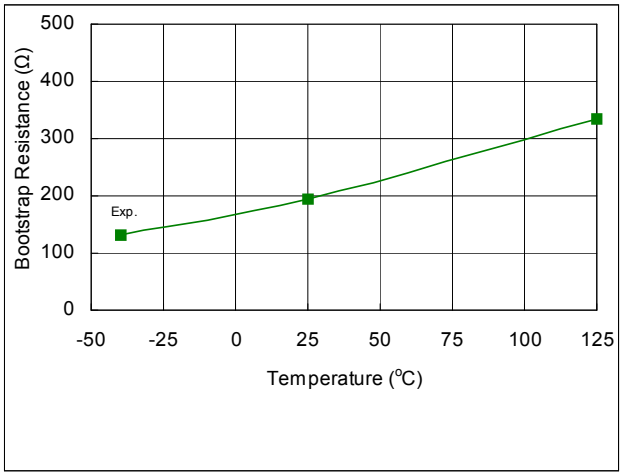


Fig. 42. Bootstrap resistance vs. temperature

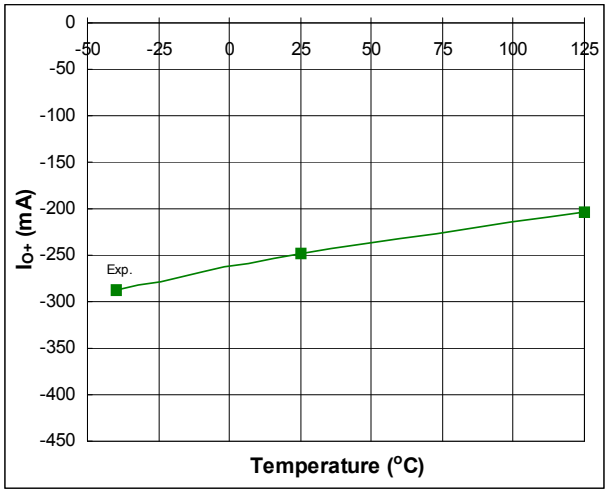


Fig. 43. Output high short circuit pulsed current vs. temperature

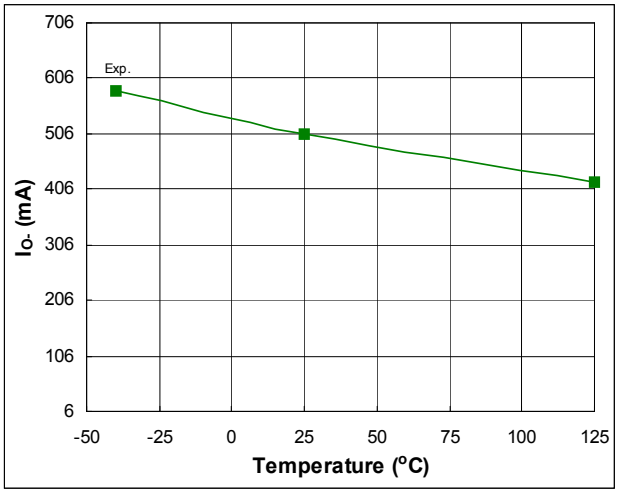


Fig. 44. Output low short circuit pulsed current vs. temperature

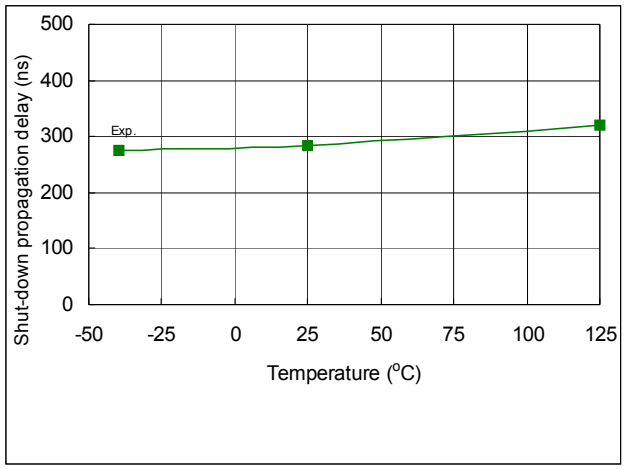


Fig. 45. Shutdown propagation delay vs. temperature

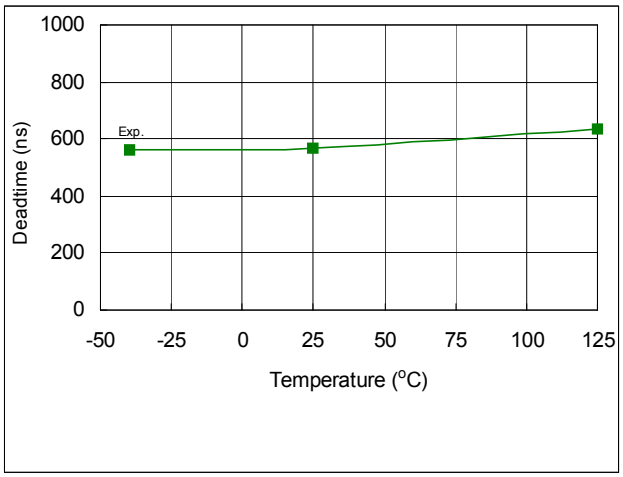


Fig. 46. Deadtime vs. temperature

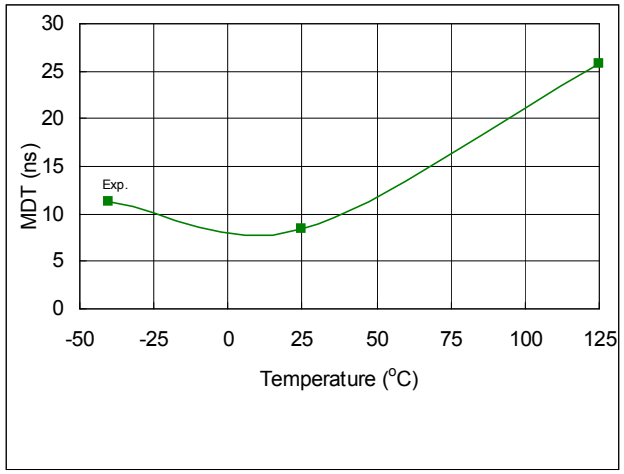


Fig. 47. Deadtime matching vs. temperature

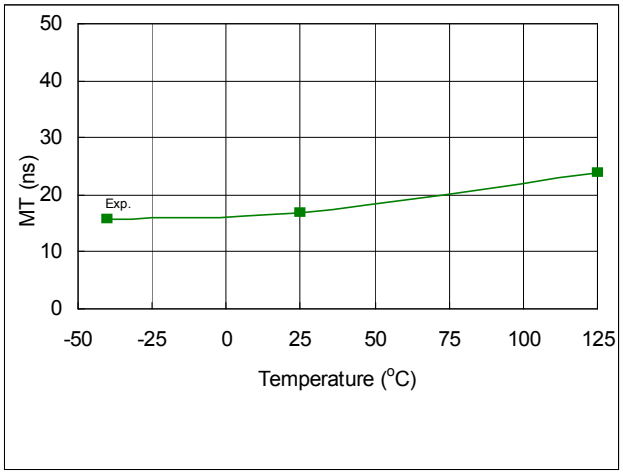


Fig. 48. Propagation delay matching time

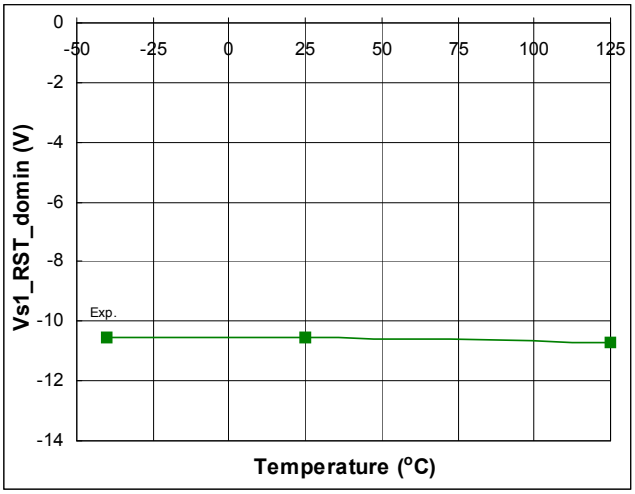
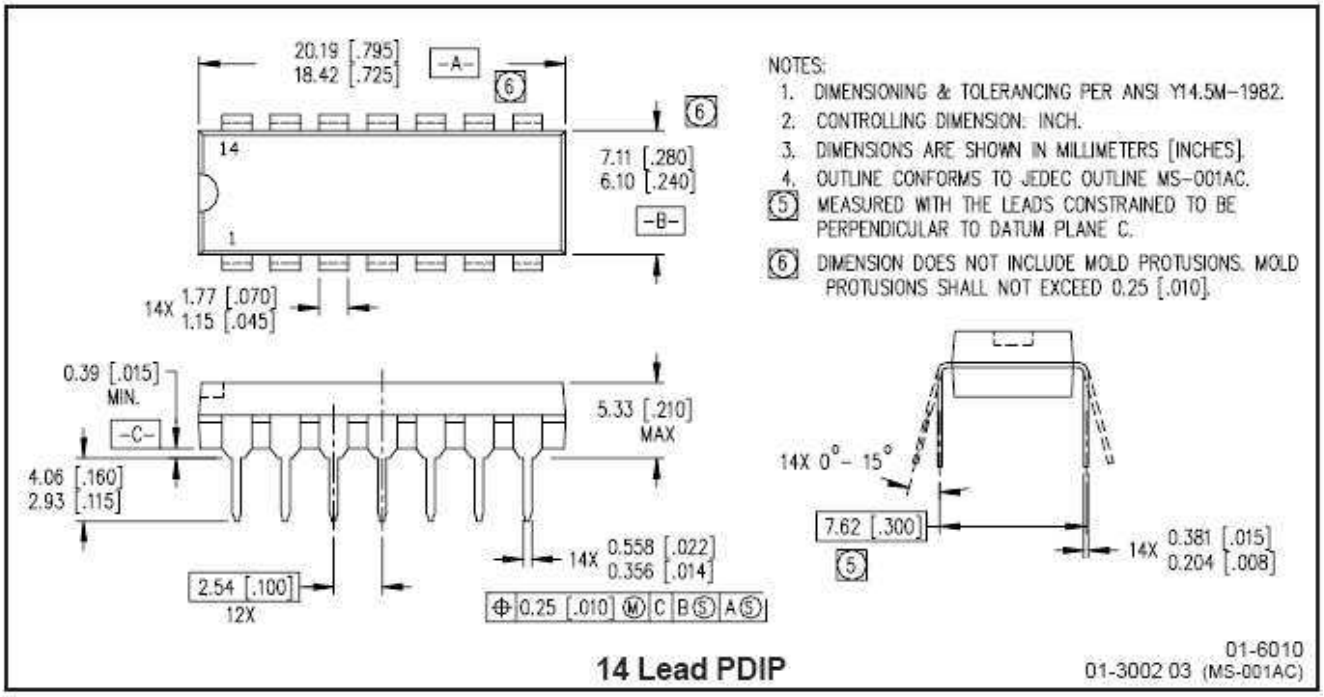
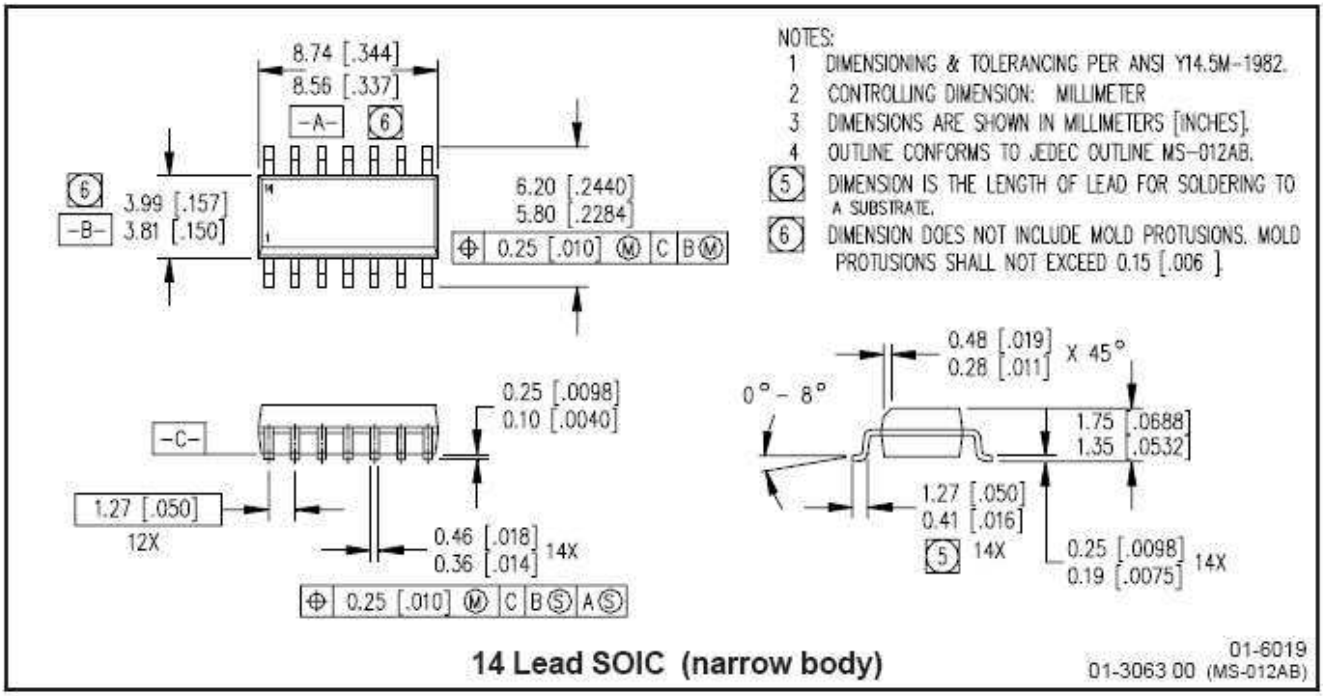


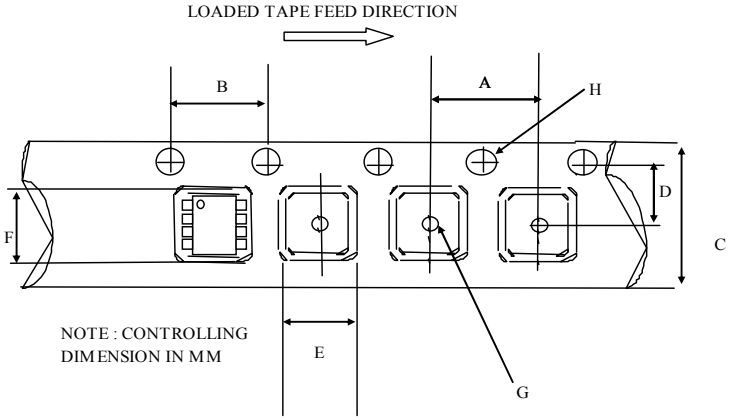
Fig. 49. Max –VS vs. temperature

Package Details



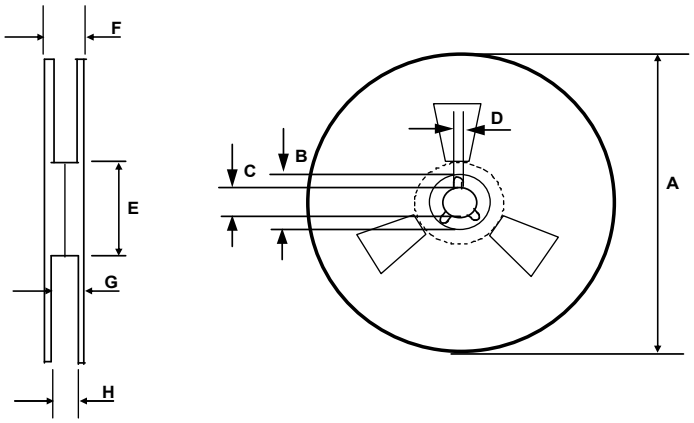


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

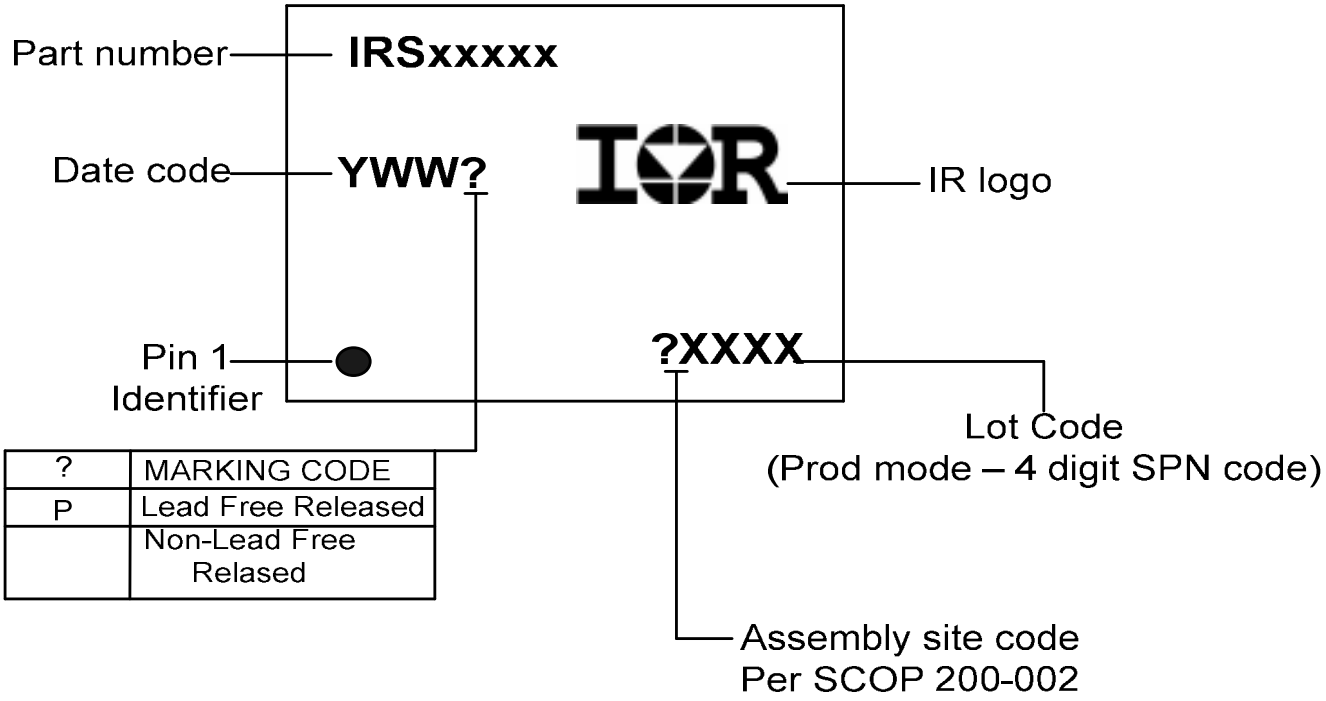
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

Ordering Information

Base Part Number	Package Type	Standard Pack Form	Complete Part Number
IRS26094D IRS26094D	SOIC 14	Tube/Bulk	IRS26094D SPBF
		Tape and Reel	IRS26094D STRPBF
	PDIP 14	Tube/Bulk	TBD
		Tape and Reel	TBD

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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