TURBOT

Rev : X205

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REVISION HISTORY:

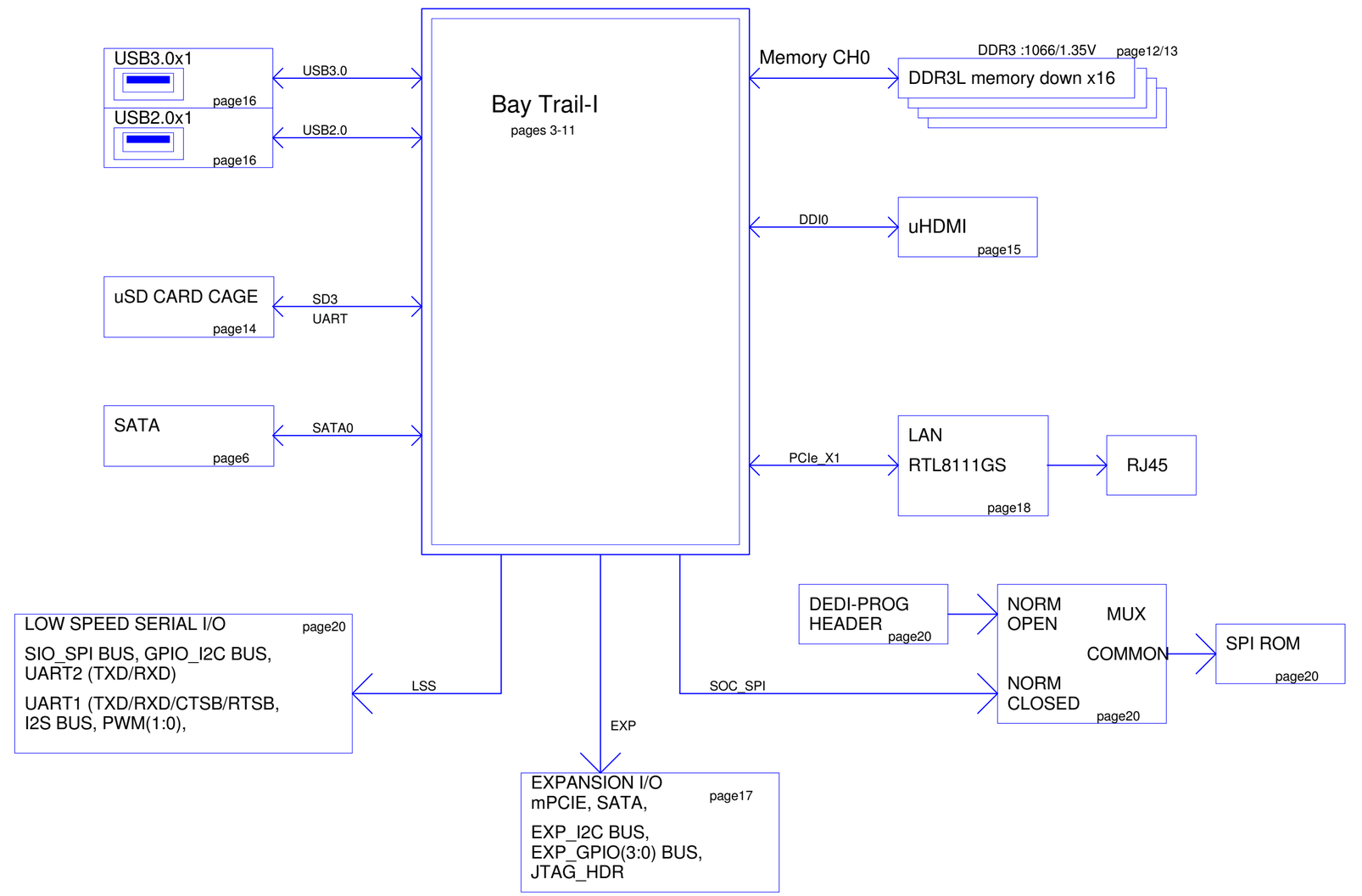
Rev	Date	Notes
X100	2015/05/22	INITIAL RELEASE OF TURBOT DESIGN
X200	2015/07/30	FIXES BASED ON ALPHA QUALIFICATION
X201	2015/08/17	SWAP IN NEW LOW-Vth FET FOR Q16, DNI U33 (SPD EEPROM)
X202	2015/08/27	STUFF R354, REPLACE U32 (USB POWER SWITCH) WITH PART FROM X100 RELEASE
X203	2015/09/23	ADD LABELS TO BOM FOR PILOT PRODUCTION RELEASE
X204	2015/10/13	BOM FIX D5, D6, D10 TO PART WITH CORRECT FOOTPRINT
X205	2015/08/27	NO STUFF R53, R54, R55, R56 TO MATCH VALIDATED PROTOTYPES

For all design files, including bill of materials and gerber files, please visit www.minnowboard.org

Prepared For:

BY:
ADI ENGINEERING
1758 WORTH PARK
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM

TITLE		
	TURBOT	
SIZE: C	DWG NO: ADI -80204-0125-G00	REV: X205
DATE: 11/16/2015	SHEET 1 of 29	



BLOCK DIAGRAM

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
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FOR HDMI VIDEO/AUDIO,

REVERSE BIT CONNECTIONS
FROM (0:2) TO (2:0), BIT3

IS THE CLOCK SIGNAL.
STRAIGHT BIT ORDER is

for EDP ONLY
HDMI

CPU1

HDMI_TX2_DP AV3 DDI0_TXP_0
HDMI_TX2_DN AV2 DDI0_TXN_0
HDMI_TX1_DP AT2 DDI0_TXP_1
HDMI_TX1_DN AT3 DDI0_TXN_1
HDMI_TX0_DP AR3 DDI0_TXP_2
HDMI_TX0_DN AR1 DDI0_TXN_2
HDMI_CLK_DP AP3 DDI0_TXP_3
HDMI_CLK_DN AP2 DDI0_TXN_3

(+V1P0S) AL3 DDI0_AUXP
(+V1P0S) AL1 DDI0_AUXN

HDMI_HPD_B (+V1P8S) D27 DDI0_HPD

HDMI_DDCDAT (+V1P8S) C26 DDI0_DDCDATA
HDMI_DDCCLK (+V1P8S) C28 DDI0_DDCCLK

(+V1P8S) B28 DDI0_VDDEN
(+V1P8S) C27 DDI0_BKLTEN
(+V1P8S) B26 DDI0_BKLTCTL

R217 1 2 402R DDI_RCOMP_P (+V1P0S) AK13 DDI0_RCOMP
DDI_RCOMP_N (+V1P0S) AK12 DDI0_RCOMP_P
AM14 RESERVED_AM14
AM13 RESERVED_AM13

GND R42 1 2 0R0 AM3 RESERVED_VSS0
GND R41 1 2 0R0 AM2 RESERVED_VSS1

Bay Trail-I Different

+V1P8S
GND C375 0.1uF
HDMI_HPD 2 U39 NC 4 SN74LVC1G14DCKR SC70-5 5 1 3
GND

T2 RESERVED_T2
T3 RESERVED_T3
AB3 RESERVED_AB3
AB2 RESERVED_AB2
Y3 RESERVED_Y3
Y2 RESERVED_Y2
W3 RESERVED_W3
W1 RESERVED_W1
V2 RESERVED_V2
V3 RESERVED_V3
R3 RESERVED_R3
R1 RESERVED_R1
AD6 RESERVED_AD6
AD4 RESERVED_AD4
AB9 RESERVED_AB9
AB7 RESERVED_AB7
Y4 RESERVED_Y4
Y6 RESERVED_Y6
V4 RESERVED_V4
V6 RESERVED_V6
A29 RESERVED_A29
C29 RESERVED_C29
AB14 RESERVED_AB14
B30 GPIO_S0_NC12
C30 RESERVED_C30

GND R102 10K0 GPIO_NC13
TP15

BAYTRAIL_I
DISPLAY SECTION

Bay Trail-M Remove eDP Port

DDI1_TXP_0 AG3 (+V1P0S)
DDI1_TXN_0 AG1 (+V1P0S)
DDI1_TXP_1 AF3 (+V1P0S)
DDI1_TXN_1 AF2 (+V1P0S)
DDI1_TXP_2 AD3 (+V1P0S)
DDI1_TXN_2 AD2 (+V1P0S)
DDI1_TXP_3 AC3 (+V1P0S)
DDI1_TXN_3 AC1 (+V1P0S)

DDI1_AUXP AK3 (+V1P0S)
DDI1_AUXN AK2 (+V1P0S)

DDI1_HPD K30 (+V1P8S) GND

DDI1_DDCDATA P30 (+V1P8S) DDI1_DDCDAT R257 1 2 2K20 GND
DDI1_DDCCLK G30 (+V1P8S) GND

DDI1_VDDEN N30 (+V1P8S)
DDI1_BKLTEN J30 (+V1P8S)
DDI1_BKLTCTL M30 (+V1P8S)

RESERVED_AH14 AH14
RESERVED_AH13 AH13
RESERVED_AF14 AF14
RESERVED_AF13 AF13
RESERVED_VSS2 AH3 R46 1 2 0R0 GND
RESERVED_VSS3 AH2 R43 1 2 0R0 GND

VGA_RED BA3 (VVGA_GPIO)
VGA_BLUE AY2 (VVGA_GPIO)
VGA_GREEN BA1 (VVGA_GPIO)
VGA_IREF AW1 R40 357R GND
VGA_IRTN AY3 GND

BD2 (VVGA_GPIO)
VGA_HSYNC BF2 (VVGA_GPIO) CRT_CLK R39 1 2 150R GND
VGA_VSYNC BC1 (VVGA_GPIO)
VGA_DDCCLK BC2 (VVGA_GPIO) CRT_DAT R38 1 2 150R
VGA_DDCDATA

RESERVED_T7 T7 (V1P24S)
RESERVED_T9 T9 (V1P24S)
RESERVED_AB13 AB13 (V1P24S)
RESERVED_AB12 AB12 (V1P24S)
RESERVED_Y12 Y12 (V1P24S)
RESERVED_Y13 Y13 (V1P24S)
RESERVED_V10 V10 (V1P24S)
RESERVED_V9 V9 (V1P24S)
RESERVED_T12 T12 (V1P24S)
RESERVED_T10 T10 (V1P24S)
RESERVED_V14 V14 (V1P24S)
RESERVED_V13 V13 (V1P24S)
RESERVED_T14 T14 (V1P24S)
RESERVED_T13 T13 (V1P24S)
RESERVED_T6 T6 (V1P24S)
RESERVED_T4 T4 (V1P24S)
RESERVED_P14 P14 (V1P24S) MCSI_RCOMP R213 1 2 150R GND

RESERVED_K34 K34 (V1P24S)
RESERVED_D32 D32 (V1P24S)
RESERVED_N32 N32 (V1P24S)
RESERVED_J34 J34 (V1P24S)
RESERVED_K28 K28 (V1P24S)
RESERVED_F28 F28 (V1P24S)
RESERVED_F32 F32 (V1P24S)
RESERVED_D34 D34 (V1P24S)
RESERVED_J28 J28 (V1P24S)
RESERVED_D28 D28 (V1P24S)
RESERVED_M32 M32 (V1P24S)
RESERVED_F34 F34 (V1P24S)

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Bay Trail-I MCSI Port

CPU-DDI/VGA

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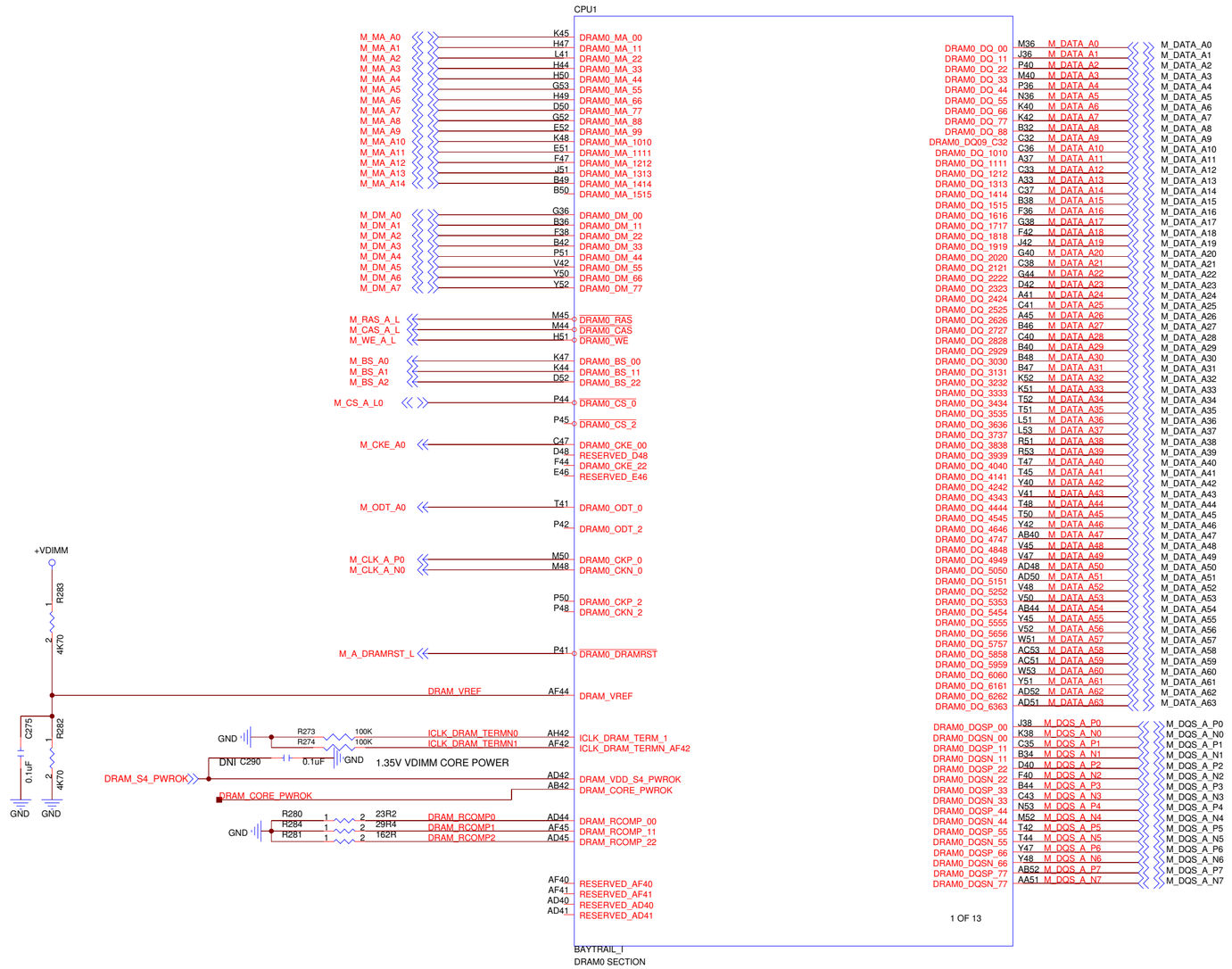
TITLE	TURBOT
SIZE C	DWG NO ADI -80204-0125-G00
REV	X205
DATE 11/16/2015	SHEET 3 of 29



CPU-DDR3-CHA

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
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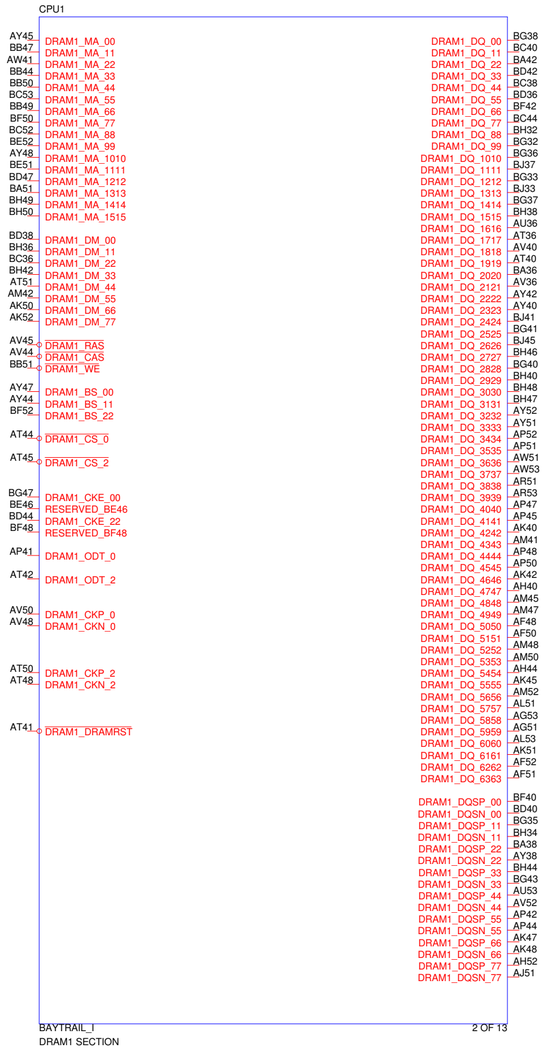

CPU-DDR3-CHB

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TITLE	TURBOT
SIZE C	DWG NO ADI -80204-0125-G00
REV	X205
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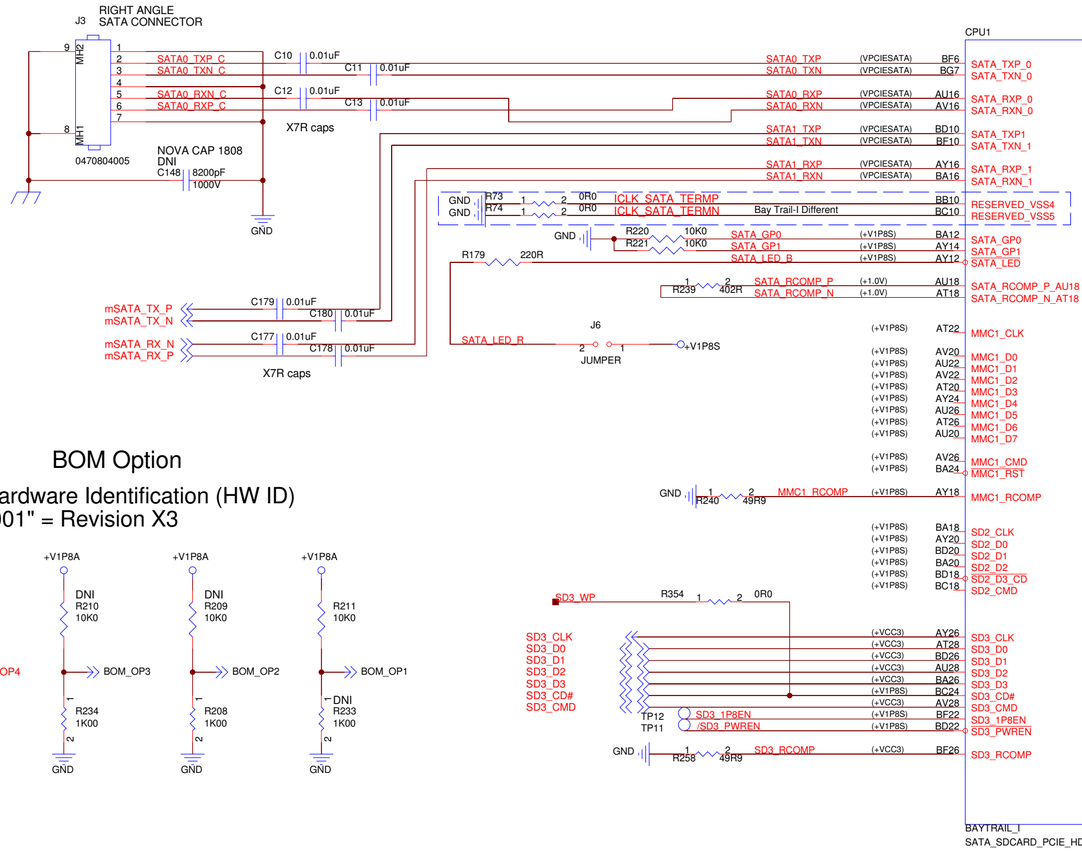

HW STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC

Top Swap(A16 Override)

H	Top address bit is unchanged
L	Top address bit is inverted

Strap Pin	Function
GPIO_S0_SC63 (LPE_I2S_FRM)	BIOS Boot Selection 0=LPC *1=SPI
GPIO_S0_SC65 (LPE_I2S_DATOUT)	Security Flash Descriptors 0=Override *1=Normal Operation

CPU-PE/HDA/SD/eMMC/Strap

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TITLE	TURBOT
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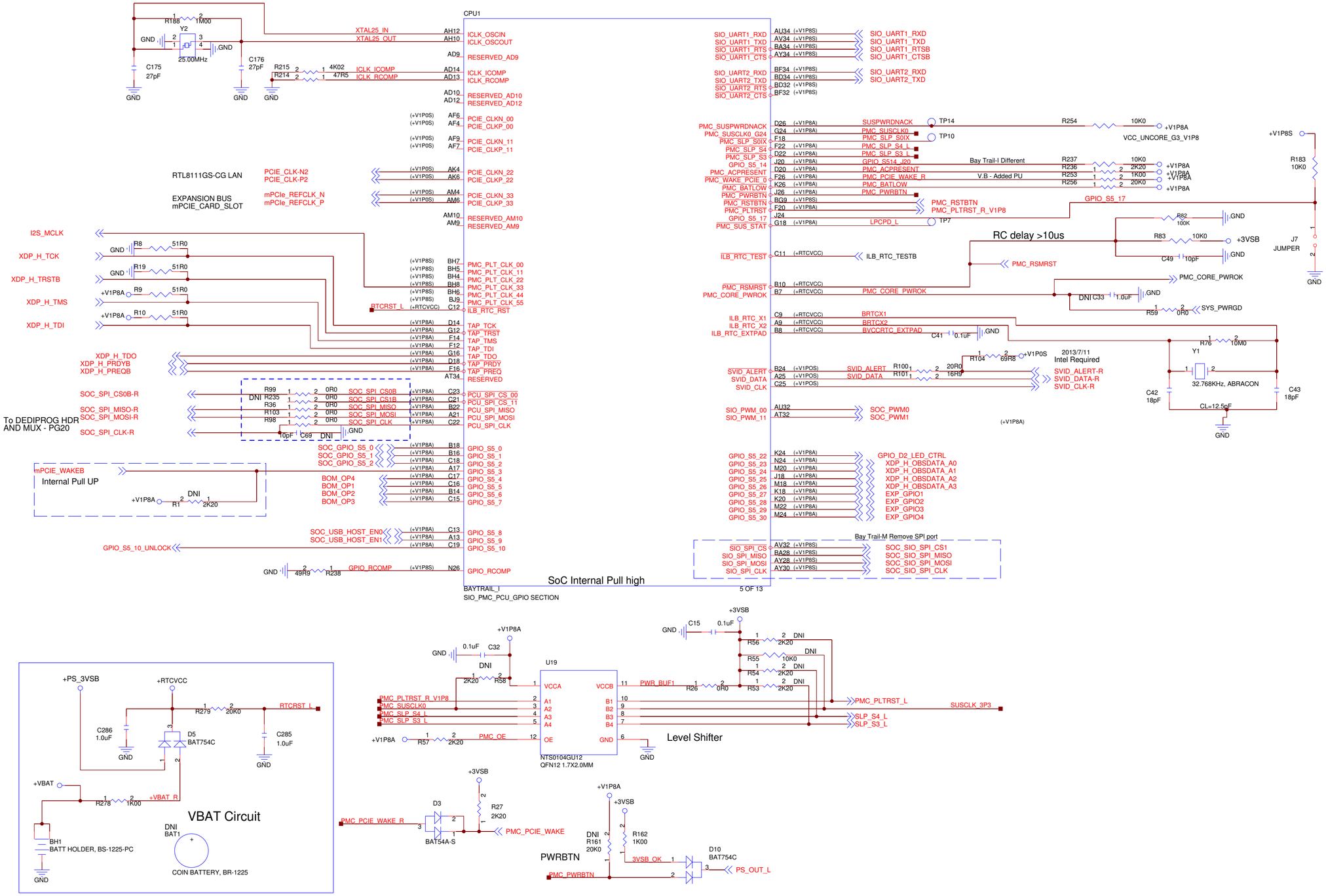

CPU-SPI/CLOCK/RTC/PMC/UART

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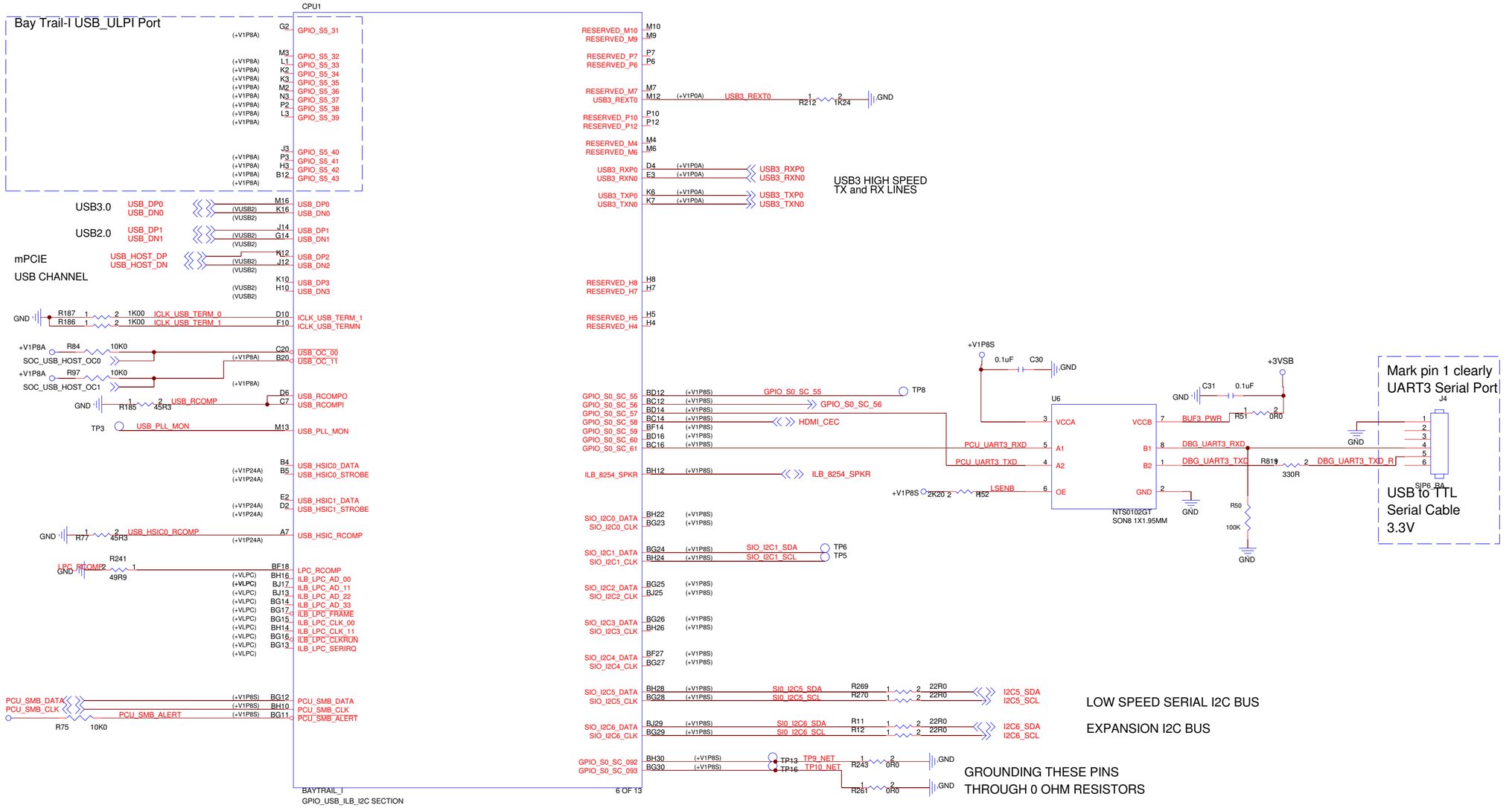
DATE: 11/16/2015	SHEET 7 of 29



CPU-USB/LPC/SMB/I2C

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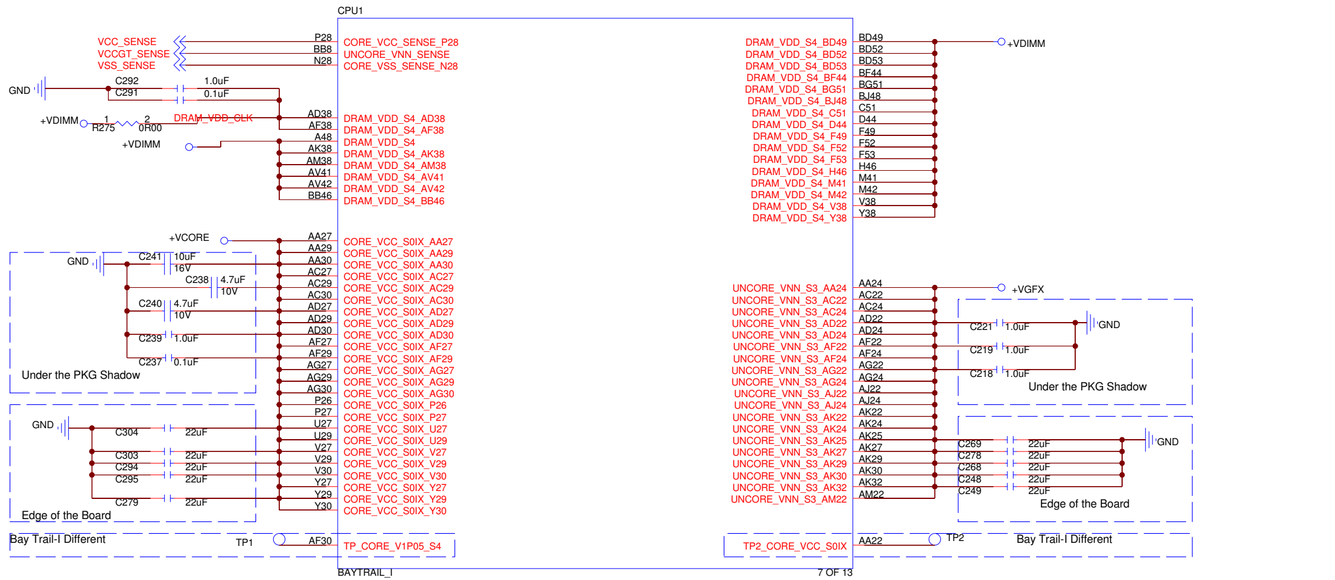

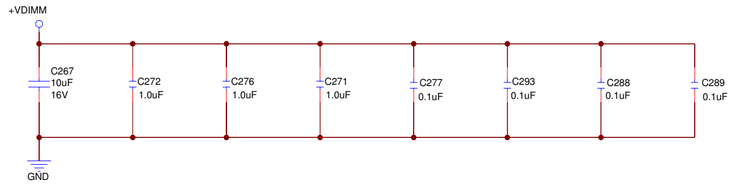

CPU-PWR1/TPM/LPC

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TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
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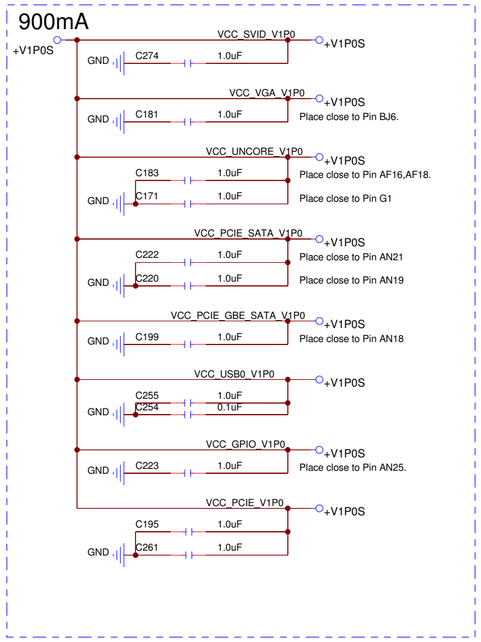

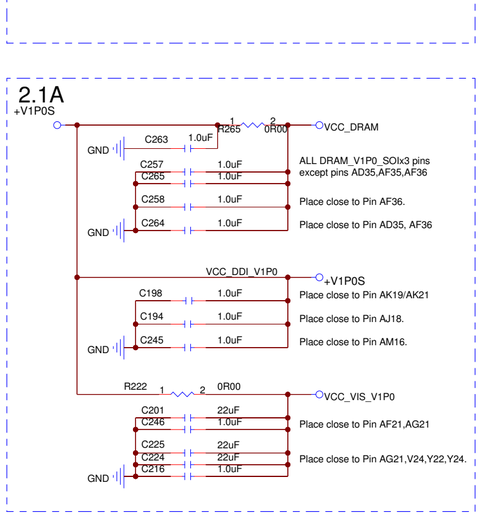

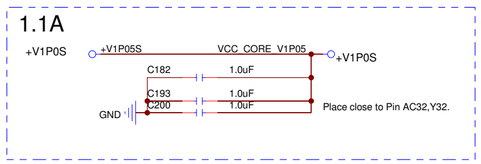

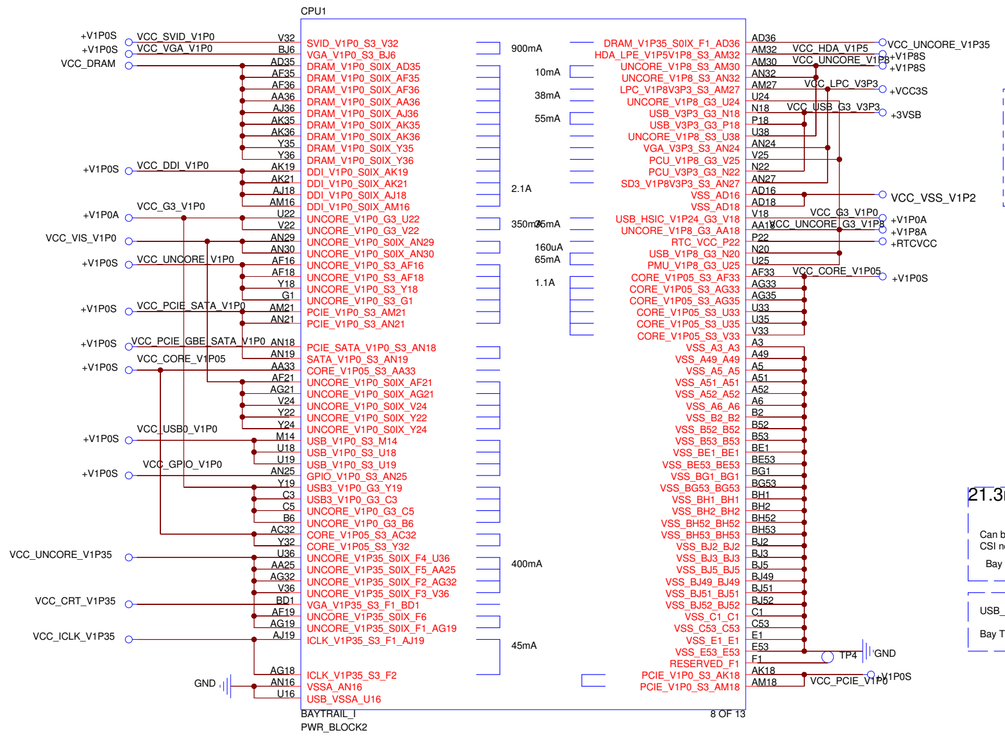

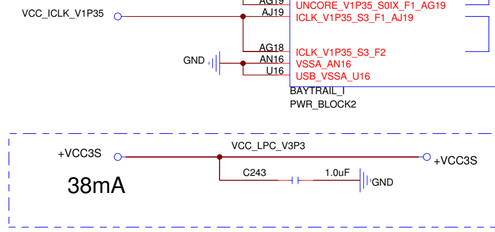

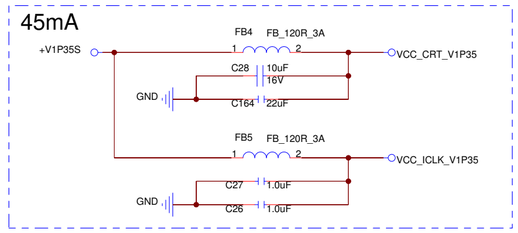

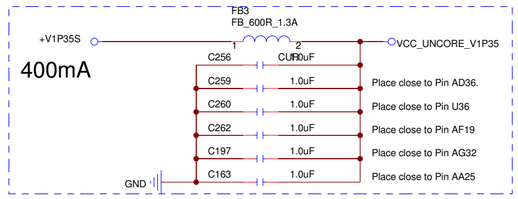

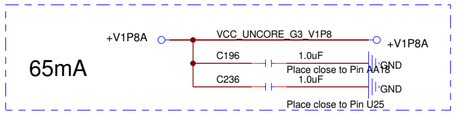

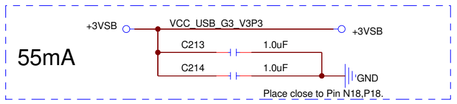

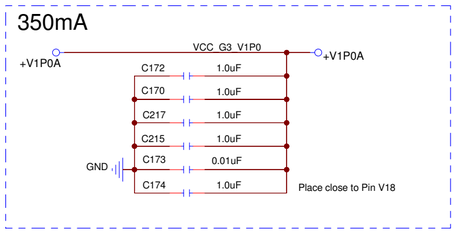

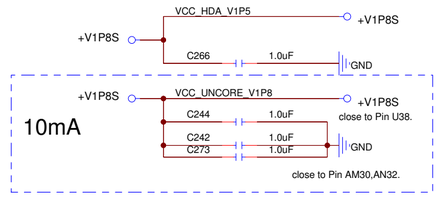

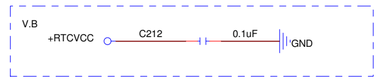

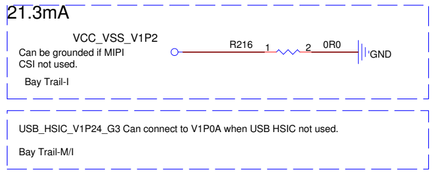

CPU-PWR2

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SIZE: C	DWG NO: ADI -80204-0125-G00
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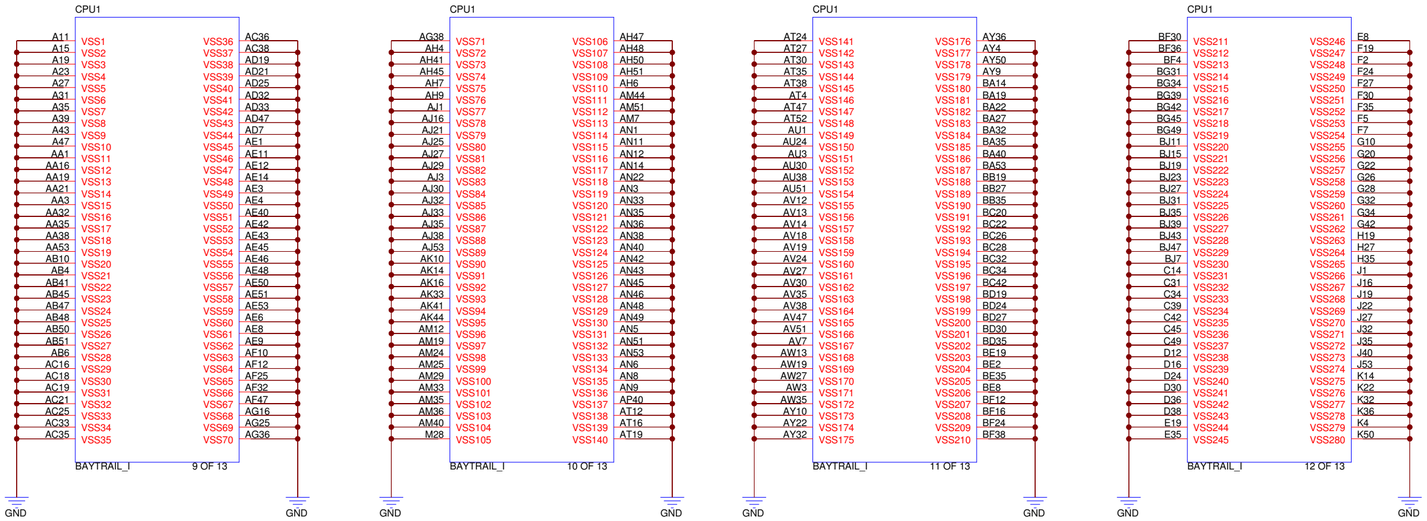

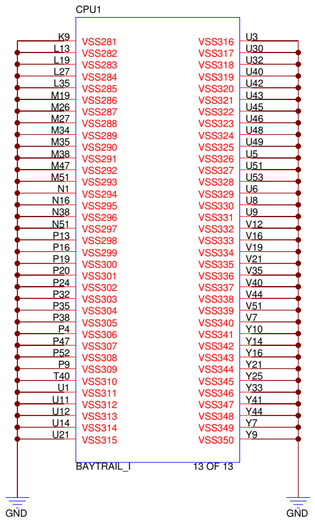

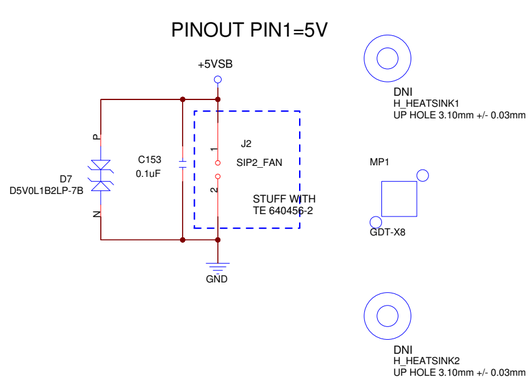

CPU-GND

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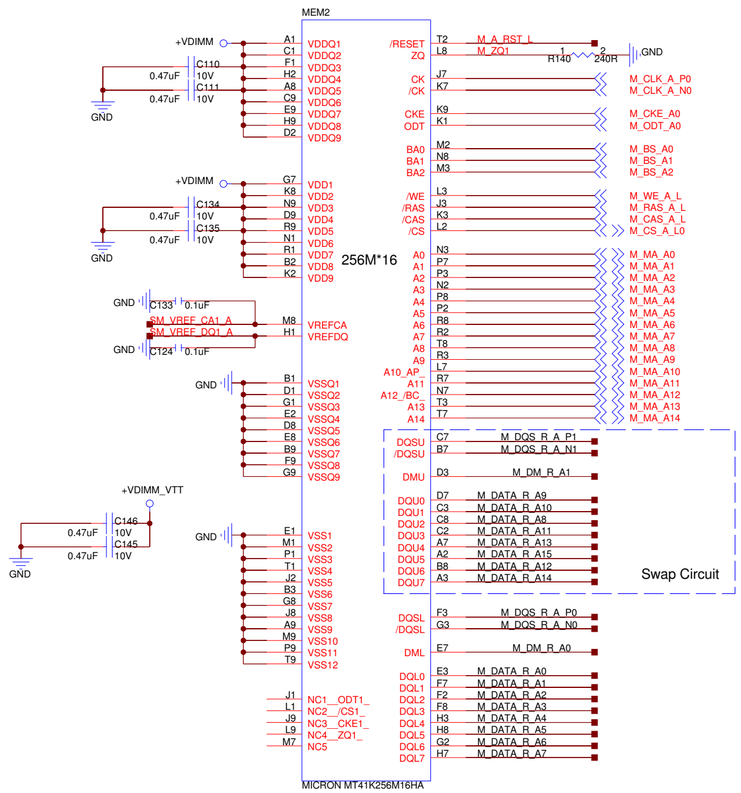

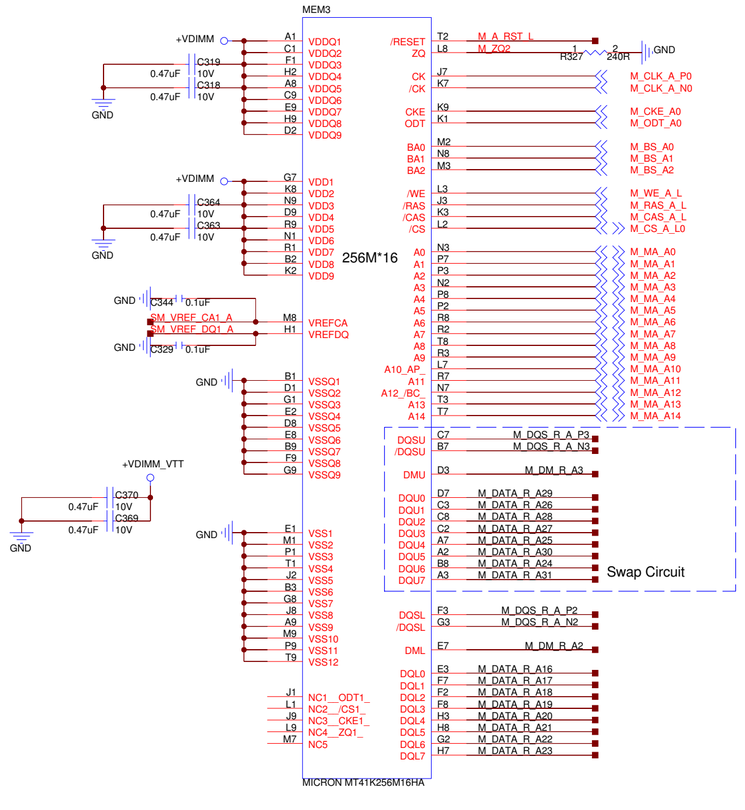

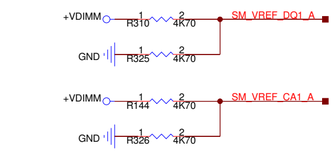

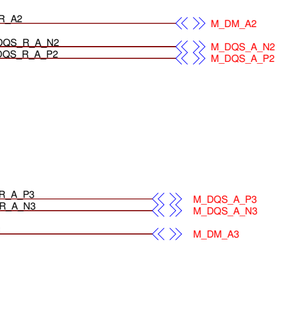

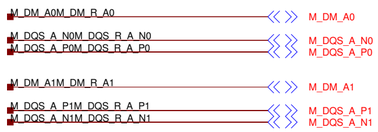

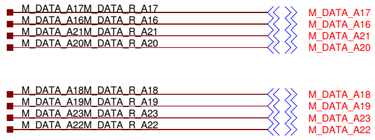

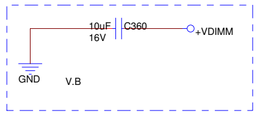

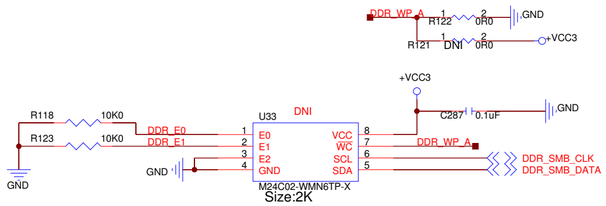

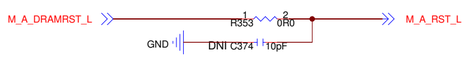

NOTE: COMPATIBLE DDR3L MEMORIES
FOR THE MINNOWMAX
ARE THE FOLLOWING:
MICRON MT41K128M16HA-125:D,
MICRON MT41K256M16HA-125:E,
MICRON MT41K512M16TNA-125:X

Memory_CHA-1

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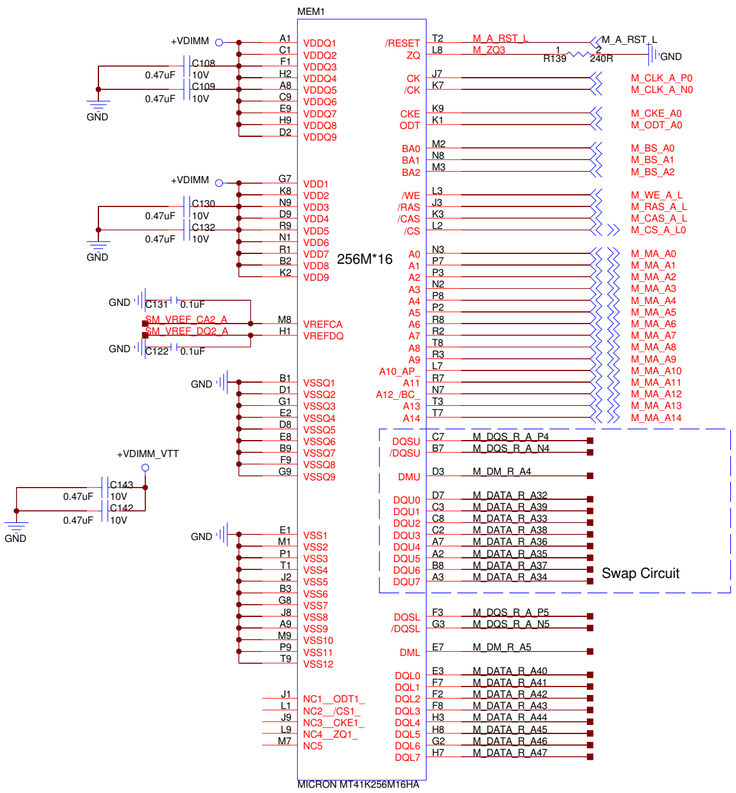

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MICRON MT41K128M16HA-125:D,
MICRON MT41K256M16HA-125:E,
MICRON MT41K512M16TNA-125:X

Memory_CHA-2

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SIZE C	DWG NO ADI -80204-0125-G00
REV	X205
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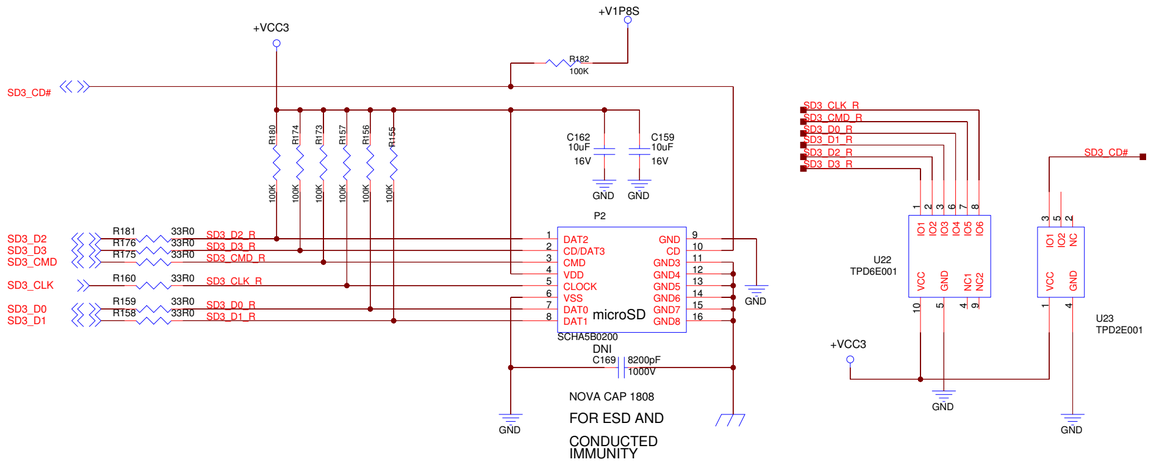

uSD CARD CAGE

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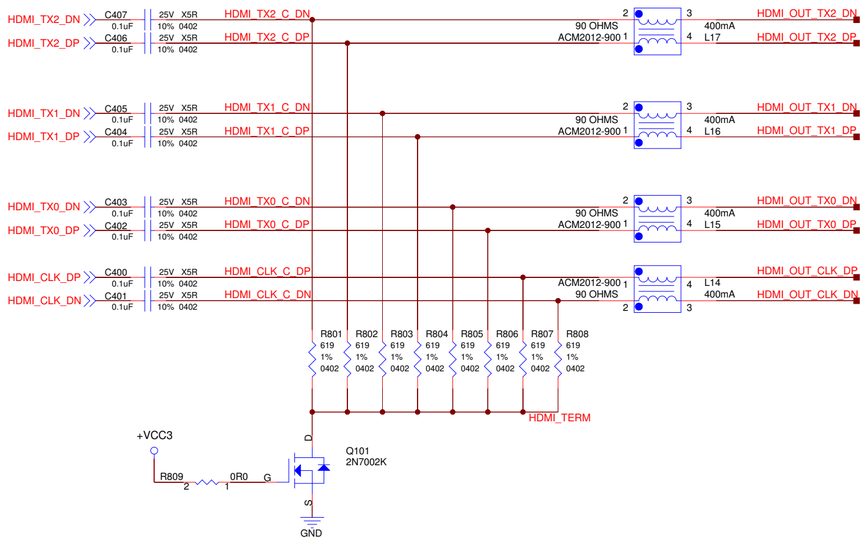
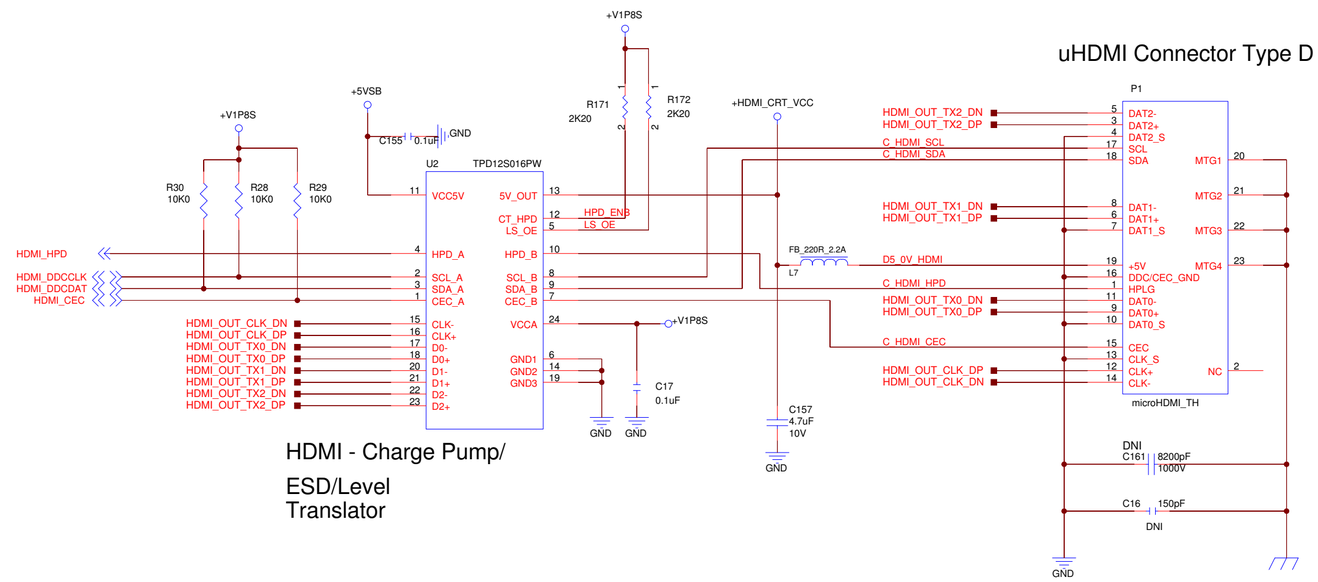
TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
REV	X205
DATE: 11/16/2015	SHEET 14 of 29

HDMI_TXn_DP/N should be longer than HDMI_CLK_DN/P





HDMI - Charge Pump/ ESD/Level Translator

uHDMI Connector Type D

uHDMI

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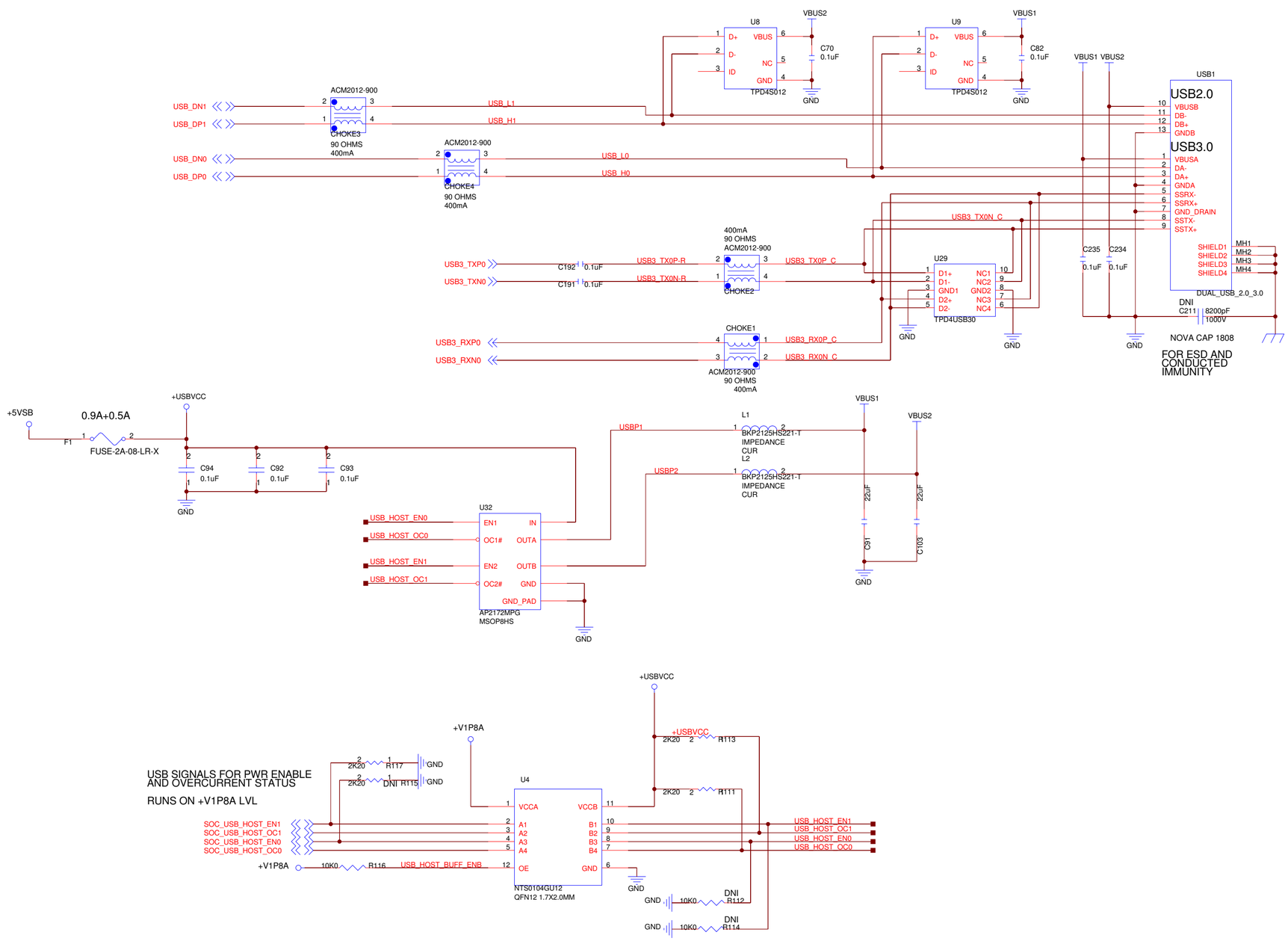
TITLE	TURBOT
SIZE C	DWG NO ADI -80204-0125-G00
REV	X205
DATE	11/16/2015
SHEET	15 of 29



USB3+USB2

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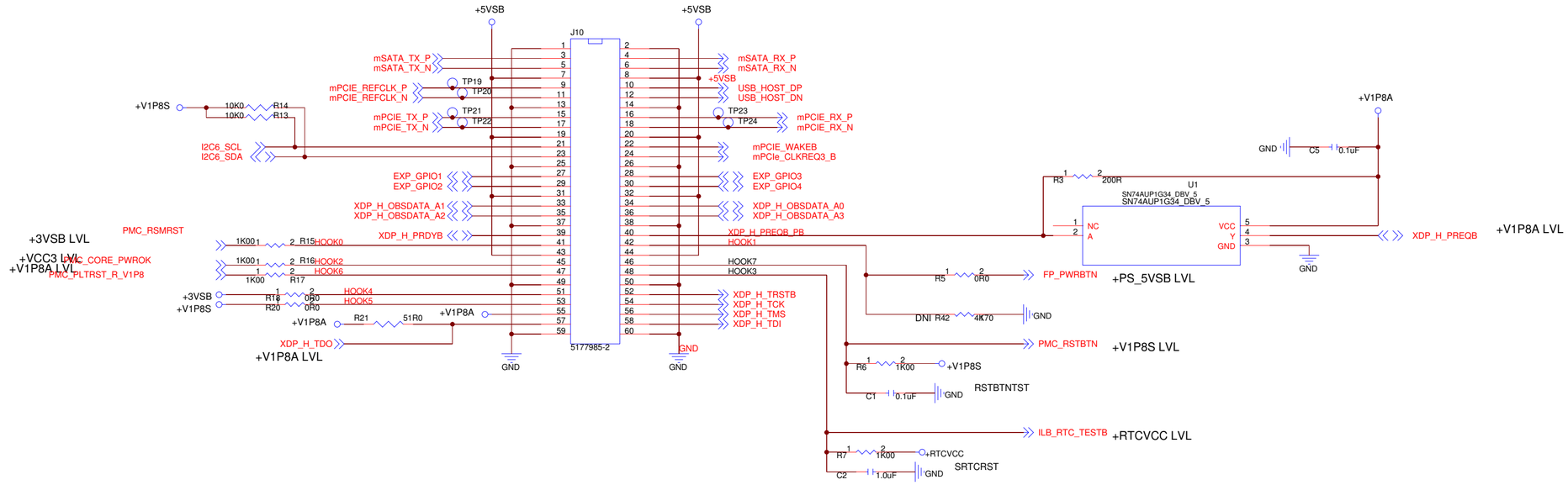
TITLE	TURBOT
SIZE C	DWG NO ADI -80204-0125-G00
REV	X205
DATE 11/16/2015	SHEET 16 of 29

EXPANSION HS CONNECTOR WITH
mPCIE, mSATA, I2S AUDIO, GPIO, and XDP I/O



EXPANSION CONNECTOR I/O

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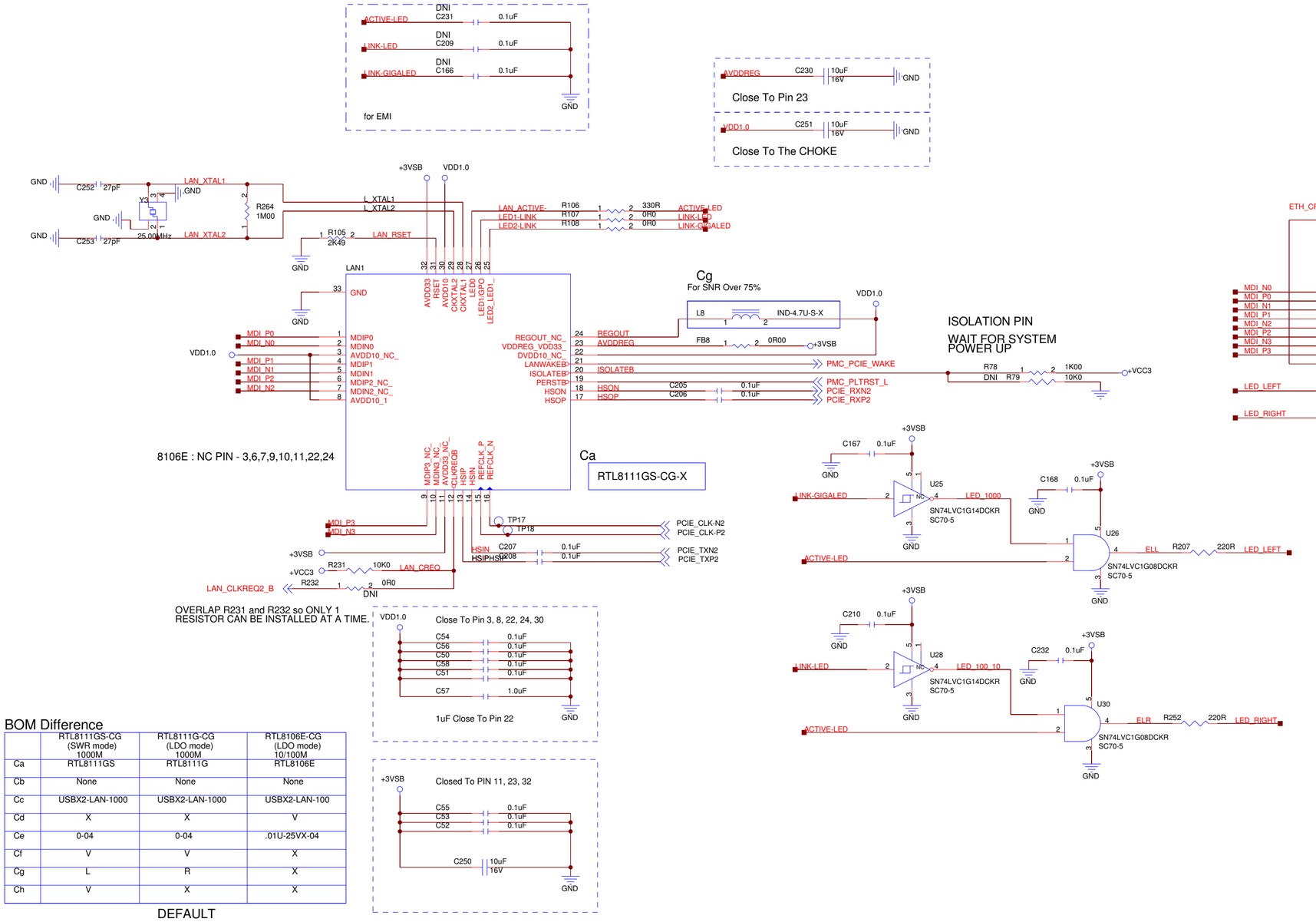
TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
REV: X205	
DATE: 11/16/2015	SHEET 17 of 29



BOM Difference

	RTL8111GS-CG (SWR mode) 1000M	RTL8111G-CG (LDO mode) 1000M	RTL8106E-CG (LDO mode) 10/100M
Ca	RTL8111GS	RTL8111G	RTL8106E
Cb	None	None	None
Cc	USBX2-LAN-1000	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	X	V
Ce	0-04	0-04	.01U-25VX-04
Cf	V	V	X
Cg	L	R	X
Ch	V	X	X

DEFAULT

LAN RT8111GS-CG

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TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
REV: X205	
DATE: 11/16/2015	SHEET 18 of 29

(BLANK)

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TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
REV: X205	
DATE: 11/16/2015	SHEET 19 of 29

POPULATE ONLY ONE OF THESE TO SELECT THE OPERATING VOLTAGE OF THE SPI FLASH.

+V1P8A
+3VSB
DNI
R618 0R00
R152 0R00
D8
BAT754C
+V_SPI
DDP_VCC
J1
HEADER 4x2
(DDP_CS)
(DDP_MISO)
(DDP_CLK)
(DDP_MOSI)
DDP_IO3L
GND

At least 0.1" on the pin 1-2 side and the pin 7-8 side to allow space for the DediProg connector

NOTE: COMPATIBLE U3 SPI ROM PARTS ARE THE FOLLOWING:
3.3V: WINBOND W25Q64BVSSIG, MICRON N25Q064A13
1.8V: WINBOND W25Q64FWSSIG, MICRON N25Q064A11

C160 1.0uF
R165 10K0
R164 10K0
R163 10K0
U3
VCC
SI/IO0
SCK
CS#
HOLD#/IO3
SO/IO1
WP#/IO2
GND
SPI_HOLD
SPI_WP
W25Q64BVSSIG
SOIC8

C383 0.1uF
C165 0.1uF
R147 100K
U18
VCCB
VCCA
SPI_MOSI
SPI_CLK
SPI_MISO
SPI_CS0
SOC_SPI_MOSI-R
SOC_SPI_CLK-R
SOC_SPI_MISO-R
SOC_SPI_CS0B-R
DDP_IO3L
NTB0104GU12
QFN12 1.7X2.0MM

+V1P8S
+3VSB
C354 0.1uF
C355 0.1uF
U14
SOC_SIO_SPI_CLK
SOC_SIO_SPI_MOSI
SOC_SIO_SPI_MISO
SOC_SIO_SPI_CS1
PMC_PLTRST_R_V1P8
SIO_SPI_CLK
SIO_SPI_MOSI
SIO_SPI_MISO
SIO_SPI_CS1
NTS0104GU12
QFN12 1.7X2.0MM

+3VSB
+V1P8S
C357 0.1uF
C356 0.1uF
U15
UART1_RTSB
UART1_CTSB
UART1_RXD
UART1_TXD
SIO_UART1_RTSB
SIO_UART1_CTSB
SIO_UART1_RXD
SIO_UART1_TXD
PMC_PLTRST_R_V1P8

SIO_SPI_CS1
SIO_SPI_MISO
SIO_SPI_MOSI
SIO_SPI_CLK
UART1_TXD
UART1_RXD
UART1_CTSB
UART1_RTSB

+PS_5VSB
+3VSB
JP1
HDR-26
GPIO_I2C_SCL
GPIO_I2C_SDA
UART2_TXD
UART2_RXD
I2SCLK_GPIO
I2SFRM_GPIO
I2SDO_GPIO
I2SDI_GPIO

+V1P8S
+3VSB
C350 0.1uF
C351 0.1uF
U7
SIO_UART2_RXD
SIO_UART2_TXD
PMC_PLTRST_R_V1P8
UART2_RXD
UART2_TXD
NTS0104GU12
QFN12 1.7X2.0MM
PICK THE ALWAYS ON 3.3V Power SUPPLY

+3VSB
+V1P8S
C353 0.1uF
C352 0.1uF
U16
I2SDI_GPIO
I2SDO_GPIO
I2SFRM_GPIO
I2SCLK_GPIO
I2S_DATIN_R
I2S_DATOUT_R
I2S_FRM_R
I2S_CLK_R
R128 0R0
R130 0R0
R129 0R0
R127 0R0
LPE_I2S_DATIN
LPE_I2S_DATOUT
LPE_I2S_FRM
LPE_I2S_CLK
PMC_PLTRST_R_V1P8

+V1P8S
+3VSB
C377 0.1uF
C376 0.1uF
R267 10K0
R266 10K0
R812 200K
U40
I2C5_SCL
I2C5_SDA
PCA9306DCUT
VSSOP8

+3VSB
+V1P8S
C349 0.1uF
C348 0.1uF
U17
I2SMCLK_GPIO
PWM0
PWM1
I2S_MCLK
SOC_PWM1
SOC_PWM0
PMC_PLTRST_R_V1P8

+V1P8A
+PS_3VSB
C346 0.1uF
C347 0.1uF
U10
SOC_GPIO_S5_2
SOC_GPIO_S5_1
SOC_GPIO_S5_0
PMC_PLTRST_R_V1P8
GPIO_S5_2
GPIO_S5_1
GPIO_S5_0
NTS0104GU12
QFN12 1.7X2.0MM
PICK THE ALWAYS ON 3.3V Power SUPPLY

SPI PROM/LSS HEADER

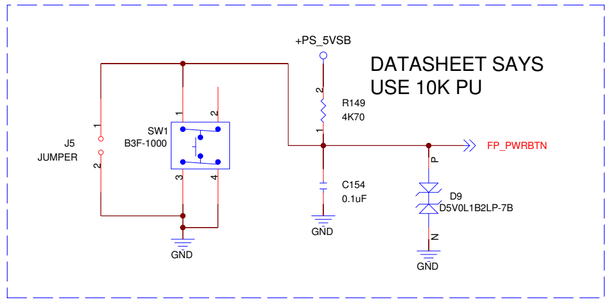
Prepared For:

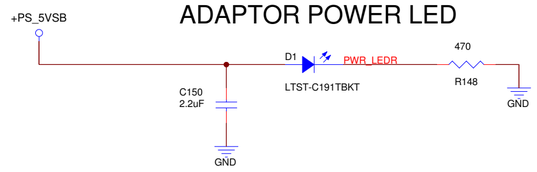
BY:
ADI ENGINEERING
1758 WORTH PARK
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM

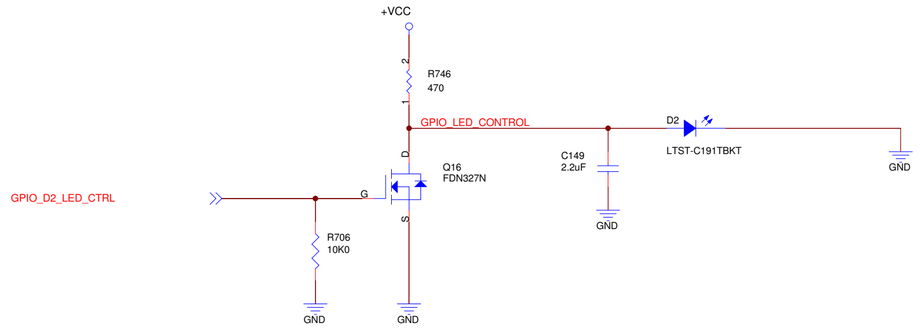
TITLE: TURBOT

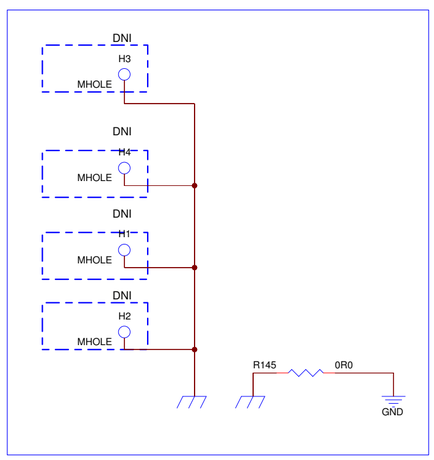
SIZE	DWG NO	REV
C	ADI -80204-0125-G00	X205

DATE 11/16/2015 SHEET 20 of 29









PWR BTN / LED / HOLES

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TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
REV: X205	
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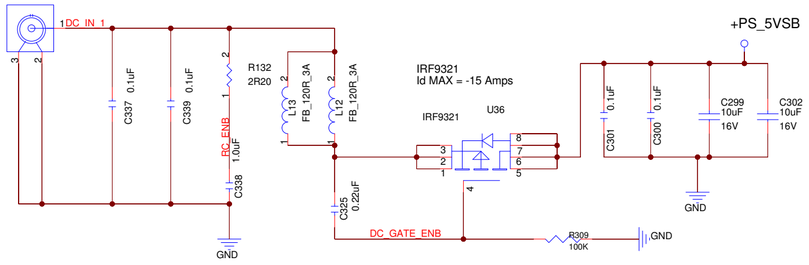
DC_IN 5V

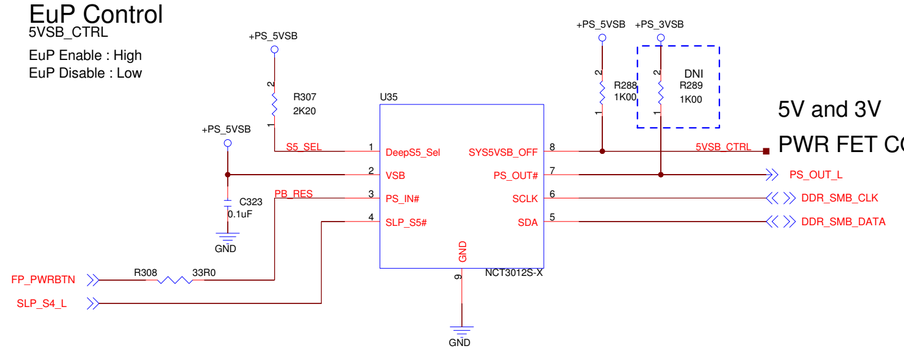


EuP Control

5VSB_CTRL

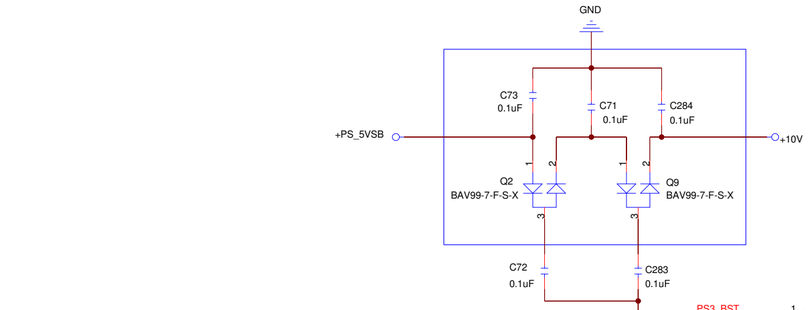
EuP Enable : High

EuP Disable : Low

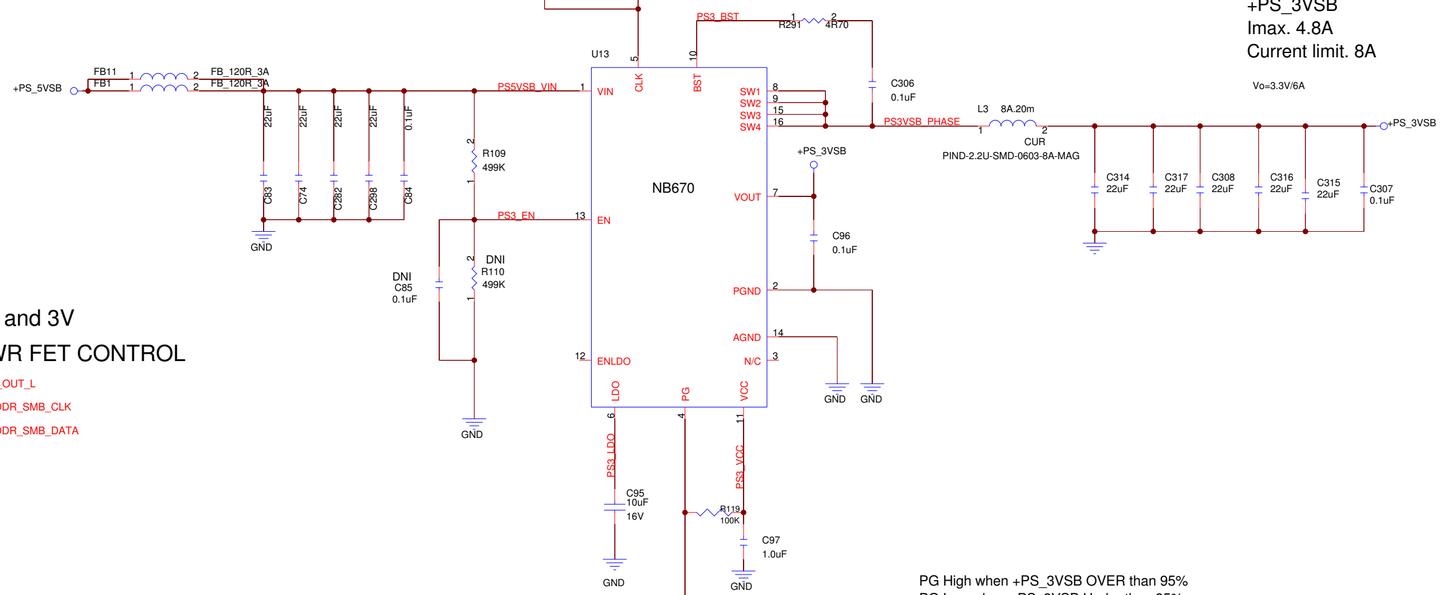


5V and 3V

PWR FET CONTROL



+3.3VSB / Boost +10V

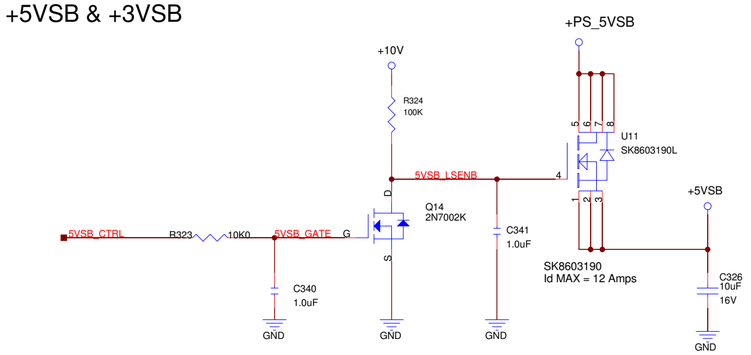


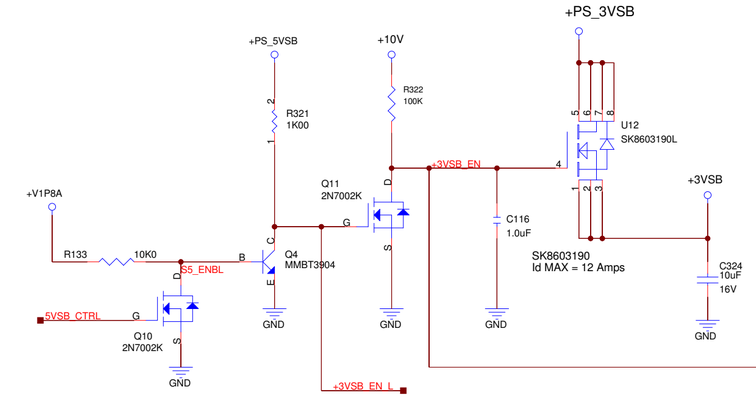
+PS_3VSB
Imax. 4.8A
Current limit. 8A

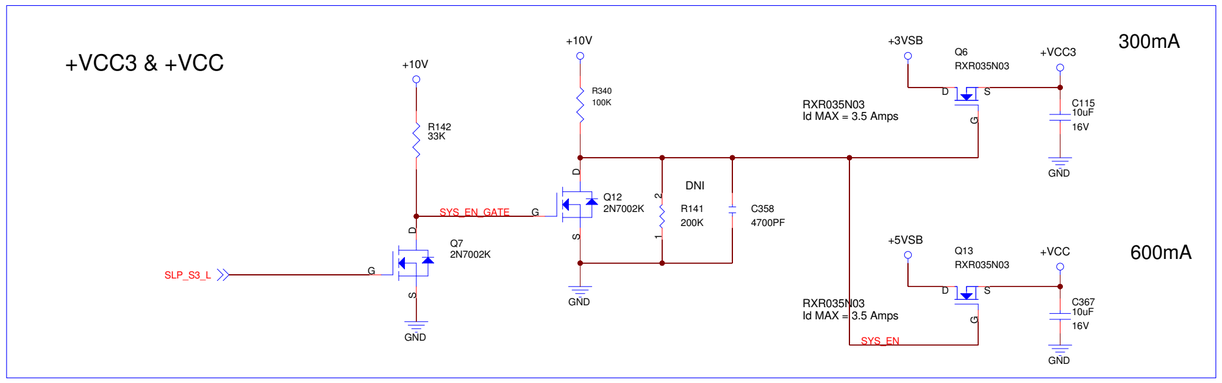
Vo=3.3V/6A

PG High when +PS_3VSB OVER than 95%
PG Low when +PS_3VSB Under than 85%

+5VSB & +3VSB







+5V

+10V

D6 BAT54A-S

+3.3V

PMC_RSMRST

VRTC LEVEL (+3VSB)

DC-5VSB/3VSB / VCC / VCC3

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TITLE	TURBOT
SIZE C	DWG NO ADI -80204-0125-G00
REV	X205
DATE 11/16/2015	SHEET 22 of 29

PDG recommend Rpu should be 70 OHMS

Intel Require

2013/7/11

6.98K-1-04
PN:05-152-698112

CLOSE PWM

CLOSE PWM

Close to SoC pinBB8

Thermal Pad
8 pcs via
Connect to GND

CLOSE QCGH1

CLOSE QCH1

CLOSE VCORE CHOKE DC side

CLOSE GFX CHOKE DC side

C1600 0.22U 25V X7R 0603

DC/DC VCORE/GFX CONTROL

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TITLE	TURBOT
SIZE C	DWG NO ADI -80204-0125-G00
REV	X205
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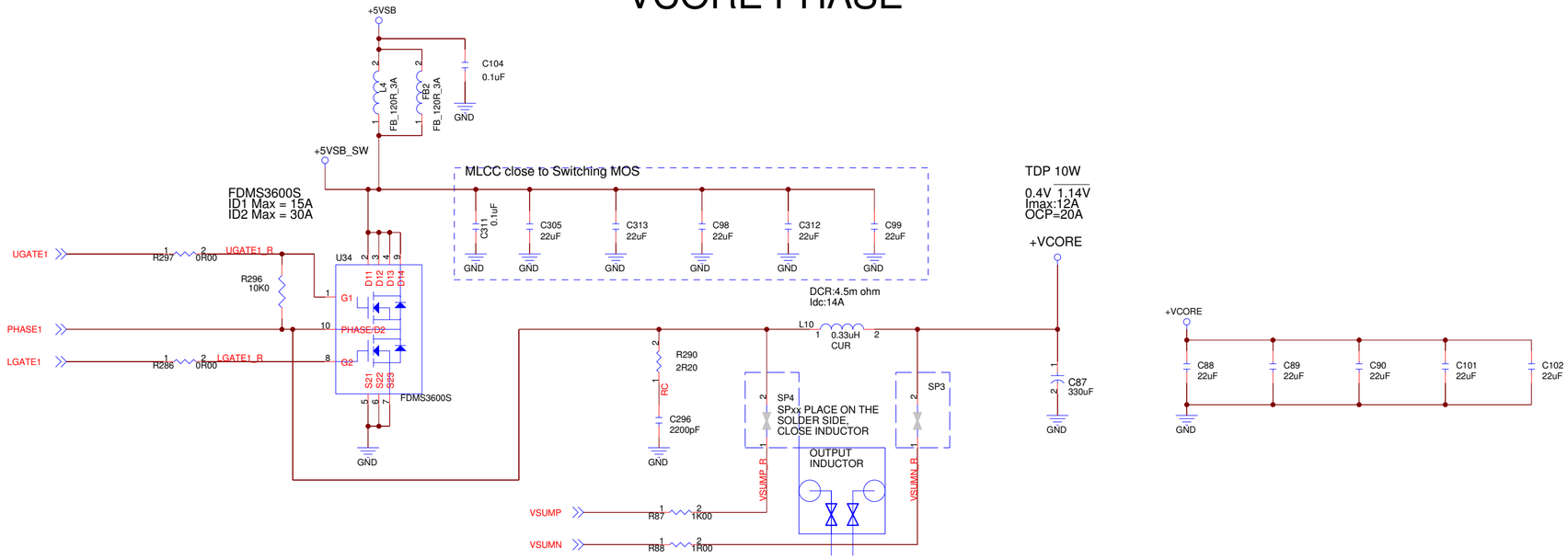
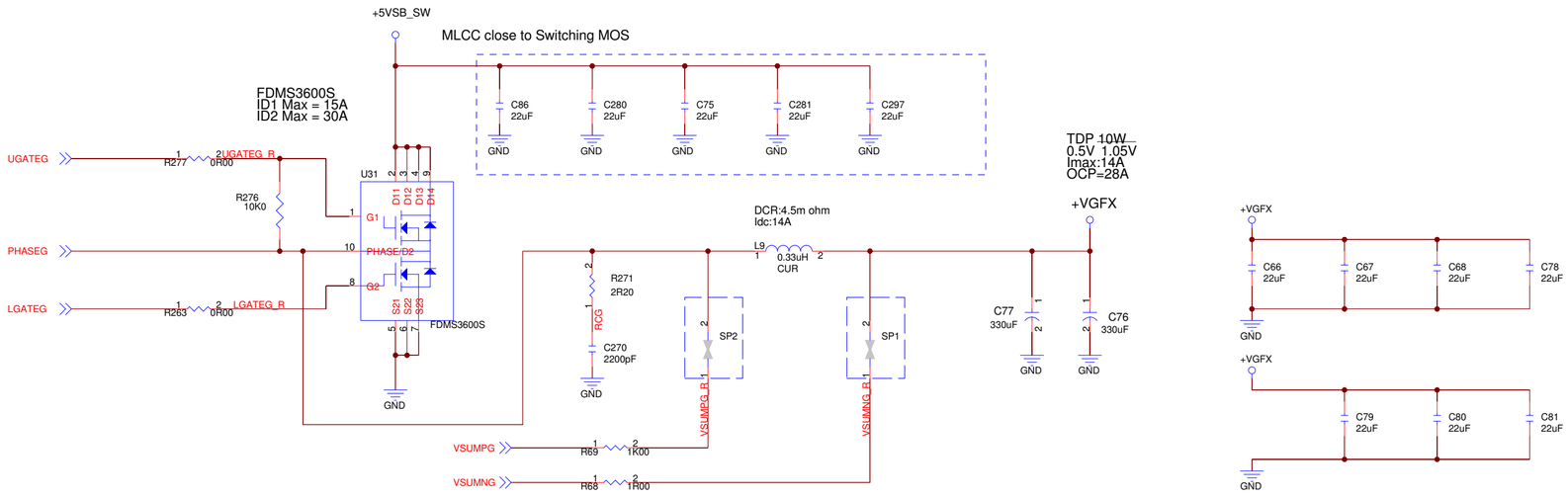
VCORE PHASE



GFX PHASE



DC/DC VCORE/GFX PHASES

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TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
REV: X205	
DATE: 11/16/2015	SHEET 24 of 29

VDIMM

F= (Vin - 0.5) / 3.85p*Vin*Rton
Rton=806K , F=285KHz

RT8207M S3 and S5 truth table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	on		on
S3	Lo	Hi	on		Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

+VDIMM_VTT

Imax:0.6A

FIX ME:
C129 is only 2V
Need more margin

1.35V
Imax. 7.1A
OCP. 11A

DCR=10mohm
Idc= 11A

DC/DC-DIMM/DDR_VTT

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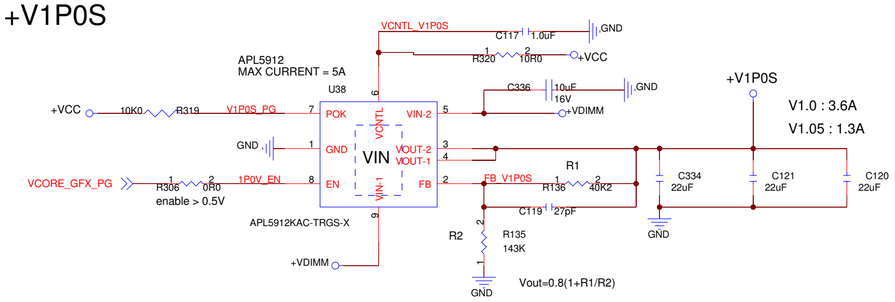
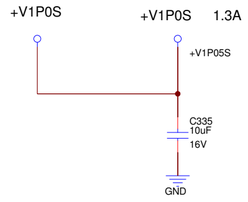
TITLE	TURBOT
SIZE C	DWG NO ADI -80204-0125-G00
REV	X205
DATE 11/16/2015	SHEET 25 of 29

+V1P0S

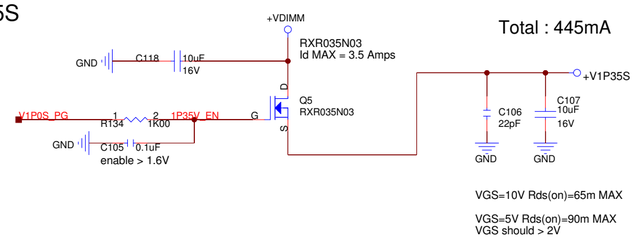


+V1P05S

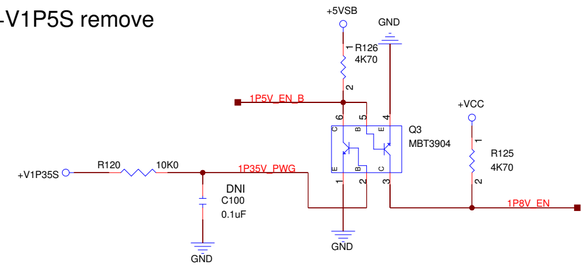
Combine +V1P0S and +V1P05S



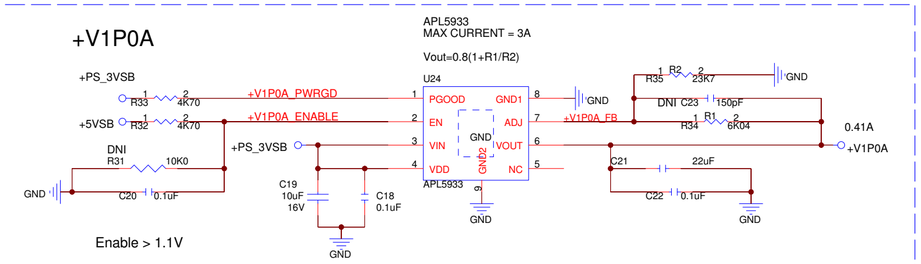
+V1P35S



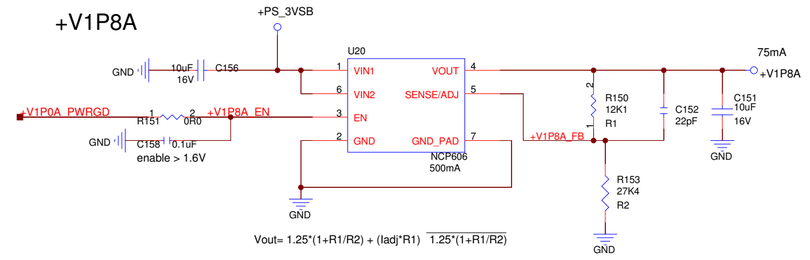
+V1P5S remove



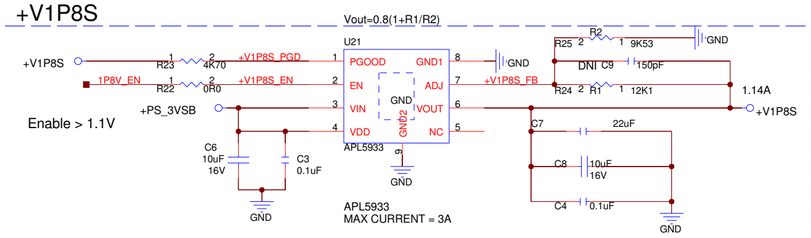
+V1P0A



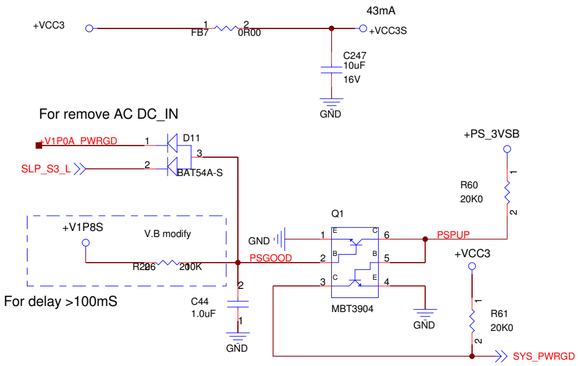
+V1P8A



+V1P8S



+VCC3S(For CPU)



DC-DC VOLTAGE

Prepared For:	BY: ADI ENGINEERING 1758 WORTH PARK CHARLOTTESVILLE, VA 22911 WWW.ADIENGINEERING.COM
TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
REV: X205	
DATE: 11/16/2015	SHEET 26 of 29

PCH-GPIO function

Pin Name	Power Well	Usage	Boot Set
GPIO_S5[00]	1P8VSB, 20k,H	SOC_GPIO_S5_0 (LSS CONN)	GPO
GPIO_S5[01]	1P8VSB, 20k,H	SOC_GPIO_S5_1 (LSS CONN)	GPO
GPIO_S5[02]	1P8VSB, 20k,H	SOC_GPIO_S5_2 (LSS CONN)	GPO
GPIO_S5[03]	1P8VSB, 20k,H	mPCIE_WAKEB	GPI
GPIO_S5[04]	1P8VSB, 20k,L	OPEN	GPO
GPIO_S5[05]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[06]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[07]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[08]	1P8VSB, 20k,H	HDMI_DC_DC ENABLE	GPO
GPIO_S5[09]	1P8VSB, 20k,H	HDMI LD SWITCH ENABLE	GPO
GPIO_S5[10]	1P8VSB, 20k,H	TXE UNLOCK control	GPO
GPIO_S0_SC[022]	1P8V, 20k,H	OPEN	GPO
GPIO_S0_SC[023]	1P8V, 20k,H	XDP_H_OBSDATA_A0	GPO
GPIO_S0_SC[024]	1P8V, 20k,H	XDP_H_OBSDATA_A1	GPO
GPIO_S0_SC[025]	1P8V, 20k,H	XDP_H_OBSDATA_A2	GPO
GPIO_S0_SC[026]	1P8V, 20k,H	XDP_H_OBSDATA_A3	GPO
GPIO_S0_SC[027]	1P8V, 20k,H	EXPANSION_BUS GPIO1	GPO
GPIO_S0_SC[028]	1P8V, 20k,H	EXPANSION_BUS GPIO2	GPO
GPIO_S0_SC[029]	1P8V, 20k,H	EXPANSION_BUS GPIO3	GPO
GPIO_S0_SC[030]	1P8V, 20k,H	EXPANSION_BUS GPIO4	GPO
GPIO_S0_SC[058]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[059]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[060]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[057]	1P8V, 20k,H	Debug Port UART3 TXD	UART
GPIO_S0_SC[061]	1P8V, 20k,H	Debug Port UART3 RXD	UART

Interrupt mapping

Function	INT# port	PCIe*1 port	Device
LAN	INTC#	port 2	RTL8111GS-CG

GPIO/HW MAPPING

Prepared For:

BY:
ADI ENGINEERING
1758 WORTH PARK
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM

TITLE			
	TURBOT		
SIZE	DWG NO		REV
C	ADI -80204-0125-G00		X205
DATE	11/16/2015	SHEET 27 of 29	

DC-IN: +5V

+PS_5VSB

EuP

N-MOS

Switching

7.5W max

+5VSB
8A max

Switching

+10V (VOLTAGE DBLR)

+PS_3VSB
4.8A max

+3VSB

N-MOS

DDR3L 1066MHz (SDRAM x4)	
+VDIMM	1.5A max
+VTT_DDR	0.5A max

0.27W*4 = 1.18W

+VTT_DDR:0.675V

LDO

N-MOS

1.917A max

Switching

1.35V 7.1A max

0.075A @V1P8A
1.14A @V1P8S

LDO

1.8V 0.075A max

1.8V

0.3A max
+VCC3

0.6A max
+VCC

N-MOS

N-MOS

LDO

1.8V 1.14A max

0.055A max

0.033A max

0.41A max

LDO

1.0V 410mA max

LDO

1.0V

2.75A max

LDO

1.05V

1.0A max

LDO

??? A max

0.75A max

1A max

0.2A max

0.07A max

??A max

1.4A max

		Bay Trail - M	Bay Trail - I
VCORE	SVID	13A	
VNN	SVID	15A	
V1P35S	1.35V	1.3A	
V1P8A	1.8V	65mA	
V1P8S	1.8V	10mA	
V1P5S	1.8V	N/A	
V3P3A	3.3V	50mA	
V3P3S	3.3V	33mA	
V1P0A	1.0V	325mA	
V1P0S	1.0V	2.75A	
V1P05S	1.05V	1.0A	
V1P2A	N/A	N/A	
V1P2S	1.2V	21.3mA	0 mA
VRTC	RTC	160uA	

Can be grounded if MIPI CSI not used.

Battery
3V

ALC282		
AVDD	5.0V	N/A
DVDD	3.3V	N/A
PVDD	1.8V	N/A

LAN RTL8111GS		
VDD3P3	3.3V	370 mA
VDD1P0	1.0V	300mA

eMMC		
VCC	3.3V	200mA
VCCQ	1.8V	150mA

CSI Connector	
3.3V	70mA

EXPANSION SLOT	
+3.3V_AUX	??A

FRONT USB3 * 1PCS	
5V	0.9A

FRONT USB2 * 1PCS	
5V	0.5A

POWER DELIVERY

Prepared For:

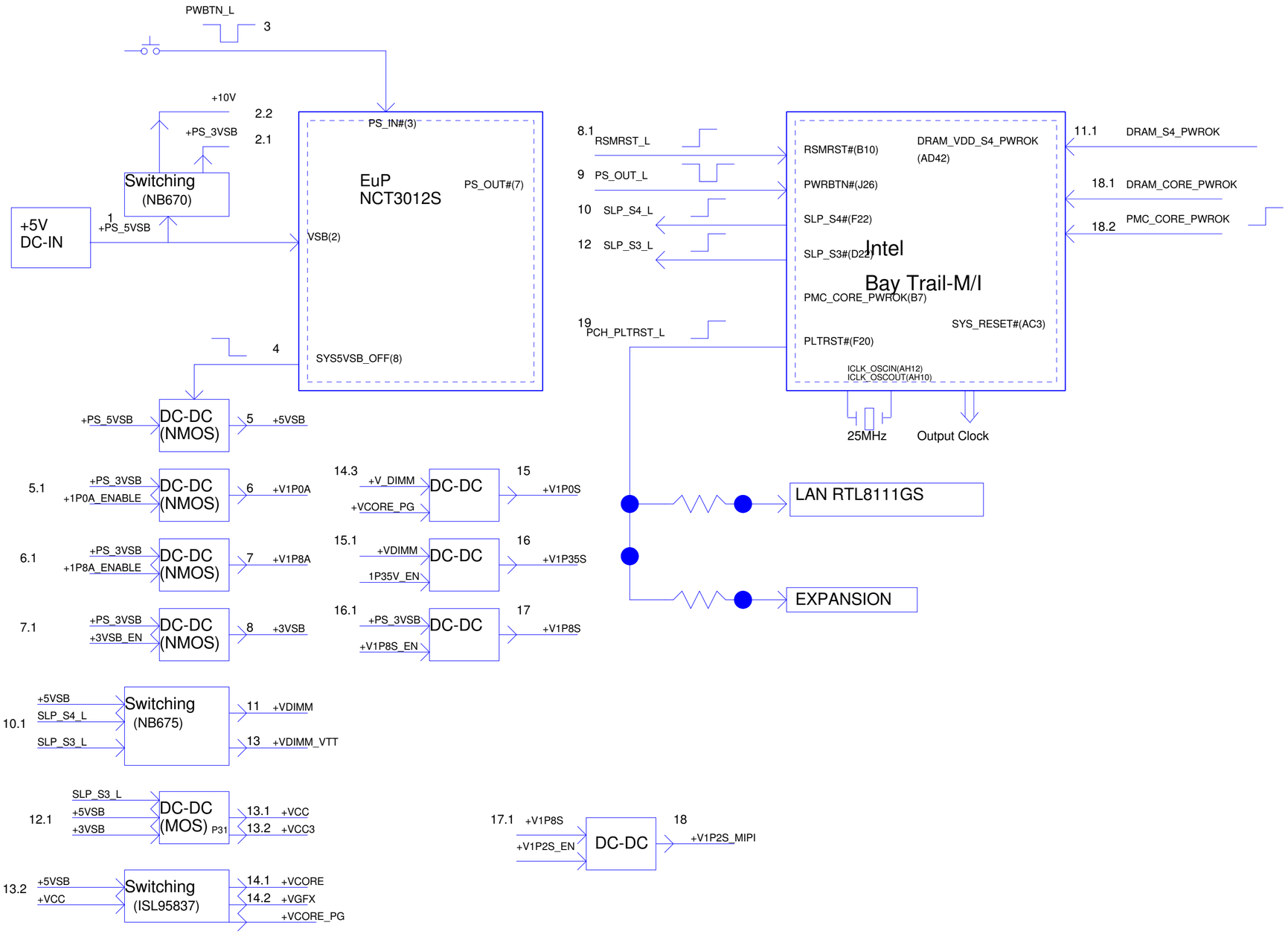
BY:
ADI ENGINEERING
1758 WORTH PARK
CHARLOTTESVILLE, VA 22911
WWW.ADIENGINEERING.COM

TITLE: TURBOT

SIZE: C | DWG NO: ADI -80204-0125-G00 | REV: X205

DATE: 11/16/2015 | SHEET 28 of 29

PWR Sequence & RST Diagram



POWER SEQUENCE

Prepared For:	BY: ADI ENGINEERING, 1758 WORTH PARK, CHARLOTTESVILLE, VA 22911, WWW.ADIENGINEERING.COM
TITLE	TURBOT
SIZE: C	DWG NO: ADI -80204-0125-G00
REV: X205	
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