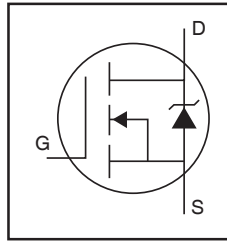


# AUIRLR2908

HEXFET® Power MOSFET

## Features

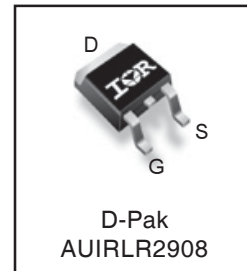
- Advanced Planar Technology
- Logic-Level Gate Drive
- Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free, RoHS Compliant
- Automotive Qualified\*



$V_{(BR)DSS}$	<b>80V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>22.5mΩ</b>
<b>max</b>	<b>28mΩ</b>
$I_D$ (Silicon Limited)	<b>39A</b> ①
$I_D$ (Package Limited)	<b>30A</b>

## Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	39①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	28	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	30	
$I_{DM}$	Pulsed Drain Current ①	150	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	120	W
	Linear Derating Factor	0.77	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 16	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited)②	180	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value ②	250	
$I_{AR}$	Avalanche Current ①	See Fig. 12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ⑥		mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.3	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	1.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount)⑤	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

HEXFET® is a registered trademark of International Rectifier.

\*Qualification standards can be found at <http://www.irf.com/>

### Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	80	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.085	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	22.5	28	mΩ	$V_{GS} = 10V, I_D = 23A$ ④
		—	25	30		$V_{GS} = 4.5V, I_D = 20A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
gfs	Forward Transconductance	35	—	—	S	$V_{DS} = 25V, I_D = 23A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -16V$

### Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge	—	22	33	nC	$I_D = 23A$
$Q_{gs}$	Gate-to-Source Charge	—	6.0	9.1		$V_{DS} = 64V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	11	17		$V_{GS} = 4.5V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 40V$
$t_r$	Rise Time	—	95	—		$I_D = 23A$
$t_{d(off)}$	Turn-Off Delay Time	—	36	—		$R_G = 8.3\Omega$
$t_f$	Fall Time	—	55	—		$V_{GS} = 4.5V$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	1890	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	260	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	35	—		$f = 1.0MHz$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	1920	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	170	—		$V_{GS} = 0V, V_{DS} = 64V, f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance ⑤	—	310	—		$V_{GS} = 0V, V_{DS} = 0V$ to 64V

### Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	39⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	150		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 23A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	75	110	ns	$T_J = 25^\circ\text{C}, I_F = 23A, V_{DD} = 25V$
$Q_{rr}$	Reverse Recovery Charge	—	210	310	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.71mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 23A$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ③  $I_{SD} \leq 23A$ ,  $di/dt \leq 400A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 1.0ms$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ Limited by  $T_{Jmax}$ , see Fig. 12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.71mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 23A$ ,  $V_{GS} = 10V$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.
- ⑩  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

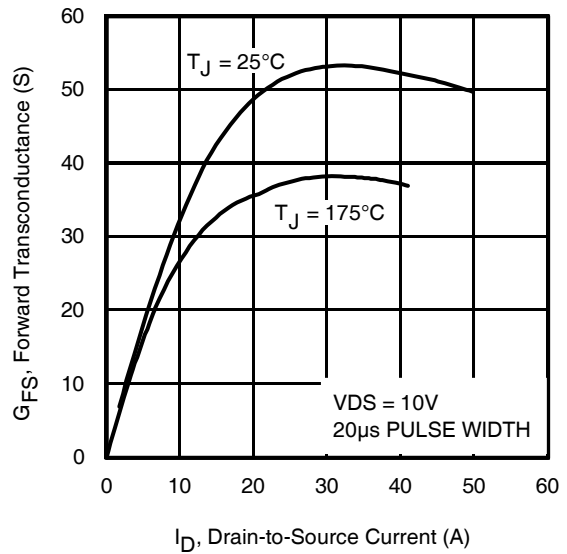
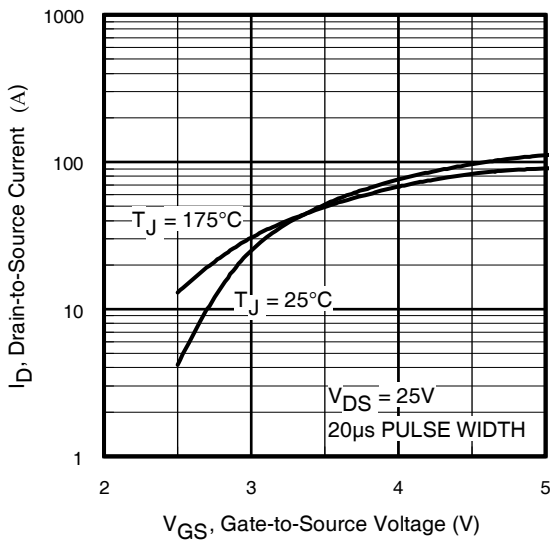
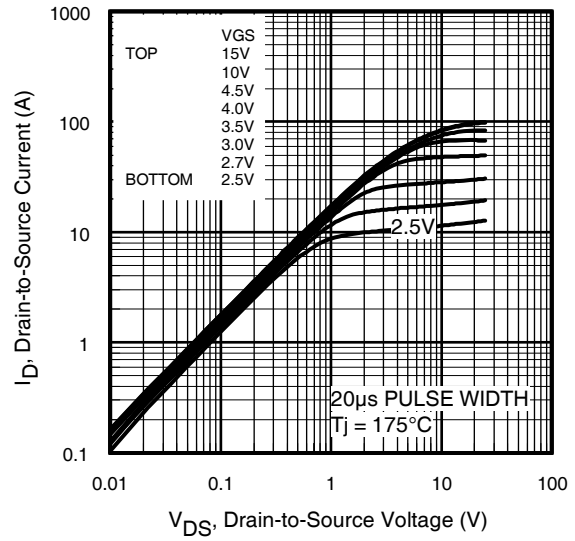
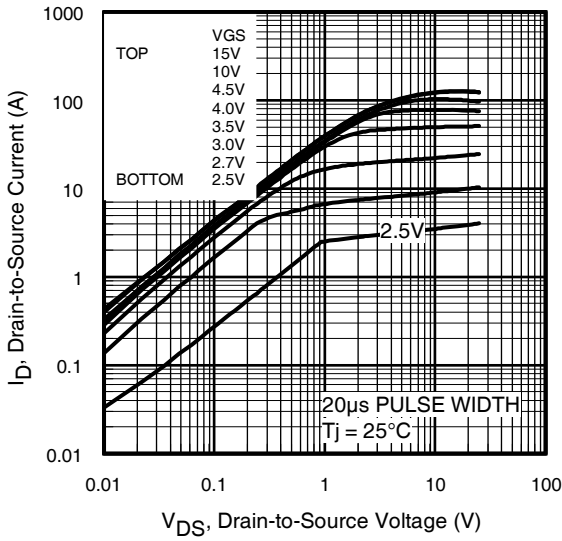
**Qualification Information<sup>†</sup>**

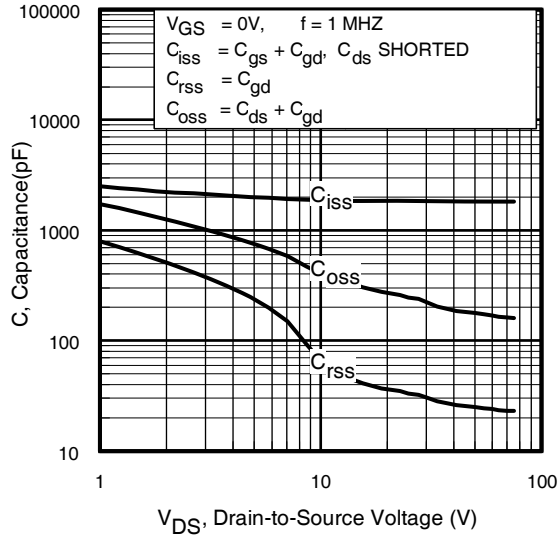
<b>Qualification Level</b>		Automotive (per AEC-Q101) <sup>††</sup>	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		D-Pak	MSL1
<b>ESD</b>	Machine Model	Class M3 (+/- 400V) <sup>†††</sup> AEC-Q101-002	
	Human Body Model	Class H1C (+/- 1500V) <sup>†††</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) <sup>†††</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

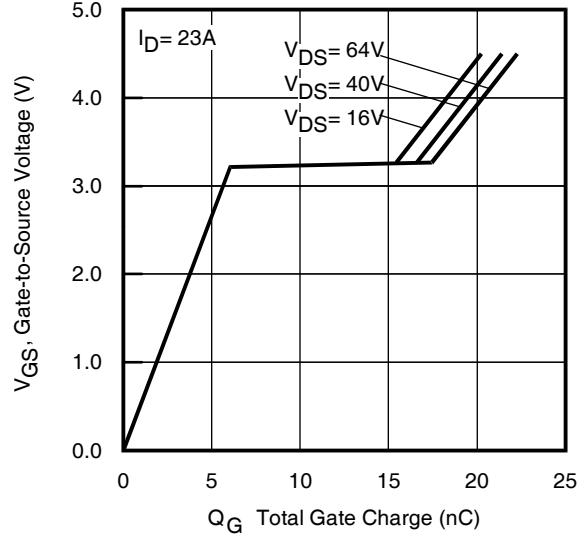
†† Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

††† Highest passing voltage.

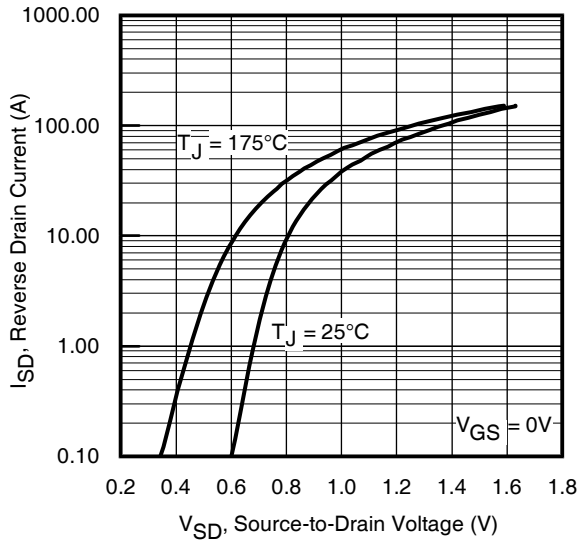




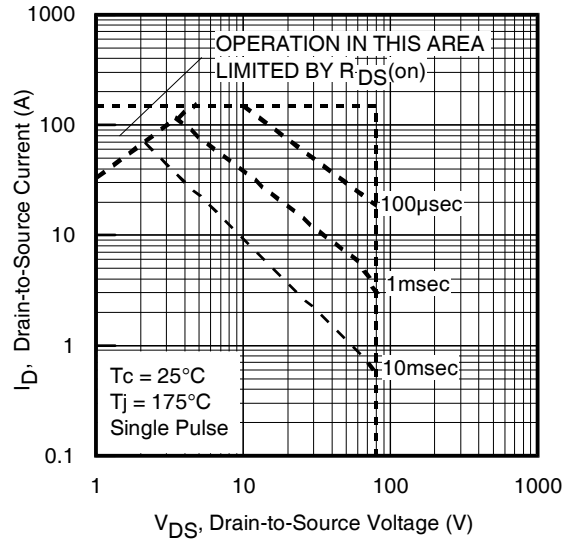
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



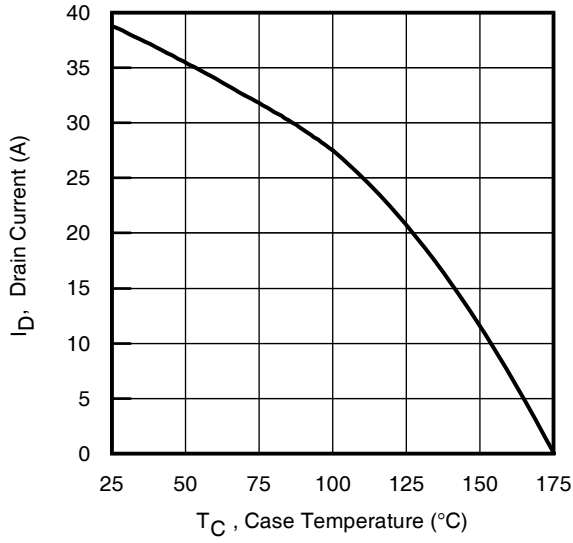
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



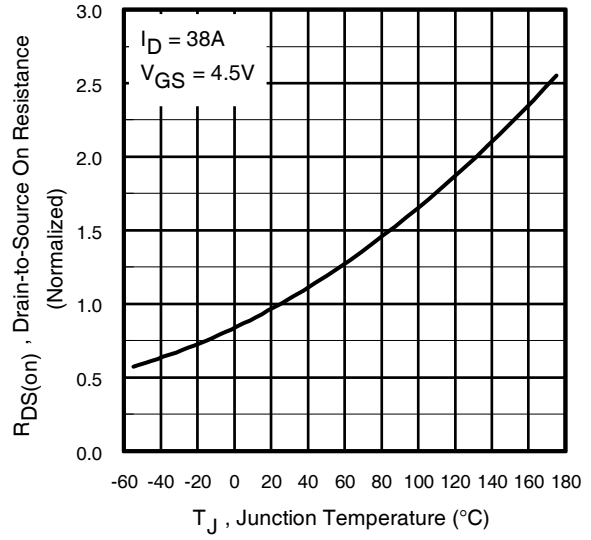
**Fig 7.** Typical Source-Drain Diode Forward Voltage



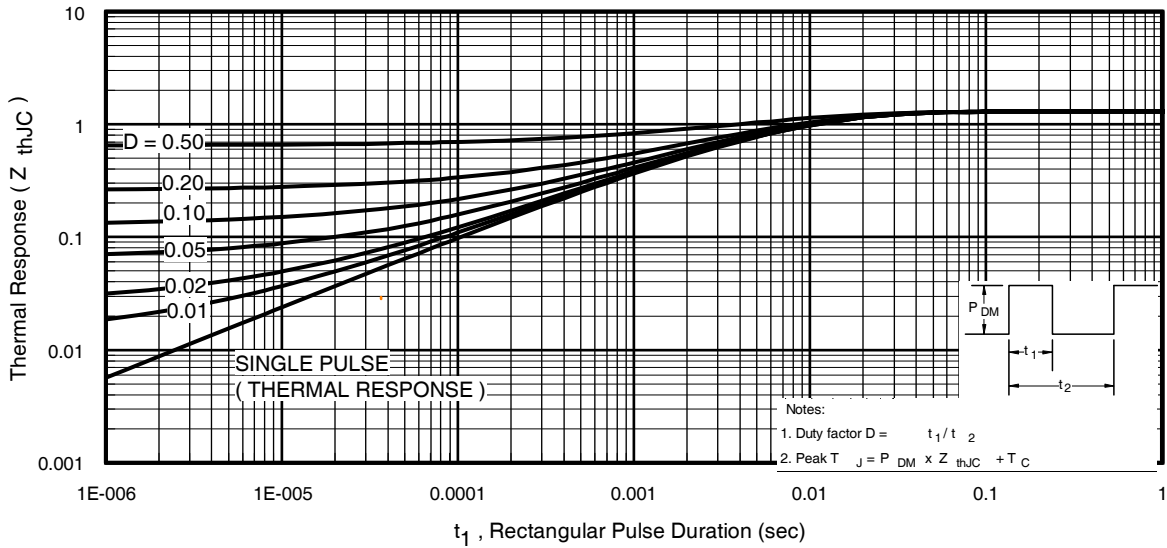
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Normalized On-Resistance vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

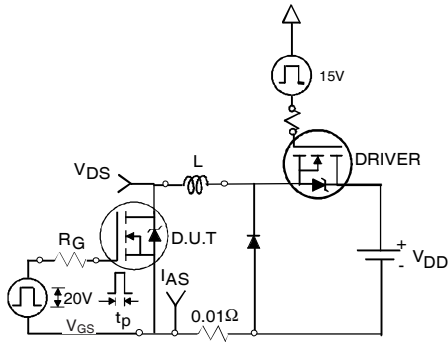


Fig 12a. Unclamped Inductive Test Circuit

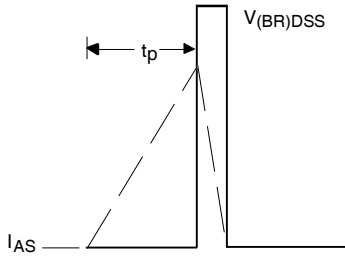


Fig 12b. Unclamped Inductive Waveforms

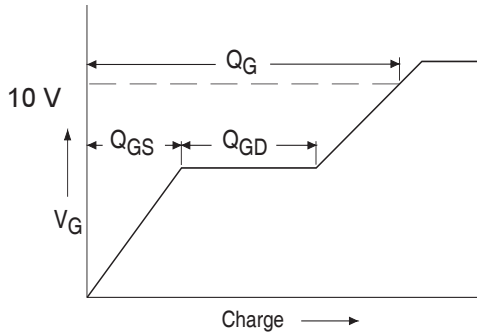


Fig 13a. Basic Gate Charge Waveform

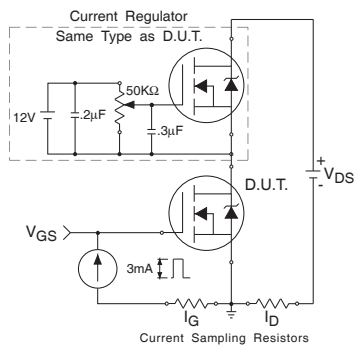


Fig 13b. Gate Charge Test Circuit  
www.irf.com

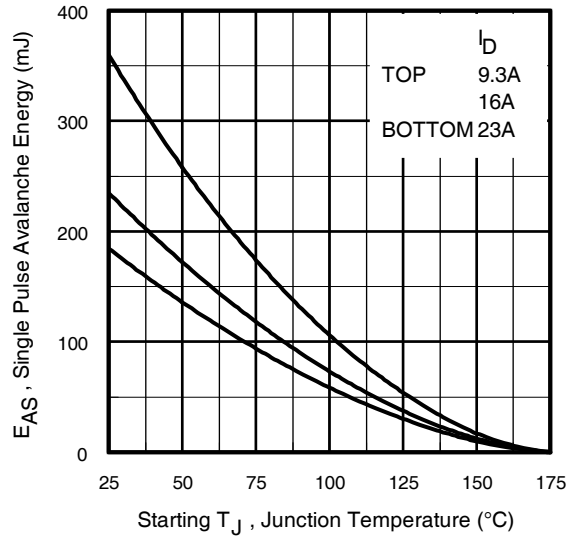


Fig 12c. Maximum Avalanche Energy vs. Drain Current

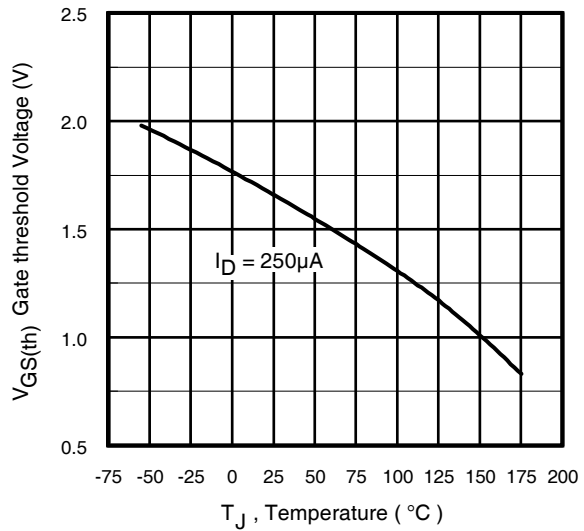


Fig 14. Threshold Voltage vs. Temperature

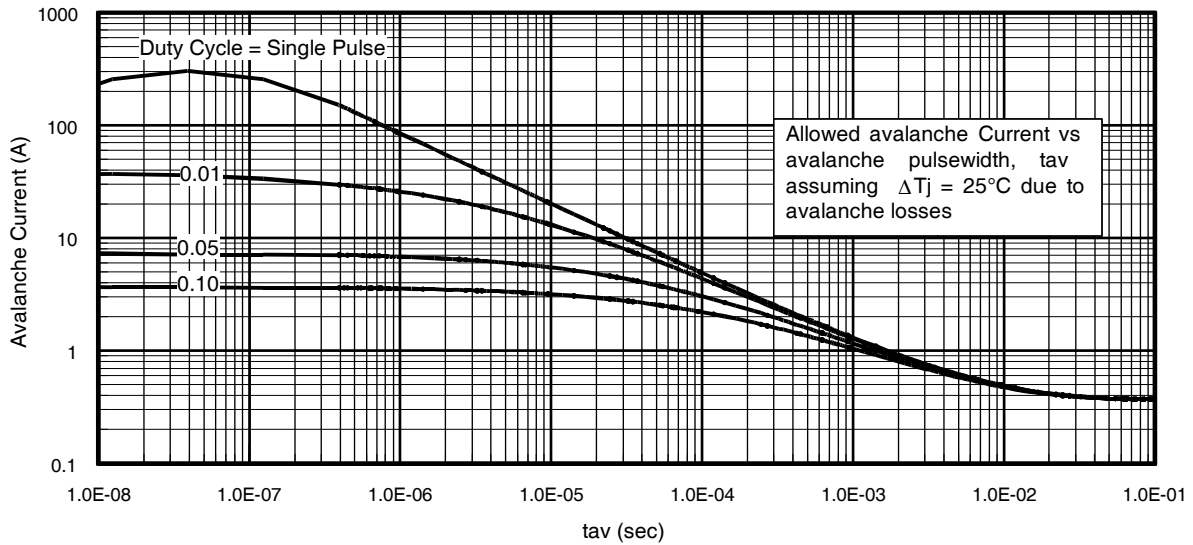
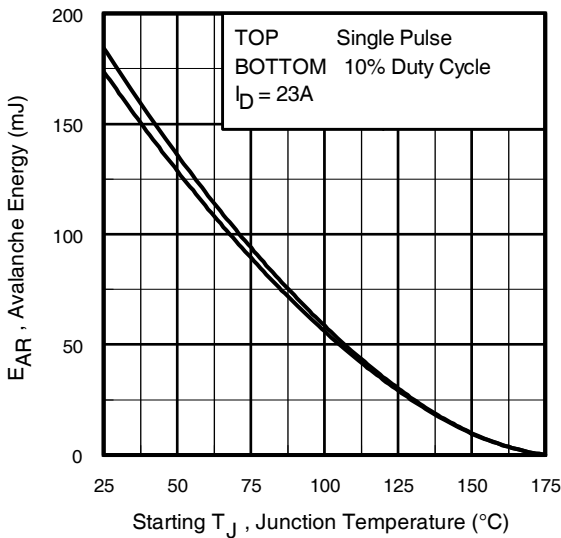


Fig 15. Typical Avalanche Current vs.Pulsewidth



**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

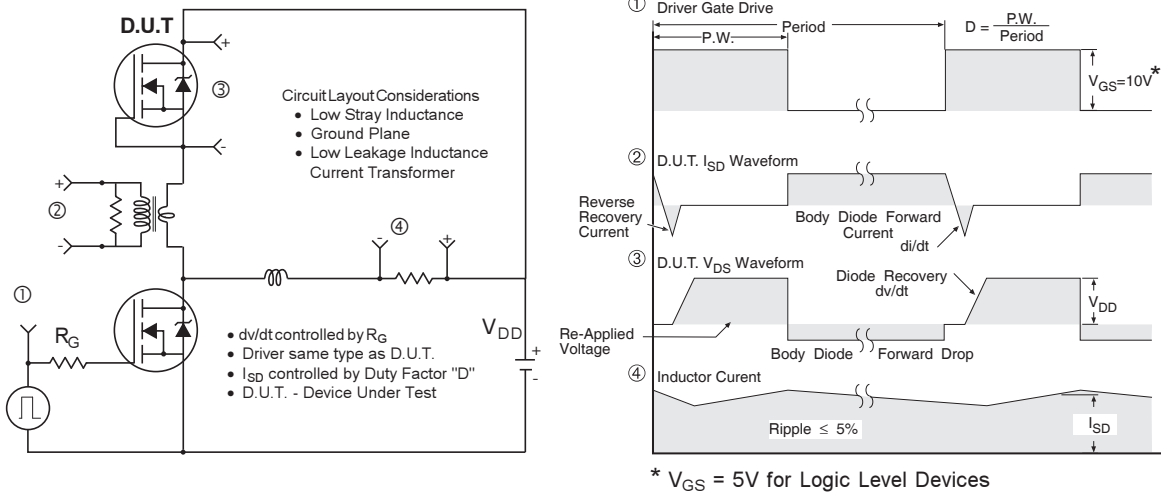
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

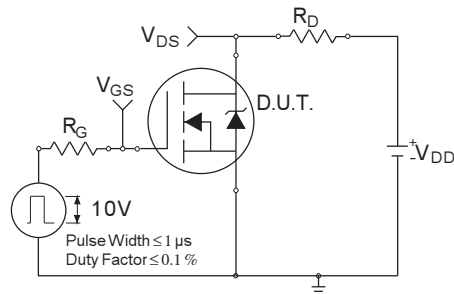
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 16. Maximum Avalanche Energy vs. Temperature

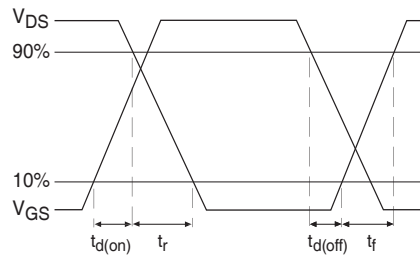




**Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



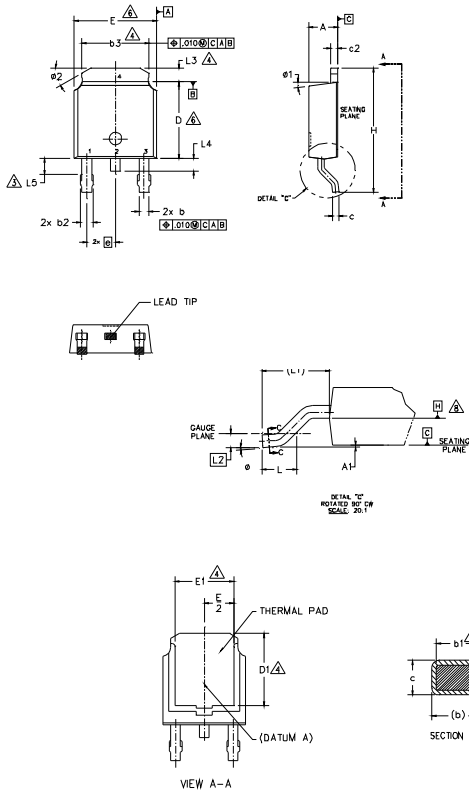
**Fig 18a. Switching Time Test Circuit**



**Fig 18b. Switching Time Waveforms**

## D-Pak (TO-252AA) Package Outline

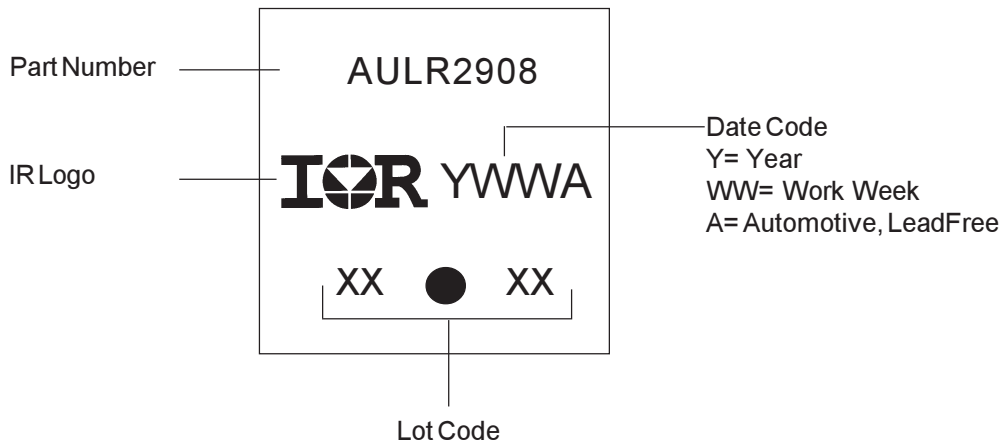
Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
  - 3.- LEAD DIMENSION UNCONTROLLED IN L5.
  - 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
  - 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
  - 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  - 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	2.18	2.39	.086	.094	7	
A1	-	0.13	-	.005		
b	0.64	0.89	.025	.035		
b1	0.65	0.79	.025	.031		
b2	0.76	1.14	.030	.045		
b3	4.95	5.46	.195	.215		
c	0.46	0.61	.018	.024		
c1	0.41	0.56	.016	.022		
c2	0.46	0.89	.018	.035		
D	5.97	6.22	.235	.245		6
D1	5.21	-	.205	-		4
E	6.35	6.73	.250	.265		6
E1	4.32	-	.170	-		4
e	2.29 BSC		.090 BSC			LEAD ASSIGNMENTS
H	9.40	10.41	.370	.410		
L	1.40	1.78	.055	.070		
L1	2.74 BSC		.108 REF.			
L2	0.51 BSC		.020 BSC		HEXFET 1.- GATE 2.- DRAIN 3.- SOURCE 4.- DRAIN	
L3	0.89	1.27	.035	.050		
L4	-	1.02	-	.040		
L5	1.14	1.52	.045	.060		
ø	0"	10"	0"	10"	ICBT & CoPAK 1.- GATE 2.- COLLECTOR 3.- EMITTER 4.- COLLECTOR	
ø1	0"	15"	0"	15"		
ø2	25"	35"	25"	35"		

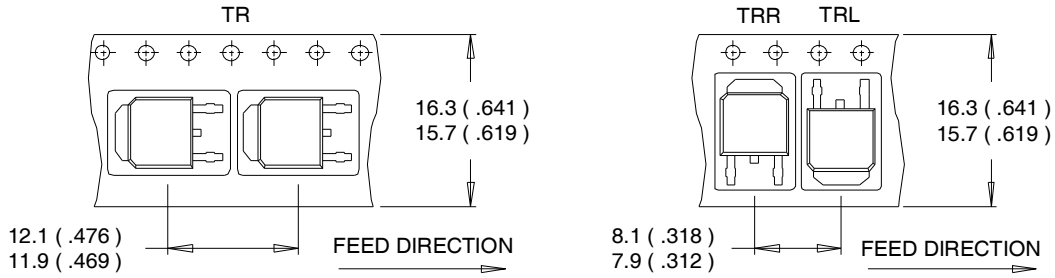
## D-Pak Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

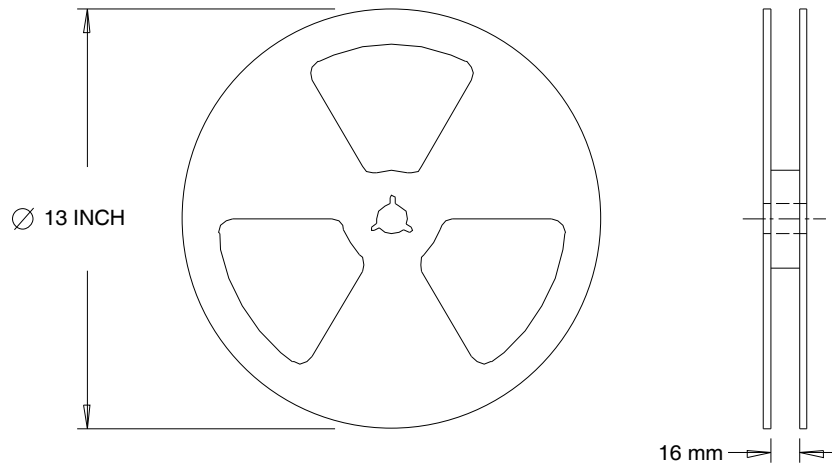
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

## Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRLR2908	Dpak	Tube	75	AUIRLR2908
		Tape and Reel	2000	AUIRLR2908TR
		Tape and Reel Left	3000	AUIRLR2908TRL
		Tape and Reel Right	3000	AUIRLR2908TRR

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