International
IOR Rectifier

AUIR0815S

AUTOMOTIVE GRADE

January 24th, 2012

BUFFER GATE DRIVER IC

Features

- High peak output current > 10A
- Low propagation delay time
- Negative turn off bias can be applied to V_{EE} using an external supply
- Two output pins permit to choose different Ron and Roff resistors.
- Low supply current
- Undervoltage lockout
- Continuous 'on' capability
- Suitable for high power inverter applications in conjunction with an external pre-driver
- Lead-Free, RoHS Compliant
- Automotive qualified

Description

The AUIR0815 buffer gate driver family, in conjunction with a pre-driver stage, is suited to drive a single half bridge in power switching applications. These buffer gate drivers incorporate the ability to enter into a low quiescent current mode.

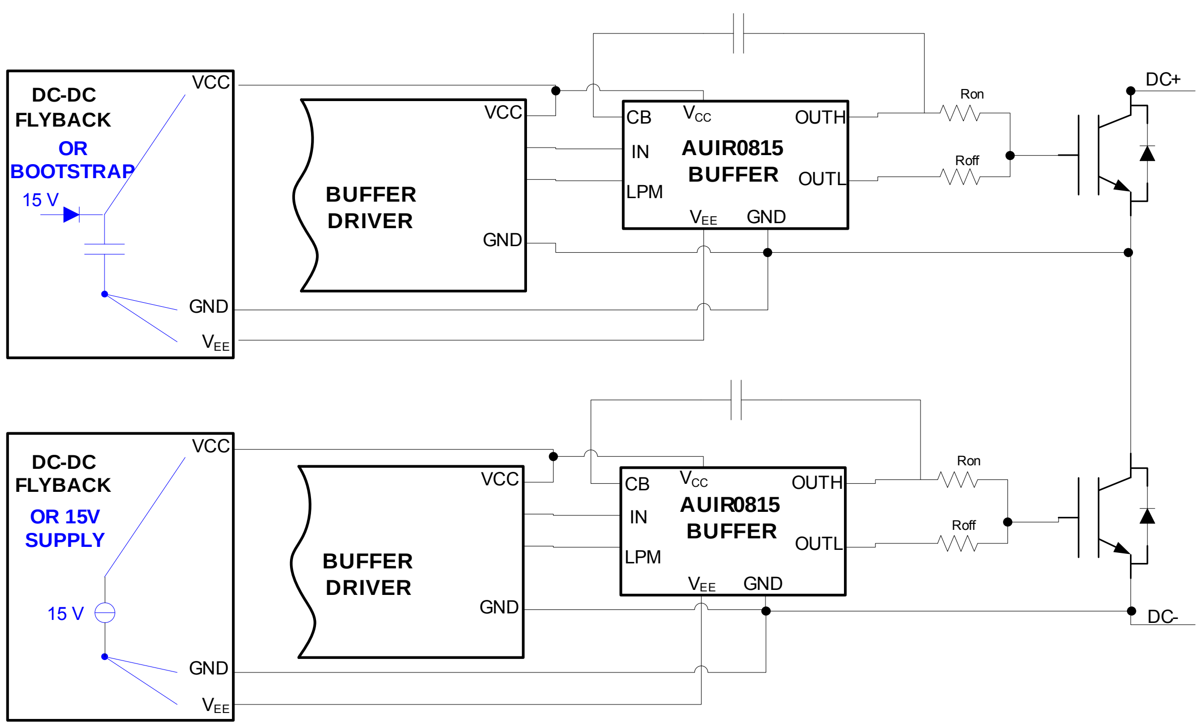
Product Summary

V_{CC} -GND	10V to 30V
GND -V_{EE}	-1V to 20V
Vcc- V_{EE}	10V to 30V
$I_{O\ drive}$	> 10A

Package

8 Pin SOIC

Typical connection



Qualification Information[†]

Qualification Level		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8N	MSL2[††] 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M1 (Pass +/-100 V) (per AEC-Q100-003)	
	Human Body Model	Class H1B (+/-1000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher MSL ratings may be available for the specific package type listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which permanent damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the “Recommended Operating Condition” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
GND	to Vcc	-37	0.3	V
V_{EE}	To Vcc	-37	0.3	V
V_{IN}	Logic input voltage to Vcc	- 40	0.3	V
VB	Vbootstrap to OUTPUT	-0.3	5.5	V
LPM	LPM voltage to Vcc	- 40	0.3(*)	V
V_{OUTH}	OUTH Output voltage	Vcc-37	V_{CC} + 0.3	V
V_{OUTL}	OUTL output voltage	V_{EE}-0.2	V_{CC} + 0.3	V
P_D	Package power dissipation @ $T_A \leq 25$ °C	—	1	W
Rth_{JA}	Thermal resistance, junction to ambient	—	80	°C/W
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	°C
T_L	Lead temperature (soldering, 10 seconds)	—	300	°C

(*) LPM is allowed to settle to an higher voltage than specified providing a current limitation of 10uA

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table

<table>
<tr><th>Symbol</th><th>Definition</th><th>Min.</th><th>Max.</th><th>Units</th></tr>
<tr><td>V_{CC-GND}</td><td>Gate driver positive supply voltage</td><td>6(*)</td><td>30</td><td rowspan="6">V</td></tr>
<tr><td>GND- V_{EE}</td><td>Gate driver negative supply voltage.
V_{EE} is Shorted to GND in case of single supply operation</td><td>-1</td><td>15</td></tr>
<tr><td>Vcc- V_{EE}</td><td>Total supply voltage</td><td>10</td><td>30</td></tr>
<tr><td>V_{OUTH}</td><td>OUTH Output voltage</td><td>Vcc-30</td><td>Vcc</td></tr>
<tr><td>V_{OUTH} - V_{EE}</td><td>Voltage difference between OUTH and V_{EE}</td><td>-5</td><td>—</td></tr>
<tr><td>V_{IN}</td><td>Logic input voltage (IN and LPM)</td><td>Vcc-35</td><td>V_{CC}</td></tr>
<tr><td>Cboot</td><td>OUTPUT pull up boot capacitor</td><td>10</td><td>20</td><td>nF</td></tr>
<tr><td>Ron</td><td>OUTH series resistor to gate</td><td>1.5</td><td>20</td><td>Ohm</td></tr>
<tr><td>Roff</td><td>OUTL series resistor to gate</td><td>1.5</td><td>20</td><td>Ohm</td></tr>
<tr><td>Cs</td><td>Snubber capacitor between OUTH and VCC</td><td>10</td><td>24</td><td>nF</td></tr>
</table>

(*)When 3V< V_{CC-GND} < V_{CC-GND_MIN} 30 Ohm max resistance pulls down OUTL to V_{EE} while OUTH is in HiZ. Guaranteed by design.

Static Electrical Characteristics

V_{CC} -GND= 15V; GND-V_{EE} =5V; 15nF connects CB to OUTH; 22nF connects Vcc to OUTH ;-40 °C < T_A < 125 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{CC}-GND supply undervoltage positive going threshold	10.2	11.7	12.8	V	LPM=HIN=1=VCC VE=GND; OUTH pulled to V_{CC}-2V with 100mA current limitation
V_{CCUV-}	V_{CC}-GND supply undervoltage negative going threshold	9.6	10.5	11.4	V	
V_{CCUVH}	V_{CC}-GND supply undervoltage lockout hysteresis	0.5	1.2	—	V	
VB_{UV}	Vbootstrap undervoltage (*)	—	4	—	V	
I_{QGG}	GND supply current	—	—	60	uA	IN=X; LPM=X
I_{QEESW}	V_{EE} supply current, IN switching	2	4	10	mA	IN switches at 10kHz 50% duty cycle; LPM=1
I_{QEE0}	V_{EE} supply current, IN=0	—	—	8.0	mA	steady state with IN=0 and LPM=1
I_{QEE025}	V_{EE} supply current, IN=0	—	—	6.5	mA	steady state with IN=0 and LPM=1 , T=25^C
I_{QEE1}	V_{EE} supply current, IN=1	—	—	3	mA	steady state with IN=1 and LPM=1
I_{QEELQ0}	V_{EE} supply current, LPM=0, IN=0	—	—	2	mA	steady state with IN=0 and LPM=0
I_{QEELQ1}	V_{EE} supply current, LPM=0, IN=1	—	—	1.5	mA	steady state with IN=1 and LPM=0
I_{QEEUV}	V_{EE} supply current, V_{CC}<V_{CCUV-}	—	—	1.8	mA	steady state with IN=X, LPM=X, V_{CC}<V_{CCUV-}
I_{QOUTL1}	Current flowing into OUTL	—	—	1.5	uA	IN=1; LPM=1 ; OUTL-GND=15V; OUTH disconnected
I_{QB}	Current into CB pin	—	—	1	mA	IN=1; LPM=1 ;CB-OUTH=5V
I_{QOUTH0}	Current flowing out from OUTH	—	—	3.5	mA	steady state with IN=0 and LPM=1, V(OUTH)=V_{EE}, OUTL disconnected
I_{BOUTH}	Current flowing out from CB, bootstrap discharged	—	20	40	mA	steady state, CB shorted to OUTH, IN=0 and LPM=1, V(OUTH)=V_{EE}, OUTL disconnected
I_{OUTH+}	OUTH high short circuit pulsed current	10	—	—	A	10A current pulse with PW<10usec
I_{OUTL-}	OUTL low short circuit pulsed current	10	—	—	A	

(*)When CB-OUTH< VB_{UV} the power nmos pulling up OUTH is turned off. The high level on OUTH is kept by a parallel PMOS (see also block diagram).

Pins: IN, LPM

V_{CC} -GND= 15V; GND-V_{EE} =5V; 15nF connects CB to OUTH; 22nF connects Vcc to OUTH; -40 °C < T_A < 125 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{INH\ vcc}$	Logic "1" IN input voltage to V_{CC}	-3.5	-2.5	-1.0	V	V_{CC}-GND> V_{CCUV-}
$V_{INL\ vcc}$	Logic "0" IN input voltage to V_{CC}	-5.5	-4.5	-3.5		
V_{INhis}	Logic IN input hysteresis	1	2	3.3		
$V_{LPMH\ vcc}$	Logic "1" LPM input voltage to V_{CC}	-3	-2.5	-1.4	V	V_{CC}-GND> V_{CCUV-}
$V_{LPML\ vcc}$	Logic "0" LPM input voltage to V_{CC}	-3.8	-3	-2.5		
V_{LPMhis}	Logic LPM input hysteresis	0.25	-	1.8		
I_{IN15}	Current flowing out from IN when V_{CC}-IN=15V	40	90	180	uA	IN=GND
I_{LPM15}	Current flowing out from LPM V_{CC}-LPM=15V	10	25	50	uA	LPM=GND

Pins: OUTH,OUTL

V_{CC} -GND= 15V; GND-V_{EE} =5V; 15nF connects CB to OUTH; 22nF connects Vcc to OUTH; -40 °C < T_A < 125 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Rup_OUTH25	Rdson pull up transistor OUTH	—	90	120	mOhm	10A current pulse with PW<10usec T_A=25^C
Rdw_OUTL25	Rdson pull down transistor OUTL	—	180	240		
Rup_OUTH	Rdson pull up transistor OUTH	—	—	180		10A current pulse with PW<10usec
Rdw_OUTL	Rdson pull down transistor OUTL	—	—	320		
I_{PMOS}	OUTH Pull up current when bootstrap cap is discharged	5	20	30	mA	IN=1 LPM=1, CB-OUTH=2.5V, OUTH pulled to VCC-1.5V

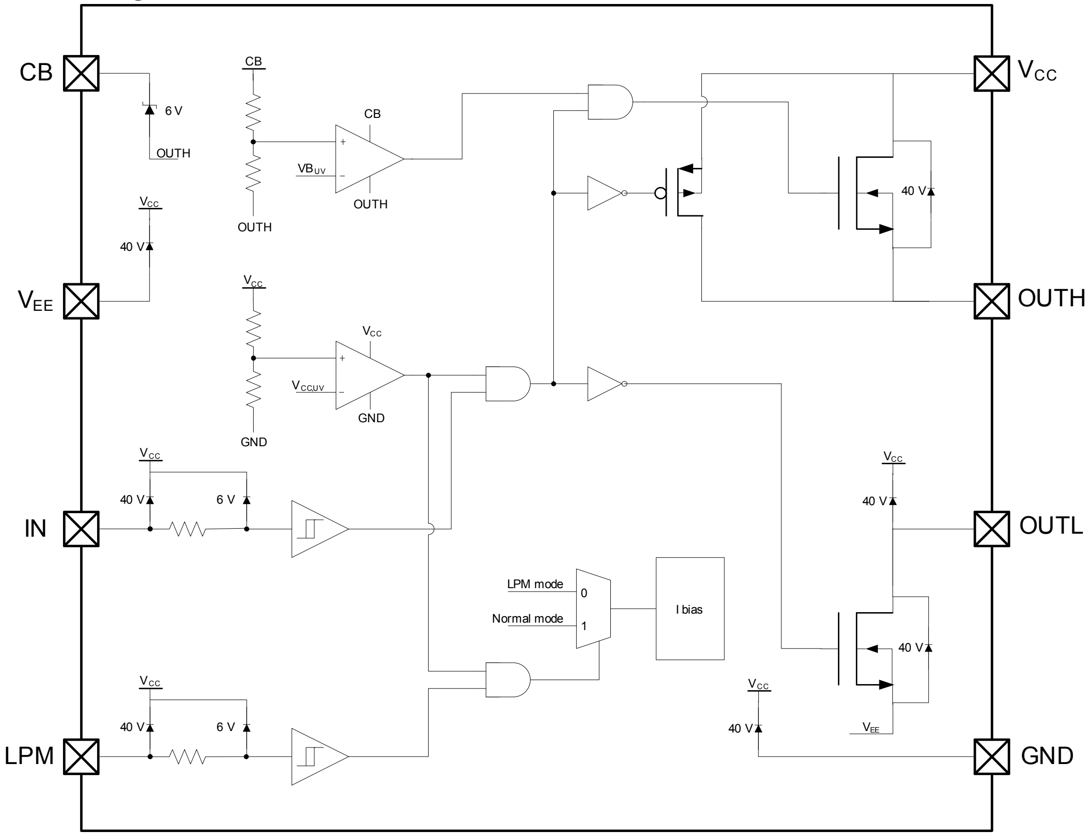
AC Electrical Characteristics

V_{CC} -GND= 15V; GND-V_{EE} =5V; 15nF connects CB to OUTH; 22nF connects Vcc to OUTH ;Ron= 5 Ohm , Roff = 5 Ohm , C_{LOAD}=100nF , -40 °C < T_A < 125 °C unless otherwise specified.
Propagation is from INPUT at GND or V_{CC} to 10% voltage variation of output
RISE FALL TIME is delay from 10% to 90% output swing

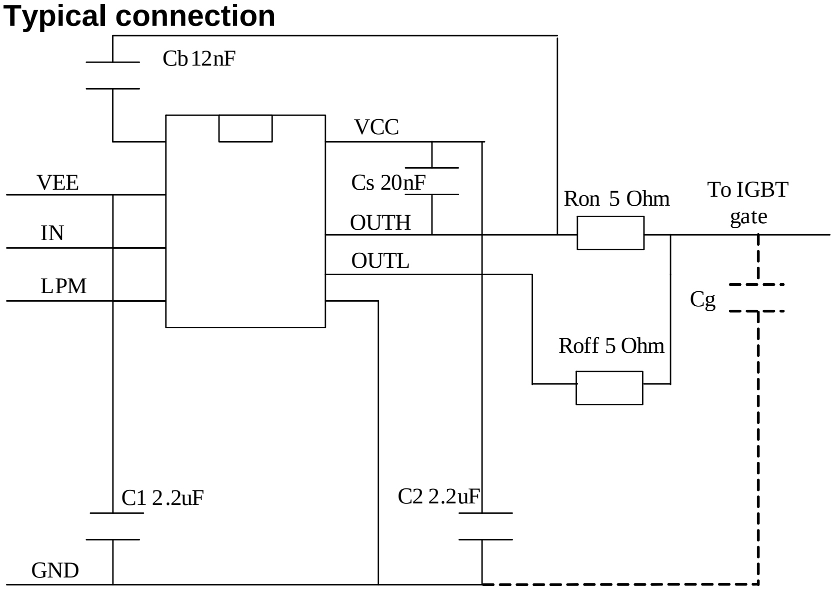
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn on propagation delay IN-OUTH	—	250	400	ns	
t_{off}	Turn off propagation delay IN-OUTL	—	250	350		
t_r	Turn on rise time OUTH	—	—	260		
t_f	Turn off fall time OUTL	—	—	150		
t_{rLQ}	Turn on rise time OUTH in Low Quiescent Currrent Mode	—	—	1000	ns	V_{EE}=GND, LPM=0, V_{CC} rises above V_{CCUV+}; C_{LOAD}=100nF Ron= 5 Ohm, Roff = 5 Ohm
t_{fLQ}	Turn off fall time OUTL in Low Quiescent Currrent Mode	—	—	1000	ns	V_{EE}=GND, LPM=0, V_{CC} falls below V_{CCUV-+}; C_{LOAD}=100nF Ron= 5 Ohm, Roff = 5 Ohm
PW_{ON}	IN high pulse width (*)	500	—	—	ns	No C_{LOAD}, -40 °C < T_A < 125 °C
PW_{OFF}	IN low pulse width (*)	500	—	—	ns	No C_{LOAD}, -40 °C < T_A < 125 °C

(*) IN pulse width lower than PW_{ONMIN} (PW_{OFFMIN}) min can be filtered

Block Diagram:



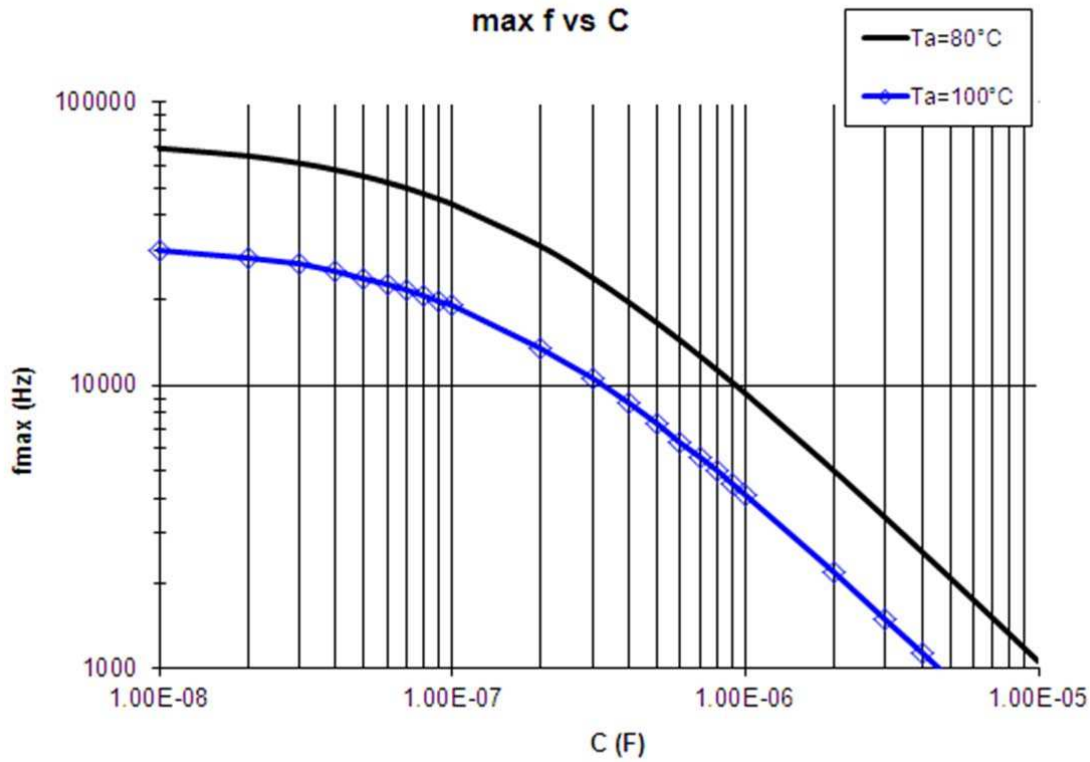
Typical connection



It is recommended:

- to have a capacitance Cs connected between OUTH and VCC to limit dv/dt in OUTH node (mandatory if Vcc-Vee>15V). See Recommended Operating Condition for Cs value.
- to avoid the condition with OUTH directly shorted to OUTL
- Use ceramic capacitor for C1 and C2 with value > 20* Cgate

Application Information And Additional Details



Recommended maximum switching frequency when driving a capacitance C with a 3 Ohm external resistor.
Cs=20nF is connected between OUTH and Vcc.
$Vcc-V_{EE}$=24V.

Truth Table

Vcc	IN	LPM	Status/Comment
$V_{CC\text{-}GND\_MIN}$ to V_{CCUV}	-	-	OUTL = V_{EE}, OUTH in HiZ → IGBT OFF; Low Quiescent Current Mode is active.
V_{CCUV} to 30V	0	1	OUTL = V_{EE}, OUTH in HiZ → IGBT OFF;
V_{CCUV} to 30V	1	1	OUTL in HiZ, OUTH = Vcc → IGBT ON;
V_{CCUV} to 30V	0	0	OUTL = V_{EE}, OUTH in HiZ → IGBT OFF; Low Quiescent Current Mode is active
V_{CCUV} to 30V	1	0	OUTL in HiZ, OUTH = Vcc → IGBT ON; Low Quiescent Current Mode is active

Role of Cboot

Cboot capacitance, connected between OUTH and CB acts as a bootstrap supplying the circuitry driving the low rdson (R_{up_OUTH}) pull-up nmos connected between Vcc and OUTH.
In the application, when IN is low, OUTH is tied to VEE and Cboot is charged to around 6V.
At IN rising the pullup nmos is turned on and it is able to provide a low impedence path between VCC and OUTH.
Mantaining IN high Cboot get discharged and therefore the pullup nmos is turned off but the parallel pmos (see Block diagram) remains on maintaining OUTH tied to VCC.

Examples of system schematics with HVIC

This section shows how IR High Voltage IC (HVIC) gate drivers can be used to drive the AUIR0815.

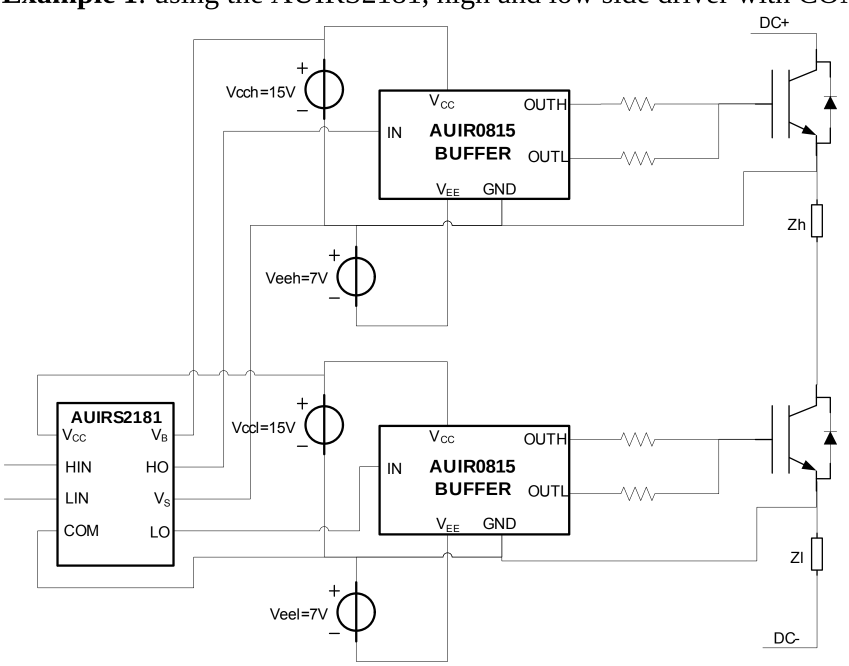
All the examples refer to an inverter leg, showing the floating voltage sources Vcch and Veeh to supply the high side AUIR0815 and Vccl and Veel to supply the low side AUIR0815.

All the examples show 7V floating voltage sources to provide a negative Vge to turn off each IGBT.
In case a negative Vge is not required these voltage sources can be replaced with a short circuit.

In case of three phase inverters, each of the high side AUIR0815 must have separated and isolated voltage supplies.
Only one DC power supply can be shared for the low sides AUIR0815 supplies (to be connected between AUIR0815 Vcc and GND pins) and the corresponding drivers supplies (to be connected between HVIC Vcc and Vss=COM) pins.

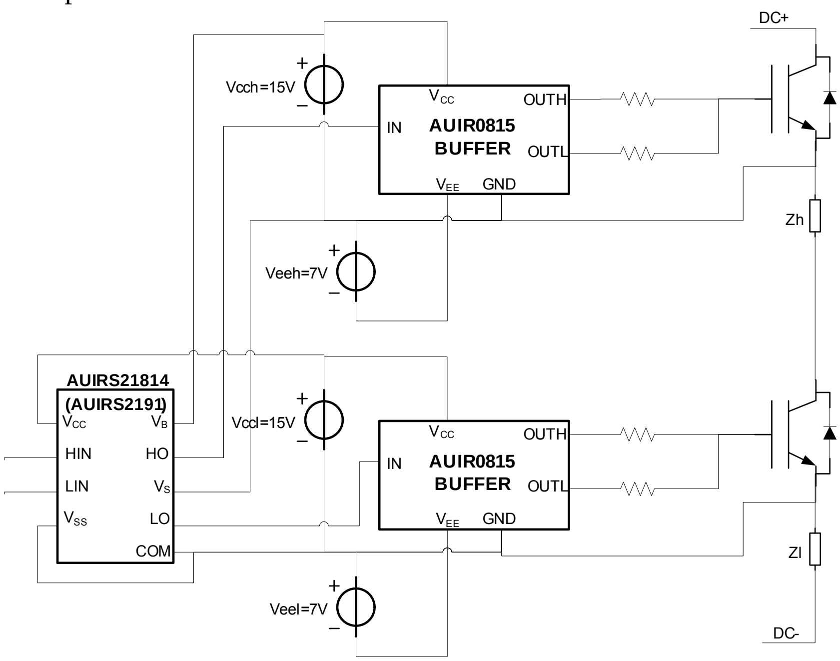
Normally high di/dt occurs at low side switch turn on. This causes voltage spikes at low side IGBT emitter node, because of the inductive impedance Zl, and the system must be robust to this.
A better immunity to the above transients can be obtained using one separate low side DC power supply for each low side.

Example 1: using the AUIRS2181, high and low side driver with COM and no VSS pin.



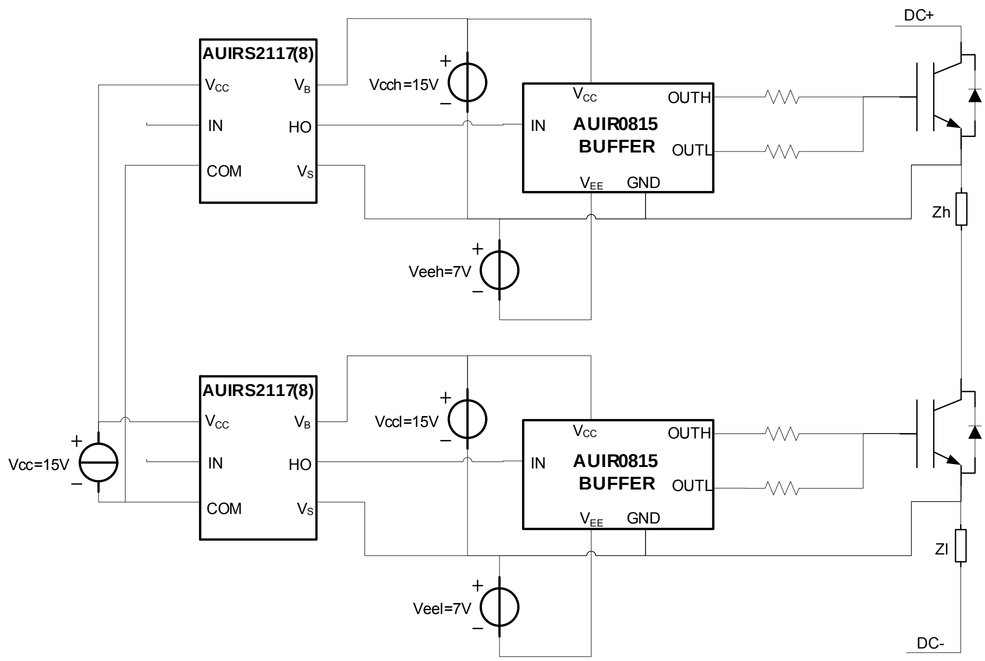
Example 1

Example 2: using the AUIRS21814 (or the AUIRS2191), high and low side driver with COM pin and VSS pin.



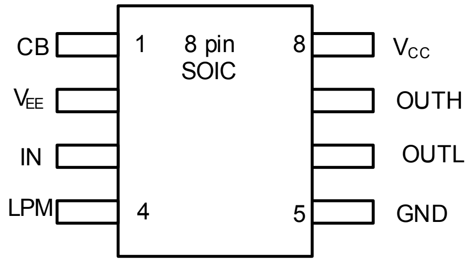
Example 2

Example 3: using the AUIRS2117(8), single channel driver.
COM can be shorted to the Vs of the low side.



Example 3

Lead Assignments

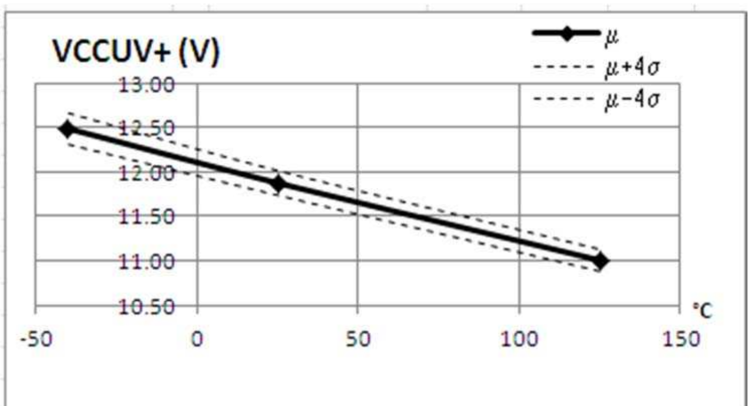


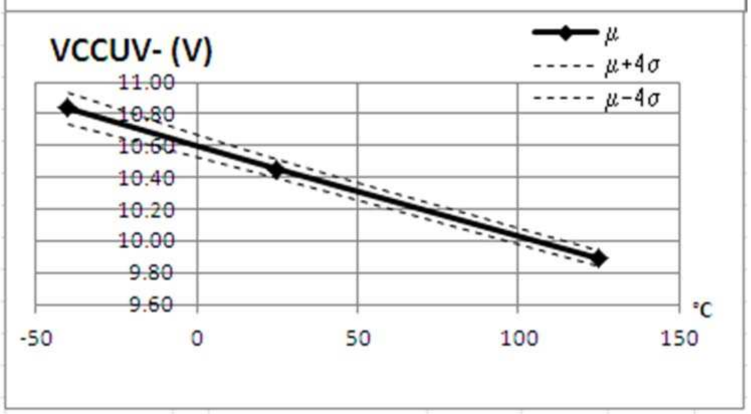
Lead Definitions

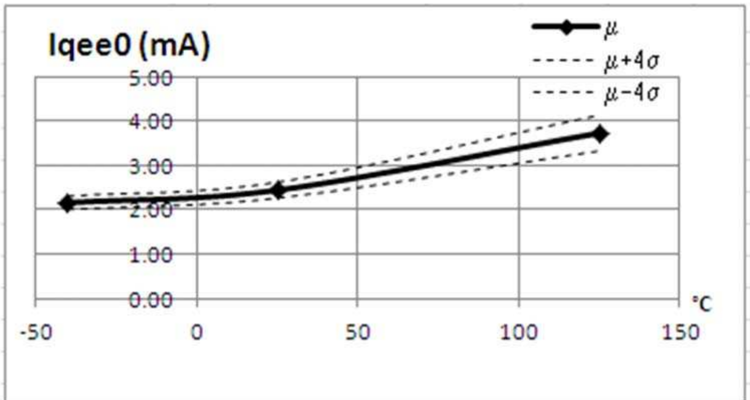
Symbol	Description
V_{CC}	Positive supply
IN	Logic input for OUT
LPM	Logic input, for Low Power Mode: LPM=0 activates the Low Quiescent Current Mode
GND	Ground
OUTH	Power Output (pull up)
OUTL	Power Output (pull down)
C_B	Boot capacitor
V_{EE}	Negative supply pin (short to GND in case of single supply operation)

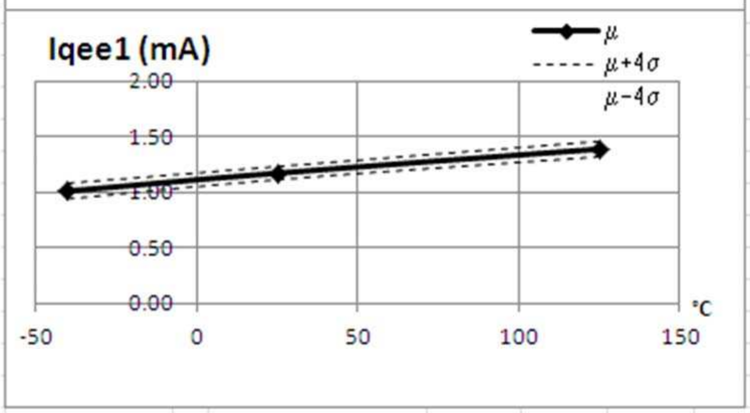
Parameter Temperature Trends

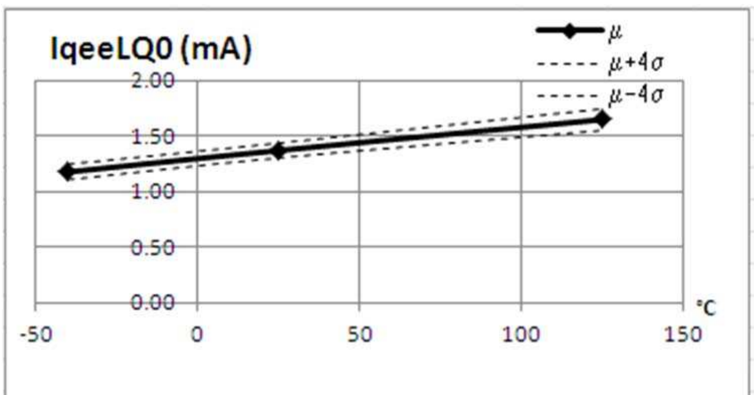
Figures illustrated in this chapter provide information on the experimental performance of the IC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

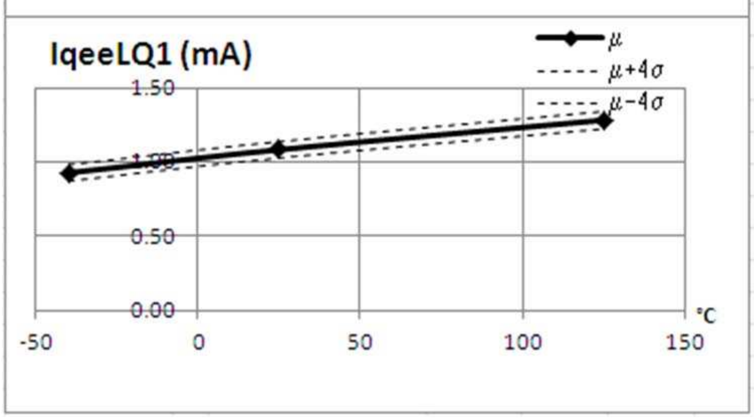


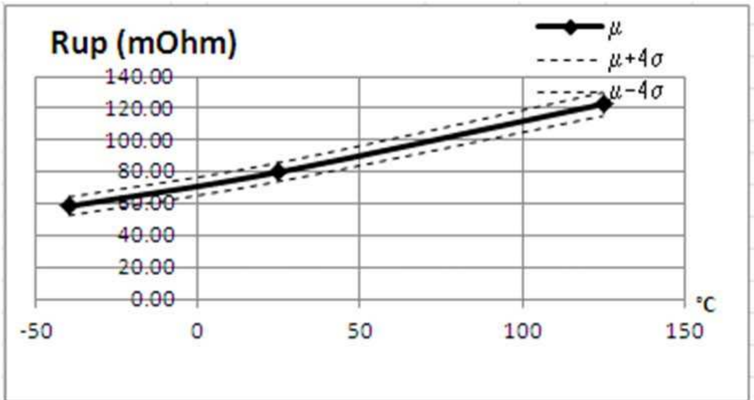


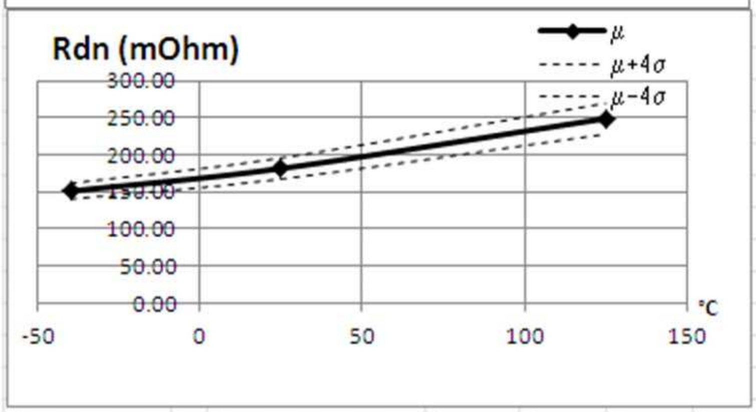

Iqee0 (mA)
μ
μ+4σ
μ-4σ
5.00
4.00
3.00
2.00
1.00
0.00
-50
0
50
100
150
°C

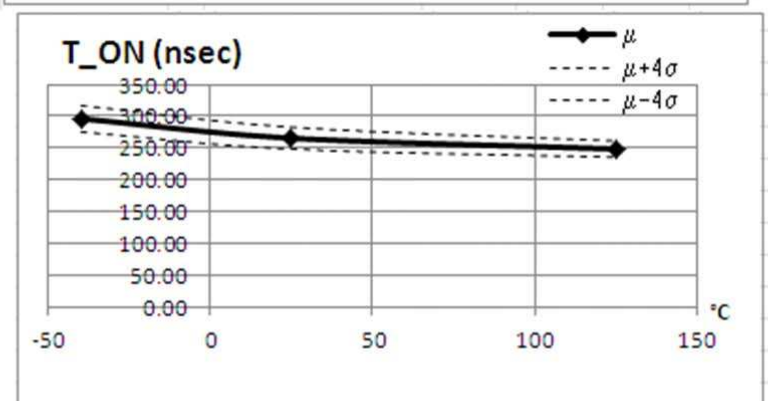

Iqee1 (mA)
μ
μ+4σ
μ-4σ
2.00
1.50
1.00
0.50
0.00
-50
0
50
100
150
°C

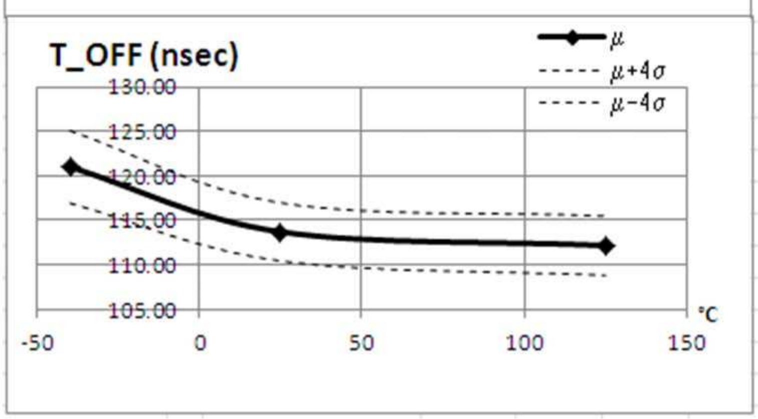

IqeeLQ0 (mA)
μ
μ+4σ
μ-4σ
2.00
1.50
1.00
0.50
0.00
-50
0
50
100
150
°C


IqeeLQ1 (mA)
μ
μ+4σ
μ-4σ
1.50
1.00
0.50
0.00
-50
0
50
100
150
°C


Rup (mOhm)
μ
μ+4σ
μ−4σ
140.00
120.00
100.00
80.00
60.00
40.00
20.00
0.00
-50
0
50
100
150
°C


Rdn (mOhm)
μ
μ+4σ
μ−4σ
300.00
250.00
200.00
150.00
100.00
50.00
0.00
-50
0
50
100
150
°C

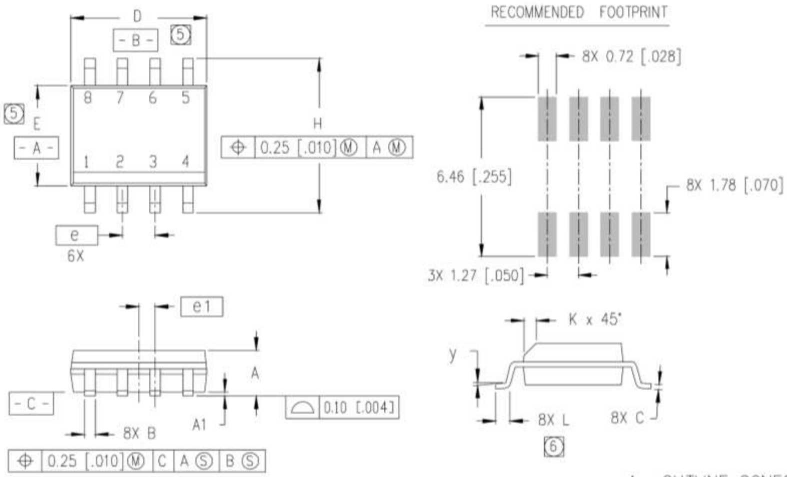

T_ON (nsec)
μ
μ+4σ
μ−4σ
350.00
300.00
250.00
200.00
150.00
100.00
50.00
0.00
-50
0
50
100
150
°C


T_OFF (nsec)
μ
μ+4σ
μ−4σ
130.00
125.00
120.00
115.00
110.00
105.00
-50
0
50
100
150
°C

International IOR Rectifier

AUIR0815S

Case Outline



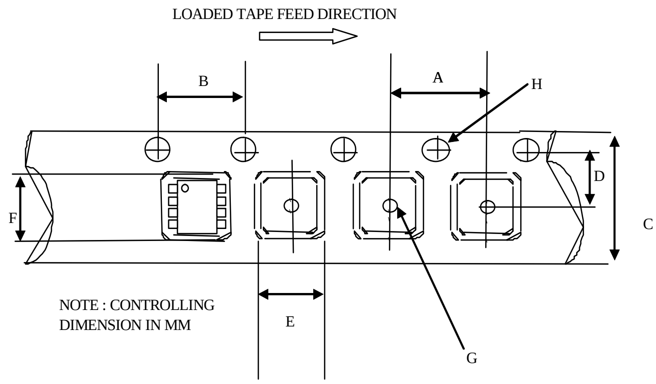
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

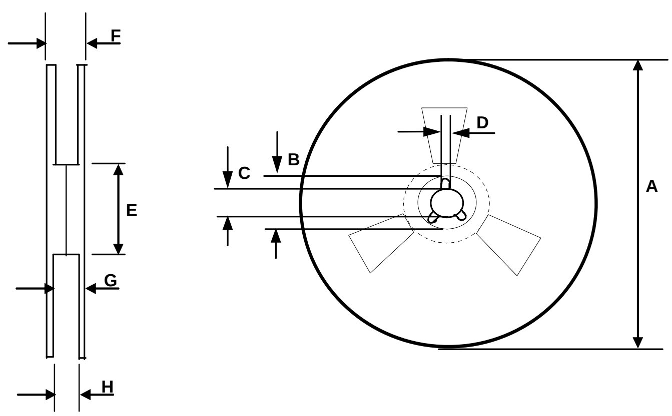
8 Lead SOIC

Tape and Reel: SOIC8



CARRIER TAPE DIMENSION FOR 8SOICN

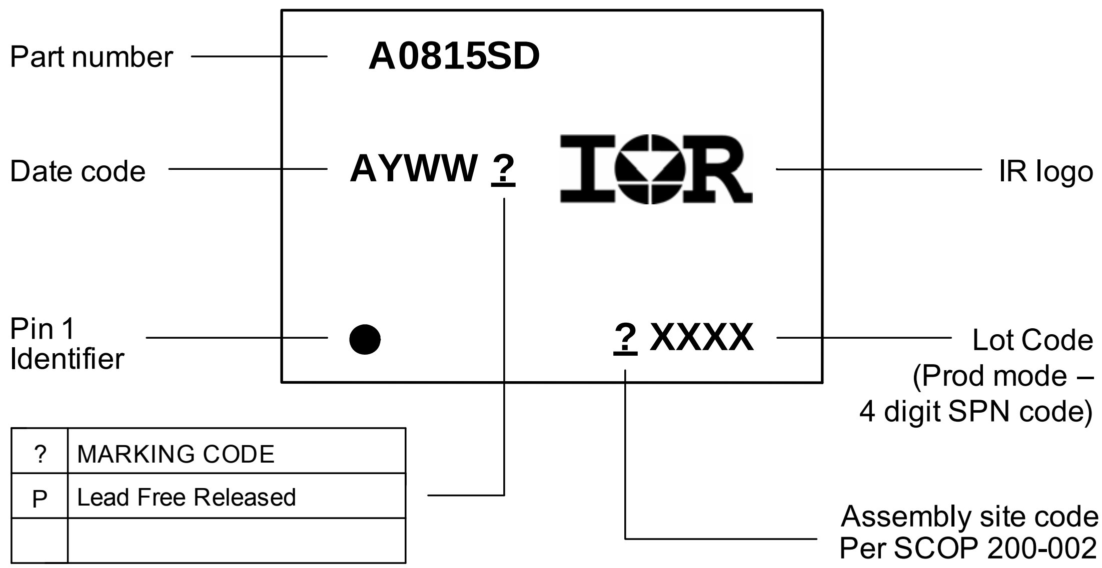
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIR0815S	SOIC8	Tube/Bulk	95	AUIR0815S
		Tape and Reel	2500	AUIR0815STR

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