To request the full datasheet, please visit www.intersil.com/products/isl94212

Multi-Cell Li-Ion Battery Manager

ISL94212

The ISL94212 Li-ion battery manager IC supervises up to 12 series connected cells. The part provides accurate monitoring, cell balancing and extensive system diagnostics functions. Three cell balancing modes are provided: Manual Balancing mode, Timed Balancing mode and Auto Balance mode. The Auto Balance mode terminates balancing functions when a charge transfer value has been met.

The ISL94212 communicates to a host microcontroller via an SPI interface and to other ISL94212 devices using a robust, proprietary, two-wire Daisy Chain system.

The ISL94212 is offered in a 64 Ld TQFP package and is specified for an operational temperature range of -40°C to +85°C.

Applications

- Light electric vehicle (LEV); E-Moto; E-Bike
- Battery backup systems; Energy Storage Systems (ESS)
- Solar Farms
- Portable and semi-portable equipment

Features

- Up to 12-cell voltage monitors, support Li-Ion CoO_2, Li-ion Mn_2O_4, and Li-ion FePO4 chemistries
- Cell voltage measurement accuracy ±10mV
- 13-bit cell voltage measurement
- Pack voltage measurement accuracy ±180mV
- 14-bit pack voltage and temperature measurements
- Cell voltage scan rate of 19.5µs per cell (234µs to scan 12 cells)
- Internal temperature monitoring
- Up to four external temperature inputs
- Robust daisy chain communications system
- Integrated system diagnostics for all key internal functions
- Hardwired and communications based fault notification
- Integrated watchdog shuts down device if communication is lost
- 7µA shutdown current: Enable = V_{SS}
- 2Mbps SPI

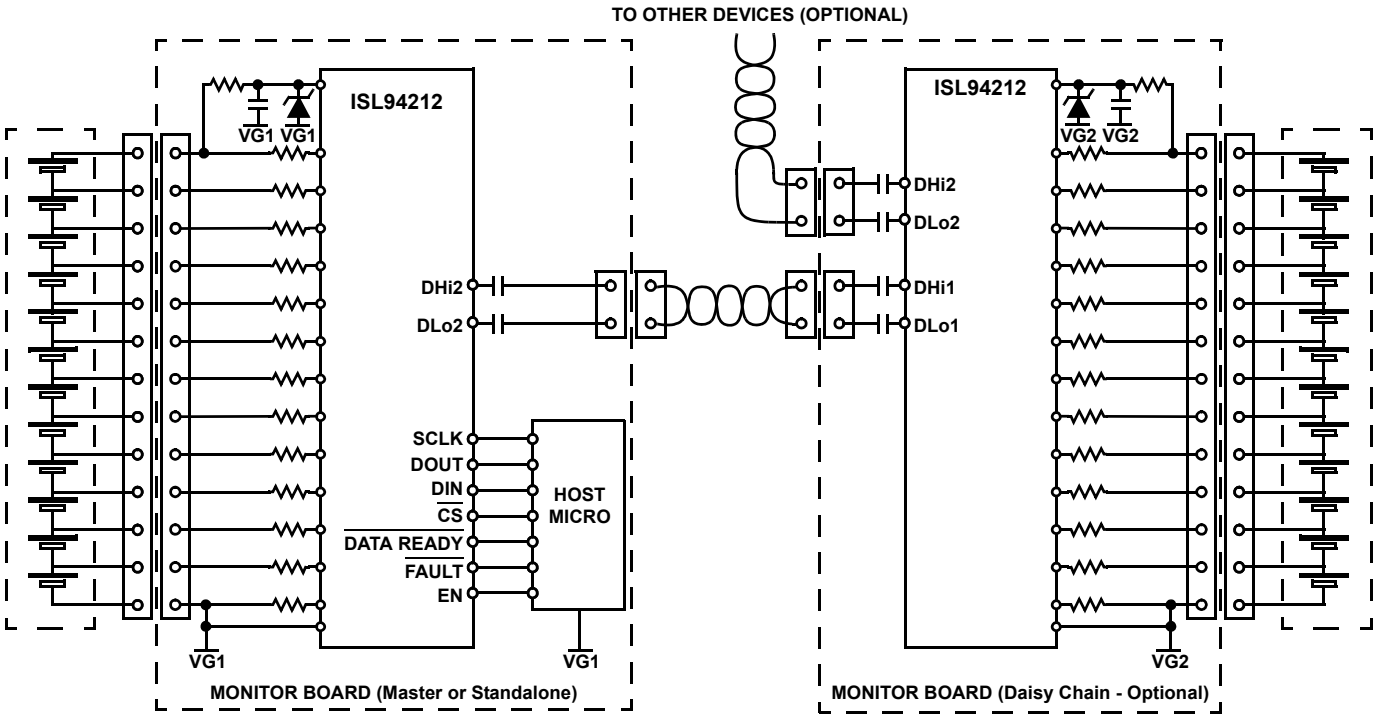

FIGURE 1. TYPICAL APPLICATION

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Ordering Information

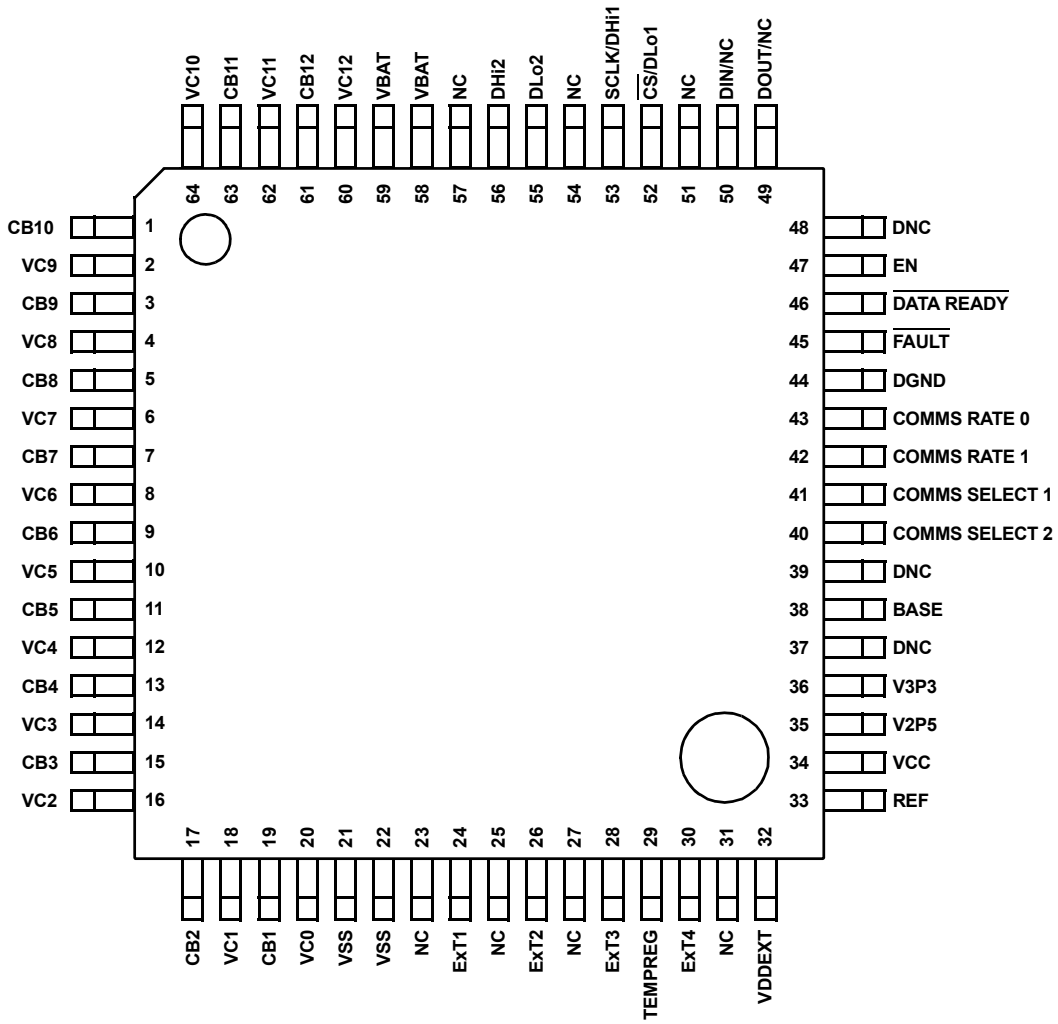
PART NUMBER (Notes 2, 3, 4)	PART MARKING	TRIM VOLTAGE, V_{NOM} (V)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL94212INZ (Note 1)	ISL94212INZ	3.3	-40 to +85	64 Ld TQFP	Q64.10x10D
ISL94212EVKIT1Z	Evaluation Kit				

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level Rating (MSL) for the package, please see the Intersil ISL94212. For more information on handling and processing moisture sensitive devices, please see Techbrief TB363.
4. For other trim options, please contact Marketing.

Pin Configuration

ISL94212
(64 LD 10x10 TQFP)
TOP VIEW



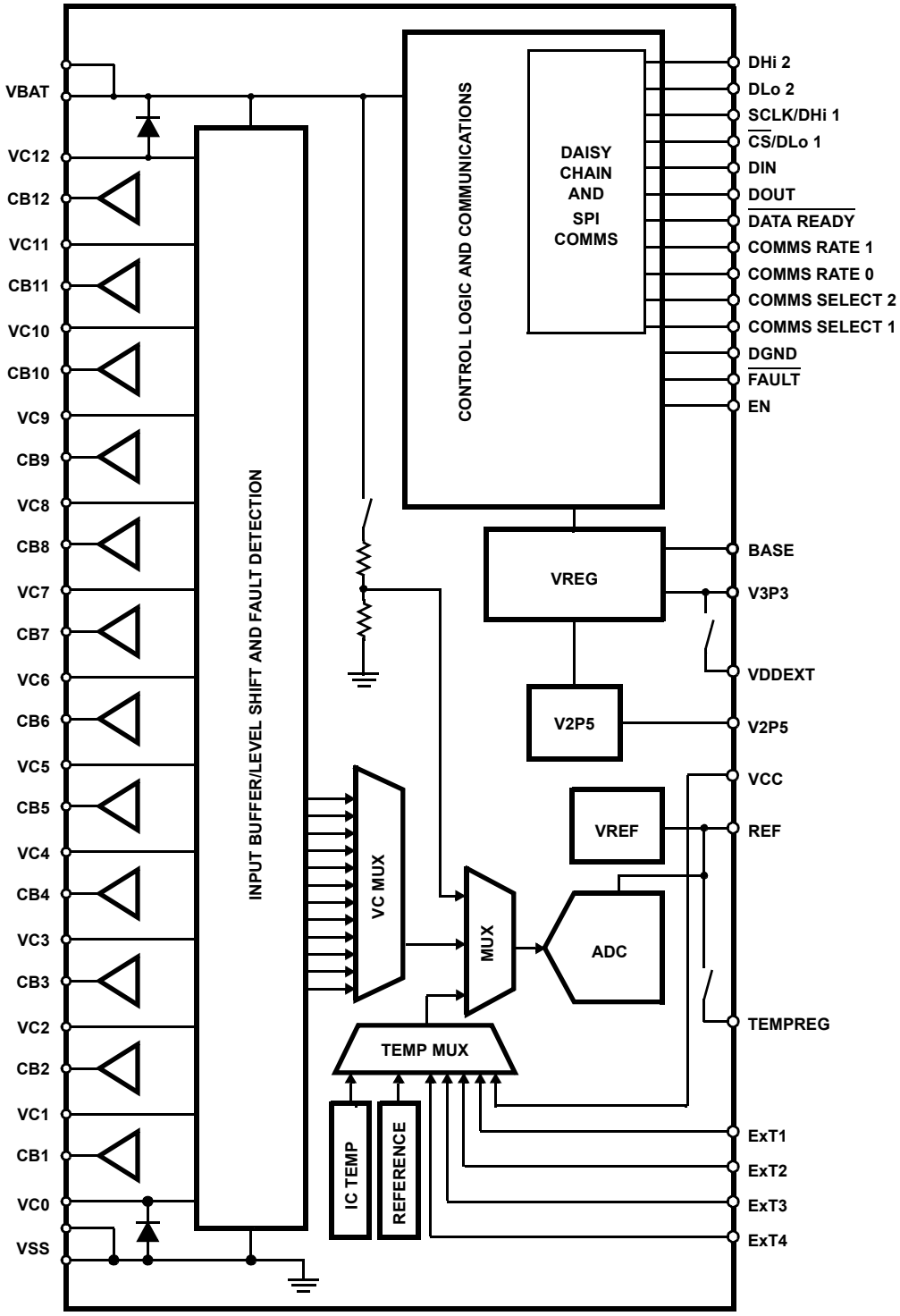
Pin Descriptions

SYMBOL	PIN NUMBER	DESCRIPTION
VC0, VC1, VC2, VC3, VC4, VC5, VC6, VC7, VC8, VC9, VC10, VC11, VC12	20, 18, 16, 14, 12, 10, 8, 6, 4, 2, 64, 62, 60	Battery cell voltage inputs. VCn connects to the positive terminal of CELLn and the negative terminal of CELLn+1. (VC12 connects only to the positive terminal of CELL12 and VC0 only connects with the negative terminal of CELL1.)
CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12	19, 17, 15, 13, 11, 9, 7, 5, 3, 1, 63, 61	Cell Balancing FET control outputs. Each output controls an external FET which provides a current path around the cell for balancing.
VBAT	58, 59	Main IC Supply pins. Connect to the most positive terminal in the battery string.
VSS	21, 22	Ground. These pins connect to the most negative terminal in the battery string.
ExT1, ExT2, ExT3, ExT4	24, 26, 28, 30	External temperature monitor or general purpose inputs. The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but may also be used as general purpose analog inputs at the user's discretion. 0V to 2.5V input range.
TEMPREG	29	Temperature monitor voltage regulator output. This is a switched 2.5V output, which supplies a reference voltage to external NTC thermistor circuits to provide ratiometric ADC inputs for temperature measurement.

Pin Descriptions (Continued)

SYMBOL	PIN NUMBER	DESCRIPTION
VDDEXT	32	External V3P3 supply input/output. Connected to the V3P3 pin via a switch, this pin may be used to power external circuits from the V3P3 supply. The switch is open when the ISL94212 is placed in **Sleep mode**.
REF	33	2.5V voltage reference decoupling pin. Connect a 2.0µF to 2.5µF X7R capacitor to VSS. Do not connect any additional external load to this pin.
VCC	34	Analog supply voltage input. Connect to V3P3 via a 33Ω resistor. Connect a 1µF capacitor to ground.
V2P5	35	Internal 2.5V digital supply decoupling pin. Connect a 1µF capacitor to DGND.
V3P3	36	3.3V digital supply voltage input. Connect the emitter of the external NPN regulator transistor to this pin. Connect a 1µF capacitor to DGND.
Base	38	Regulator control pin. Connect the external NPN transistor's base. Do not let this pin float,
DNC	37, 39, 48	Do not connect. Leave pins floating.
Comms Select 1	41	Communications port 1 mode select pin. Connect via a 1kΩ resistor to V3P3 for Daisy Chain communications on port 1 or to DGND for SPI operation on port 1.
Comms Select 2	40	Communications port 2 mode select pin. Connect via a 1kΩ resistor to V3P3 to enable port 2 or to DGND to disable this port.
Comms Rate 0, Comms Rate 1	43, 42	Daisy Chain communications data rate setting. Connect via a 1kΩ resistor to DGND ('0') or to V3P3 ('1') to select between various communication data rates.
DGND	44	Digital Ground.
$\overline{\text{Fault}}$	45	Logic fault output. Asserted low if a fault condition exists.
$\overline{\text{Data Ready}}$	46	SPI data ready. Asserted low when the device is ready to transmit data to the host microcontroller.
EN	47	Enable input. Tie to V3P3 to enable the part. Tie to DGND to disable (all IC functions are turned off).
DOUT/NC	49	Serial Data Output (SPI) or NC (Daisy Chain). 0V to 3.3V push-pull output.
DIN/NC	50	Serial Data Input (SPI) or NC (Daisy Chain). 0V to 3.3V input.
$\overline{\text{CS}}$/DLo1	52	Chip-Select, active low 3.3V input (SPI) or Daisy Chain port 1 Lo connection.
SCLK/DHi1	53	Serial-Clock Input (SPI) or Daisy Chain port 1 Hi connection.
DHi2	56	Daisy Chain port 2 Hi connection.
DLo2	55	Daisy Chain port 2 Lo connection.
NC	23, 25, 27, 31, 51, 54, 57	No internal connection.

Block Diagram



Absolute Maximum Ratings

Unless otherwise specified. With respect to VSS.

DIN, SCLK, $\overline{CS}$, DOUT, $\overline{Data\ Ready}$, Comms Select n, ExTn, TEMPREG, REF, V3P3, VCC, $\overline{Fault}$, Comms Rate n, Base, EN, VDDEXT. . . . . -0.2V to 4.1V
V2P5. . . . . -0.2V to 2.9V
VBAT . . . . . -0.5V to 63V
Dhi1, DLo1, DHi2, DLo2 . . . . . -0.5V to (VBAT + 0.5V)
VC0 . . . . . -0.5V to + 9.0V
VC1 . . . . . -0.5V to + 18V
VC2 . . . . . -0.5V to + 18V
VC3 . . . . . -0.5V to + 27V
VC4 . . . . . -0.5V to + 27V
VC5 . . . . . -0.5V to + 36V
VC6 . . . . . -0.5V to + 36V
VC7 . . . . . -0.5V to + 45V
VC8 . . . . . -0.5V to + 45V
VC9 . . . . . -0.5V to + 54V
VC10 . . . . . -0.5V to + 63V
VC11 . . . . . -0.5V to + 63V
VC12 . . . . . -0.5V to + 63V
VCn (for n = 0 to 12). . . . . -0.5 to VBAT + 0.5V
CBn (for n = 1 to 12) . . . . . -0.5 to VBAT + 0.5V
CBn (for n = 1 to 9) . . . . . V(VCn-1) - 0.5V to V(VCn-1) + 9V
CBn (for n = 10 to 12). . . . . V(VCn) - 9V to V(VCn) + 0.5V
Current into VCn, VBAT, VSS (Latch up Test) . . . . . ±100mA
ESD Rating
  Human Body Model (Tested per JESD22-A114F) 2kV
  Machine Model (Tested per JESD22A115-A) 200V
  Charge Device Model (Tested per JESD22-C101D) 750V
Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

NOTE: DOUT, $\overline{Data\ Ready}$, and $\overline{Fault}$ are digital outputs and should not be driven from external sources. V2P5, REF, TEMPREG and BASE are analog outputs and should not be driven from external sources.

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (C/W)	θ_{JC} (C/W)
64 Ld TQFP Package (Notes 5, 6)	42	9

Max Continuous Package Power Dissipation 400mW
Storage Temperature . . . . . -55°C to +125°C
Max Operating Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

T_A, Ambient Temperature Range . . . . . -40°C to +85°C
V_{BAT} . . . . . 6V to 60V
V_{BAT} (Daisy Chain Operation) . . . . . 10V to 60V
VCn (for n = 1 to 12) . . . . . V(VCn-1) to V(VCn-1) + 5V
VC0 . . . . . -0.1V to 0.1V
CBn (for n = 1 to 9) . . . . . V(VCn-1) to V(VCn-1) + 9V
CBn (for n = 10 to 12). . . . . V(VCn) - 9V to V(VCn)
DIN, SCLK, $\overline{CS}$, DOUT, $\overline{Data\ Ready}$, Comms Select 1, Comms Select 2, TEMPREG, REF, V3P3, VCC, $\overline{Fault}$, Comms Rate 0, Comms Rate 1, EN, VDDEXT. . . . . 0V to 3.6V
ExT1,ExT2,ExT3,Ext4 . . . . . 0V to 2.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Power-up Condition Threshold	V_{POR}	V_{BAT} voltage (rising)	**4.8**	5.1	**5.6**	V
Power-up Condition Hysteresis	V_{PORhys}			400		mV
Initial Power-up Delay	t_{POR}	Time after VPOR condition V_{REF} from 0V to 0.95 x V_{REF}(nom) (EN tied to V3P3) Device can now communicate			**27.125**	ms
Enable Pin Power-up Delay	t_{PUD}	Delay after EN = 1 to V_{REF} from 0V to 0.95 x V_{REF}(nom) (V_{BAT} = 39.6V) - Device can now communicate			**27.125**	ms

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{BAT} Supply Current	I_{VBAT}	Non-daisy chain configuration. Device enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	**10**	35	**75**	µA
			39.6V	**10**	64	**220**	µA
			60V	**10**	90	**230**	µA
	$I_{VBATMASTER}$	Daisy chain configuration – master device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	**400**	530	**660**	µA
			39.6V	**500**	680	**900**	µA
			60V	**550**	750	**1000**	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATMID}$	Daisy chain configuration – mid stack device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	**700**	1020	**1300**	µA
			39.6V	**900**	1250	**1600**	µA
			60V	**1000**	1400	**1700**	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATTOP}$	Daisy chain configuration – top device. Enabled. No communications, ADC, measurement, balancing or open wire detection activity.	6V	**400**	530	**660**	µA
			39.6V	**500**	680	**900**	µA
			60V	**550**	750	**1000**	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATSLEEP1}$	Sleep mode (EN = 1, daisy chain configuration).		**10**	19	**36**	µA
	$I_{VBATSLEEP2}$	Sleep mode (EN = 1, standalone, non-daisy chain)		**5**	9	**18**	µA
	$I_{VBATSHDN}$	Shutdown. device “off” (EN = 0) (daisy chain and non-daisy chain configurations)		**5**	7	**18**	µA
V_{BAT} Supply Current Tracking. Sleep Mode.	$I_{VBATΔSLEEP}$	EN = 1, daisy chain sleep mode configuration. V_{BAT} current difference between any two devices operating at the same temperature and supply voltage.		**0**		**10.5**	µA
V_{BAT} Incremental Supply Current, Balancing	$I_{VBATBAL}$	All balancing circuits on. Incremental current: Add to non-balancing V_{BAT} current. V_{BAT} = 39.6V		**200**	300	**400**	µA
V3P3 Regulator Voltage (Normal)	V_{3P3N}	EN = 1, load current range 0 to 5 mA. V_{BAT} = 39.6V		**3.2**	3.35	**3.5**	V
V3P3 Regulator Voltage (Sleep)	V_{3P3S}	EN = 1, load current range. No load. (SLEEP). V_{BAT} = 39.6V		**2.4**	2.7	**3.05**	V
V3P3 Regulator Control Current	I_{Base}	Current sourced from base output. V_{BAT} = 6V		**1**	1.5		mA
V3P3 Supply Current	I_{V3P3}	Device enabled No measurement activity, normal mode		**0.8**	1	**1.3**	mA
V_{REF} Reference Voltage	V_{REF}	EN = 1, no load, normal mode			2.5		V

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
VDDEXT Switch Resistance	R_{VDDEXT}	Switch ON-resistance, V_{BAT} = 39.6V	**5**	12	**22**	Ω
VCC Supply Current	I_{VCC}	Device enabled (EN = 1). Standalone or daisy configuration. No ADC or daisy chain communications active.	**2.0**	3.25	**5.0**	mA
	$I_{VCCACTIVE1}$	Device enabled (EN = 1). Standalone or daisy configuration. Average current during 16ms scan continuous operation. V_{BAT} = 39.6V		6.0		mA
	$I_{VCCSLEEP}$	Device enabled (EN = 1). Sleep mode. V_{BAT} = 39.6V		2.4		µA
	$I_{VCCSHDN}$	Device disabled (EN = 0). Shutdown mode.	**0**	1.2	**9.0**	µA
MEASUREMENT SPECIFICATIONS						
Cell Voltage Input Measurement Range	V_{CELL}	VC(N) - VC(N-1). For design reference.	**0**		**5**	V
Cell Monitor Voltage Resolution	$V_{CELLRES}$	[VC(N)-VC(N-1)] LSB step size (13-bit signed number), 5V full scale value		0.61		mV
ISL94212 Cell Monitor Voltage Error (Absolute)	ΔV_{CELLA}	Absolute cell measurement error (Cell measurement error compared with applied voltage with 1k series resistor.) Temperature = 0°C to +50°C, V_{CELL} = 2.6V to 4.0V	-10		10	mV
		Temperature = +50°C to +85°C, V_{CELL} = 2.0V to 4.3V	-25		25	mV
		Temperature = -40°C to 0°C, V_{CELL} = 2.0V to 4.3V	-35		35	mV
ISL94212 Cell Monitor Voltage Error (Relative)	ΔV_{CELLB}	Relative cell measurement error (Max absolute cell measurement error Min absolute cell measurement error) Temperature = 0°C to +50°C	0		7.5	mV
		Temperature = -40°C to 0°C	0		7.5	mV
		Temperature = +50°C to +85°C	0		20	mV
Cell Input Current. Note: Cell accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12)	I_{VCELL}	VC0 input	**-2.0**	-1	**-0.5**	µA
		VC1, VC2, VC3 inputs	**-3.0**	-2	**-0.9**	µA
		VC4 input	**-0.8**	0	**0.9**	µA
		VC5, VC6, VC7, VC8, VC9, VC10, VC11 inputs	**0.5**	2	**3.2**	µA
		VC12 input	**0.4**	1	**2.0**	µA
V_{BAT} Monitor Voltage Resolution	$VBAT_{RES}$	ADC resolution referred to input (V_{BAT}) level. 14b unsigned number. Full scale value = 79.67V.		4.863		mV
V_{BAT} Monitor Voltage Error	ΔV_{BAT}	Temperature = 0°C to +50°C, Measured at V_{BAT} = 31.2V to 43.2V	-180		180	mV
		Temperature = 0°C to +50°C, Measured at V_{BAT} = 24V to 48V	-230		230	mV
		Temperature = 0°C to +50°C, Measured at V_{BAT} = 6V to 59.4V	-390		390	mV
		Temperature = -40°C to +85°C, Measured at V_{BAT} = 31.2V to 39.6V	-320		320	mV
		Temperature = -40°C to +85°C, Measured at V_{BAT} = 6V to 48V	-440		440	mV
		Temperature = -40°C to +85°C, Measured at V_{BAT} = 6V to 59.4V	-650		650	mV

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
External Temperature Monitoring Regulator	V_{TEMP}	Voltage on TEMPREG output. (0 to 2mA load)	**2.475**	2.5	**2.525**	V
External Temperature Output Impedance	R_{TEMP}	Output impedance at TEMPREG pin.	**0**	0.1	**0.2**	Ω
External Temperature Input Range	V_{EXT}	ExTn input voltage range. For design reference.	**0**		**2344**	mV
External Temperature Input Pull-up	$R_{EXTTEMP}$	Pull-up resistor to $V_{TEMPREG}$ applied to each input during measurement		10		MΩ
External Temperature Input Offset	V_{EXTOFF}	V_{BAT} = 39.6V	**-12**		**12**	mV
External Temperature Input INL	V_{EXTINL}		**-0.65**		**0.65**	mV
External Temperature Input Gain Error	V_{EXTG}		**-8**		**18.5**	mV
Internal Temperature Monitor Error	V_{INTMON}			±10		°C
Internal Temperature Monitor Resolution	T_{INTRES}	Output resolution (LSB/°C). 14b number.		31.9		LSB/°C
Internal Temperature Monitor Output	T_{INT25}	Output count at +25°C		9180		Decimal
OVER-TEMPERATURE PROTECTION SPECIFICATIONS						
Internal Temperature Limit Threshold	T_{INTSD}	Balance stops and auto scan stops. Temperature rising or falling.		150		°C
External Temperature Limit Threshold	T_{XT}	Corresponding to 0V (min) and $V_{TEMPREG}$ (max) External temperature input voltages higher than 15/16 $V_{TEMPREG}$ are registered as open input faults.	**0**		**16383**	Decimal
FAULT DETECTION SYSTEM SPECIFICATIONS						
Undervoltage Threshold	V_{UV}	Programmable. Corresponding to 0V (min) and 5V (max)	**0**		**8191**	Decimal
Overvoltage Threshold	V_{OV}	Programmable. Corresponding to 0V (min) and 5V (max)	**0**		**8191**	Decimal
V3P3 Power-good Window	V_{3PH}	3.3V Power-good window high threshold. V_{BAT} = 39.6V	**3.7**	3.90	**4.05**	V
	V_{3PL}	3.3V Power-good window low threshold. V_{BAT} = 39.6V	**2.5**	2.65	**2.8**	V
V2P5 Power-good Window	V_{2PH}	2.5V Power-good window high threshold. V_{BAT} = 39.6V	**2.55**	2.7	**2.9**	V
	V_{2PL}	2.5V Power-good window low threshold. V_{BAT} = 39.6V	**1.90**	2.0	**2.15**	V
VCC Power-good Window	V_{VCCH}	VCC Power-good window high threshold. V_{BAT} = 39.6V	**3.6**	3.75	**4.0**	V
	V_{VCCL}	VCC Power-good window low threshold. V_{BAT} = 39.6V	**2.55**	2.7	**2.85**	V
V_{REF} Power-good Window	V_{RPH}	V_{REF} Power-good window high threshold. V_{BAT} = 39.6V	**2.525**	2.7	**2.9**	V
	V_{RPL}	V_{REF} Power-good window low threshold. V_{BAT} = 39.6V	**2.0**	2.30	**2.50**	V

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{REF} Reference Accuracy Error	V_{RACC}	V_{REF} value calculated using stored coefficients. V_{BAT} = 39.6V, V_{REF} typical = 2.5V (See "Voltage Reference Check Calculation" on page 62.) Temperature = 0°C to +50°C	-15		15	mV
		Temperature = -40°C to 0°C	-40		40	mV
		Temperature = +50°C to +85°C	-22		22	mV
Voltage Reference Check Timeout	t_{VREF}	Time to check voltage reference value from power-on, enable or wake up		20		ms
Oscillator Check Timeout	t_{OSC}	Time to check main oscillator frequency from power-on, enable or wake up		20		ms
Oscillator Check Filter Time	t_{OSCF}	Minimum duration of fault required for detection		100		ms
CELL OPEN WIRE DETECTION (See sections "Scan Wires" on page 22, "ISCN, PIN37, PIN39" on page 30, and "Open Wire Test" on page 35.)						
Open Wire Current	I_{OW}	ISCN bit = 0; V_{BAT} = 39.6V	**0.125**	0.15	**0.175**	mA
		ISCN bit = 1; V_{BAT} = 39.6V	**0.85**	1.0	**1.15**	mA
Open Wire Detection Time	t_{OW}	Open wire current source "on" time		4.6		ms
Open VC0 Detection Threshold	V_{VC0}	CELL1 negative terminal (with respect to VSS) V_{BAT} = 39.6V	**1.2**	1.5	**1.8**	V
Open VC1 Detection Threshold	V_{VC1}	CELL1 positive terminal (with respect to VSS) V_{BAT} = 39.6V	**0.6**	0.7	**0.8**	V
Primary Detection Threshold, VC2 to VC12	V_{VC2_12P}	V(VC(n - 1)) - V(VCn), n = 2 to 12 V_{BAT} = 39.6V	**-2**	-1.5	**0**	V
Secondary Detection Threshold, VC2 to VC12	V_{VC2_12S}	Via ADC. VC2 to VC12 only V_{BAT} = 39.6V	**-100**	-30	**50**	mV
Open V_{BAT} Fault Detection Threshold	V_{VBO}	VC12 - V_{BAT}		200		mV
Open VSS Fault Detection Threshold	V_{VSSO}	VSS - VC0		250		mV
MEASUREMENT FUNCTION TIMING (Note 8)						
Cell Sample Time Start		Time to sample the first cell (CELL12) following $\overline{CS}$ going High. Scan voltages command		65	**71.5**	µs
Cell Sample Time Duration		Time to scan all 12 cells (sample of CELL12 to sample of CELL1) scan voltages command.		233	**257**	µs
Scan Voltages Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		770	**847**	µs
Scan Temperatures Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		2690	**2959**	µs
Scan Mixed Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		830	**913**	µs
Scan Wires Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		59.4	**65.3**	ms
Scan All Processing Time		Time from start of scan to registers loaded to $\overline{DATA\ READY}$ going low		63.2	**69.5**	ms

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Measure Cell Voltage Processing Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		180	**198**	µs
Measure V_{BAT} Voltage Processing Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		130	**143**	µs
Measure Internal Temperature Processing Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		110	**121**	µs
Measure External Temperature Input Processing Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		2520	**2772**	µs
Measure Secondary Voltage Reference Time		Time from start of measurement to register(s) loaded to $\overline{\text{DATA READY}}$ going low		2520	**2772**	µs
CELL BALANCE OUTPUT SPECIFICATIONS						
Cell Balance Pin Output Impedance	R_{CBL}	CBn output off impedance between CB(n) to VC(n-1): cells 1 to 9 and between CB(n) to VC(n): cells 10 to 12.	**3**	4	**5**	MΩ
Cell Balance Output Current	I_{CBH1}	CBn output on. (CB1-CB9); V_{BAT} = 39.6V; device sinking current.	**-28**	-25	**-21**	µA
	I_{CBH2}	CBn output on. (CB10-CB12); V_{BAT} = 39.6V; device sourcing current.	**21**	25	**28**	µA
Cell Balance Output Leakage in Shutdown	I_{CBSD}	EN = GND. V_{BAT} = 39.6V.	**-500**	10	**700**	nA
External Cell Balance FET Gate Voltage	VGS	CBn Output on; External 320kΩ between VCn and CBn (n = 10 to 12) and between CBn and VCn-1 (n = 1 to 9)	**7.05**	8.0	**8.95**	V
Internal Cell Balance Output Clamp	VCBCL	I_{CB} = 100µA.	**8.9**			V
LOGIC INPUTS: SCLK, $\overline{\text{CS}}$, DIN						
Low Level Input Voltage	VIL				**0.8**	V
High Level Input Voltage	VIH		**1.75**			V
Input Hysteresis	VHYS		**100**			mV
Input Current	IIN	0V < V_{IN} < V3P3	**-1**		**+1**	µA
Input Capacitance	CIN				**10**	pF
LOGIC INPUTS: EN, COMMS SELECT1, COMMS SELECT2, COMMS RATE 0, COMMS RATE 1						
Low Level Input Voltage	VIL				**0.3*V3P3**	V
High Level Input Voltage	VIH		**0.7*V3P3**			V
Input Hysteresis	VHYS		**0.05*V3P3**			V
Input Current	IIN	0V < V_{IN} < V3P3	**-1**		**+1**	µA
Input Capacitance	CIN				**10**	pF
LOGIC OUTPUTS: DOUT, $\overline{\text{FAULT}}$, $\overline{\text{DATA READY}}$						
Low Level Output Voltage	VOL1	At 3mA sink current	**0**		**0.4**	V
	VOL2	At 6mA sink current	**0**		**0.6**	V
High Level Output Voltage	VOH1	At 3mA source current	**V3P3 – 0.4V**		**V3P3**	V
	VOH2	At 6mA source current	**V3P3 – 0.6V**		**V3P3**	V

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SPI INTERFACE TIMING (See Figures 2 and 3)						
SCLK Clock Frequency	f_{SCLK}				**2**	MHz
Pulse Width of Input Spikes Suppressed	t_{IN1}		**50**		**200**	ns
Enable Lead Time	t_{LEAD}	Chip select low to ready to receive clock data	**200**			ns
Clock High Time	t_{HIGH}		**200**			ns
Clock Low Time	t_{LOW}		**200**			ns
Enable Lag Time	t_{LAG}	Last data read clock edge to chip select high.	**250**			ns
CHIP SELECT High Time	$t_{CS:WAIT}$	Minimum high time for $\overline{CS}$ between bytes.	**200**			ns
Slave Access Time	t_A	Chip select low to DOUT active.			**200**	ns
Data Valid Time	t_V	Clock low to DOUT valid.			**350**	ns
Data Output Hold Time	t_{HO}	Data hold time after falling edge of SCLK.	**0**			ns
DOUT Disable Time	t_{DIS}	DOUT disabled following rising edge of $\overline{CS}$.			**240**	ns
Data Setup Time	t_{SU}	Data input valid prior to rising edge of SCLK.	**100**			ns
Data Input Hold Time	t_{HI}	Data input to remain valid following rising edge of SCLK.	**80**			ns
$\overline{\text{Data Ready}}$ Start Delay Time	$t_{DR:ST}$	Chip select high to $\overline{\text{Data Ready}}$ low.	**100**			ns
$\overline{\text{Data Ready}}$ Stop Delay Time	$t_{DR:SP}$	Chip select high to $\overline{\text{Data Ready}}$ high.			**750**	ns
$\overline{\text{Data Ready}}$ High Time	$t_{DR:WAIT}$	Time between bytes.	**0.6**			µs
SPI Communications Timeout	$t_{SPI:TO}$	Time the $\overline{CS}$ remains high before SPI communications time out - requiring the start of a new command.		100		µs
DOUT Rise Time	t_R	Up to 50pF load.			**30**	ns
DOUT Fall Time	t_F	Up to 50pF load.			**30**	ns
DAISY CHAIN COMMUNICATIONS INTERFACE: DHI1, DLo1, DHI2, DLo2						
Daisy Chain Clock Frequency		Comms Rate (0, 1) = 11	**450**	500	**550**	kHz
		Comms Rate (0, 1) = 10	**225**	250	**275**	kHz
		Comms Rate (0, 1) = 01	**112.5**	125	**137.5**	kHz
		Comms Rate (0, 1) = 00	**56.25**	62.5	**68.75**	kHz
Common Mode Reference Voltage				$V_{BAT}/2$		V

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Scan and Measurement start times are synchronized by the receiver to the falling edge of the 24^{th} clock pulse (Daisy Chain systems) or to the falling edge of the 16^{th} clock pulse (non-daisy chain, single device systems) of the Scan or Measure command. Clock pulses are at the SCLK pin for master and standalone devices, and at the DHi/DLo1 pins for middle and top daisy chain devices. Max values are based on characterization of the internal clock and are not 100% tested.
9. Biasing setup as in Figure 44 on page 60 or equivalent.

Timing Diagrams

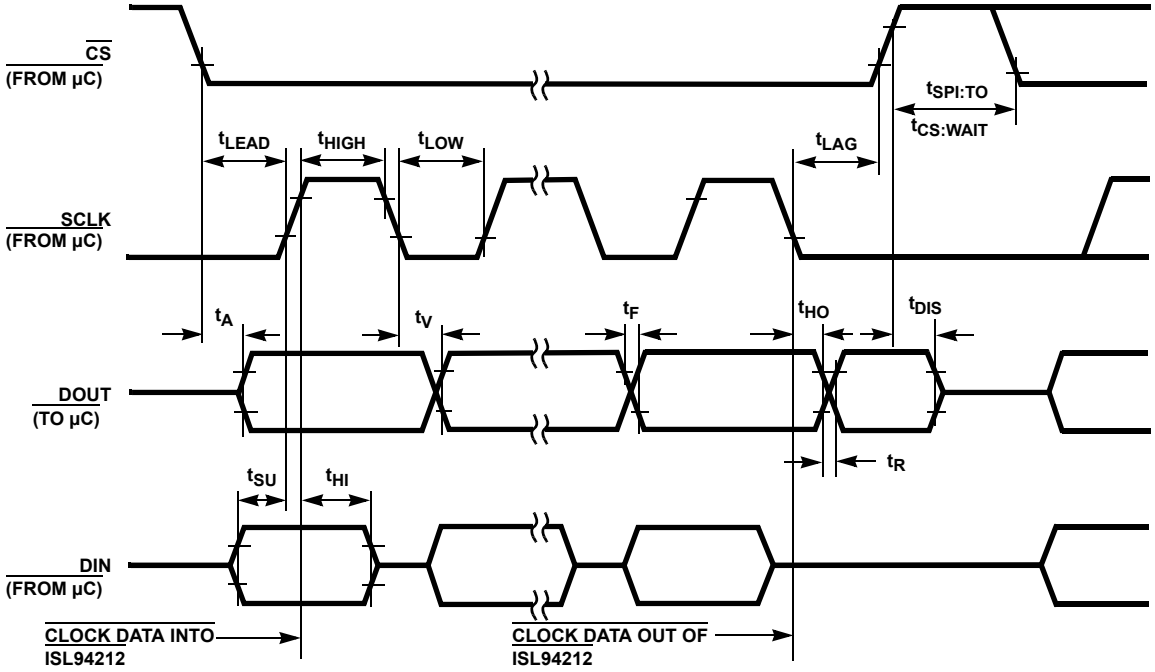


FIGURE 2. SPI FULL DUPLEX (4-WIRE) INTERFACE TIMING

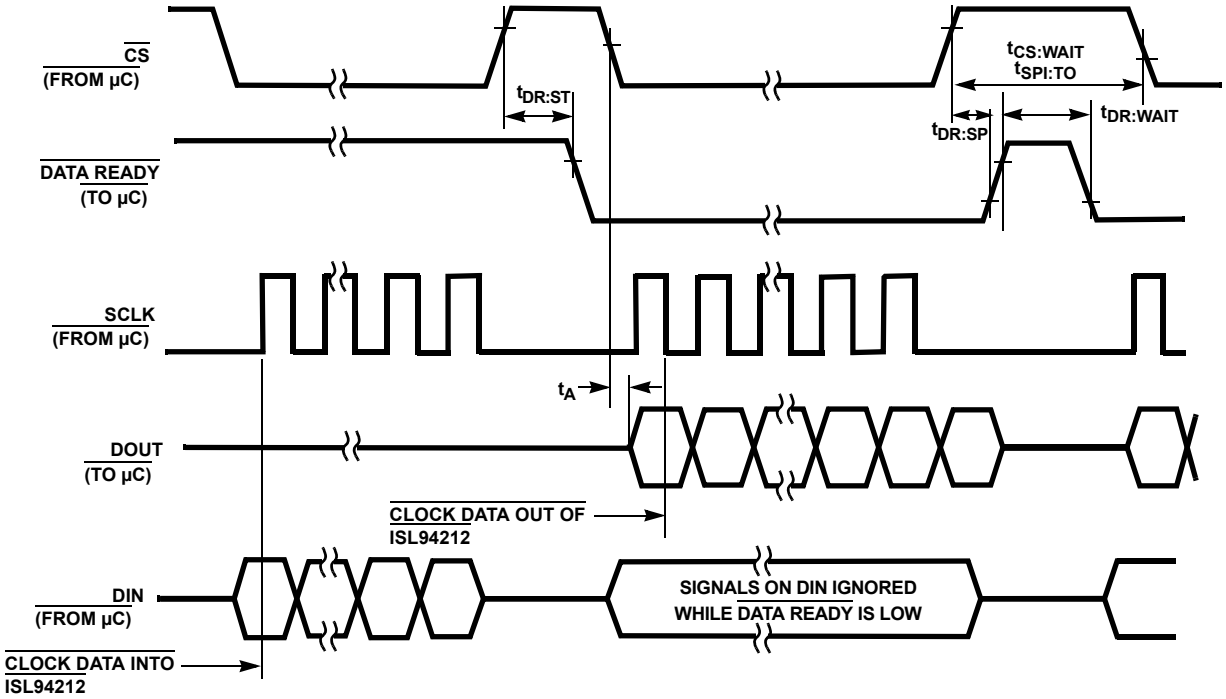


FIGURE 3. SPI HALF DUPLEX (3-WIRE) INTERFACE TIMING

Typical Performance Curves

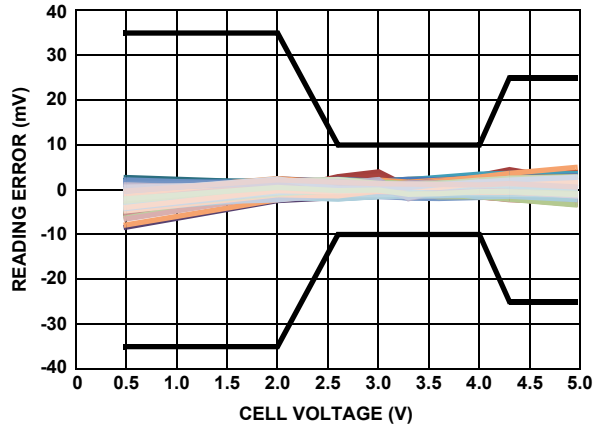


FIGURE 4. CELL VOLTAGE READING ERROR FROM 0°C TO +50°C

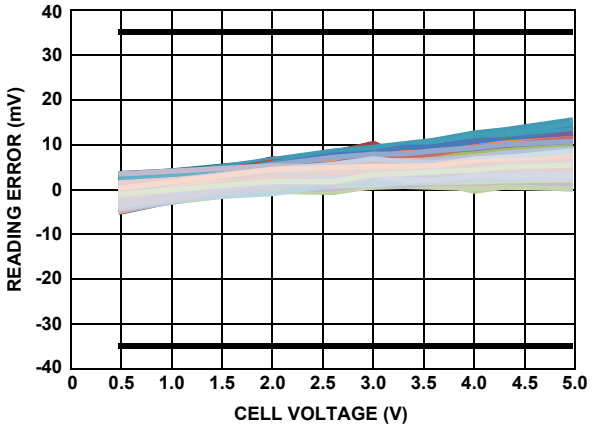


FIGURE 5. CELL VOLTAGE READING ERROR FROM -40°C TO +85°C

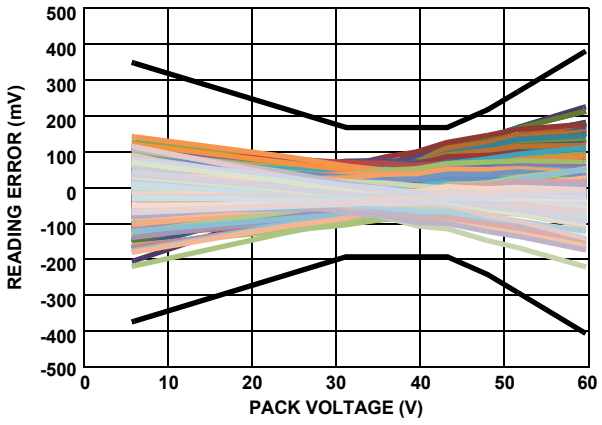


FIGURE 6. PACK VOLTAGE READING ERROR FROM 0°C TO +50°C

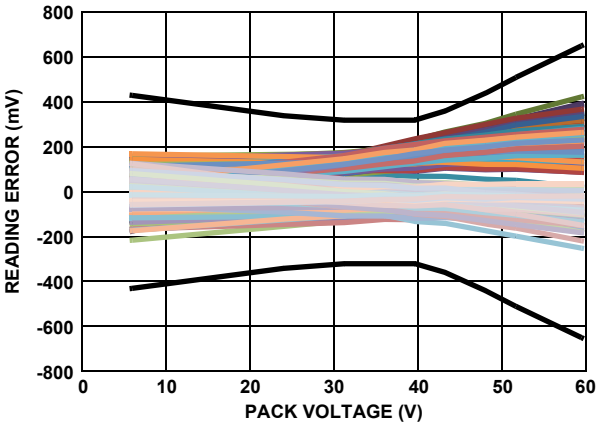


FIGURE 7. PACK VOLTAGE READING ERROR FROM -40°C TO +85°C

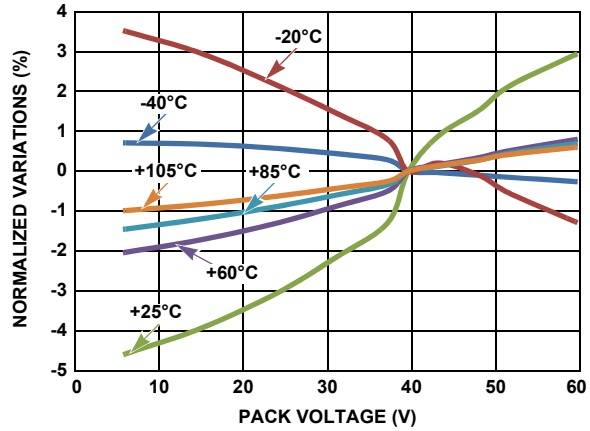


FIGURE 8. IC TEMPERATURE ERROR vs PACK VOLTAGE

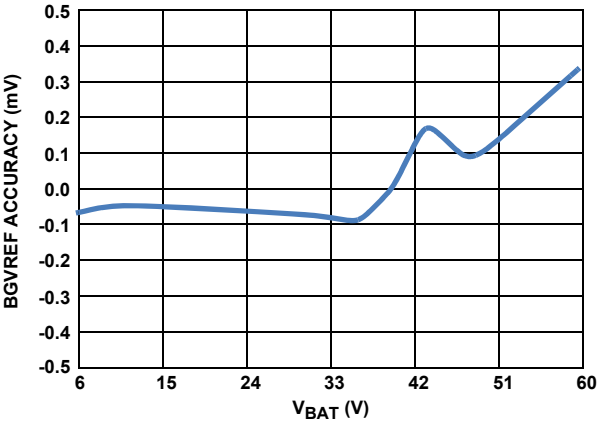


FIGURE 9. VOLTAGE REFERENCE CHECK FUNCTION vs PACK VOLTAGE (AT +25°C)

Typical Performance Curves (Continued)

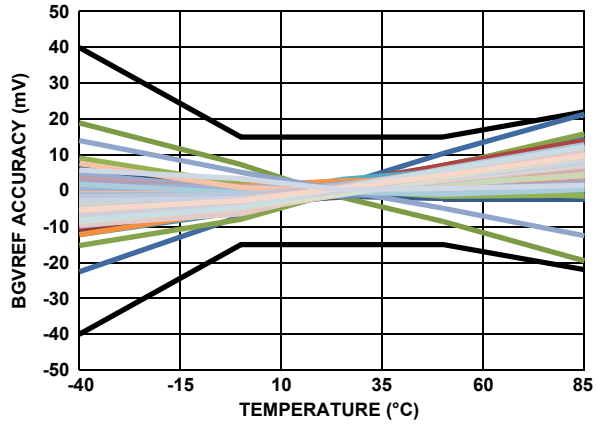


FIGURE 10. VOLTAGE REFERENCE CHECK FUNCTION vs TEMPERATURE (V_{BAT} = 39.6)

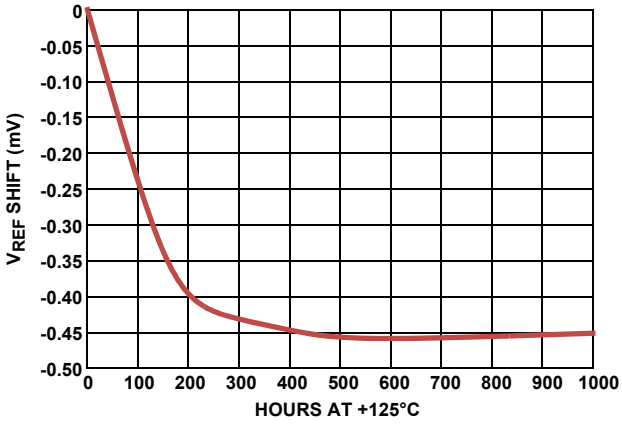


FIGURE 11. V_{REF} SHIFT OVER HTOL

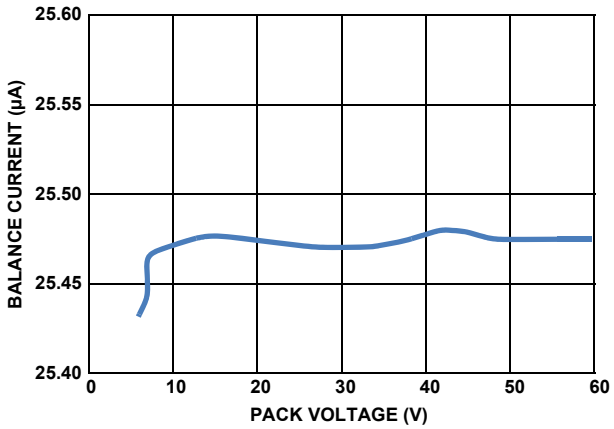


FIGURE 12. BALANCE CURRENT vs PACK VOLTAGE

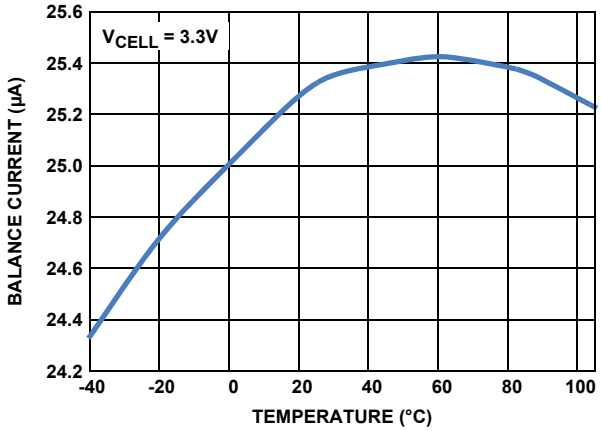


FIGURE 13. BALANCE CURRENT vs TEMPERATURE

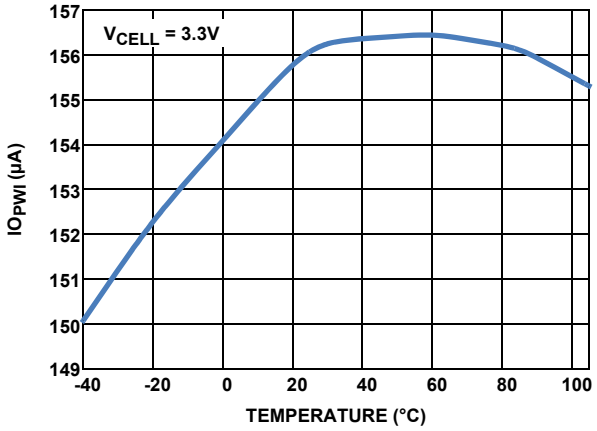


FIGURE 14. OPEN WIRE TEST CURRENT vs TEMPERATURE (150µA SETTING)

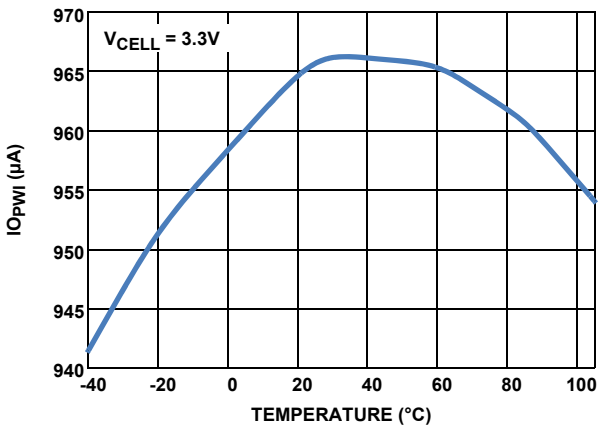


FIGURE 15. OPEN WIRE TEST CURRENT vs TEMPERATURE (1mA SETTING)

Typical Performance Curves (Continued)

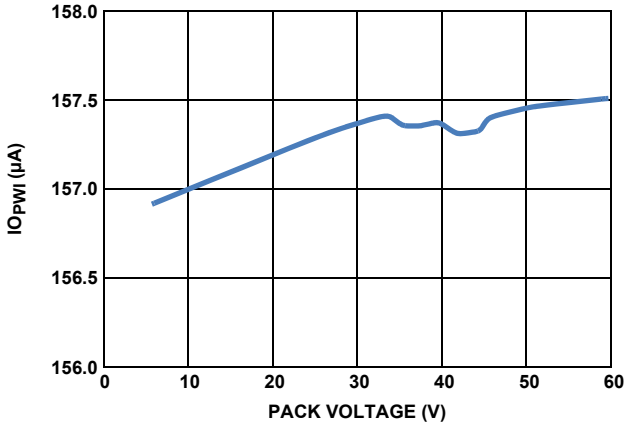


FIGURE 16. OPEN WIRE TEST CURRENT vs PACK VOLTAGE (150µA SETTING)

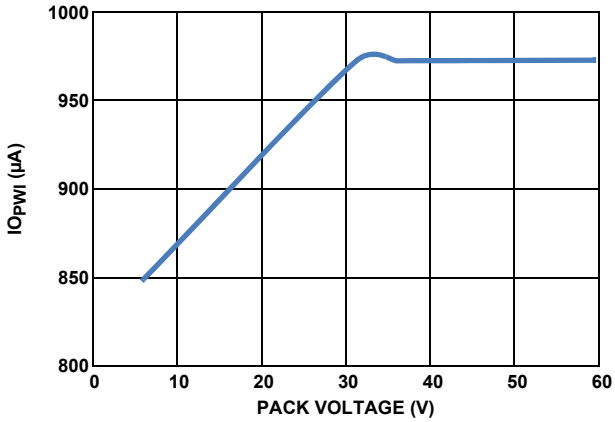


FIGURE 17. OPEN WIRE TEST CURRENT vs PACK VOLTAGE (1mA SETTING)

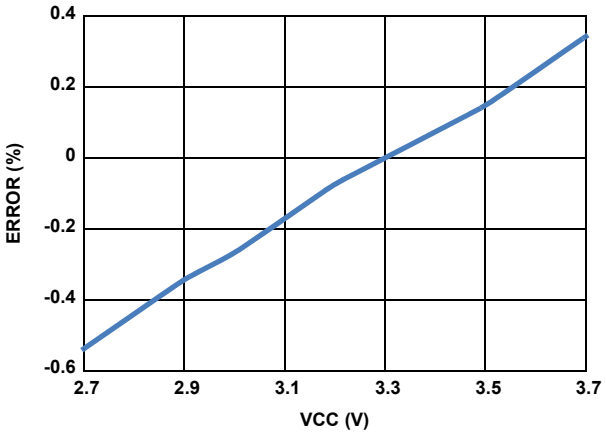


FIGURE 18. 4MHz OSCILLATOR ERROR vs VCC

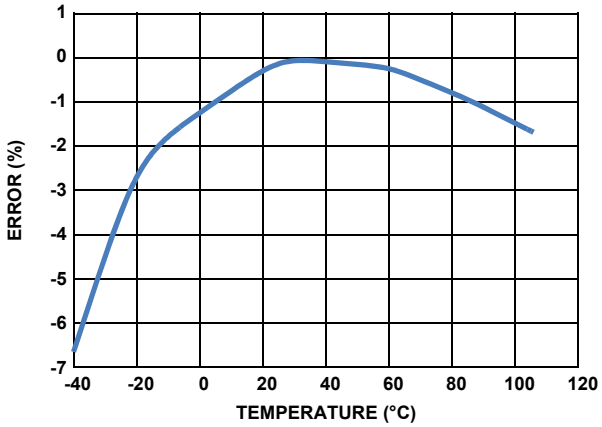


FIGURE 19. 4MHz OSCILLATOR ERROR vs TEMPERATURE

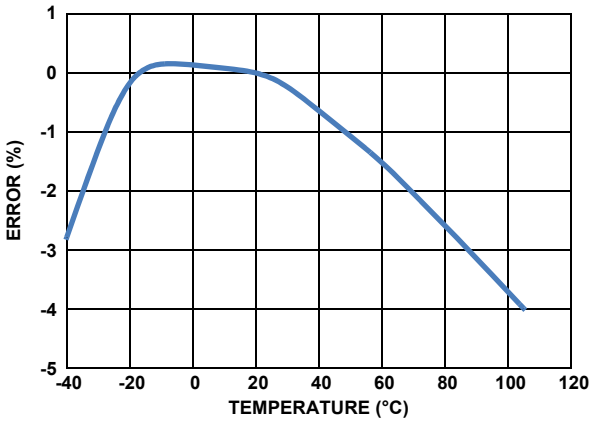


FIGURE 20. 32kHz OSCILLATOR ERROR vs TEMPERATURE

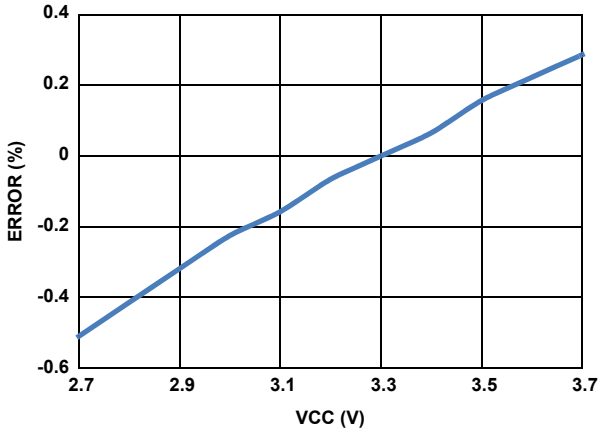


FIGURE 21. 32kHz OSCILLATOR ERROR vs VCC

Typical Performance Curves (Continued)

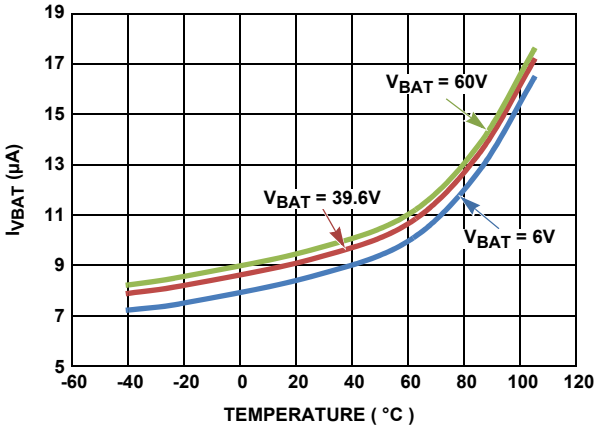


FIGURE 22A. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (STANDALONE MODE)

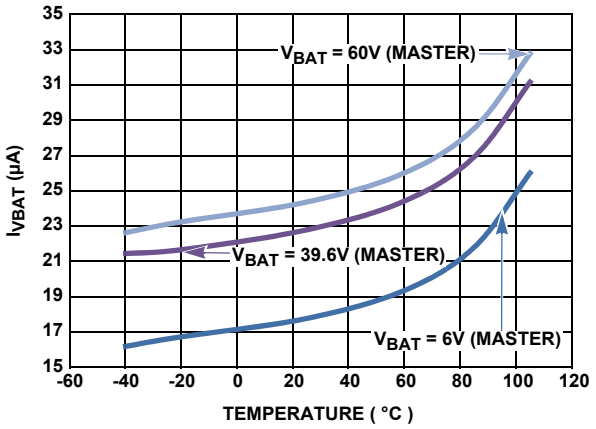


FIGURE 22B. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

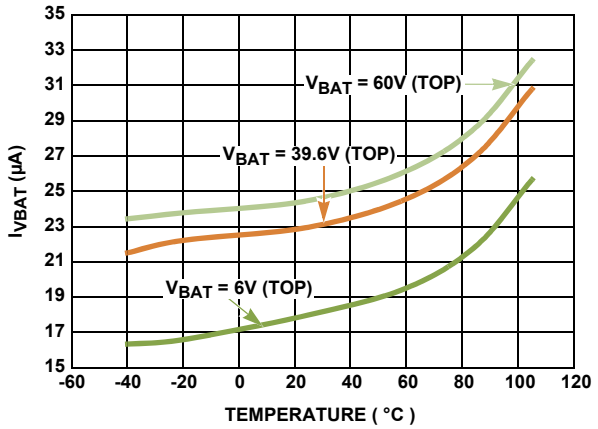


FIGURE 22C. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

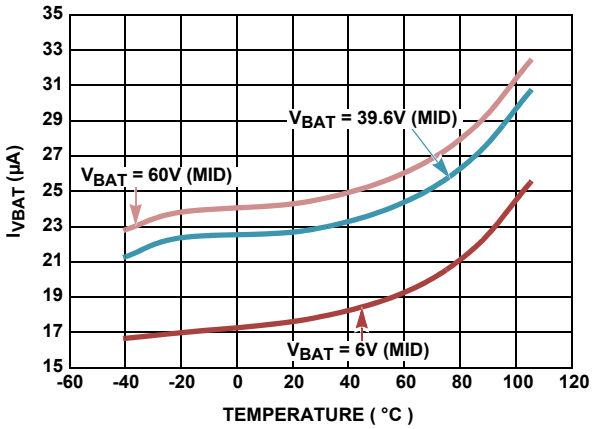


FIGURE 22D. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MODE)

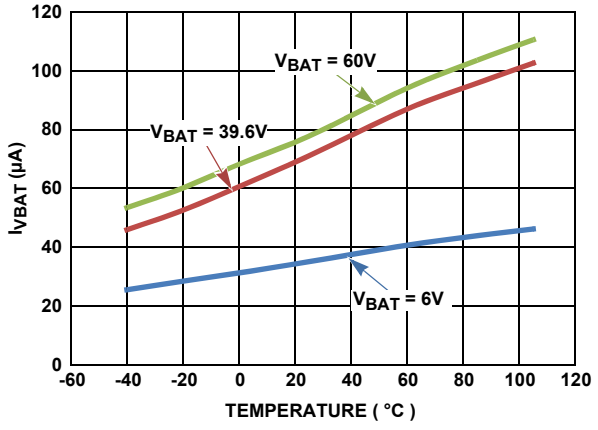


FIGURE 23A. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (STANDALONE MODE)

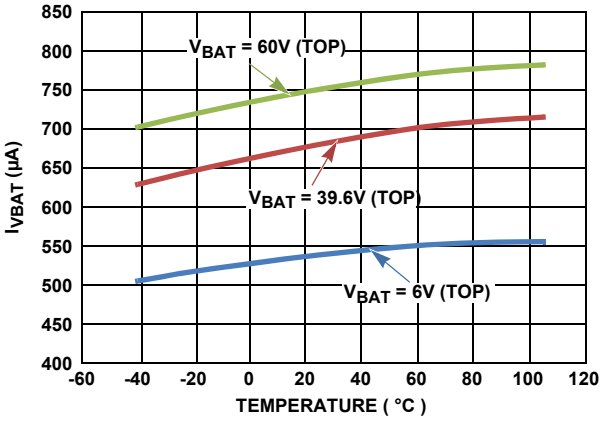


FIGURE 23B. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN TOP)

Typical Performance Curves (Continued)

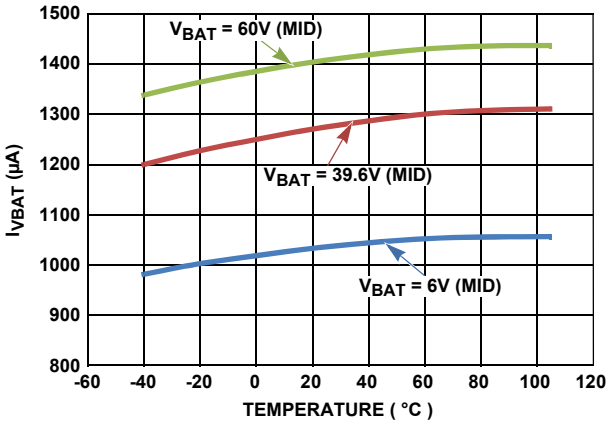


FIGURE 23C. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MIDDLE)

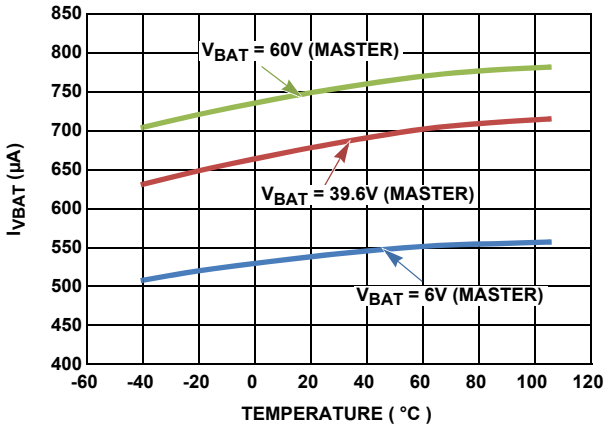


FIGURE 23D. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MASTER)

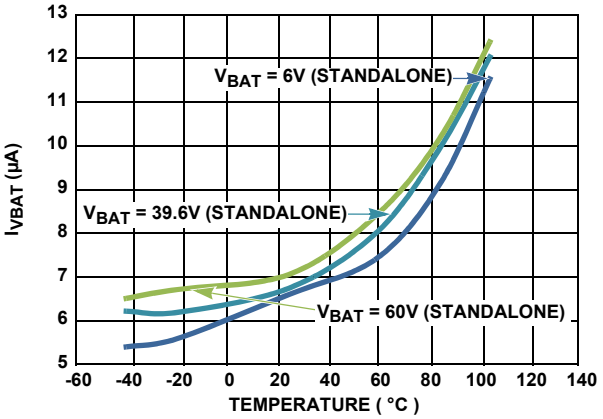


FIGURE 24A. PACK VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

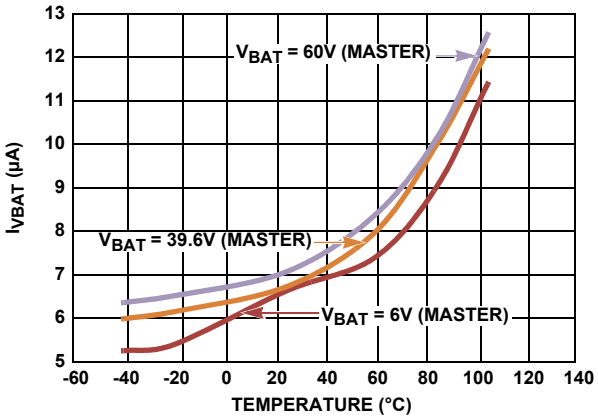


FIGURE 24B. V_{BAT} SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

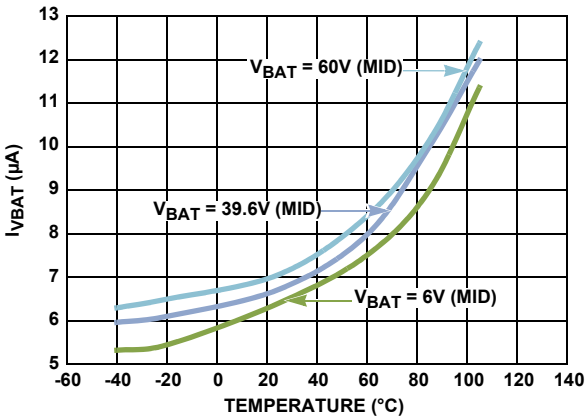


FIGURE 24C. V_{BAT} VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

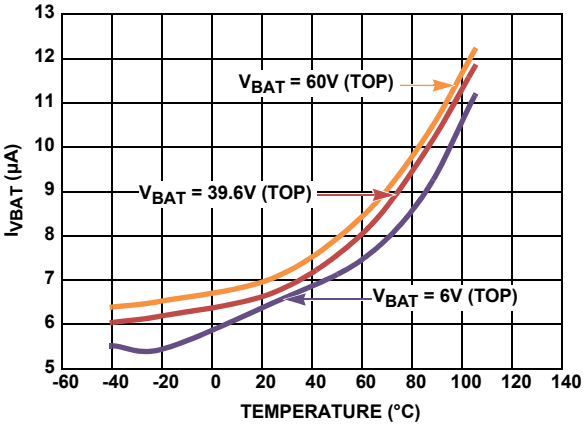


FIGURE 24D. V_{BAT} VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

Typical Performance Curves (Continued)

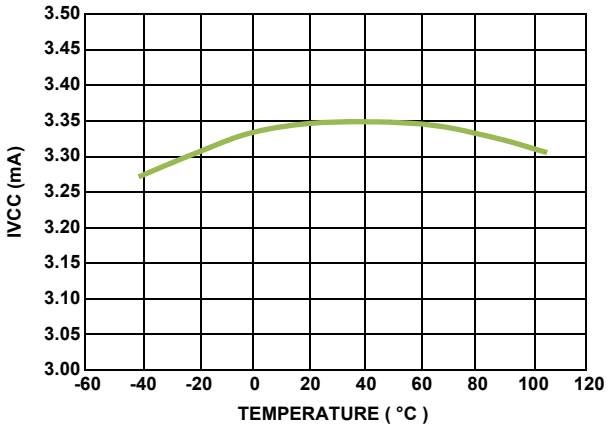


FIGURE 25. VCC SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V

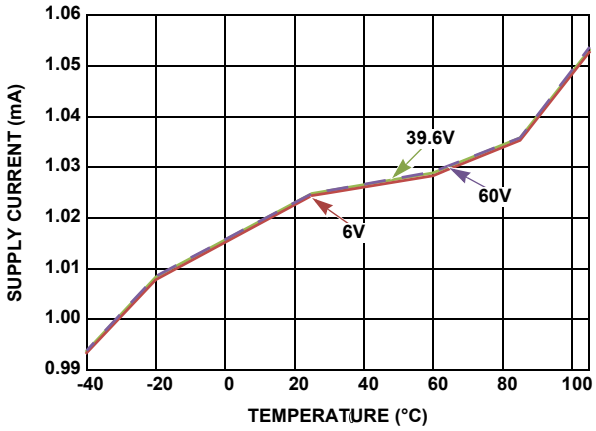


FIGURE 26. V3P3 SUPPLY CURRENT vs TEMPERATURE

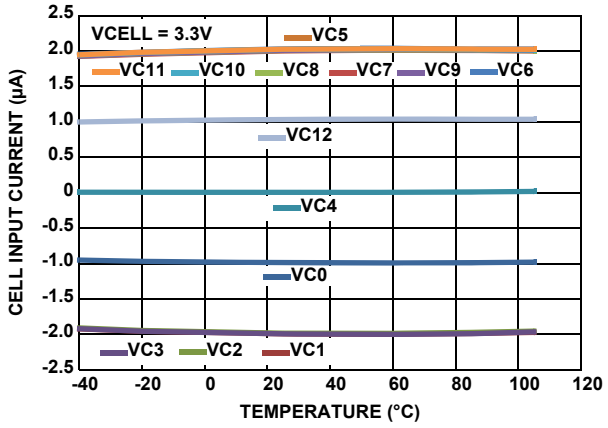


FIGURE 27. CELL INPUT CURRENT vs TEMPERATURE

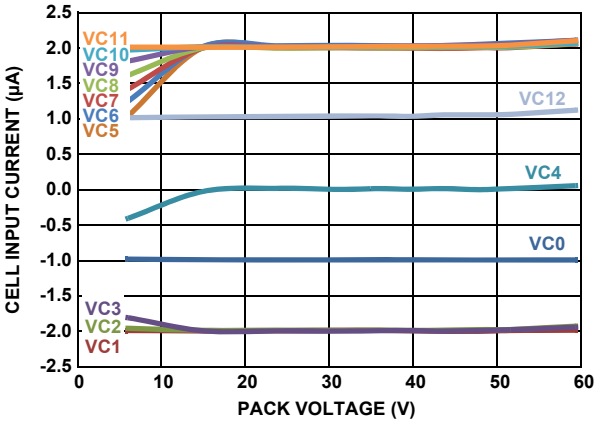


FIGURE 28. CELL INPUT CURRENT vs PACK VOLTAGE (+25°C)

Device Description and Operation

The ISL94212 is a Li-ion battery manager IC that supervises up to 12 series connected cells. Up to 14 ISL94212 devices can be connected in series to support systems with up to 168 cells. The ISL94212 provides accurate monitoring, cell balance control, and diagnostic functions. The ISL94212 includes a voltage reference, 14 bit A/D converter and registers for control and data. An external microcontroller communicates to the ISL94212 through an SPI interface. Series connected ISL94212 devices communicate to each other via a proprietary daisy chain communications interface.

The ISL94212 devices handle daisy chain communications differently depending on their position within the daisy chain. The ISL94212 at one end of the daisy chain acts as a master device for communication purposes. The master device, also called the bottom device, occupies the first position in the daisy chain and communicates to a host microcontroller using an SPI interface. A single daisy chain port then connects the master device to the next device in the daisy chain.

The device at the other end of the daisy chain from the master is the top device. The top device has a single daisy chain port connection to the device below. Devices other than the master and top devices are middle devices. Middle devices have two daisy chain port connections. The up port connects to the device above while the down port connects to the device below. The master ISL94212 device is device number 1. The top device is device number n, where n equals the total number of ISL94212 devices in the daisy chain. The middle devices are numbered 2 to (n-1) with device number 2 being connected to the master device. If n = 2, then there is a master device and a top device, with no middle device.

When multiple ISL94212 devices are connected to a series of cells, their power supply domains are normally non-overlapping. The lower (VSS) supply of each ISL94212 nominally connects to the same potential as the upper (V_{BAT}) supply of the ISL94212 device below.

The ISL94212 provides two multiple parameter measurement “scanning” modes in addition to single parameter direct measurement capability. These scanning modes provide pseudo simultaneous measurement of all cell voltages in the stack. In daisy chain applications all measurement data is sent with the corresponding device stack address (the position within the daisy chain), parameter identifier, and data address. In stand alone applications (non-daisy chain) data is sent without additional address information. This maximizes the throughput for full duplex SPI operation. Daisy chain communication throughput is maximized by allowing streamed data (accessed by a “read all data” address).

The addressed device, the top device and the bottom device act as masters for the purposes of communications timing. All other devices are repeaters, passing data up or down the chain.

The only filtering applied to the ADC measurements is that resulting from external protection circuits and the limited bandwidth of the measurement path. No additional filtering is performed within the part. This arrangement is typically needed to maintain timing integrity between the cell voltage and pack current measurements. The ISL94212 does not measure current. The system performs this separately using other measurement systems. However, the ISL94212 does apply filtering to the fault detection systems.

Power Modes

The ISL94212 has three main power modes: **Normal mode**, **Sleep mode** and **Shutdown mode** (“off”).

Sleep mode is entered in response to a *Sleep* command or after a watchdog timeout. Only the communications input circuits, low speed oscillator and internal registers are active in **Sleep mode**, allowing the part to perform timed scan and balancing activity and to wake up in response to communications.

Drive the enable pin low to place the part in **Shutdown mode**. When entering Shutdown mode, the internal bias for most of the IC is powered down except digital core, sleep mode regulators, and digital input buffers. When exiting, the device powers up and does not reload the factory programmed configuration data from EEPROM.

The **Normal mode** consists of an Active state and a standby state. In the Standby state, all systems are powered and the device is ready and waiting to perform an operation in response to commands from the host microcontroller. In the Active state, the device performs an operation, such as ADC conversion, open wire detection, etc.

Measurement Modes

The ISL94212 provides three types of measurement modes.

- Scan Once
- Scan Continuous
- Measure

In **Scan Once mode** the part performs the requested scan a single time. In **Scan Continuous mode** the ISL94212 performs repeated scans at intervals controlled by registers settings. **Measure mode** allows a single parameter to be measured.

The ISL94212 ignores a Scan or Measure command, when the device is already in a scan mode or measure mode. But, the command passes through to other devices in the daisy chain. All other communications functions respond normally while the device is scanning or measuring.

Measurement Mode Commands

Measurement modes are activated by commands from an external microcontroller. The ISL94212 uses a memory mapped command structure. Commands are sent to the device using a memory read operation from a specific address. The addresses for the measurement mode commands[1] are shown in Table 1.

There are other commands that perform other actions, but these are discussed in other sections.

1. In this document, the terminology for a hex value (e.g., h0000) is modified by a leading value (e.g., 16’) which defines the number of bits. For the measurement mode command address, a value of 6’h02 refers to a binary value of ‘00 0010’.

TABLE 1. MEASUREMENT MODE COMMAND ADDRESSES

REGISTER ADDRESS	COMMAND SUFFIX	COMMAND
SCAN ONCE		
6'h01	6'h00	Scan Voltages
6'h02	6'h00	Scan Temperatures
6'h03	6'h00	Scan Mixed
6'h04	6'h00	Scan Wires
6'h05	6'h00	Scan All
SCAN CONTINUOUS		
6'h06	6'h00	Scan Continuous
MEASURE		
6'h08	6 bit addr of element to measure	Measure

Scan Once

Five different scan functions are available in single scan (**Scan Once mode**.) Each Scan function is activated by a command from the host microcontroller. The scan functions are:

1. Scan Voltages
2. Scan Temperatures
3. Scan Mixed
4. Scan Wires
5. Scan All

The **Scan Once** functions are synchronous: all addressed stack devices begin scanning immediately following command receipt. There is a scan start latency between subsequent stack devices of one daisy chain clock cycle (e.g., for a stack of 10 devices with a daisy chain operating at 500kHz, the scan start latency between the bottom and top stack devices is approximately 20µs).

Scan Voltages

The **Scan Voltages** command causes the addressed part (or all parts if the common address is used) to scan through the cell voltage inputs followed by the Pack Voltage. IC temperature is also recorded for use with the internal calibration routines. Cell voltages connected to each device are scanned in order from cell-12 (top) to cell-1 (bottom). Cell overvoltage and undervoltage compares are performed on each cell voltage sample. The V_{BAT} and VSS connections are also checked at the end of the scan.

Cell voltage and pack voltage data, along with any fault conditions are stored in local memory ready for reading by the system host microcontroller. If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan. Devices revert to the standby state on completion of the scan activity.

Scan Temperatures

The **Scan Temperatures** command causes the addressed part (or all parts if the common address is used) to scan through the internal and 4 external temperature signals followed by multiplexer loopback and reference measurements. The loopback and reference measurements are part of the internal diagnostics function. Over-temperature compares are performed on each temperature measurement depending on the condition of the appropriate bit in the *Fault Setup* register.

Temperature data, along with any fault conditions, are stored in local memory ready for reading by the system host microcontroller. If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan. Devices revert to the standby state on completion of the scan activity.

Scan Mixed

The **Scan Mixed** command causes the addressed part (or all parts if the common address is used) to scan through the cell voltage inputs (followed by the pack voltage) with a single external input (ExT1) interposed. IC temperature is also recorded for use with the internal calibration routines. Cell voltages connected to each device are scanned in order from cell-12 (top) to cell-1 (bottom). The external input ExT1 is scanned in the middle of the cell voltages such that half the cells are sampled before ExT1 and half after ExT1. This mode allows ExT1 to be used for an external voltage measurement, such as a current sensing and performs it along with the cell voltage measurements, reducing the latency between measurements. Cell overvoltage and cell undervoltage compares are performed on each cell voltage sample. The V_{BAT} and VSS conditions are also checked at the end of the scan.

The **Scan Mixed** command is intended for use in standalone systems, or by the Master device in stacked applications, and would typically measure a single system parameter, such as battery current. Other stack devices also measure their ExT1 input but these would normally be ignored by the host.

Cell voltage, pack voltage and ExT1 data, along with any fault conditions are stored in local memory ready for reading by the system host microcontroller. Access the data from the ExT1 measurement by a direct *Read ET1 Voltage* command or by the All Temperatures read command. If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan. Devices revert to the standby state on completion of the scan activity.

Scan Wires

The **Scan Wires** command causes the addressed part (or all parts if the common address is used) to measure all the VCn pin voltages while applying load currents to each input pin in turn. This is part of the fault detection system.

If there is a fault condition, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan. No cell voltage data is sent as a result of the *Scan Wires* command. Devices revert to the standby state on completion of this activity.

Scan All

The **Scan All** command incorporates the Scan Voltages, Scan Wires and Scan Temperatures commands and causes the addressed part (or all parts if the common address is used) to execute each of these three scan functions once, in sequence (see Figure 29 on page 25 for example on timing).

Scan Continuous

Scan Continuous mode is used primarily for fault monitoring and incorporates the scan voltages, scan temperatures and scan wires commands.

The **Scan Continuous** command causes the addressed part to set the SCAN bit in the Device Setup register and performs a succession of scans at a predetermined scan rate. Each device operates asynchronously on its own clock. This is similar to the **Scan All** command except that the scans are repeated at intervals determined by the SCN0-3 bits in the Fault Setup register. The Scan Inhibit command is used to stop scanning (i.e., receipt of this command by the target device resets the SCAN bit and stops the scan continuous function).

The ISL94212 provides an option that pauses cell balancing activity while measuring cell voltages in **Scan Continuous mode**. This is controlled by the BDDS bit in the Device Setup register. If BDDS is set, then cell balancing is inhibited during cell voltage measurement and for 10ms before the cell voltages are scanned. Balancing is reenabled at the end of the scan to allow balancing to continue. This function only applies during the scan continuous and the auto balance functions and allows the implementation of a circuit arrangement that can be used to diagnose the condition of external balancing components. It is up to the host microcontroller to manually stop balancing functions (if required) when operating a scan once or measure command.

The **Scan Continuous** scan interval is set using the SCN3:0 bits (lower nibble of the Fault Setup register.) The temperature and wire scans occur at slower rates and depend on the value of the scan interval selected. The scan system is synchronized such that the wire and temperature scans always follow a voltage scan. The three scan sequences, depending on the scans required at a particular instance, are as follows:

- Scan Voltages
- Scan Voltages, Scan Wires
- Scan Voltages, Scan Wires, Scan Temperatures.

The temperature and wire scans occur at 1/5 the voltage scan rate for voltage scan intervals above 128ms. Below this value the temperature scan interval is fixed at 512ms. The behavior of the wire scan interval is determined by the WSCN bit in the Fault Setup register. A bit value of '1' causes the wire scan to be performed at the same rate as the temperature scan. A bit value of '0' causes the wire scan rate to track the voltage scan rate for voltage scan intervals above 512ms while at and below this value the wire scan is performed at a fixed 512ms rate. Table 2 shows the various scan rate combinations available.

Data is not automatically returned while devices are in **Scan Continuous mode** except in the case where a fault condition is detected. The results of voltage and temperature scans are stored in local volatile memory and may be accessed at any time by the system host microcontroller. Devices may be operated in **Scan Continuous mode** while in **Normal mode** or in **Sleep mode**. Devices revert to the **Sleep mode** or remain in **Normal mode**, as applicable on completion of each scan.

The response to a detected fault condition is to send the fault signal, either immediately in the case of standalone devices or daisy chain devices in **Normal mode**, or following transmission of the wakeup signal if the device is being used in a daisy chain configuration and is in **Sleep mode**.

To operate the "Scan Continuous" function in **Sleep mode** the host microcontroller simply configures the ISL94212, starts the **Scan Continuous mode** and then sends the Sleep command. The ISL94212 then wakes itself up each time a scan is required. Note that for the fastest scan settings (scan interval codes 0000, 0001 and 0010) the main measurement functions do not power down between scans, since the ISL94212 remains in **Normal mode**.

TABLE 2. SCAN CONTINUOUS TIMING MODES

SCAN INTERVAL SCN3:0	SCAN INTERVAL (ms)	TEMP SCAN (ms)	WIRE SCAN WSCN = 0 (ms)	WIRE SCAN WSCN = 1 (ms)
0000	16	512	512	512
0001	32	512	512	512
0010	64	512	512	512
0011	128	512	512	512
0100	256	1024	512	1024
0101	512	2048	512	2048
0110	1024	4096	1024	4096
0111	2048	8192	2048	8192
1000	4096	16384	4096	16384
1001	8192	32768	8192	32768
1010	16384	65536	16384	65536
1011	32768	131072	32768	131072
1100	65536	262144	65536	262144

Measure

This command allows a single cell voltage, internal temperature, any of the four external temperature inputs or the secondary voltage reference measurements to be made. The command incorporates a 6-bit suffix that contains the address of the required measurement element. See Table 3 on page 24. The device matching the target address responds by conducting the single measurement and loading the result to local memory. The host microcontroller then reads from the target device to obtain the measurement result. All devices revert to the standby state on completion of this activity.

TABLE 3. MEASURE COMMAND TARGET ELEMENT ADDRESSES

MEASURE COMMAND	MEASURE ELEMENT ADDRESS (SUFFIX)	DESCRIPTION
6'h08	6'h00	V_{BAT} Voltage
	6'h01	Cell 1 Voltage
	6'h02	Cell 2 Voltage
	6'h03	Cell 3 Voltage
	6'h04	Cell 4 Voltage
	6'h05	Cell 5 Voltage
	6'h06	Cell 6 Voltage
	6'h07	Cell 7 Voltage
	6'h08	Cell 8 Voltage
	6'h09	Cell 9 Voltage
	6'h0A	Cell 10 Voltage
	6'h0B	Cell 11 Voltage
	6'h0C	Cell 12 Voltage
	6'h10	Internal temperature reading
	6'h11	External temperature input 1 reading
	6'h12	External temperature input 2 reading
	6'h13	External temperature input 3 reading
	6'h14	External temperature input 4 reading
	6'h15	Reference voltage (raw ADC) value. Use to calculate corrected reference value using reference coefficient data. See page 2 data, address 6'h38 – 6'h3A.

Cell Voltage Measurement Accuracy

The cell voltage monitoring system comprises two basic elements; a level shift to eliminate the cell common mode voltage and an analog-to-digital conversion of the cell voltage.

Each ISL94212 is calibrated at a specific cell input voltage value, V_{NOM}. Cell voltage measurement error data is given in "MEASUREMENT SPECIFICATIONS" on page 9 for various voltage and temperature ranges with voltage ranges defined with respect to V_{NOM}. Plots showing the typical error distribution over the full input range are included in the "Typical Performance Curves" section beginning on page 15.

Temperature Monitoring

One internal and four external temperature inputs are provided together with a switched bias voltage output (TEMPREG, pin 29). The voltage at the TEMPREG output is nominally equal to the ADC reference voltage such that the external voltage measurements are ratiometric to the ADC reference (see Figure 44 on page 60).

The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but may also be used as general purpose analog inputs. Each temperature input is applied to the ADC via a multiplexer. The ISL94212 converts the voltage at each input and loads the 14-bit result to the appropriate register.

The TEMPREG output is turned "on" in response to a **Scan temperatures** or **Measure temperature** command. A dwell time of 2.5ms is provided to allow external circuits to settle, after which the ADC measures each external input in turn. The TEMPREG output turns "off" after measurements are completed.

Figure 29 on page 25 shows an example temperature scan with the ISL94212 operating in **scan continuous mode** with a scan interval of 512ms. The preceding voltage and wire scans are shown for comparison.

The external temperature inputs are designed such that an open connection results in the input being pulled up to the full scale input level. This function is provided by a switched 10MΩ pull-up from each input to VCC. This feature is part of the fault detection system and is used to detect open pins.

The internal IC temperature, along with the auxiliary reference voltage and multiplexer loopback signals, are sampled in sequence with the external signals using the scan temperatures command.

The converted value from each temperature input is also compared to the external over-temperature limit and open connection threshold values on condition of the [*TST4:1*] bits in the Fault Setup register (see "Fault Setup:" on page 42.) If a TSTn bit is set to "1", then the temperature value is compared to the external temperature threshold and a fault occurs if the measured value is lower than the threshold value. If a TSTn bit is set to "0", then the temperature measurement is not compared to the threshold value and no fault occurs. The [TST4:1] bits are "0" by default.

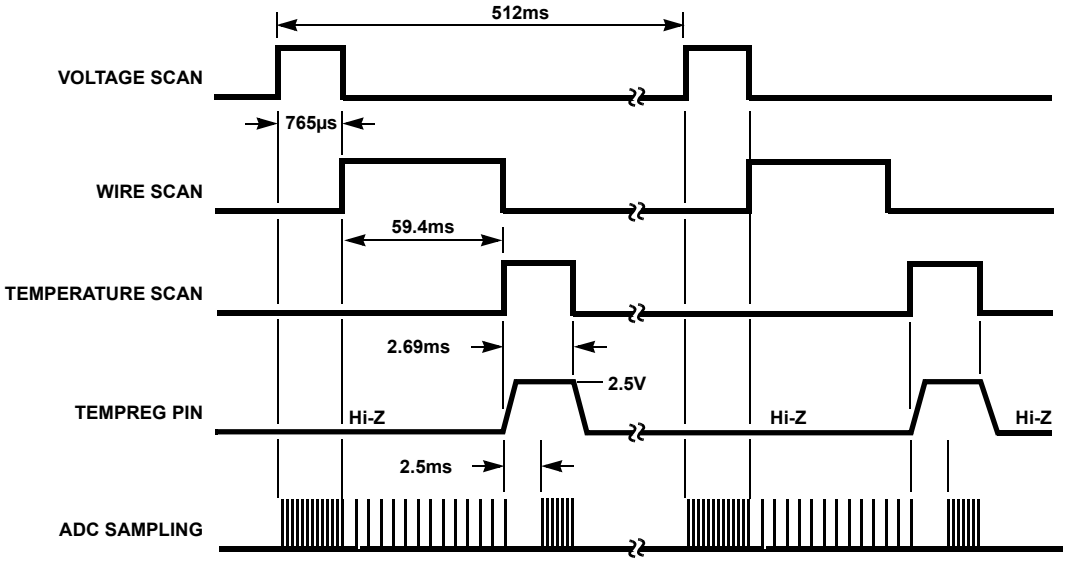


FIGURE 29. SCAN TIMING EXAMPLE DURING **SCAN CONTINUOUS MODE** AND **SCAN ALL MODE**

Cell Balancing Functions

Cell balancing is an important function in a battery pack consisting of a stack of multiple Li-ion cells. As the cells charge and discharge, differences in each cell's ability to take on and give up charge, typically leads to cells with different states of charge. The problem with a stack of cells having different states of charge is that Li-ion cells have a maximum voltage, above which it should not be charged and a minimum voltage, below which it should not be discharged. The extreme case, where one cell in the stack is at the maximum voltage and one cell is at the minimum voltage, results in a nonfunctional battery stack, since the battery stack cannot be charged or discharged.

Cell balancing is performed using external MOSFETs and external current setting resistors (see Figure 30 on page 30). Each MOSFET is controlled independently by the CB1 to CB12 pins of the ISL94212. The CB1 to CB12 outputs are controlled either directly, or indirectly by an external microcontroller through bits in various control registers.

The balancing functions within the ISL94212 are controlled by multiple registers:

- Balance Setup register (All balance modes, see Table 4)
- Balance Status register (All balance modes, see Table 7 on page 26)
- Device Setup register (auto balance mode only, see Table 13 on page 30)
- Watchdog/Balance Time register (timed and auto balance modes, see Table 9 on page 27)
- Balance Values registers (auto balance only, see example in Table 11 on page 28)

Additional registers are provided for the balance timeout (**Timed mode** and **Auto Balance mode**) and balance value (**Auto Balance mode** only).

Balance Setup Register

TABLE 4. BALANCE SETUP REGISTER (ADDRESS 6'h13)

7	6	5	4	3	2	1 9	0 8
BSP2	BSP1	BSP0	BWT2	BWT1	BWT0	BMD1	BMD0
						BEN	BSP3

The Balance Setup register (see Table 7) contents break down into 4 sub groups.

- Balance wait time: BWT[2:0] bits (also referred to as balance dwell time)
- Balance status pointer: BSP[3:0] bits
- Balance enable: BEN bit
- Balance mode: BMD[1:0] bits

BALANCE WAIT TIME

The balance wait time control bits, BWT[2:0], set the interval between balancing operations in **Auto Balance mode**, as shown in Table 5.

TABLE 5. BALANCE WAIT TIME CONTROL BITS

BWT[2:0]	SECONDS
000	0
001	1
010	2
011	4
100	8
101	16
110	32
111	64

BALANCE STATUS POINTER

See "Balance Status Register".

BALANCE ENABLE

When all of the other balance control bits are properly set, setting the balance Enable bit to "1" starts the balance operation. The BEN bit can be set by writing directly to the Balance Setup register or by sending a Balance Enable command.

BALANCE MODE

Three methods of cell balance control are provided (see Table 6).

TABLE 6. BALANCE MODE CONTROL BITS

BMD[1:0]	BALANCE MODE
00	Off
01	Manual
10	Timed
11	Auto

In **Manual mode**, the host microcontroller directly controls the state of each MOSFET output. In **Timed mode**, the host microcontroller programs a balance duration value and selects which cells are to be balanced, then starts the balance operation. The ISL94212 turns all the FETs off when the balance duration has been reached. In **Auto Balance mode**, the host microcontroller programs the ISL94212 to control the balance MOSFETs to remove a programmed "charge delta" value from each cell. The ISL94212 does this by controlling the amount of charge removed from each cell over a number of cycles, rather than trying to balance all cells to a specific voltage.

Balance Status Register

TABLE 7. BALANCE STATUS REGISTER AND BALANCE STATUS POINTER

	BALANCE STATUS REGISTER (ADDRESS 6'h14)											
BSP [3:0]	BAL 12	BAL 11	BAL 10	BAL 9	BAL 8	BAL 7	BAL 6	BAL 5	BAL 4	BAL 3	BAL 2	BAL 1
0000	Reserved for Manual and Timed Balance modes											
0001	Auto balance status register 1											
0010	Auto balance status register 2											
0011	Auto balance status register 3											
0100	Auto balance status register 4											
0101	Auto balance status register 5											
0110	Auto balance status register 6											
0111	Auto balance status register 7											
1000	Auto balance status register 8											
1001	Auto balance status register 9											
1010	Auto balance status register 10											
1011	Auto balance status register 11											
1100	Auto balance status register 12											

The Balance Status register contents control which external balance FET is turned on during a balance event. Each bit in the Balance Status register controls one external balancing FET, such that Bit 0 [BAL1] controls the cell 1 FET and Bit 11 [BAL12] controls the FET for cell 12 (see Table 7.) Bits are set to enable the balancing for that cell and cleared to disable balancing.

The Balance Status register is a "multiple instance" register. There are 13 locations within this register. The Balance Status Pointer BSP[3:0] points to one of these 13 locations in the register (see Table 7). Only one location in the Balance Status register may be accessed at a time.

The Balance Status register instance at pointer location 0 (*BSP[3:0]* = 0000) is used for **Manual Balance mode** and **Timed Balance mode**. The Balance Status register instances at pointer locations 1 to 12 (BSP[3:0] = 4'h1 to 4'hC) are used for **Auto Balance mode**. The arrangement is illustrated in Table 7.

In **Auto Balance mode**, the ISL94212 increments the Balance Status pointer on each auto balance cycle to step through Balance Status register locations 1 to 12. This allows the programming of up to twelve different balance profiles for each Auto Balance operation. On each Auto Balance cycle, the Balance Status pointer increments by one. When the operation encounters a zero value at a pointer location, the Auto Balance operation returns to the pattern at location 1 and resumes balancing with that pattern.

More information about the Auto Balance mode is provided in "Auto Balance Mode" on page 27. Example balancing setup information is provided in "Auto Balance Mode Cell Balancing Example" on page 64.

Manual Balance Mode

Select **Manual Balance mode** by setting the balance mode bits BMD[1:0] to 2'b01.

To manually control the cells to be balanced, set the balance status pointer to zero: BSP[3:0] = 4'b0000. Then, program the cells to be balanced by setting bits in the Balance Status register (e.g., to balance cell 5, set the BAL5 bit to 1).

Enable balancing, either by setting the BEN bit in the balance setup register or by sending a balance enable command.

Disable balancing either by resetting the BEN bit or by sending a balance inhibit command.

The balance enable and balance inhibit commands may be used with the "Address All" device address to control all devices in a stack simultaneously.

Balancing is not possible in **Manual Balance mode** while the ISL94212 is in **Sleep mode**. If the watchdog timer is off and the *Sleep* command is received while the device is balancing, then balancing stops immediately and the device goes into the **Sleep mode**.

If the watchdog timer is active during balancing and the device receives the *Sleep* command, then balancing also stops immediately and the device goes into the **Sleep mode**, but the *WDTM* bit is set when the watchdog timer expires. (see Table 8).

TABLE 8. MANUAL AND TIMED BALANCE MODE WATCHDOG TIMER, BALANCE, SLEEP OPERATION

WATCHDOG TIMER	ACTIONS
Off	Receiving a Sleep command immediately stops balancing and the device enters the **Sleep mode**.
On	If the device has not received a Sleep command before the watchdog timer expires, then when the watchdog timer does expire, balance stops, the WDTM bit is set and the device enters the **Sleep mode**.
	Receiving a Sleep command immediately stops balancing and the device enters the **Sleep mode**. Then, when the watchdog timer expires, the WDTM bit is set.

The watchdog timer function protects the battery from excess discharge due to balancing, in the event that communications is lost while the part is in **Manual Balance mode**. All balancing ceases and the device goes into the **Sleep mode** if the watchdog timeout value is exceeded.

Timed Balance Mode

Select **Timed Balance mode** by setting the balance mode bits BMD[1:0] to 2'b10.

To set up a timed balance operation, set the balance status pointer to zero: BSP[3:0] = 4'b0000. Then program the cells to be balanced by setting bits in the Balance Status register (e.g., to balance cells 7 and 10, set BAL7 and BAL10 bits to 1).

Set the balance on time. The balance on time is programmable in 20 second intervals from 20 seconds to 42.5 minutes using BTM[6:0] bits. These bits are in locations [13:7] of the Watchdog/Balance Time register. See Tables 9 and 10 for details.

TABLE 9. WATCHDOG/BALANCE TIME REGISTER (ADDRESS 6'h15)

7	6	5 13	4 12	3 11	2 10	1 9	0 8
BTM0	WDG6	WDG5	WDG4	WDG3	WDG2	WDG1	WDG0
		BTM6	BTM5	BTM4	BTM3	BTM2	BTM1

TABLE 10. BALANCE CYCLE ON TIME SETTINGS

BTM[6:0]	MINUTES
0000000	Disabled
0000001	0.33
0000010	0.67
0000011	1.00
-	-
1111101	41.67
1111110	42.00
1111111	42.33

Enable balancing, either by setting the BEN bit in the balance setup register or by sending a balance enable command. The selected balance FETs (corresponding to the bits set in balance status register location 4'b0000) turn on when BEN is asserted and turn off when the balance timeout period is met.

Resetting BEN, either directly or by using the balance inhibit command stops the balancing functions and resets the timer values. When BEN is reasserted, or when a new balance enable command is received, balancing resumes, using the full time specified by the BTM[6:0] bits.

When the balance timeout period is met, the End Of Balance (EOB) bit in the Device Setup register is set and BEN is reset.

Balancing is not possible in the **Timed Balance mode** while the ISL94212 is in **Sleep mode**. If the watchdog timer is off and the Sleep command is received while the device is balancing, then balancing stops immediately and the device goes into **Sleep mode**.

If the watchdog timer is active during balance and the device receives the *Sleep* command, then balancing also stops immediately and the device enters **Sleep mode**, but the WDTM bit is set when the watchdog timer expires (see Table 8).

The watchdog can be disabled at any time by writing the watchdog password (6'h3A) to the watchdog password bits [WP5:0] in the Device Setup register (see Table 13 on page 30), and then writing 6'h00 to the watchdog timeout bits [WDG5:0] in the Watchdog/Balance time register (see Table 9).

Auto Balance Mode

Auto Balance mode provides the capability to perform balancing autonomously and in an intelligent manner. Thermal issues are accommodated by the provision of the multiple instance Balance Status register and a balance wait time. Cells are balanced with periodic measurements being performed at the balance cycle on time interval (see Table 10). These measurements are used to calculate the reduction in State of Charge (SOC) with each balancing cycle and to terminate balancing of a particular cell when the total SOC change target has been reached.

Select Auto Balance mode by setting the balance mode bits BMD[1:0] to 2'b11.

In **Auto Balance mode,** the ISL94212 cycles through each balance status register instance and turns on the balancing outputs corresponding to the bits set in each balance status register instance.

AUTO BALANCE SEQUENCE

The Auto Balance sequence is programmed using the "multiple instance" Balance Status register and the balance status pointer bits.

The first cycle of the auto balance operation begins with the balance status pointer at location 1, specifying the first Balance Status register instance. For the next auto balance cycle, the balance status pointer increments to location 2. For each subsequent cycle, the pointer increments to the next Balance Status register instance, until a zero value instance is encountered. At this point the sequence repeats from the

balance status register instance at the balance status pointer location 1 until all the cells have met their SOC adjustment value.

For example, to balance odd numbered cells during the first cycle and even numbered cells on the second cycle:
(see example in "Cell Balancing – Auto Mode" on page 64.)

- First set the balance status pointer to 1:
  BSP[3:0] = 0001.
- Specify the even bits by setting
  Balance Status register bits 0, 2, 4, 6, 8 and 10 to "1".
  Balance Status register = 14'h0555
- Set the balance status pointer to 2:
  BSP[3:0] = 0010.
- Specify the odd bits by setting
  Balance Status register bits 1, 3, 5, 7, 9 and 11 to "1".
  Balance Status register = 14'h0AAA
- Set the balance status pointer to 3:
  BSP[3:0] = 0011.
- Specify sequence termination by resetting all the bits in the *Balance Status* register to zero. The next cycle will go back to balance status pointer = 1.
  Balance Status register = 14'h0000.
- Leave the balance status pointer to 3:
  BSP[3:0] = 0011.

AUTO BALANCE TIMING

Set the desired interval between balancing cycles using the balance wait time bits BWT[2:0] (locations [4:2] of the Balance Setup register), see Table 4 on page 25 and Table 5 on page 25.

Set the balance cycle on time using the BTM[6:0] bits (locations [13:7] of the Watchdog/Balance Time register), see Tables 9 and 10 on page 27.

Set or clear the BDDS bit, Bit 7 in the Device Setup register, as required. If BDDS is set, then cell balancing is turned off 10ms before the cell voltage scan at the end of each balance cycle. If BDDS is cleared, then balance functions remain "on" during Auto Balance mode cell scan measurements. BDDS must be set in Auto Balance mode when using the standard battery connection configuration shown in Figure 37 on page 51.

AUTO BALANCE (DELTA SOC) VALUE

The next step in setting up an Auto Balance operation is to program the balance value for each cell. The balance value (delta SOC) is the difference between the present charge in a cell and the desired charge for that cell.

The method for calculating the state of charge for a cell is left to the system designer. Typically, determining the state of charge is dependent on the chosen cell type and manufacturer, is dependent on cell voltage, charge and discharge rates, temperature, age of the cell, number of cycles, and other factors. Tables for determining SOC are often available from the battery cell manufacturer.

The balance value itself is a function of the current SOC, required SOC, balancing leg impedance, and sample interval. This value is calculated by the host microcontroller for each cell. The balancing leg impedance is made up of the external balance FET and balancing resistor. The sample interval is equal to the balance cycle on time period (e.g., each cell voltage is sampled at the end of the balance on time).

The balancing value B for each cell is calculated using the formula shown in Equation 1. (See also "Balance Value Calculation Example" on page 64):

$$B = \frac{8191}{5} \times (CurrentSOC - TargetSOC) \times \frac{Z}{dt} \quad \text{(EQ. 1)}$$

Where:

B = the balance register value
CurrentSOC = the present SOC of the cell (Coulombs)
TargetSOC = the required SOC value (Coulombs)
Z = the balancing leg impedance (ohms)
dt = the sampling time interval
(Balance cycle on time in seconds)
8191/5 = a voltage to Hex conversion value

The balancing leg impedance is normally the sum of the balance FET $r_{DS(ON)}$ and the balance resistor.

The balancing value (B) can also be defined as in the set of equations following. Auto balance is guided by Equations 2 and 3:

$$SOC = I \times t = \frac{V}{Z} \times t \quad \text{(EQ. 2)}$$

$$B = SOC \times \frac{Z}{dt} = \frac{V}{Z} \times t \times \frac{Z}{dt} = \frac{V}{dt} \times t \quad \text{(EQ. 3)}$$

Where:

dt = Balance cycle on time
t = Total balance time

Looking at Equations 2 and 3, the impedance drops out of the equation, leaving only voltage and time elements. Thus, "B" becomes a collection of voltages that integrate during the balance cycle on time, and accumulate over the total balance time period, to equal the programmed delta capacity.

Twelve 28-bit registers are provided for the balance value for each cell. The balance values are programmed for all cells as needed using Balance Value registers 6'h20 to 6'h37 (see Table 11 for the contents of the CELL1 Balance Values Register).

TABLE 11. BALANCE VALUES REGISTER CELL1 (ADDRESS 6'h20, 6'h21)

ADDR	7 15	6 14	5 13	4 12	3 11	2 10	1 9	0 8
6'20	B0107	B0106	B0105	B0104	B0103	B0102	B0101	B0100
			B0113	B0112	B0111	B0110	B0109	B0108
6'21	B0121	B0120	B0119	B0118	B0117	B0116	B0115	B0114
			B0127	B0126	B0125	B0124	B0123	B0122

At the end of each balance cycle on time interval the ISL94212 measures the voltage on each of the cells that were balanced during that interval. The measured values are then subtracted from the balance values for those cells. This process continues until the balance value for each cell is zero, at which time the auto balancing process is complete.

AUTO BALANCE OPERATION

Once all of the cell balance FET controls, the balance values and the timers are set up, balance is enabled either by setting the BEN bit in the Balance Setup register or by sending a balance enable command.

Once enabled, the ISL94212 cycles through each instance of the Balance Status register for the duration given by the balance timeout. Between each balance status register instance, the device does a scan all operation and inserts a delay equal to the balance wait time. The process continues with the balance status pointer wrapping back to 1 until all the balance value registers equal zero. If one cell balance value register reaches zero before the others, balancing for that cell stops, but the others continue.

Resetting BEN, either directly or by using the Balance Inhibit command, stops the balancing functions but maintains the current Balance Value register contents. Auto balancing continues from the balance status register location 1 when BEN is reasserted.

When auto balancing is complete, the End of balance (EOB) bit in the Device Setup register is set and BEN bit is reset.

Balancing is not possible using the **Auto Balance Mode** while the ISL94212 is in **Sleep mode**. If the sleep command is received while the device is balancing (and the watchdog timer is off) then balancing continues until it is finished and device enters **Sleep mode**. If the watchdog timer is active during the **Auto Balance mode** and the device receives the sleep command, then balancing immediately stops and device enters **Sleep mode**. The WDTM bit is set when the watchdog timer expires (see Table 12).

TABLE 12. AUTO BALANCE MODE WATCHDOG TIMER, BALANCE, SLEEP OPERATION

WATCHDOG TIMER	ACTIONS
Off	Receiving a Sleep command puts the device into **Sleep mode** when the auto balance operation is finished.
On	If the device has not received a Sleep command, then when the watchdog timer expires, balance stops, the WDTM bit is set and the device enters **Sleep mode**.
	When the device receives a Sleep command, balance stops immediately. When the watchdog timer expires, the WDTM bit is set and the device enters **Sleep mode**.

The watchdog can be disabled at any time by writing the watchdog password (6'h3A) to the watchdog password bits [WP5:0] in the Device Setup register (see Table 13 on page 30) and then writing 6'h00 to the watchdog timeout bits [WDG5:0] in the Watchdog/Balance Time register (see Table 9 on page 27).

Balance FET Drivers

External balancing FETs are controlled by current sources or current sinks attached to the cell balancing (CB) pins. The gate voltage on each FET is then controlled by a locally placed gate-to-source resistor. Voltage clamps are included at each CB output to limit the maximum gate drive voltage. Series gate resistors are used to protect both the external FET and internal IC circuits from external voltage transient effects. An internal gate-to-source connected resistor is used to provide a redundant gate discharge path.

A mix of N-channel and P-channel devices are used for the external FETs in order to remove the need for a charge pump. Cell 12, Cell 11 and Cell 10 balance positions use P-channel devices. The remaining positions use N-channel devices. The basic balance FET drive arrangement is shown in Figure 30.

Additional circuit guidelines are provided in the "Typical Applications Circuits" on page 50.

Reduced cell counts for fewer than 12 cells are accommodated by removing connections to the cells in the middle of the stack first. The top and bottom cell locations are always occupied. See "Operating the ISL94212 with Reduced Cell Counts" on page 56 for suggested cell configurations when using fewer than 12 cells.

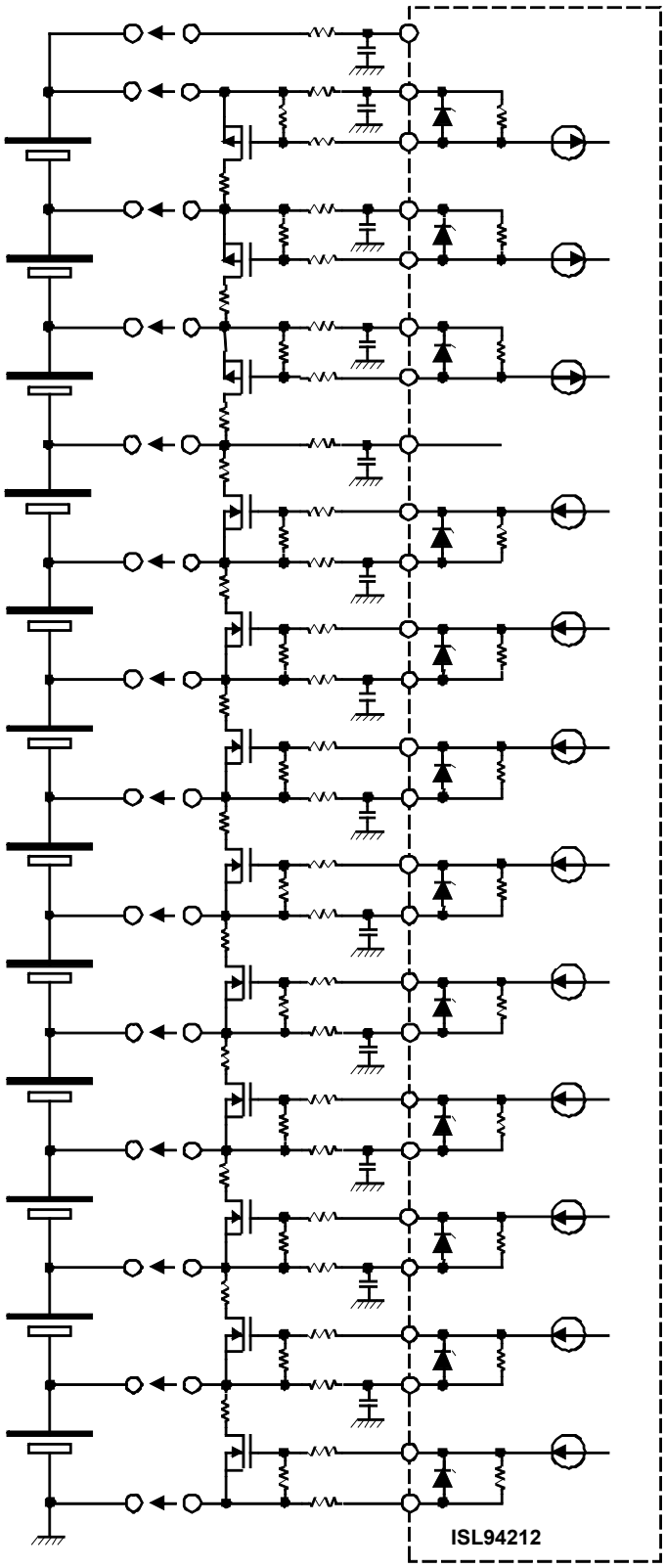


FIGURE 30. EXTERNAL FET DRIVING CIRCUITS

Device Setup Register

TABLE 13. DEVICE SETUP REGISTER (ADDRESS 6'h19)

7	6	5 13	4 12	3 11	2 10	1 9	0 8
BDDS		ISCN	SCAN	EOB		PIN37	PIN39
		WP5	WP4	WP3	WP2	WP1	WP0

BDDS

A function is provided to allow any cell balancing activity to be paused while measuring cell voltages in scan continuous mode and auto balance mode. This is controlled by the BDDS bit in the Device Setup register (address 6'h19) (see Table 13). If BDDS is set, then cell balancing is inhibited during cell voltage measurement and for 10ms before the cell voltage scan. Balancing is reenabled at the end of the scan. This function only applies during the scan continuous mode and the auto balance mode. It is up to the host microcontroller to manually stop balancing functions (if required) before sending a scan or measure command.

WATCHDOG PASSWORD

Before writing a zero to the watchdog timer, which turns off the timer, it is necessary to write a password to the [WP5:0] bits. The password value is 6'h3A.

EOB

This End of balance bit indicates that a **Timed Balance mode** or an **Auto Balance mode** has completed.

SCAN

This bit is set in response to a Scan Continuous command and cleared by the Scan Inhibit command.

ISCN, PIN37, PIN39

The ISCN bit is used in the Open Wire scan. PIN37 and PIN39 bits show the state of the respective device pins.

Cell Balance Enabled Register

TABLE 14. CELLS BEING BALANCED REGISTER (ADDRESS 6'h3B)

7	6	5 13	4 12	3 11	2 10	1 9	0 8
CBEN 8	CBEN 7	CBEN 6	CBEN 5	CBEN 4	CBEN 3	CBEN 2	CBEN 1
				CBEN 12	CBEN 11	CBEN 10	CBEN 9

To facilitate the system monitoring of the cell balance operation, the ISL94212 has a register that shows the present state of the balance drivers. Table 14 shows the Cells Being Balanced register, located on Page 2 at address 6'h3B. If the bit is "1" it indicates that the CBn output is enabled. A "0" indicates that the CBn output is disabled.

System Configuration

The ISL94212 provides two communications systems. An SPI synchronous port is provided for communication between a microcontroller and the ISL94212. For standalone (non-daisy chain) systems, the SPI port is the only port needed. In systems where there is more than one ISL94212, daisy chain (asynchronous) ports provide communication between the SPI port on the Master and other ISL94212 devices.

The communications setup is controlled by the COMMS SELECT 1 and COMMS SELECT 2 pins on each device. These pins specify whether the ISL94212 is a standalone device, the daisy chain master, the daisy chain top, or a middle position in the daisy chain. See Figures 31 and 32 and Table 15. This configuration also specifies the use of SPI or daisy chain on the communication ports.

TABLE 15. COMMUNICATIONS MODE CONTROL

COMMS SELECT 1	COMMS SELECT 2	PORT 1 COMM	PORT 2 COMM	COMMUNICATIONS CONFIGURATION
0	0	SPI (Full Duplex)	Disabled	Standalone
0	1	SPI (Half Duplex)	Enabled	Daisy Chain, Master device setting
1	0	Daisy Chain	Disabled	Daisy Chain, Top device setting
1	1	Daisy Chain	Enabled	Daisy Chain Middle device setting

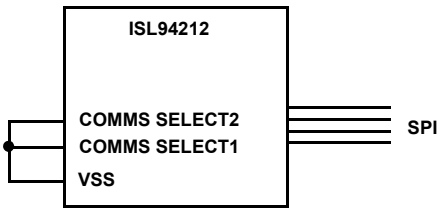


FIGURE 31. NON-DAISY CHAIN COMMUNICATIONS CONNECTIONS AND SELECT

All communications are conducted through the SPI port in single 8-bit byte increments. The MSB is transmitted first and the LSB is transmitted last.

Commands in non-daisy chain systems are composed of a read/write bit, page address (3 bits), data address (6 bits) and data (6 bits). Commands in daisy chain systems are composed of a device address (4 bits), a read/write bit, page address (3 bits), data address (6 bits), data (6 bits), and CRC (4 bits).

Commands and data are memory mapped to 14-bit data locations. The memory map is arranged in pages. Pages 1 and 2 are used for volatile data. Page 3 contains the action and communications administration commands. Page 4 accesses non-volatile memory. Page 5 is used for factory test.

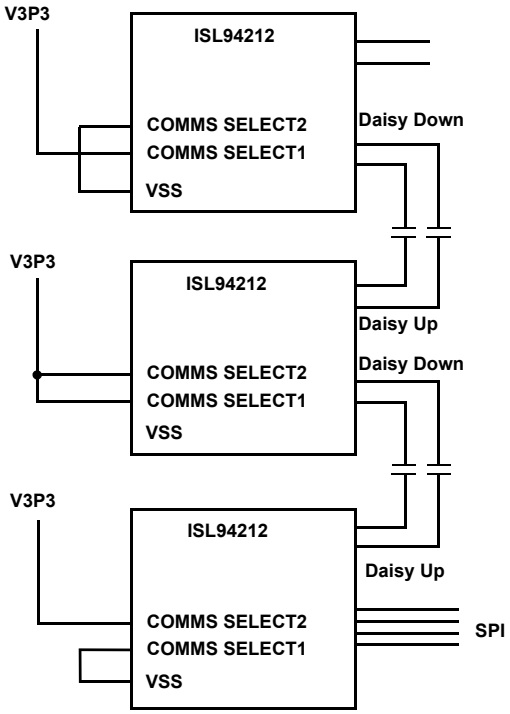


FIGURE 32. DAISY CHAIN COMMUNICATIONS CONNECTIONS AND SELECTION

SPI Interface

The ISL94212 operates as a SPI slave capable of bus speeds up to 2Mbps. Four lines make up the SPI interface: SCLK, DIN, DOUT and $\overline{CS}$. The SPI interface operates in either full duplex or half duplex mode depending on the daisy chain status of the part.

The DOUT line is normally tri-stated (high impedance) to allow use in a multidrop bus. DOUT is only active when $\overline{CS}$ is low.

Full Duplex Operation

In non-daisy chain applications, the SPI bus operates as a standard, full duplex, SPI port. Read and write commands are sent to the ISL94212 in 8-bit blocks. $\overline{CS}$ is taken high between each block. Data flow is controlled by interpreting the first bit of each transaction and counting the requisite number of bytes. It is the host microcontroller's responsibility to ensure that commands are correctly formulated as an incorrect formulation, (e.g., read bit instead of write bit), would cause the port to lose synchronization. There is a timeout period associated with the $\overline{CS}$ inactive (high) condition, which resets all the communications counters. This effectively resets the SPI port to a known starting condition. If $\overline{CS}$ stays high for more than 100µs then the SPI state machine resets.

The ISL94212 responds to read commands by loading the requested data to its output buffer. The output buffer contents are then loaded to the shift register when $\overline{CS}$ goes low and are shifted out on the *DOUT* line on the falling edges of *SCLK*. This sequence continues until all the requested data has been sent. All single register read commands and responses are 2-bytes long. All bytes are handled in pairs during device reads. Device writes are 3-bytes long.

A pending device response from a previous command is sent by the ISL94212 during the first 2 bytes of the 3-byte Write transaction. The third byte from the ISL94212 is then discarded by the host microcontroller. This maintains sequencing during 3-byte (Write) transactions.

Half Duplex Operation

The SPI operates in half duplex mode in Daisy Chain applications (see Table 15 on page 31). Data flow is controlled by a handshake system using the $\overline{\text{DATA READY}}$ and $\overline{\text{CS}}$ signals. $\overline{\text{DATA READY}}$ is controlled by the ISL94212. $\overline{\text{CS}}$ is controlled by the host microcontroller. This handshake accommodates the delay between command receipt and device response due to the latency of the daisy chain communications system.

Responses from stack devices are received by the stack Master (stack bottom device). The stack Master then asserts its $\overline{\text{DATA READY}}$ output once the first full data byte is available. The host microcontroller responds by asserting $\overline{\text{CS}}$ and clocking the data out of the *DOUT* port. The $\overline{\text{DATA READY}}$ line is then cleared and DOUT is tri-stated in response to $\overline{\text{CS}}$ being taken high. In this mode the DIN and DOUT lines may be connected externally.

Half duplex communications are conducted using the $\overline{\text{DATA READY}}$/$\overline{\text{CS}}$ handshake as follows:

1. The host microcontroller sends a command to the ISL94212 using the $\overline{\text{CS}}$ line to select the ISL94212 and clocking data into the ISL94212 DIN pin.
2. The ISL94212 asserts $\overline{\text{DATA READY}}$ low when it is ready to send data to the host microcontroller. When $\overline{\text{DATA READY}}$ is low, the ISL94212 is in transmit mode and will ignore any data on DIN.
3. The host microcontroller asserts $\overline{\text{CS}}$ low and clocks 8 bits of data out of DOUT using *SCLK*.
4. The host microcontroller then raises $\overline{\text{CS}}$. The ISL94212 responds by raising $\overline{\text{DATA READY}}$ and tri-stating DOUT.
5. The ISL94212 reasserts $\overline{\text{DATA READY}}$ for the next byte and so on.

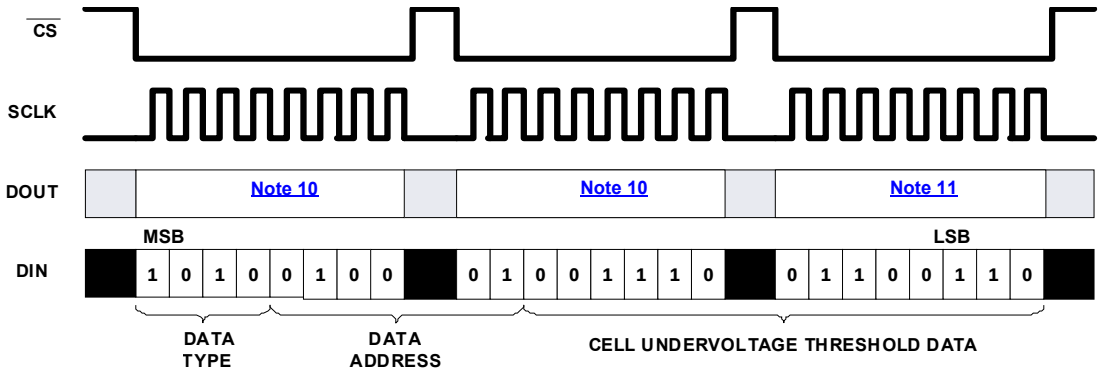
The host microcontroller must service the ISL94212 if $\overline{\text{DATA READY}}$ is low before sending further commands. Any data sent to DIN while $\overline{\text{DATA READY}}$ is low is ignored by the ISL94212.

A 4 byte data buffer is provided for SPI communications. This accommodates all single transaction responses. Multiple responses, such as those that may be produced by a device detecting an error would overflow this buffer. It is important therefore that the host microcontroller reads the first byte of data before a 5th byte arrives on the Master device's daisy chain port so as not to risk losing data.

The $\overline{\text{DATA READY}}$ output from the ISL94212 is not asserted if $\overline{\text{CS}}$ is already asserted. It is possible for the microcontroller to interrupt a sequential data transfer by asserting $\overline{\text{CS}}$ before the ISL94212 asserts $\overline{\text{DATA READY}}$. This causes a conflict with the communications and is not recommended. A conflict created in this manner would be recognized by the microcontroller either not receiving the expected response or receiving a communications failure notification.

Interface timing for full and half duplex SPI transfers are shown in Figures 2 and 3 on page 14.

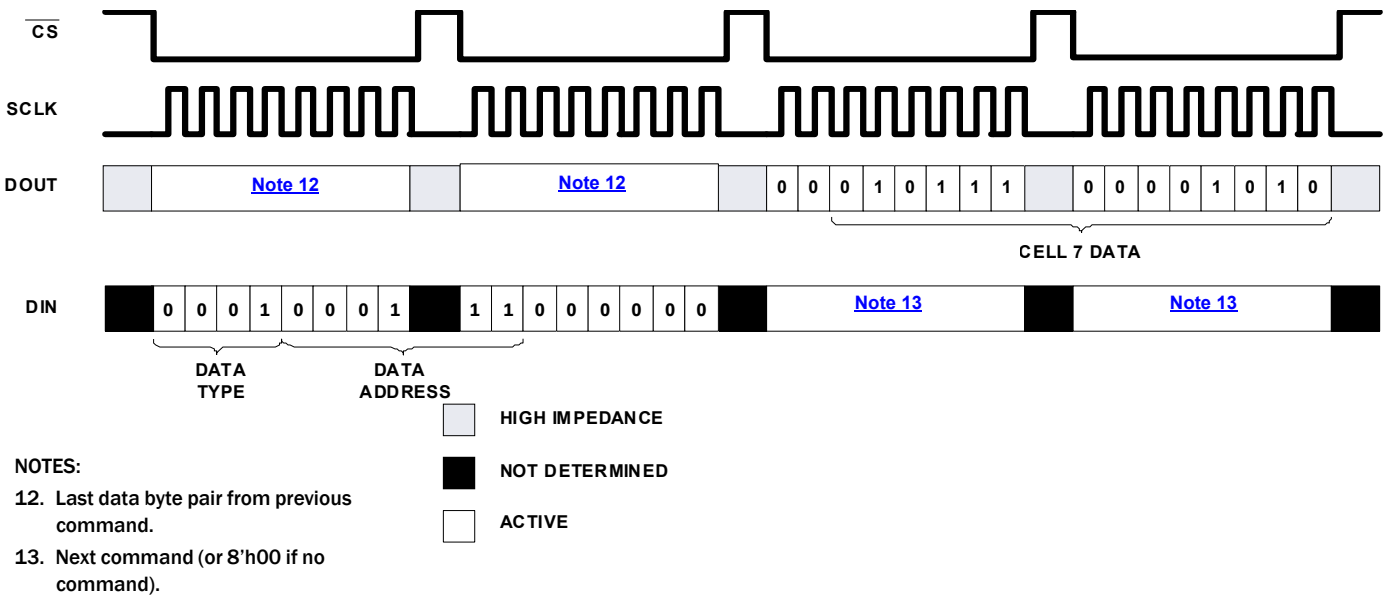
Examples of full duplex SPI read and write sequences are shown in Figures 33 and 34.



NOTES:

10. Last data byte pair from previous command.
11. Not defined.

FIGURE 33. SPI WRITE EXAMPLE: WRITE UNDERVOLTAGE THRESHOLD DATA



NOTES:

12. Last data byte pair from previous command.
13. Next command (or 8'h00 if no command).

FIGURE 34. SPI READ EXAMPLE: READ CELL 7 DATA

Non-daisy Chain Systems

In non-daisy chain (standalone) systems, all communications sent from the master are 2 or 3 bytes in length. Data read and action commands are 2 bytes. Data writes are 3 bytes. Device responses are 2 bytes in length and contain data only.

Commands are composed of a $\overline{\text{read}}$/write bit, page (3 bits), data address (6 bits) and data (6 bits).

Action commands, such as scan and communications administration commands are treated as reads.

Non-daisy chain communications are conducted without CRC (Cyclical Redundancy Check) error detection.

The rules for non-daisy chain installations are shown in Table 16.

TABLE 16. ISL94212 DATA INTERPRETATION RULES FOR NON-DAISY CHAIN INSTALLATIONS

FIRST BIT IN SEQUENCE	PAGE	DATA ADDRESS	INTERPRETATION
0	011	001000	Measure command. Last six bits of transmission contain element address.
0	Any	All other	Device read or action command. Last six bits of transmission are zero.
1	Any	Any	Device write command.

Normal Communications

Non-daisy chain devices do not generate a response to write or system level commands. Data integrity may be verified by reading register contents after writing. The ISL94212 does nothing in response to a write or administration command that is not recognized. An unrecognized read command returns 16'h0000. An incomplete command, such as may occur if communications are interrupted, is registered as an unrecognized command either when $\overline{\text{CS}}$ is taken high or after a timeout period. The communications interface is reset after the timeout period.

The following commands have no meaning in non-daisy chain systems such as:

- Identify
- ACK
- NAK

The Sleep and Wakeup commands are sent as normal commands.

The device resets on receipt of the Reset command.

Alarm Signals

The $\overline{\text{FAULT}}$ logic output is asserted low in response to a fault condition. The output then remains low until the bits of the Fault Status register are reset. The host microcontroller writes 14'h0000 to this register to clear the bits. Bits in the fault data registers must first be cleared before the associated bits in the Fault Status register can be cleared. Additionally, the fault status of each part may be obtained at any time by reading the Fault Status register.

The $\overline{\text{FAULT}}$ logic output is asserted in **Sleep mode**, if a fault has been detected and has not been cleared.

Communication Faults

There is no specific response to a communications fault. A fault is indicated by an absence of normal communications function.

Non-daisy chain device responses are 2-byte sequences containing 14-bit data with leading zeros. Non-daisy chain responses are conducted without CRC (Cyclical Redundancy Check) error detection.

Fault Response in Sleep Mode

When a standalone device is in **Sleep mode**, the device may still detect faults if operating in the **Scan Continuous mode**. If an error occurs, the $\overline{\text{FAULT}}$ output pin is asserted low.

Example Communications

An example read response is shown in Figure 35.

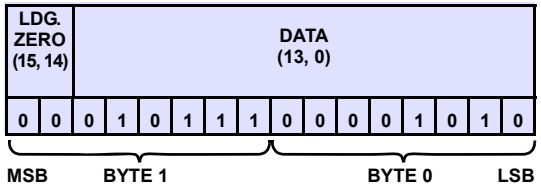


FIGURE 35. NON-DAISY CHAIN DEVICE RESPONSE EXAMPLE: CELL 7 VOLTAGE = 16'h170A (3.6V)

Examples of the various write command structures for non-daisy chain installations are shown in Figures 36A through 36F.

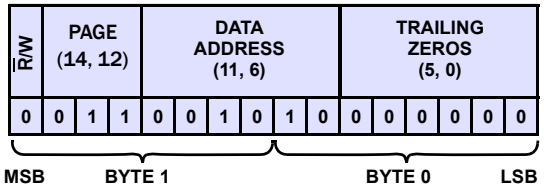


FIGURE 36A. DEVICE LEVEL COMMAND: *SLEEP*

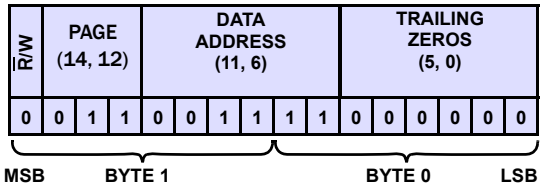


FIGURE 36B. DEVICE LEVEL COMMAND: *WAKE UP*

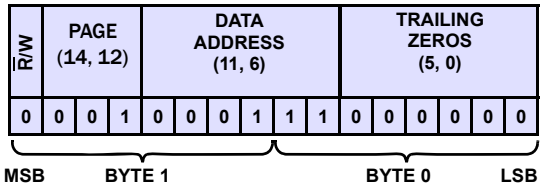


FIGURE 36C. DEVICE READ: GET CELL 7 DATA

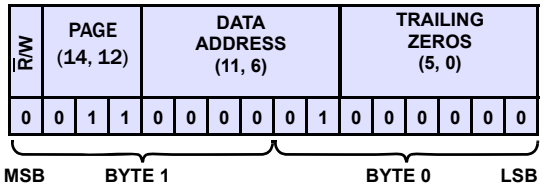


FIGURE 36D. DEVICE LEVEL COMMAND: *SCAN VOLTAGES*

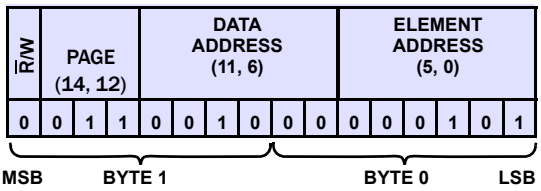


FIGURE 36E. DEVICE LEVEL COMMAND: *MEASURE* CELL 5 VOLTAGE

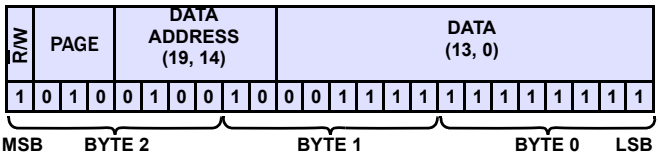


FIGURE 36F. DEVICE WRITE: WRITE EXTERNAL TEMPERATURE LIMIT = 14'h0FFF

FIGURE 36. NON-DAISY CHAIN DEVICE READ AND WRITE EXAMPLES

Daisy Chain Systems

The daisy chain communication is intended for use with large stacks of battery cells where a number of ISL94212 devices are used.

Memory Checksum

There are two checksum operations, one for the EEPROM and one for the Page 2 registers.

Two registers are provided to verify the contents of EEPROM memory. One (Page 4, address 6'h3F) contains the correct checksum value, which is calculated during factory testing at Intersil. The other (Page 5, address 6'h00) contains the checksum value calculated each time the nonvolatile memory is loaded to shadow registers, either after a power cycle or after a device reset. An inequality between these two numbers indicates corruption of the shadow register contents (and possible corruption of EEPROM data). The external microcontroller needs to compare the two registers, since it is not automatic. Resetting the device (using the Reset command) reloads the shadow registers. A persistent difference between these two register values indicates EEPROM corruption.

All Page 2 registers (device configuration registers) are subject to a checksum calculation. A Calculate Register Checksum command calculates the Page 2 checksum and saves the value internally (it is not accessible). The Calculate Register Checksum command may be run any time, but should be sent whenever a Page 2 register is changed.

A Check Register Checksum command recalculates the Page 2 checksum and compares it to the internal value. The occurrence of a Page 2 checksum error sets the PAR bit in the Fault Status register and causes a Fault response accordingly. The normal response to a PAR error is for the host microcontroller to rewrite the Page 2 register contents. A PAR fault also causes the device to cease any scanning or cell balancing activity.

See items 42 through 49 in Table 18 on page 36.

Settling Time Following Diagnostic Activity

The majority of diagnostic functions within the ISL94212 do not affect other system activity and there is no requirement to wait before conducting further measurements. The exceptions to this are the open wire test and cell balancing functions.

Open Wire Test

The open wire test loads each VCn pin in turn with 150µA or 1mA current. This disturbs the cell voltage measurement while the test is being applied e.g., a 1mA test current applied with an input path resistance of 1kΩ reduces the pin voltage by 1V. The time required for the cell voltage to settle following the open wire test is dependent on the time constant of components used in the cell input circuit. The standard input circuit (Figure 37 on page 51) with the components given in Table 21 on page 55 provide settling to within 0.1mV in approximately 2.8ms. This time should be added at the end of each open wire scan to allow the cell voltages to settle.

Cell Balancing

The standard applications circuit (Figure 37 on page 51) configures the balancing circuits so that the cell input measurement reads close to zero volts when balancing is activated. There are time constants associated with the turn-on and turn-off characteristics of the cell balancing system that must be allowed for when conducting cell voltage measurements.

The turn-on time of the balancing circuit is primarily a function of the 25µA drive current of the cell balancing output and the gate charge characteristic of the MOSFET and needs to be determined for a particular setup. Turn-on settling times to within 2mV of final “on” value are typically less than 5ms.

The turn-off time is a function of the MOSFET gate charge and the VGS connected resistor and capacitor values (for example R_{27} and C_{27} in Figure 37 on page 51) and is generally longer than the turn-on time. As with the turn-on case, the turn-off time needs to be determined for the particular components used. Turn-off settling times in the range 10ms to 15ms are typical for settling to within 0.1mV of final value.

Fault Signal Filtering

Filtering is provided for the cell overvoltage, cell undervoltage, V_{BAT} open and VSS open tests. These fault signals use a totalizing method in which an unbroken sequence of positive results is required to validate a fault condition. The sequence length (number of sequential positive samples) is set by the [TOT2:0] bits in the Fault Setup register. See Table 17.

Separate filter functions are provided for each cell input and for the V_{BAT} and VSS open faults. The filter is reset whenever a test results in a negative result (no fault). All filters are reset when the Fault Status register [TOT2:0] bits are changed. When a fault is detected, the [TOT2:0] bits should be rewritten.

The cell overvoltage, cell undervoltage, V_{BAT} open and VSS open faults are sampled at the same time at the end of a Scan Voltages command. The cell undervoltage and cell overvoltage signals are also checked following a Measure cell voltage command.

Fault Diagnostics

The ISL94212 incorporates extensive fault diagnostics functions, which include cell overvoltage and undervoltage as well as open cell input detection. The current status of all faults is accessible using the ISL94212 registers. Table 18 shows a summary of commands and responses for the various fault diagnostics functions.

TABLE 17. FAULT TOTALIZING TIME (ms) AS A FUNCTION OF SCAN INTERVAL AND NUMBER OF TOTALIZED SAMPLES

SCAN INTERVAL CODE	SCAN INTERVAL (ms)	TOTALIZE – FAULT SETUP REGISTER							
		1 000	2 001	4 010	8 011	16 100	32 101	64 110	128 111
0000	16	16	32	64	128	256	512	1024	2048
0001	32	32	64	128	256	512	1024	2048	4096
0010	64	64	128	256	512	1024	2048	4096	8192
0011	128	128	256	512	1024	2048	4096	8192	16384
0100	256	256	512	1024	2048	4096	8192	16384	32768
0101	512	512	1024	2048	4096	8192	16384	32768	65536
0110	1024	1024	2048	4096	8192	16384	32768	65536	131072
0111	2048	2048	4096	8192	16384	32768	65536	131072	262144
1000	4096	4096	8192	16384	32768	65536	131072	262144	524288
1001	8192	8192	16384	32768	65536	131072	262144	524288	1048576
1010	16384	16384	32768	65536	131072	262144	524288	1048576	2097152
1011	32768	32768	65536	131072	262144	524288	1048576	2097152	4194304
1100	65536	65536	131072	262144	524288	1048576	2097152	4194304	8388608

TABLE 18. SUMMARY OF FAULT DIAGNOSTICS COMMANDS AND RESPONSES

ITEM	DIAGNOSTIC FUNCTION	ACTION REQUIRED	REGISTER READ/WRITE	COMMENTS
1	Static fault detection functions.	Check Fault Status (or look for normal fault response)	Read Fault Status register	The main internal functions of the ISL94212 are monitored continuously. Bits are set in the Fault Status register is response to faults being detected in these functions.
2	Oscillator check function	Check for device in **Sleep mode** if stack returns a Communications Failure response.		Oscillator faults are detected as part of the Static Fault detection functions. The response to an oscillator fault detection is to set the *OSC* bit in the Fault Status register and then to enter **Sleep mode**. A sleeping device does not respond to normal communications, producing a communications failure notification from the next device down the stack. The normal recovery procedure is send repeated Sleep and Wakeup commands ensure all devices are awake.
3	Cell overvoltage	Set cell overvoltage limit	Write Overvoltage Limit register	Full scale value 14'h1FFF = 5V
4		Set fault filter sample value	Write TOT bits in Fault Setup register	Default is 3'b011 (8 samples) - (see "Fault Setup:" on page 42)
5		Identify which inputs have cells connected	Write Cell Setup register	A '0' bit value indicates cell is connected. A '1' bit value indicates no cell connected to this input. The overvoltage test is not applied to unconnected cells.
6		Scan cell voltages	Send Scan Voltages command	A cell overvoltage condition is flagged after a number of sequential overvoltage conditions are recorded for a single cell. The number is programmed above in item 4.
7		Check fault status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
8		Check overvoltage fault register	Read Overvoltage Fault register	Only required if the Fault Status register returns a fault condition.
9		Reset fault bits		Reset bits in Overvoltage Fault register followed and bits in Fault Status register.
10		Reset fault filter		Change the value of the [TOT2:0] bits in the Fault Setup register and then change back to the required value. This resets the filter. The filter is also reset if a false overvoltage test is encountered.
11	Cell Undervoltage	Set cell Undervoltage Limit	Write Undervoltage Limit register	Full scale value 14'h1FFF = 5V
12		Set fault filter sample value	Write TOT Bits in Fault Setup register	Default is 3'b011 (8 samples)
13		Identify which inputs have cells connected	Write Cell Setup register	A '0' bit value indicates cell is connected. A '1' bit value indicates no cell connected to this input. The undervoltage test is not applied to unconnected cells.
14		Scan cell voltages	Send Scan Voltages command	A cell undervoltage condition is flagged after a number of sequential undervoltage conditions are recorded for a single cell. The number is programmed above in item 12.
15		Check Fault Status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
16		Check undervoltage fault register	Read undervoltage Fault register	Only required if the Fault Status register returns a fault condition.
17		Reset fault bits		Reset bits in undervoltage fault register followed by bits in Fault Status register.
18		Reset fault filter		Change the value of the [TOT2:0] bits in the Fault Setup register and then change back to the required value. This resets the filter. The filter is also reset if a false undervoltage test is encountered.
19	V_{BAT} or VSS Connection Test	Set fault filter sample value	Write TOT bits in Fault Setup register	Default is 3'b011 (8 samples)

TABLE 18. SUMMARY OF FAULT DIAGNOSTICS COMMANDS AND RESPONSES (Continued)

ITEM	DIAGNOSTIC FUNCTION	ACTION REQUIRED	REGISTER READ/WRITE	COMMENTS
20		Scan cell voltages	Send Scan Voltages command	A open condition on V_{BAT} or VSS is flagged after a number of sequential open conditions are recorded for a single cell. The number is programmed in item 19.
21		Check Fault Status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
22		Reset fault bits		Reset bits in the Fault Status register.
23		Reset fault filter		Change the value of the [TOT2:0] bits in the Fault Setup register and then change back to the required value. This resets the filter. The filter is also reset if a false open test is encountered.
24	Open Wire Test	Set Scan current value	Write Device Setup register: ISCN = 1 or 0	Sets scan current to 1mA (recommended) by setting ISCN = 1. Or, set the scan current to 150µA by setting ISCN = 0.
25		Identify which inputs have cells connected	Write Cell Setup register	A '0' bit value indicates cell is connected. A '1' bit value indicates no cell connected to this input. Cell inputs VC2 to VC12: the open wire detection system is disabled for cell inputs with a '1' setting in the Cell Setup register. Cell inputs VC0 and VC1 are not affected by the Cell Setup register.
26		Activate Scan Wires function	Send Scan Wires command	Wait for Scan Wires to complete.
27		Check Fault Status	Read Fault Status register	The device sends the *Fault Status* register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
28		Check Open Wire Fault register	Read Open Wire Fault register	Only required if the Fault Status register returns a fault condition.
29		Reset fault bits		Reset bits in Open Wire Fault register followed by bits in Fault Status register.
30	Over-temperature Indication	Set External Temperature limit	Write External Temp Limit register	Full scale value 14'h3FFF = 2.5V
31		Identify which inputs are required to be tested	Write Fault Setup register bits TST1 to TST4	A '1' bit value indicates input is tested. A '0' bit value indicates input is not tested.
32		Scan temperature inputs	Send Scan Temperatures command	An over-temperature condition is flagged immediately if the input voltage is below the limit value.
33		Check Fault Status	Read Fault Status register	The device sends the *Fault Status* register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
34		Check Over-temperature fault register	Read Over-temperature Fault register	Only required if the Fault Status register returns a fault condition.
35		Reset fault bits		Reset bits in Over-temperature Fault register followed by bits in Fault Status register.
36	Reference Check Function	Read reference coefficient A	Read Reference Coefficient A register	
37		Read reference coefficient B	Read Reference Coefficient B register	
38		Read reference coefficient C	Read Reference Coefficient C register	
39		Scan temperature inputs	Send Scan Temperatures command	
40		Read reference voltage value	Read Reference Voltage register	
41		Calculate voltage reference value		See Voltage Reference Check Calculation in the "Worked Examples" on page 62 of this data sheet.

TABLE 18. SUMMARY OF FAULT DIAGNOSTICS COMMANDS AND RESPONSES (Continued)

ITEM	DIAGNOSTIC FUNCTION	ACTION REQUIRED	REGISTER READ/WRITE	COMMENTS
42	Register Checksum	Calculate register checksum value	Send Calc Register Checksum command	This causes the ISL94212 to calculate a checksum based on the current contents of the page 2 registers. This action must be performed each time a change is made to the register contents. The checksum value is stored for later comparison.
43		Check register checksum value	Send Check Register Checksum command	The checksum value is recalculated and compared to the value stored by the previous Calc Register Checksum command. The PAR bit in the Fault Status register is set if these two numbers are not the same.
44		Check Fault Status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected, if the register value is zero before the fault is detected.
45		Re-write registers	Load all page 2 registers with their correct values.	This is only required if a PAR fault is registered. It is recommended that the host reads back the register contents to verify values prior to sending a Calc Register Checksum command.
46		Reset fault bits		Reset bits in the Fault Status register.
47	EEPROM MISR Checksum	Read checksum value stored in EEPROM	Read the EEPROM MISR Register	
48		Read checksum value calculated by ISL94212	Read the MISR Checksum register	The checksum value is calculated each time the EEPROM contents are loaded to registers, either following the application of power, cycling the EN pin followed by a host initiated *Reset* command, or simply the host issuing a Reset command.
49		Compare checksum values		Correct function is indicated by the two values being equal. Memory corruption is indicated by an unequal comparison. In this event the host should send a Reset command and repeat the check process.

Sleep Mode

Devices enter **Sleep mode** in response to a Sleep command, a watchdog time out or in response to an oscillator fault. Devices wakeup in response to a Wakeup command or to a Scan Continuous cycle if the device was set to **Sleep mode** with **Scan Continuous mode** active.

Using a Sleep command or Wakeup command does not require that the devices in a stack are identified first. They do not need to know their position in the stack.

In a daisy chain system, the Sleep command must be written using the Address All stack address: 1111. The command is not recognized if sent with an individual device address and causes the addressed device to respond NAK. The top stack device responds ACK on receiving a valid Sleep command.

Having received a valid Sleep command, devices wait before entering the **Sleep mode**. This is to allow time for the top stack device to respond ACK, or for all devices that don't recognize the command to respond NAK, and for the host microcontroller to respond with another command. Receipt of any valid communications on port 1 of the ISL94212 before the wait period expires cancels the Sleep command. Receipt of another Sleep command restarts the wait timers. Table 19 provides the maximum wait time for various daisy chain data rates. The communications fault checking timeout is not applied to the Sleep command. A problem with the communications is indicated by a lack of response to the host microcontroller. The host microcontroller may choose to do nothing if no response is received in which case devices that received the Sleep command go to sleep when the wait time expires. Devices that do not receive the message go to sleep when their watchdog timer expires (as long as this is enabled).

TABLE 19. MAXIMUM WAIT TIME FOR DEVICES ENTERING SLEEP MODE

	MAXIMUM WAIT TIME FROM TRANSMISSION OF SLEEP COMMAND				UNIT
Daisy Chain Data Rate	500	250	125	62.5	kHz
Time to Enter Sleep mode	500	1000	2000	4000	µs

NOTE: Devices exit **Sleep mode** on receipt of a valid Wakeup command.

Wakeup

The host microcontroller wakes up a stack of sleeping devices by sending the Wakeup command to the Master stack device. The Wakeup command must be written using the Address All stack address: 1111. The command is not recognized if sent with an individual device address and causes the Master device to respond NAK.

The Master exits **Sleep mode** on receipt of a valid Wakeup command and proceeds to transmit the Wakeup signal to the next device in the stack. The Wakeup signal is a few cycles of a 4kHz clock. Each device in the chain wakes up on receipt of the Wakeup signal and proceeds to send the signal onto the next device. Any communications received on port 1 by a device which is transmitting the Wakeup signal on port 2 are ignored. The Top stack device, after waking up, waits for some time before sending an ACK response to the Master. This wait time is necessary to allow for the Wakeup signal being originated by a stack device other than the Master. See "Fault Response in Sleep Mode" in the following section for more information. The Master device passes the ACK on to the host microcontroller to complete the Wakeup sequence. The total time required to wakeup a complete stack of devices is dependent on the number of devices in the stack. Table 20 gives the maximum time from Wakeup command transmission to receipt of ACK response ($\overline{\text{DATA READY}}$ asserted low) for stacks of 8 devices and 14 devices at various daisy chain data rates (interpolate linearly for different number of devices).

TABLE 20. MAXIMUM WAKEUP TIMES FOR STACKS OF 8 DEVICES AND 14 DEVICES (WAKEUP COMMAND TO ACK RESPONSE)

	MAXIMUM WAKEUP TIMES				UNIT
Daisy Chain Data Rate	500	250	125	62.5	kHz
Stack of 8 Devices	63	63	63	63	ms
Stack of 14 Devices	100	100	100	100	ms

There is no additional checking for communications faults while devices are waking up. A communications fault is indicated by the host microcontroller not receiving an ACK response within the expected time.

Fault Response in Sleep Mode

Devices may detect faults if operating in **Scan Continuous mode** while also in **Sleep mode**.

Daisy chain devices registering a fault in **Sleep mode** proceed to wakeup the other devices in the stack (e.g., Middle devices send the Wakeup signal on both ports). Any communications received by a device on one port while it is transmitting the Wakeup signal on its other port are ignored. After receiving the Wakeup signal, the top stack device waits before sending an ACK response on port 1. This is to allow other stack devices to wakeup. The total wait time is dependent on the number of devices in the stack. The time from a device detecting a fault to receipt of the ACK response is also dependent on the stack position of the device. See Table 20 for maximum response times for stacks of 8 and 14 devices.

The normal host microcontroller response to receiving an ACK while the stack is in **Sleep mode** is to read the Fault Status register contents of each device in the stack to determine which device (or devices) has a fault.

System Registers

System registers contain 14-bits each. All register locations are memory mapped using a 9-bit address. The MSBs of the address form a 3-bit page address. Page 1 (3'b001) registers are the measurement result registers for cell voltages and temperatures. Page 3 (3'b011) is used for commands. Pages 1 and 3 are not subject to the checksum calculations. Page addresses 4 and 5 (3'b100 and 3b'101), with the exception of the EEPROM checksum registers, are reserved for internal functions.

All page 2 registers (device configuration registers), together with the EEPROM checksum registers, are subject to a checksum

calculation. The checksum is calculated in response to the Calculate Register Checksum command using a Multiple Input Shift Register (MISR) error detection technique. The checksum is tested in response to a Check Register Checksum command. The occurrence of a checksum error sets the PAR bit in the Fault Status register and causes a Fault response accordingly. The normal response to a PAR error is for the host microcontroller to re-write the page 2 register contents. A PAR fault also causes the device to cease any scanning or cell balancing activity.

A description of each register is included in "Register Descriptions" as follows and includes a depiction of the register with bit names and initialization values at power-up, when the EN pin is toggled and the device receives a Reset Command, or when the device is reset. Bits which reflect the state of external pins are notated "Pin" in the initialization space. Bits which reflect the state of nonvolatile memory bits (EEPROM) are notated "NV" in the initialization space. Initialization values are shown below each bit name.

Reserved bits (indicated by grey areas) should be ignored when reading and should be set to "0" when writing to them.

Register Descriptions

Cell Voltage Data

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b001	Read Only	6'h00 - 6'h0C and 6'h0F	**Measured cell voltage and pack voltage values.** Address 001111 accesses all cell and Pack Voltage data with one read operation. Cell and Pack Voltage values are output as 13-bit signed integers with the 14^{th} bit (MSB) denoting the sign, (e.g., positive full scale is 14'h1FFF, 8191 decimal, negative full scale is 14'h2000, 8192 decimal).

ACCESS	PAGE ADDR	REGISTER ADDRESS		DESCRIPTION
Read Only	3'b001	6'h00	VBAT Voltage	$if\ldots HEXvalue_{10} \geq 8191 \rightarrow VBAT = \frac{(HEXvalue_{10} - 16384) \times 15.9350784 \times 2.5}{8192}$
		6'h01	Cell 1 Voltage	$VCx = \frac{(HEXvalue_{10} - 16384) \times 2 \times 2.5}{8192}$
		6'h02	Cell 2 Voltage	
		6'h03	Cell 3 Voltage	
		6'h04	Cell 4 Voltage	
		6'h05	Cell 5 Voltage	
		6'h06	Cell 6 Voltage	$else \rightarrow VBAT = \frac{HEXvalue_{10} \times 15.9350784 \times 2.5}{8192}$
		6'h07	Cell 7 Voltage	
		6'h08	Cell 8 Voltage	
		6'h09	Cell 9 Voltage	$VCx = \frac{HEXvalue_{10} \times 2 \times 2.5}{8192}$
		6'h0A	Cell 10 Voltage	
		6'h0B	Cell 11 Voltage	
		6'h0C	Cell 12 Voltage	
		6'h0F	Read all cell voltages	

Temperature Data, Secondary Voltage Reference Data, Scan Count

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b001	See individual register	6'h10 - 6'h16 and 6'h1F	**Measured temperature, Secondary reference, Scan Count.** Address 011111 accesses all these data in a continuous read. Temperature and reference values are output as 14-bit unsigned integers, (e.g., full scale is 14'h3FFF (16383 decimal)). $Vtemp = \frac{HEXvalue_{10} \times 2.5}{16384}$

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read Only	3'b001	6'h10	Internal temperature reading.
		6'h11	External temperature input 1 reading.
		6'h12	External temperature input 2 reading.
		6'h13	External temperature input 3 reading.
		6'h14	External temperature input 4 reading.
		6'h15	Reference voltage (raw ADC) value. Use to calculate corrected reference value using reference coefficient data. See page 2 data, address 6'h38 – 6'h3A.
Read/ Write	3'h001	6'h16	Scan Count: Current scan instruction count. Count is incremented each time a scan command is received and wraps to zero when overflowed. Register may be compared to previous value to confirm scan command receipt. Bit Designations:

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SCN3	SCN2	SCN1	SCN0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read Only	3'h001	6'h1F	Read all: Temperature Data, Secondary Voltage Reference Data, Scan Count (locations 6'h10 - 6'h16)

Fault Registers

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'h010	Read/ Write	6'h00 - 6'h05 and 6'h0F	**Fault registers.** Fault setup and status information. Address 6'h0F accesses all fault data in a continuous read (Daisy Chain configuration only).

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'h010	6'h00	**Overvoltage Fault:** Overvoltage fault on cells 12 to 1 correspond with bits OF12 to OF1, respectively. Default values are all zero. Bits are set to 1 when faults are detected. The contents of this register may be reset via register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		OF12	OF11	OF10	OF9	OF8	OF7	OF6	OF5	OF4	OF3	OF2	OF1
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/ Write	3'h010	6'h01	**Undervoltage Fault:** Undervoltage fault on cells 12 to 1 correspond with bits UF12 to UF1, respectively. Default values are all zero. Bits are set to 1 when faults are detected. The contents of this register may be reset via register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		UF12	UF11	UF10	UF9	UF8	UF7	UF6	UF5	UF4	UF3	UF2	UF1
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/ Write	3'h010	6'h02	**Open Wire Fault:** Open Wire fault on Pins VC12 to VC0 correspond with bits OC12 to OC0, respectively. Default values are all zero. Bits are set to 1 when faults are detected. The contents of this register may be reset via register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	OC12	OC11	OC10	OC9	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

<table>
<tr><th>ACCESS</th><th>PAGE ADDR</th><th>REGISTER ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h03</td><td>
Fault Setup:
These bits control various Fault configurations.
Default values are shown below, as are descriptions of each bit.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>TST4</td><td>TST3</td><td>TST2</td><td>TST1</td><td>TST0</td><td>TOT2</td><td>TOT1</td><td>TOT0</td><td>WSCN</td><td>SCN3</td><td>SCN2</td><td>SCN1</td><td>SCN0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>SCN0, 1, 2, 3</td><td>Scan interval code. Decoded to provide the scan interval setup for the auto scan function. Initialized to 0000 (16ms scan interval). See Table 2 on page 23.</td></tr>
<tr><td>WSCN</td><td>Scan wires timing control. Set to 1 for tracking of the temperature scan interval. Set to 0 for tracking of the cell voltage scan interval above 512ms. Interval is fixed at 512ms for faster cell scan rates. See Table 2 on page 23.</td></tr>
<tr><td>TOT0, 1, 2</td><td>Fault totalize code bits. Decoded to provide the required fault totalization. An unbroken sequence of positive fault results equal to the totalize amount is needed to verify a fault condition. Initialized to 011 (8 sample totalizing.) See Table 17 on page 35.
This register must be re-written following an error detection resulting from totalizer overflow.</td></tr>
<tr><td>TST0</td><td>Controls temperature testing of internal IC temperature. Set bit to 1 to enable internal temperature test. Set to 0 to disable (not recommended). Initialized to 1 (on).</td></tr>
<tr><td>TST1 to TST4</td><td>Controls temperature testing on the external temperature inputs 1 to 4, respectively. Set bit to 1 to enable the corresponding temperature test. Set to 0 to disable. Allows external inputs to be used for general voltage monitoring without imposing a limit value.
TST1 to TST4 are initialized to 0 (off).</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>ACCESS</th><th>PAGE ADDR</th><th>REGISTER ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h04</td><td>
Fault Status:
The $\overline{\text{FAULT}}$ logic output is an OR function of the bits in this register: the output will be asserted low if any bits in the Fault Status register are set.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MUX</td><td>REG</td><td>REF</td><td>PAR</td><td>OVSS</td><td>OV_{BAT}</td><td>OW</td><td>UV</td><td>OV</td><td>OT</td><td>WDGF</td><td>OSC</td><td colspan="2">RESERVED</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="3">OSC</td><td colspan="12">Oscillator fault bit. Bit is set in response to a fault on either the 4MHz or 32kHz oscillators. Note that communications functions may be disrupted by a fault in the 4MHz oscillator.</td></tr>
<tr><td colspan="3">WDGF</td><td colspan="12">Watchdog timeout fault. Bit is set in response to a watchdog timeout.</td></tr>
<tr><td colspan="3">OT</td><td colspan="12">Over-temperature fault. ‘OR’ of over-temperature fault bits: TFLT0 to TFLT4. This bit is latched. The bits in the Over-temperature Fault register must first be reset before this bit can be reset. Reset by writing 14’h0000 to this register.</td></tr>
<tr><td colspan="3">OV</td><td colspan="12">Overvoltage fault. ‘OR’ of Overvoltage fault bits: OF1 to OF12. This bit is latched. The bits in the Overvoltage Fault register must first be reset before this bit can be reset. Reset by writing 14’h0000 to this register.</td></tr>
<tr><td colspan="3">UV</td><td colspan="12">Undervoltage fault. ‘OR’ of Undervoltage fault bits: UF1 to UF12. This bit is latched. The bits in the Undervoltage Fault register must first be reset before this bit can be reset. Reset by writing 14’h0000 to this register.</td></tr>
<tr><td colspan="3">OW</td><td colspan="12">Open Wire fault. ‘OR’ of open wire fault bits: OC0 to OC12. This bit is latched. The bits in the Open Wire Fault register must first be reset before this bit can be reset. Reset by writing 14’h0000 to this register.</td></tr>
<tr><td colspan="3">OV_{BAT}</td><td colspan="12">Open wire fault on V_{BAT} connection. Bit set to 1 when a fault is detected. May be reset via register write (14’h0000).</td></tr>
<tr><td colspan="3">OVSS</td><td colspan="12">Open wire fault on VSS connection. Bit set to 1 when a fault is detected. May be reset via register write (14’h0000).</td></tr>
<tr><td colspan="3">PAR</td><td colspan="12">Register checksum (Parity) error. This bit is set in response to a register checksum error. The checksum is calculated and stored in response to a Calc Register Checksum command and acts on the contents of all page 2 registers. The Check Register Checksum command is used to repeat the calculation and compare the results to the stored value. The PAR bit is then set if the two results are not equal. This bit is not set in response to a nonvolatile EEPROM memory checksum error. See table on page 49.</td></tr>
<tr><td colspan="3">REF</td><td colspan="12">Voltage reference fault. This bit is set if the voltage reference value is outside its “power-good” range.</td></tr>
<tr><td colspan="3">REG</td><td colspan="12">Voltage regulator fault. This bit is set if a voltage regulator value (V3P3, VCC or V2P5) is outside its “power-good” range.</td></tr>
<tr><td colspan="3">MUX</td><td colspan="12">Temperature multiplexer error. This bit is set if the VCC loopback check returns a fault. The VCC loopback check is performed at the end of each temperature scan.</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h05</td><td>
Cell Setup:
Default values are shown below, as are descriptions of each bit.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>FFSN</td><td>FFSP</td><td>C12</td><td>C11</td><td>C10</td><td>C9</td><td>C8</td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="3">C1 to C12</td><td colspan="12">Enable/disable cell overvoltage, undervoltage and open wire detection on cell 1 to 12, respectively. Set to 1 to disable OV/UV and open wire tests.</td></tr>
<tr><td colspan="3">FFSP</td><td colspan="12">Force ADC input to Full Scale Positive. All cell scan readings forced to 14'h1FFF. All temperature scan readings forced to 14'h3FFF.</td></tr>
<tr><td colspan="3">FFSN</td><td colspan="12">Force ADC input to Full Scale Negative. All cell scan readings forced to 14'h2000. All temperature scan readings forced to 14'h0000.</td></tr>
<tr><td colspan="15">NOTE: The ADC input functions normally if both FFSN and FFSP are set to '1' but this setting is not supported.</td></tr>
</table>
</td></tr>
</table>

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'h010	6'h06	**Over-temperature Fault:** Over-temperature fault on cells 12 to 1 correspond with bits OF12 to OF1, respectively. Default values are all zero. Bits are set to 1 when fault are detected. The contents of this register may be reset via register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TFLT4	TFLT3	TFLT2	TFLT1	TFLT0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

TFLT0	Internal over-temperature fault. Bit set to 1 when a fault is detected. May be reset via register write (14'h0000).
TFLT1 - TFLT4	External over-temperature inputs 1 to 4 (respectively.) Bit set to 1 when a fault is detected. May be reset via register write (14'h0000).

Read Only	3'h010	6'h0F	Read all Fault and Cell Setup data from locations: 6'h00 - 6'h06.

Setup Registers

BASE ADDR (PAGE)	Access	ADDRESS RANGE	DESCRIPTION
3'b010		6'h10 - 6'h1D and 6'h1F	**Device Setup registers.** All device setup data.

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'b010	6'h10	**Overvoltage Limit:** Overvoltage Limit Value Overvoltage limit is compared to the measured values for cells 1 to 12 to test for an Overvoltage condition at any of the cells. Bit 0 is the LSB, Bit 12 is the MSB. Bit 13 is not used and must be set to 0.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	OV12	OV11	OV10	OV9	OV8	OV7	OV6	OV5	OV4	OV3	OV2	OV1	OV0
0	1	1	1	1	1	1	1	1	1	1	1	1	1

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'b010	6'h11	**Undervoltage Limit:** Undervoltage Limit Value Undervoltage limit is compared to the measured values for cells 1 to 12 to test for an undervoltage condition at any of the cells. Bit 0 is the LSB, Bit 12 is the MSB. Bit 13 is not used and must be set to 0.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	UV12	UV11	UV10	UV9	UV8	UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'b010	6'h12	**External Temperature Limit:** Over-temperature limit value Over-temperature limit is compared to the measured values for external temperatures 1 to 4 to test for an over-temperature condition at any input. The temperature limit assumes NTC temperature measurement devices (i.e., an over-temperature condition is indicated by a temperature reading below the limit value). Bit 0 is the LSB, Bit 13 is the MSB.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETL13	ETL12	ETL11	ETL10	ETL9	ETL8	ETL7	ETL6	ETL5	ETL4	ETL3	ETL2	ETL1	ETL0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

<table>
<tr><th>ACCESS</th><th>PAGE ADDR</th><th>REGISTER ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h13</td><td>
Balance Setup:
Default values are shown below, as are descriptions of each bit.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>BEN</td><td>BSP3</td><td>BSP2</td><td>BSP1</td><td>BSP0</td><td>BWT2</td><td>BWT1</td><td>BWT0</td><td>BMD1</td><td>BMD0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>BMD0, 1</td><td>Balance mode. These bits set balance mode.
<table>
<tr><td>BMD1</td><td>BMD0</td><td>Mode</td></tr>
<tr><td>0</td><td>0</td><td>OFF</td></tr>
<tr><td>0</td><td>1</td><td>Manual</td></tr>
<tr><td>1</td><td>0</td><td>Timed</td></tr>
<tr><td>1</td><td>1</td><td>Auto</td></tr>
</table>
</td></tr>
<tr><td>BWT0, 1, 2</td><td>Balance wait time. Register contents are decoded to provide the required wait time between device balancing. This is to assist with thermal management and is used with the Auto Balance mode. See Table 4 on page 25.</td></tr>
<tr><td>BSP0, 1, 2, 3</td><td>Balance Status register pointer. Points to one of the 13 incidents of the Balance Status register. Balance Status register 0 is used for Manual Balance mode and Timed Balance mode. Balance status registers 1 to 12 are used for Auto Balance mode. Reads and writes to the Balance Status register are accomplished by first configuring the Balance Status register pointer (e.g., to read (write) Balance Status register 5, load 0101 to the Balance Status register pointer, then read (write) to the Balance Status register). See Table 7 on page 26.</td></tr>
<tr><td>BEN</td><td>Balance enable. Set to ‘1’ to enable balancing. ‘0’ inhibits balancing. Setting or clearing this bit does not affect any other register contents. Balance Enable and Balance Inhibit commands are provided to allow control of this function without requiring a register write. These commands have the same effect as setting this bit directly. This bit is cleared automatically when balancing is complete and the EOB bit (see “6’h19” on page 46) is set.</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h14</td><td>
Balance Status
The Balance Status register is a Multiple Incidence register controlled by the BSP0-4 bits in the Balance Setup register. See Table 7 on page 26.
Bit 0 is the LSB, Bit 11 is the MSB.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>BAL 12</td><td>BAL 11</td><td>BAL 10</td><td>BAL 8</td><td>BAL 8</td><td>BAL 7</td><td>BAL 6</td><td>BAL 5</td><td>BAL 4</td><td>BAL 3</td><td>BAL 2</td><td>BAL 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>BAL1 to BAL12</td><td>Cell 1 to Cell 12 balance control, respectively. A bit set to 1 enables balance control (turns FET on) of the corresponding cell. Writing this bit enables balance output for the current incidence of the Balance Status register for the cells corresponding to the particular bits, depending on the condition of BEN in the Balance Setup register. Read this bit to determine the current status of each cell’s balance control.</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h15</td><td>
Watchdog/Balance Time
Defaults are shown below:
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>BTM6</td><td>BTM5</td><td>BTM4</td><td>BTM3</td><td>BTM2</td><td>BTM1</td><td>BTM0</td><td>WDG6</td><td>WDG5</td><td>WDG4</td><td>WDG3</td><td>WDG2</td><td>WDG1</td><td>WDG0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>WDG0 to WDG6</td><td>Watchdog timeout setting. Decoded to provide the time out value for the watchdog function. The watchdog may only be disabled (set to 7’h00) if the watchdog password is set. The watchdog setting can be changed to a nonzero value without writing to the watchdog password. See “Device Setup Register” on page 30. Initialized to 7’h7F (128 minutes).</td></tr>
<tr><td>BTM0 to BTM6</td><td>Balance timeout setting. Decoded to provide the time out value for Timed Balance mode and Auto Balance mode. Initialized to 7’00 (Disabled). See Table 9 on page 27.</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>ACCESS</th><th>PAGE ADDR</th><th>REGISTER ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h16
6’h17</td><td>User Register
28 bits of register space arranged as 2 x 14 bits available for user data. These registers have no effect on the operation of the ISL94212. These registers are included in the register checksum function.</td></tr>
<tr><td rowspan="8">Read Only</td><td rowspan="8">3’b010</td><td rowspan="8">6’h18</td><td>Comms Setup
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>CRAT1</td><td>CRAT0</td><td>CSEL 2</td><td>CSEL 1</td><td>SIZE 3</td><td>SIZE 2</td><td>SIZE 1</td><td>SIZE 0</td><td>ADDR 3</td><td>ADDR 2</td><td>ADDR 1</td><td>ADDR 0</td></tr>
<tr><td>0</td><td>0</td><td>COMS RATE1 pin</td><td>COMS RATE0 pin</td><td>COMS SEL2 pin</td><td>COMS SEL1 pin</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>ADDR0-3</td><td>Device stack address. The stack address (device position in the stack) is determined automatically by the device in response to an “Identify” command. The resulting address is stored in ADDR0-3 and is used internally for communications paring and sequencing. The stack address may be read by the user but not written to.</td></tr>
<tr><td>SIZE0-3</td><td>Device stack size (top stack device address). Corresponds to the number of devices in the stack. The stack size is determined automatically by the stack devices in response to an “Identify” command. The resulting number is stored in SIZE0-3 and is used internally for communications paring and sequencing. The stack size may be read by the user but not written to.</td></tr>
<tr><td>CSEL1, 2</td><td>Communications setup bits. These bits reflect the state of the COMMS SELECT 1,2 pins and determine the operating mode of the communications ports. See Table 15 on page 31.</td></tr>
<tr><td>CRAT0, 1</td><td>Communications rate bits. These bits reflect the state of the COMMS RATE 0,1 pins and determine the bit rate of the Daisy Chain communications system.</td></tr>
<tr><td rowspan="8">Read/ Write</td><td rowspan="8">3’b010</td><td rowspan="8">6’h19</td><td>Device Setup
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>WP5</td><td>WP4</td><td>WP3</td><td>WP2</td><td>WP1</td><td>WP0</td><td>BDDS</td><td>RESERVED</td><td>ISCN</td><td>SCAN</td><td>EOB</td><td>RESERVED</td><td>PIN37</td><td>PIN39</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Pin</td><td>Pin</td></tr>
</table></td></tr>
<tr><td>PIN37, PIN39</td><td>These bits indicate the signal level on pin 37 and pin 39 of the device.</td></tr>
<tr><td>EOB</td><td>End Of Balance. This bit is set by the device when balancing is complete. This function is used in the Timed Balance mode and Auto Balance mode. The BEN bit is cleared as a result of this bit being set. Initialized to 1.</td></tr>
<tr><td>SCAN</td><td>Scan Continuous mode. This bit is set in response to a Scan Continuous command and cleared by a Scan Inhibit command.</td></tr>
<tr><td>ISCN</td><td>Set wire scan current source/sink values. Set to 0 for 150µA. Set to 1 for 1mA.</td></tr>
<tr><td>BDDS</td><td>Balance condition during measurement. Controls the balance condition in Scan Continuous mode and Auto Balance mode. Set to 1 to have balancing functions turned off 10ms prior to and during cell voltage measurement. Set to 0 for normal operation (balancing functions not affected by measurement).</td></tr>
<tr><td>WP5:0</td><td>Watchdog disable password. These bits must be set to 6’h3A (111010) before the watchdog can be disabled. Disable watchdog by writing 7’h00 to the watchdog bits.</td></tr>
<tr><td rowspan="4">Read Only Value set in EEPROM</td><td rowspan="4">3’b010</td><td rowspan="4">6’h1A</td><td>Internal Temperature Limit
Bit 0 is the LSB, Bit 13 is the MSB.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>ITL 13</td><td>ITL 12</td><td>ITL 11</td><td>ITL 10</td><td>ITL 8</td><td>ITL 8</td><td>ITL 7</td><td>ITL 6</td><td>ITL 5</td><td>ITL 4</td><td>ITL 3</td><td>ITL 2</td><td>ITL 1</td><td>ITL 0</td></tr>
<tr><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td></tr>
</table></td></tr>
<tr><td>ITL1 to ITL12</td><td>IC over-temperature limit value. Over-temperature limit is compared to the measured values for internal IC temperature to test for an over-temperature condition. The internal temperature limit value is stored in nonvolatile memory during test and loaded to these register bits at power-up. The register contents may be read by the user but not written to.</td></tr>
<tr><td>Read Only</td><td>3’b010</td><td>6’h1B
6’h1C</td><td>Serial Number
The 28b serial number programmed in nonvolatile memory during factory test is mirrored to these 2 x 14 bit registers. The serial number may be read at any time but may not be written.</td></tr>
</table>

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION													
Read Only Value set in EEPROM	3'b010	6'h1D	**Trim Voltages**													
			13	12	11	10	9	8	7	6	5	4	3	2	1	0
			TV5	TV4	TV3	TV2	TV1	TV0	RESERVED							
			NV	NV	NV	NV	NV	NV	Ignore the Contents of these bits							
			TV5:0			Trim voltage (VNOM). The nominal cell voltage is programmed to nonvolatile memory during test and loaded to the Trim Voltage register at power up. The VNOM value is a 7-bit representation of the 0V to 5V cell voltage input range with 50 (7'h32) representing 5V (e.g., LSB = 0.1V). The parts are additionally marked with the trim voltage by the addition of a two digit code to the part number e.g., 3.3V is denoted by the code 33. (1 bit per 0.1V of trim voltage, so 0 to 50 decimal covers the full range.)									
Read Only	3'h010	6'h1F	Read all setup data from locations: 6'h10 - 6'h1D.													

Cell Balance Registers

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b010	Read/ Write	6'h20 - 6'h37	**Cell balance registers.** These registers are loaded with data related to change in SOC desired for each cell. This data is then used during **Auto Balance mode**. The data value is decremented with each successive ADC sample until a zero value is reached. The register space is arranged as 2 x 14-bit per cell for 24 x 14-bit total. The registers are cleared at device power up or by a Reset command. See "Auto Balance Mode" on page 27.

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'b010	6'h20	Cell 1 balance value bits 0 to 13.
		6'h21	Cell 1 balance value bits 14 to 27.
		~	
		6'h36	Cell 12 balance value bits 0 to 13.
		6'h37	Cell 12 balance value bits 14 to 27.

Reference Coefficient Registers

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b010	Read Only	6'h38 - 6'h3A	Reference Coefficients. Bit 13 is the MSB, Bit 0 is the LSB

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION													
Read Only Value set in EEPROM	3'b010	6'h38	**Reference Coefficient C** Reference calibration coefficient C LSB. Use with coefficients A and B and the measured reference value to obtain the compensated reference measurement. This result may be compared to limits given in the "Electrical Specifications" table beginning on page 7 to check that the reference is within limits. The register contents may be read by the user but not written to.													
			13	12	11	10	9	8	7	6	5	4	3	2	1	0
			RCC 13	RCC 12	RCC 11	RCC 10	RCC 9	RCC 8	RCC 7	RCC 6	RCC 5	RCC 4	RCC 3	RCC 2	RCC 1	RCC 0
			NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read Only	3'b010	6'h39	**Reference Coefficient B** Reference calibration coefficient B LSB. Use with coefficients A and C and the measured reference value to obtain the compensated reference measurement. This result may be compared to limits given in the "Electrical Specifications" table beginning on page 7 to check that the reference is within limits. The register contents may be read by the user but not written to.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCB 13	RCB 12	RCB 11	RCB 10	RCB 9	RCB 8	RCB 7	RCB 6	RCB 5	RCB 4	RCB 3	RCB 2	RCB 1	RCB 0
NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read Only	3'b010	6'h3A	**Reference Coefficient A** Reference calibration coefficient A LSB. Use with coefficients B and C and the measured reference value to obtain the compensated reference measurement. This result may be compared to limits given in the "Electrical Specifications" table beginning on page 7 to check that the reference is within limits. The register contents may be read by the user but not written to.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCA 8	RCA 7	RCA 6	RCA 5	RCA 4	RCA 3	RCA 2	RCA 1	RCA 0	RESERVED				
NV	NV	NV	NV	NV	NV	NV	NV	NV	Ignore the content of these bits				

Cells In Balance Register

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b010	Read Only	6'h3B	Cells In balance (valid for non-daisy chain configuration only).

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read Only	3'b010	6'h3B	**Cells Balance Enabled** This register reports the current condition of the cell balance outputs. Bit 0 is the LSB, Bit 11 is the MSB.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		CBEN 12	CBEN 11	CBEN 10	CBEN 8	CBEN 8	CBEN 7	CBEN 6	CBEN 5	CBEN 4	CBEN 3	CBEN 2	CBEN 1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
BALI1 to BALI12		Indicates the current balancing status of cell 1 to cell 12 (respectively). "1" indicates balancing is enabled for this cell. "0" indicates that balancing is turned off.											

Device Commands

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b011	Read Only	6'h01 - 6'h14	Device commands. Actions and communications administration. Not physical registers but memory mapped device commands. Commands from host and device responses are all configured as reads (BASE ADDR MSB = 0). Write operations breaks the communication rules and produce NAK from the target device.

PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
3'b011	6'h01	**Scan Voltages.** Device responds by scanning V_{BAT} and all 12 cell voltages and storing the results in local memory.
	6'h02	**Scan Temperatures.** Device responds by scanning external temperature inputs, internal temperature, and the secondary voltage reference, and storing the results in local memory.
	6'h03	**Scan Mixed.** Device responds by scanning V_{BAT}, cell and ExT1 voltages and storing the results in local memory. The ExT1 measurement is performed in the middle of the cell voltage scans to minimize measurement latency between the cell voltages and the voltage on ExT1.
	6'h04	**Scan Wires.** Device responds by scanning for pin connection faults and stores the results in local memory.
	6'h05	**Scan All.** Device responds by performing the functions of the Scan Voltages, Scan Temperatures, and Scan Wires commands in sequence. Results are stored in local memory
	6'h06	**Scan Continuous.** Places the device in **Scan Continuous mode** by setting the Device Setup register *SCAN* bit.
	6'h07	**Scan Inhibit.** Stops **Scan Continuous mode** by clearing the Device Setup register *SCAN* bit.
	6'h08	**Measure.** Device responds by measuring a targeted single parameter (cell voltage/V_{BAT}/external or internal temperatures or secondary voltage reference).
	6'h09	**Identify.** Special mode function used to determine device stack position and address. Devices record their own stack address and the total number of devices in the stack.
	6'h0A	**Sleep.** Places the part in **Sleep mode** (wakeup via daisy comms). See "Sleep Mode" on page 39.
	6'h0B	**NAK.** Device response if communications is not recognized. The device responds NAK down the Daisy Chain to the host microcontroller. The host microcontroller typically retransmits on receiving a NAK.
	6'h0C	**ACK.** Used by host microcontroller to verify communications without changing anything. Devices respond with ACK.
	6'h0E	**Comms Failure.** Used in daisy chain implementations to communicate comms failure. If a communication is not acknowledged by a stack device, the last stack device that did receive the communication responds with Comms Failure. This is part of the communications integrity checking. Devices downstream of a communications fault are alerted to the fault condition by the watchdog function.
	6'h0F	**Wakeup.** Used in daisy chain implementations to wakeup a sleeping stack of devices. The Wakeup command is sent to the Bottom stack device (Master device) via SPI. The Master device then wakes up the rest of the stack by transmitting a low frequency clock. The Top stack device responds ACK once it is awake. See "Wakeup" on page 39.
	6'h10	**Balance Enable.** Enables cell balancing by setting *BEN*. May be used to enable cell balancing on all devices simultaneously using the address All Stack Address 1111.
	6'h11	**Balance Inhibit.** Disables cell balancing by clearing *BEN*. May be used to disable cell balancing on all devices simultaneously using the address All Stack Address 1111.
	6'h12	**Reset.** Resets all digital registers to its power-up state (i.e., reloads the factory programmed configuration data from non-volatile memory. Stops all scan and balancing activity. Daisy chain devices must be reset in sequence starting with the Top stack device and proceeding down the stack to the Bottom (Master) device. The Reset command must be followed by an Identify command (Daisy chain configuration) before volatile registers can be re-written.
	6'h13	**Calculate register checksum.** Calculates the checksum value for the current Page 2 register contents (registers with base address 0010). See "System Registers" on page 39.
	6'h14	**Check register checksum.** Verifies the register contents are correct for the current checksum. An incorrect result sets the *PAR* bit in the Fault status register, which starts a standard fault response. See "System Registers" on page 39.

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
100	Read Only	6'h3F	Nonvolatile memory Multiple Input Shift Register (MISR) register. This checksum value for the nonvolatile memory contents. It is programmed during factory testing at Intersil.
101	Read Only	6'h00	MISR shadow register checksum value. This value is calculated when shadow registers are loaded from nonvolatile memory either after a power cycle or a reset.

Nonvolatile Memory (EEPROM) Checksum

A checksum is provided to verify the contents of EEPROM memory. Two registers are provided. One contains the correct checksum value, which is calculated during factory testing at Intersil. The other contains the checksum value that is calculated each time the non volatile memory is loaded to shadow registers, either after a power cycle or after a device reset. Also refer to "Memory Checksum" on page 34.

Applications Circuits Information

Typical Applications Circuits

Typical applications circuits are shown in Figures 37 to 40. Table 21 on page 55 contains recommended component values. All external (off-board) inputs to the ISL94212 are protected against battery voltage transients by RC filters, they also provide a current limit function during hot plug events. The ISL94212 is calibrated for use with 1kΩ series protection resistors at the cell inputs. V_{BAT} uses a lower value resistor to accommodate the V_{BAT} supply current of the ISL94212. A value of 27Ω is used for this component. As much as possible, the time constant produced by the filtering applied to V_{BAT} should be matched to that applied to the cell 12 monitoring input. Component values given in Table 21 produce the required matching characteristics.

Figure 37 on page 51 shows the standard arrangement for connecting the ISL94212 to a stack of 12 cells. The cell input filter is designed to maximize EMI suppression. These components should be placed close to the connector with a well controlled ground to minimize noise for the measurement inputs. The balance circuits shown in Figure 37 provide normal cell monitoring when the balance circuit is turned off, and a near zero cell voltage reading when the balance circuit is turned on. This is part of the diagnostic function of the ISL94212.

Figure 38 on page 52 shows connections for the daisy chain system, setup pins, power supply and external voltage inputs for daisy chain devices other than the Master (stack bottom) device. The remaining circuits are discussed in more detail later in this datasheet.

Figure 39 on page 53 shows the daisy chain system, setup pins, microcontroller interface, power supply and external voltage inputs for the daisy chain master device. Figure 39 is also applicable to standalone (non-daisy chain) devices although in this case the daisy chain components connected to DHi2 and DLo2 would be omitted.

Figure 40 on page 54 shows an alternate arrangement for the battery connections in which the cell input circuits are connected directly to the battery terminal and not via the balance resistor. In this condition the balance diagnostic function capability is removed.

Typical Application Circuits

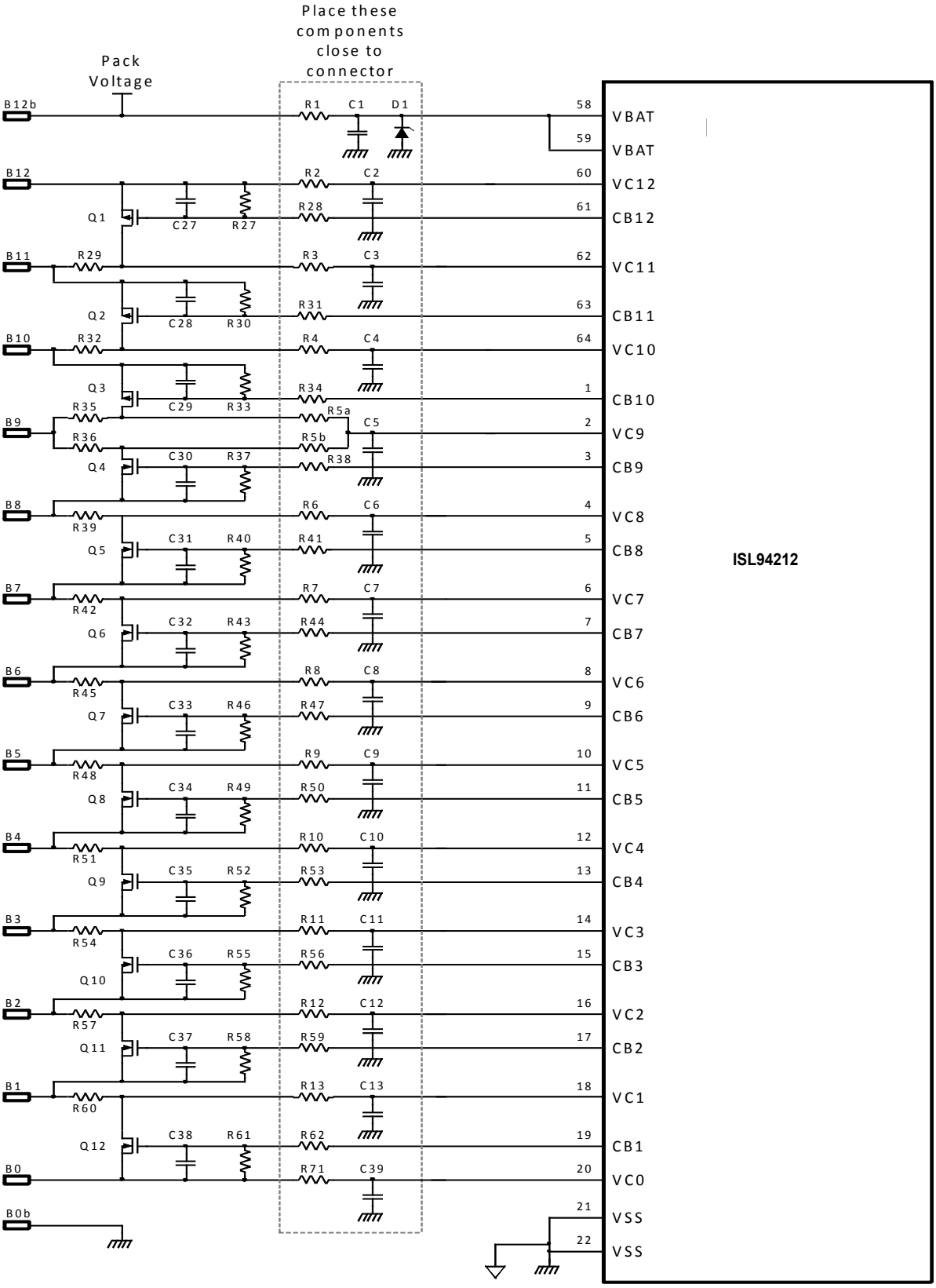


FIGURE 37. BATTERY CONNECTION CIRCUITS

Typical Application Circuits (Continued)

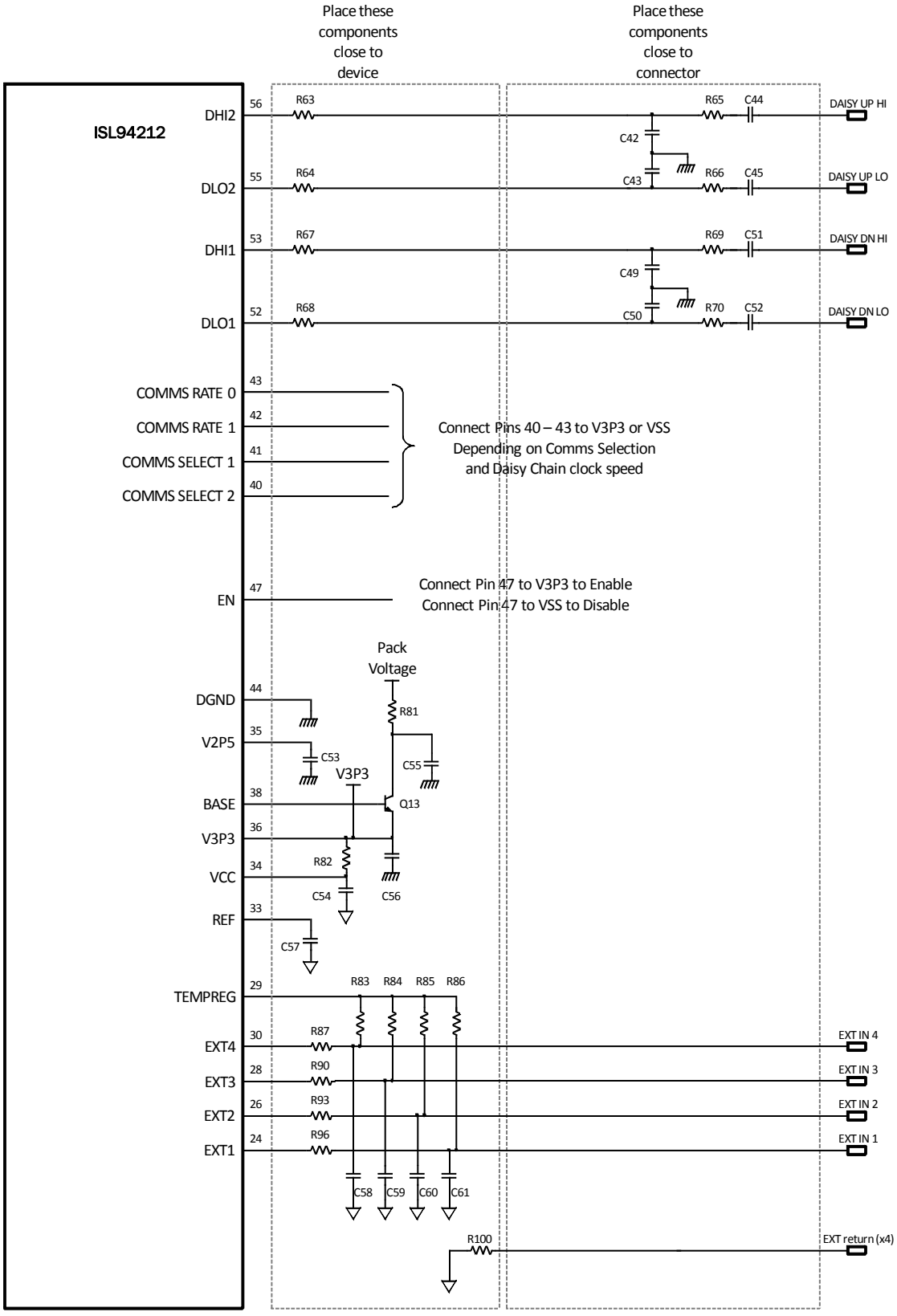


FIGURE 38. NON BATTERY CONNECTIONS, MIDDLE AND TOP DAISY CHAIN DEVICES

Typical Application Circuits (Continued)

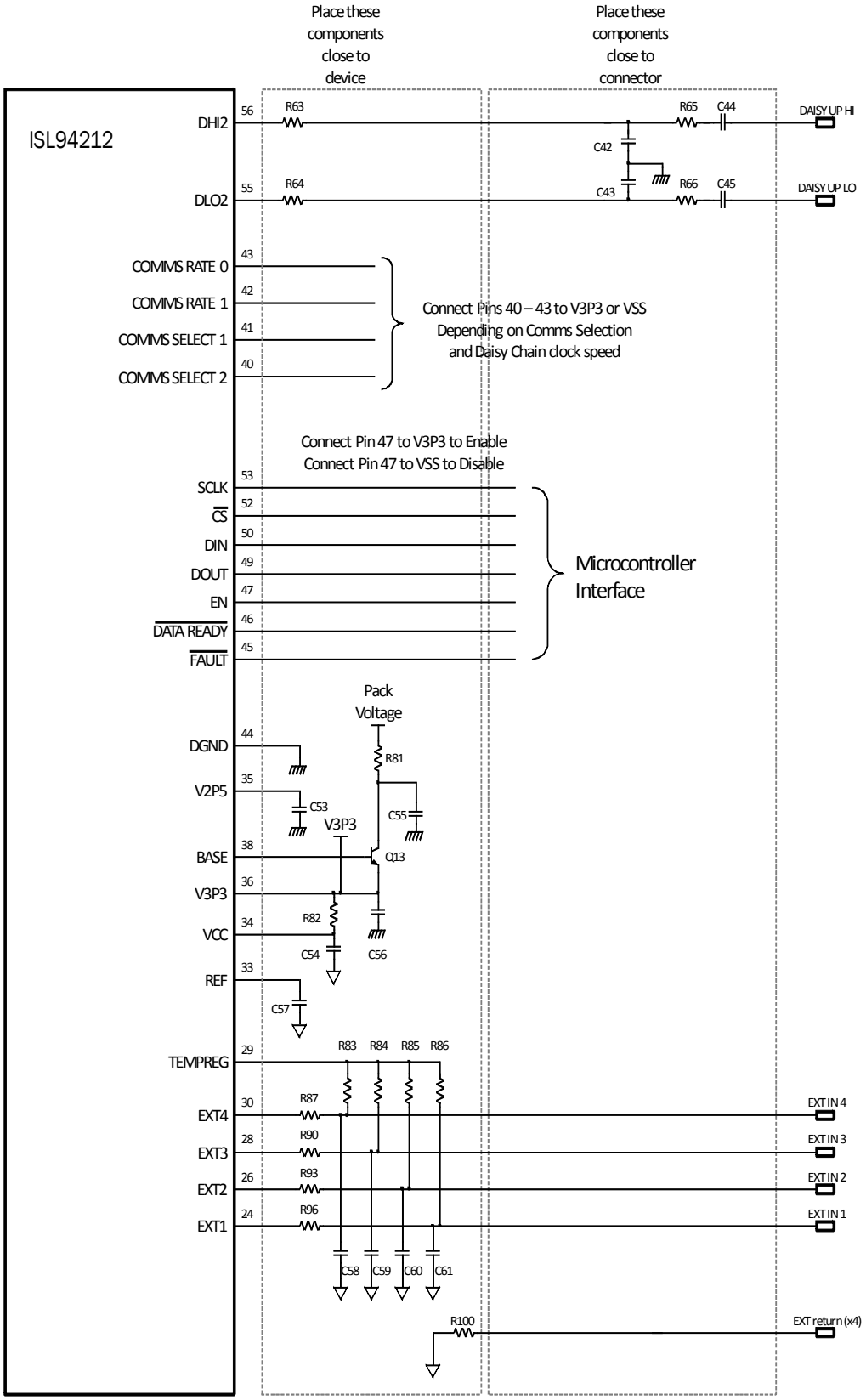


FIGURE 39. NON BATTERY CONNECTIONS, MASTER DAISY CHAIN DEVICE

Typical Application Circuits (Continued)

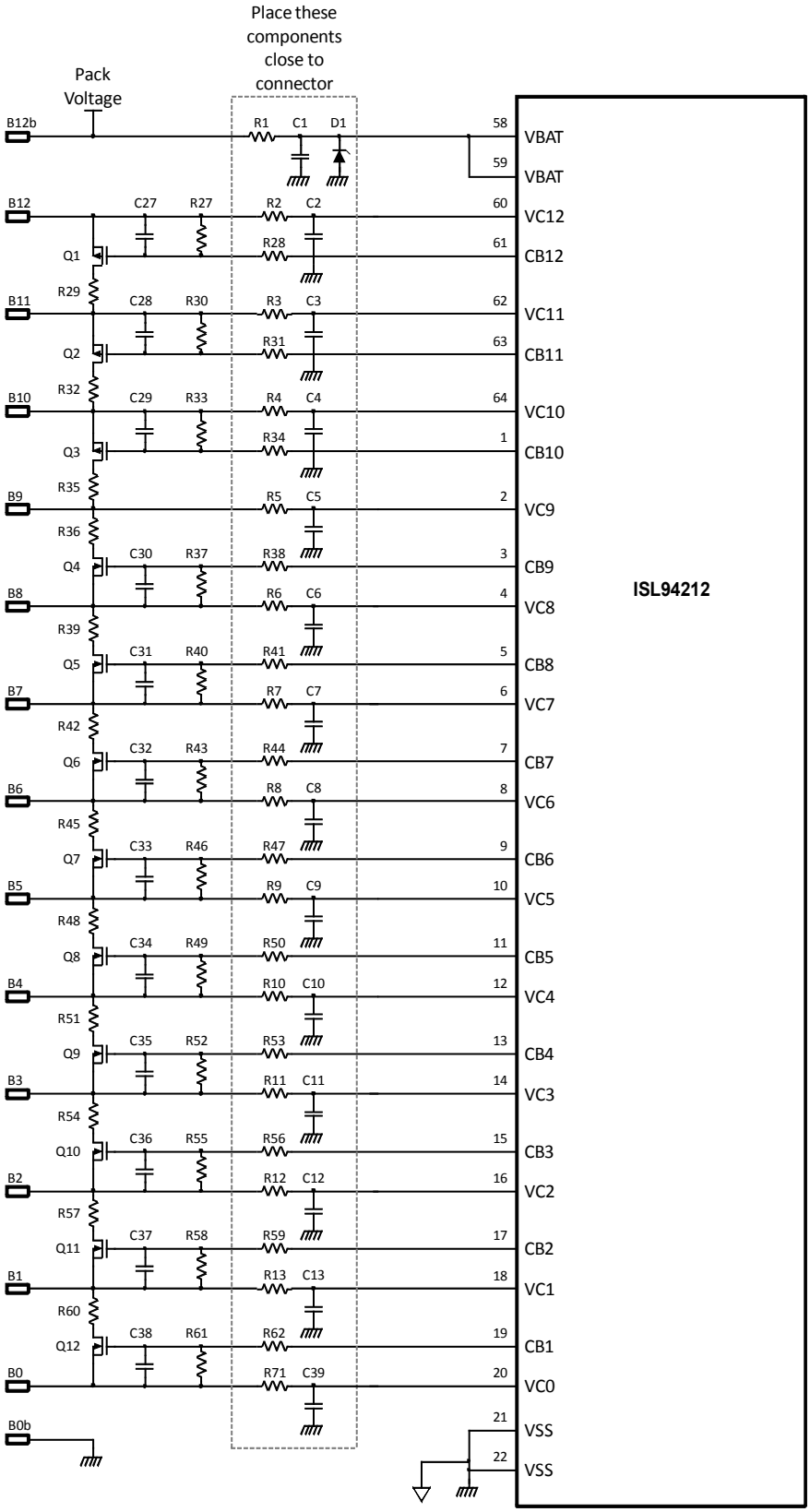


FIGURE 40. BATTERY CONNECTION CIRCUITS ALTERNATIVE CONFIGURATION

Notes on Board Layout

TABLE 21. RECOMMENDED COMPONENT VALUES FOR FIGURES (Figures 37 to 40)

RESISTORS		
VALUE		**COMPONENTS**
0		R101
27		R1
33		R82
1k		R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R71
100		R29, R32, R35, R36, R39, R42, R45, R48, R51, R54, R57, R60, R63, R64, R67, R68, R81
2k		R5a, R5b
470		R65, R66, R69, R70
10k		R28, R31, R34, R38, R41, R44, R47, R50, R53, R56, R59, R62, R83, R84, R85, R86, R87, R90, R93, R96, R100a, R100b, R100c, R100d
330k		R27, R30, R33, R37, R40, R43, R46, R49, R52, R55, R58, R61
CAPACITORS		
VALUE	**VOLTAGE**	**COMPONENTS**
200p	100	C42, C43, C49, C50
220p	500	C44, C45, C51, C52
10n	50	C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C58, C59, C60, C61
22n	100	C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C39
220n	100	C1
1µ	10	C53, C54, C56
1µ	100	C55
2.2µ	10	C57
ZENER DIODES		
VALUE	**EXAMPLE**	**COMPONENTS**
60V	1N5371BRLG	D1

Referring to Figure 37 on page 51 (battery connection circuits), the basic input filter structure comprises resistors R_2 to R_{13}, R_{71} and capacitors C_2 to C_{13}, C_{39}. These components provide protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the connector as possible. The ground terminals of the capacitors must be connected directly to a solid ground plane. Do not use vias to connect these capacitors to the input signal path or to ground. Any vias should be placed in line to the signal inputs so that the inductance of these forms a low pass filter with the grounded capacitors.

Referring to Figure 38 on page 52, the daisy chain components are shown to the top right of the drawing. These are split into two sections. Components to the right of this section should be placed close to the board connector with the ground terminals of capacitors connected directly to a solid ground plane. This is the same ground plane that serves the cell inputs. Components to the left of this section should be placed as closely to the device as possible.

The battery connector and daisy chain connectors should be placed closely to each other on the same edge of the board to minimize any loop current area.

Two grounds are identified on the circuit diagram. These are nominally referred to as noisy and quiet grounds. The noisy ground, denoted by an “earth” symbol carries the EMI loop currents and digital ground currents while the quiet ground is used to define the decoupling voltage for voltage reference and the analog power supply rail. The quiet and noisy grounds should be joined at the VSS pin. Keep the quiet ground area as small as possible.

The circuits shown to the bottom right of Figure 38 on page 52 provide signal conditioning and EMI protection for the external temperature inputs. These inputs are designed to operate with external NTC thermistors. See “External Inputs” on page 61 for more information about component selection.

Component Selection

Certain failures associated with external components can lead to unsafe conditions in electronic modules. A good example of this is a component that is connected between high energy signal sources failing short. Such a condition can easily lead to the component overheating and damaging the board and other components in its proximity.

One area to consider with the external circuits on the ISL94212 is the capacitors connected to the cell monitoring inputs. These capacitors are normally protected by the series protection resistors but could present a safety hazard in the event of a dual point fault where both the capacitor and associated series resistor fail short. Also, a short in one of these capacitors would dissipate the charge in the battery cell if left uncorrected for an extended period of time. It is recommended that capacitors C_1 to C_{13} be selected to be “fail safe” or “open mode” types. An alternative strategy would be to replace each of these capacitors with two devices in series, each with double the value of the single capacitor.

A dual point failure in the balancing resistor (R_{29}, R_{32}, R_{35}, etc.) of Figure 37 on page 51 and associated balancing MOSFET (Q_1 to Q_{12}) could also give rise to a shorted cell condition. It is recommended that the balancing resistor be replaced by two resistors in series.

Operating the ISL94212 with Reduced Cell Counts

When using the ISL94212 with fewer than 12 cells it is important to ensure that each used cell has a normal input circuit connection to the top and bottom monitoring inputs for that cell. The simplest way to use the ISL94212 with any number of cells is to always use the full input circuit arrangement for all inputs, and short together the unused inputs at the battery terminal. In this way each cell input sees a normal source impedance independent of whether or not it is monitoring a cell.

The cell balancing components associated with unconnected cell inputs are not required and can be removed. Unused cell balance outputs should be tied to the adjacent cell voltage monitoring pin.

The input circuit component count can be reduced in cases where fewer than 10 cells are being monitored. It is important that cell inputs that are being used are not connected to other (unused) cell inputs as this would affect measurement accuracy. Figure 41 on page 57, Figure 42 on page 58, and Figure 43 on page 59 show examples of systems with 10 cells, 8 cells, and 6 cells, respectively.

The component notations and values used in Figures 42 and 43 are the same as those used in Figures 37 to 40.

In Figure 43 the resistor associated with the input filter on VC9 is noted as R_5, rather than R_{5a}. This value change is needed to maintain the correct input network impedance in the absence of the cell 9 balance circuits.

Typical Application Circuits

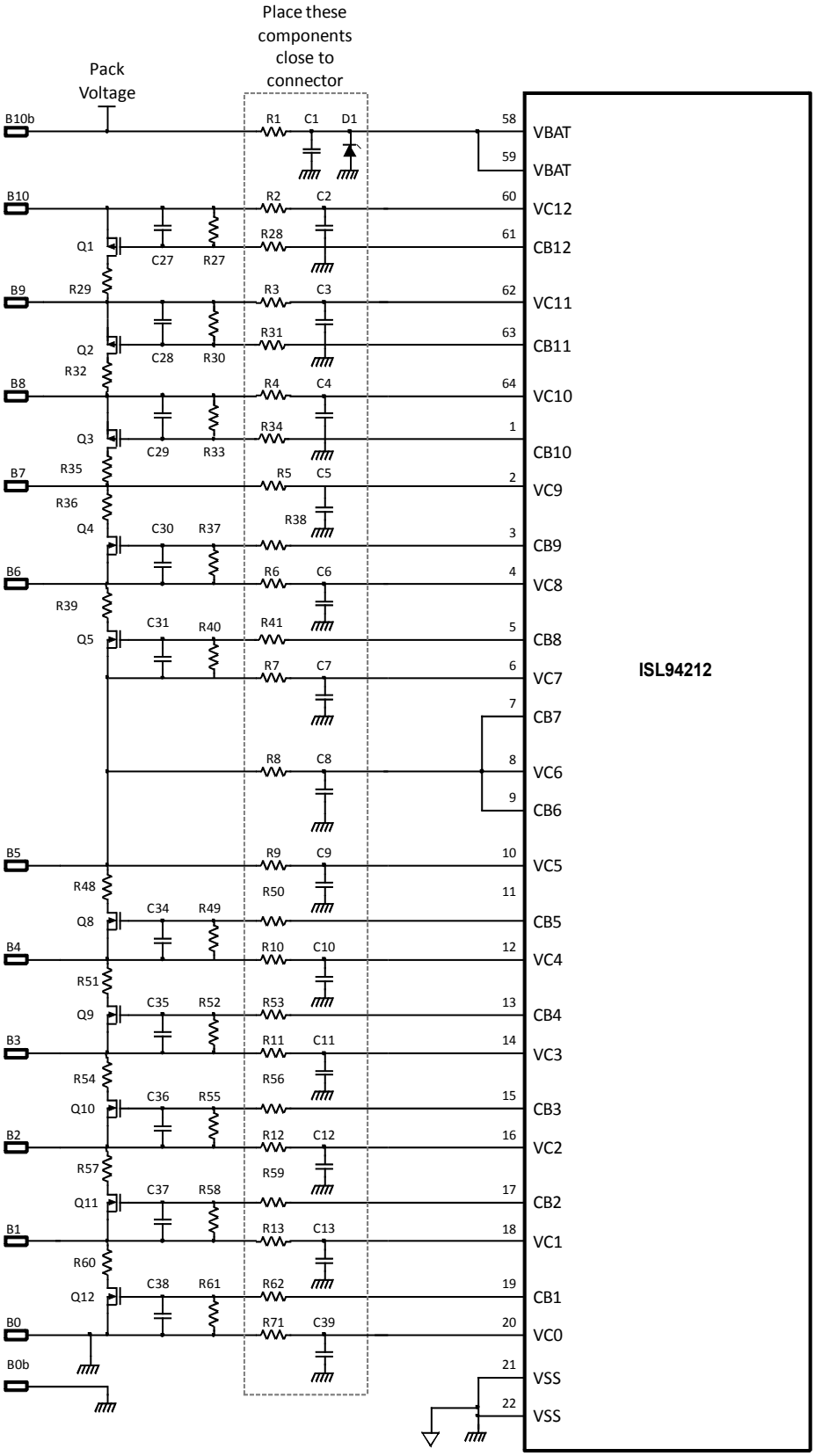


FIGURE 41. BATTERY CONNECTION CIRCUITS, SYSTEM WITH 10 CELLS

Typical Application Circuits (Continued)

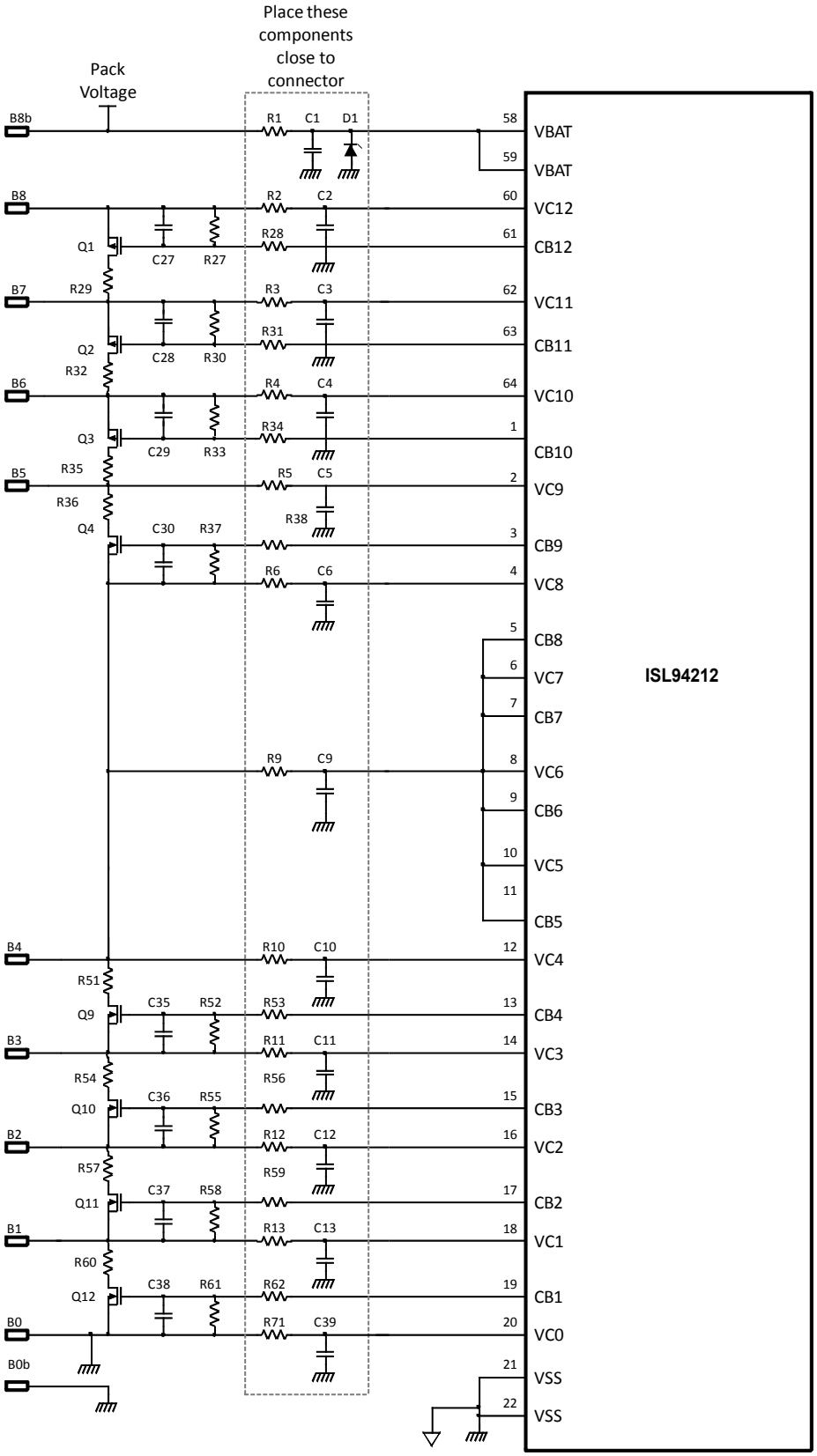


FIGURE 42. BATTERY CONNECTION CIRCUITS, SYSTEM WITH 8 CELLS

Typical Application Circuits (Continued)

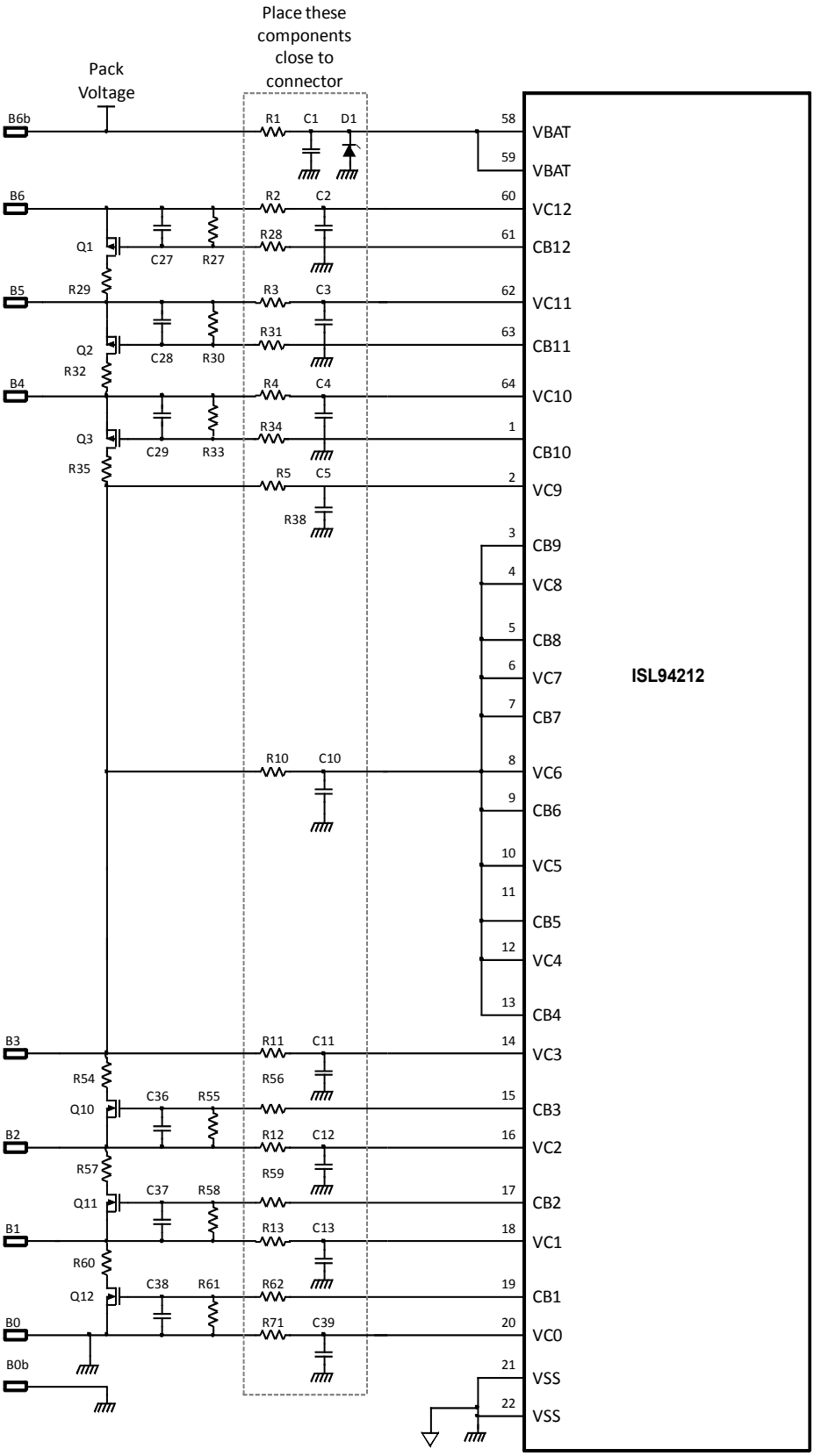
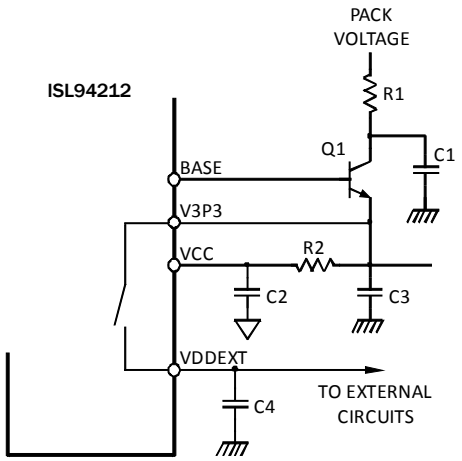


FIGURE 43. BATTERY CONNECTION CIRCUITS, SYSTEM WITH 6 CELLS



COMPONENT	VALUE
R_1	Note 14
R_2	33Ω
C_1	Note 15
C_2	1µF
C_3	1µF
C_4	1µF
Q_1	Note 16

NOTES:

14. R_1 should be sized to pass the maximum supply current at the minimum specified battery pack voltage.
15. C_1 should be selected to produce a time constant with R_1 of a few milliseconds. C_1 and R_1 provide transient protection for the collector of Q_1. Component values and voltage ratings should be obtained through simulation of measurement of the worst case transient expected on V_{BAT}.
16. Q_1 should be selected for power dissipation at the maximum specified battery voltage and load current. The load current includes the V3P3 and VCC currents for the ISL94212 and the maximum current drawn by external circuits supplied via VDDEXT. The voltage rating should be determined as described in Note 15.

FIGURE 44. ISL94212 REGULATOR AND EXTERNAL CIRCUIT SUPPLY ARRANGEMENT

Power Supplies

The two VBAT pins, along with V3P3, VCC and VDDEXT are used to supply power to the ISL94212. Power for the high voltage circuits and **Sleep mode** internal regulators is provided via the VBAT pins. V3P3 is used to supply the logic circuits and VCC is similarly used to supply the low voltage analog circuits. The V3P3 and VCC pins must not be connected to external circuits other than those associated with the ISL94212 main voltage regulator. The VDDEXT pin is provided for use with external circuits.

The ISL94212 main low voltage regulator uses an external NPN pass transistor to supply 3.3V power for the V3P3 and VCC pins. This regulator is enabled whenever the ISL94212 is in **Normal mode** and may also be used to power external circuits via the VDDEXT pin. An internal switch connects the VDDEXT pin to the V3P3 pin. Both the main regulator and the switch are off when the part is placed in **Sleep mode** or **Shutdown mode** (EN pin LOW.) The pass transistor's base is connected to the ISL94212 BASE pin. A suitable configuration for the external components associated with the V3P3, VCC and VDDEXT pins is shown in Figure 44. The external pass transistor is required. Do not allow this pin to float.

Voltage Reference Bypass Capacitor

A bypass capacitor is required between REF (pin 33) and the analog ground VSS. The total value of this capacitor should be in the range 2.0µF to 2.5µF. Use X7R type dielectric capacitors for this function. The ISL94212 continuously performs a power-good check on the REF pin voltage starting 20ms after a power-up, enable or wakeup condition. If the REF capacitor is too large, then the reference voltage may not reach its target voltage range before the Power-good check starts and result in a REF Fault. If the capacitor is too small, then it may lead to inaccurate voltage readings.

Cell Balancing Circuits

The ISL94212 uses external MOSFETs for the cell balancing function. The gate drive for these is derived from on-chip current sources on the ISL94212, which are 25µA nominally. The current sources are turned on and off as needed to control the external MOSFET devices. The current sources are turned off when the device is in **Shutdown mode** or in **Sleep mode**. The ISL94212 uses a mix of N-channel and P-channel MOSFETs for the external balancing function. The top three cell locations, cell 10, 11, 12 are configured to use P-channel MOSFETs while the remaining cell locations, cell 1 through 9, use N-channel MOSFETs.

Consider a circuit for a one cell balancing system. An N-channel MOSFET (cell locations 1 through 9) is shown. The gate of the external FET is normally protected against excessive voltages during cell voltage transients by the action of the parasitic Cgs and Cgd capacitances. These momentarily turn on the FET in the event of a large transient, thus limiting the Vgs values to reasonable levels. A 10nF capacitor is included between the MOSFET gate and source terminals to protect against EMI effects. This capacitor provides a low impedance path to ground at high frequencies and prevents the MOSFET turning on in response to high frequency interference.

The external component values should be chosen to prevent the 9V clamp at the output from the ISL94212 from activating.

Cell Voltage Measurements During Balancing

The standard cell balancing circuit (Figure 37 on page 51) is configured so that the cell measurement is taken from the drain connection of the balancing MOSFET. When balancing is enabled for a cell, the resulting cell measurement is then the voltage across the balancing MOSFET (VGS voltage). This system provides the diagnostic for the cell balancing function. The input voltage of the cell adjacent to the MOSFET drain connection is also affected by this mechanism: the input voltage for this cell increases by the same amount that the voltage of the balance cell decreases.

For example, if cell 2 and cell 3 are both at 3.6V and balancing is enabled for cell 2, then the voltage across the balancing MOSFET may be only 50mV. In this case, cell 2 would read 50mV and cell 3 would read 7.15V. The cell 3 value in this case is outside the measurement range of the cell input. Cell 3 would then read full scale voltage, which is 4.9994V. This full scale voltage reading will occur if the sum of the voltages on the two adjacent cells is greater than the total of 5V plus the “balancing on” voltage of the balanced cell. Table 22 shows the cell affected when each cell is balanced.

TABLE 22. CELL READINGS DURING BALANCING

CELL BALANCED	CELL WITH LOW READING	CELL WITH HIGH READING
1	1	2
2	2	3
3	3	4
4	4	5
5	5	6
6	6	7
7	7	8
8	8	9
9	9*	10*
10	10*	9*
11	11	10
12	12	11

NOTE: *cells 9 and 10 produce a different result from the other cells. Cell 9 uses an N-channel MOSFET while cell 10 uses a P-channel MOSFET. The circuit arrangement used with these devices produces approximately half the normal cell voltage when balancing is enabled. The adjacent cell then sees an increase of half the voltage of the balanced cell.

The voltage measurement behavior outlined above is modified by impedances in the cell connector and any associated wiring. The balance current passes through the connections at the top and bottom of the balanced cell. This effect further reduces the measured voltage on the balanced cell and also increase the voltage measured on cells above and below the balanced cell. For example, if cell 4 is balanced with 100mA and the total impedance of the connector and wiring for each cell connection is 0.1Ω, then cell 4 would read low by an additional 20mV (10mV due to each connection) while cells 3 and 5 would both read high by 10mV.

Balancing with Scan Continuous Mode Enabled

Cell balancing may be active while the ISL94212 is operating in **Scan Continuous mode**. In **Scan Continuous mode** the ISL94212 scans cell voltages, temperatures and open wire conditions at a rate determined by the Scan Interval bits in the Fault Setup register. (See Table 2 on page 23). The behavior of the balancing functions while operating in **Scan Continuous mode** is controlled by the BDDS bit in the Device Setup register. If BDDS is set, then cell balancing is inhibited during cell voltage measurements and for 10ms before the cell voltage scan to allow the balance devices to turn off. Balancing is reenabled at the end of the scan and then balancing continues.

External Inputs

The ISL94212 provides 4 external inputs for use either as general purpose analog inputs or for NTC type thermistors. Each of the external inputs has an internal pull-up resistor, which is connected by a switch to the VCC pin whenever the TEMPREG output is active. This arrangement results in an open input being pulled up to the V_{CC} voltage.

Inputs above 15/16 of full scale are registered as open inputs and cause the relevant bit in the Over-temperature Fault register, along with the OT bit in the Fault Status register to be set, on condition of the respective temperature test enable bit in the Fault Setup register. The user must then read the register value associated with the faulty input to determine if the fault was due to an open input (value above 15/16 full scale) or an over-temperature condition (value below the external temp limit setting).

The arrangement of the external inputs is shown in Figure 44 using the ExT4 input as an example. It is important that the components are connected in the sequence shown in Figure 44, e.g., C_1 must be connected such the trace from this capacitor’s positive terminal connects to R_2 before connecting to R_1. This guarantees the correct operation of the various fault detection functions.

Board Level Calibration

For best accuracy, the ISL94212 may be recalibrated after soldering to a board using a simple resistor trim. The adjustment method involves obtaining the average cell reading error for the cell inputs at a single temperature and cell voltage value and applying a select-on-test resistor to zero the average cell reading error.

The adjustment system uses a resistor placed either between VDDEXT and V_{REF} or V_{REF} and VSS as shown in Figure 45. The value of resistor R_1 or R_2 is then selected based on the average error measured on all cells at 3.3V per cell and room temperature e.g., with 3.3V on each cell input scan the voltage values using the ISL94212 and record the average reading error (ISL94212 reading – cell voltage value). Table 23 shows the value of R_1 and R_2 required for various measured errors.

To use Table 23, find the measured error value closest to the result obtained with measurements using the ISL94212 and select the corresponding resistor value. Alternatively, if finer adjustment resolution is required then this may be obtained by interpolation using Table 23.

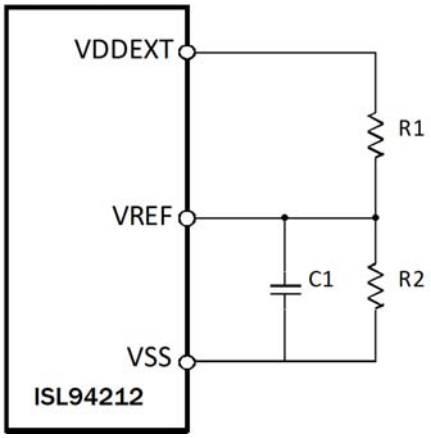


FIGURE 45. CELL READING ACCURACY ADJUSTMENT SYSTEM

TABLE 23. COMPONENT VALUES FOR ACCURACY CALIBRATION ADJUSTMENT OF FIGURE 45

MEASURED ERROR AT VC = 3.3V (mV) $V_{78600} - V_{CELL}$ (mV)	R_1 (kΩ)	R_2 (kΩ)
4	205	DNP
3	274	DNP
2	412	DNP
1	825	DNP
0	DNP	DNP
-1	DNP	2550
-2	DNP	1270
-3	DNP	866
-4	DNP	649

DNP = Do Not populate

Worked Examples

The following worked examples are provided to assist with the setup and calculations associated with various functions.

Voltage Reference Check Calculation

TABLE 24. EXAMPLE REGISTER DATA

R/$\overline{W}$	PAGE	ADDRESS	PARAMETER	VALUE (HEX)	DECIMAL
0	001	010000	IC Temperature	14'h2425	9253
0	001	010101	Reference Voltage	14'h20A7	8359
0	010	111000	Coefficient C	14'h00A4	164
0	010	111001	Coefficient B	14'h3FCD	-51
0	010	111010	Coefficient A	9'h006	6

Coefficients A, B and C are two's compliment numbers. B and C have a range +8191 to -8192. A has a range +255 to -256.

Coefficient B above is a negative number (Hex value > 1FFF). The value for B is 14'h3FCD - 14h3FFF- 1 or (16333_{10} -16383_{10} - 1) = -51.

Coefficient A occupies the upper 9 bits of register 6'b111010 (6'h3A). One way to extract the coefficient data from this register is to divide the complete register value by 32 and rounding the result down to the nearest integer. With 9'h006 in the upper 9 bits, and assuming the lower 5 bits are 0, the complete register value will be 14'h0C0 = 192 decimal. Divide this by 32 to obtain 6.

Coefficients A, B and C are used with the IC temperature reading to calibrate the Reference Voltage reading. The calibration is applied by subtracting an adjustment of the form (see Equation 4) from the Reference Voltage reading.

$$\text{Adjustment} = \frac{A}{256 \times 8192} \times dT^2 + \frac{B}{8192} \times dT + C \quad \text{(EQ. 4)}$$

An example calculation using the data from Table 24 is given in Equation 5.

$$dT = \frac{9253 - 9180}{2} = 36.5 \quad \text{(EQ. 5)}$$

Where 9180 is the Internal Temperature Monitor reading at +25°C (see the "Electrical Specifications" table, T_{INT25} on page 10).

$$\text{Adjustment} = \frac{6}{256 \times 8192} \times (36.5)^2 - \frac{51}{8192} \times 36.5 + 164 = 163.8 \quad \text{(EQ. 6)}$$

$$\text{Corrected } V_{REF} = 8359 - 163.8 = 8195.2 \quad \text{(EQ. 7)}$$

$$V_{REF} \text{ value} = \frac{8195.2}{16384} \times 5 = 2.5010 \quad \text{(EQ. 8)}$$

Cell Balancing – Manual Mode

Refer to "Manual Balance Mode" on page 26.

EXAMPLE: ACTIVATE BALANCING ON CELLS 1, 5, 7 AND 11

Step 1. Write *Balance Setup* register: Set **Manual Balance mode**, Balance Status pointer, and turn off balance.

BMD = 01 (**Manual Balance mode**)
BWT = XXX
BSP = 0000 (Balance status pointer location 0)
BEN = 0 (Balancing disabled)

Note: Green text indicates a register change.

BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX00 000X XX01

X = don't care

Step 2. Write Balance Status register: Set bits 0, 4, 6 and 10

BAL12:1 = 0100 0101 0001

BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0100 0101 0001

Step 3. Enable balancing using Balance Enable command

BALANCE ENABLE COMMAND

R/W	PAGE	ADDRESS	DATA
0	011	010000	00 0000

Or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX1X XXXX XXXX

The balance FETs attached to cells 1, 5, 7 and 11 turn on.

Turn balancing off by resetting BEN or by sending the Balance Inhibit command (Page 3, address 6'h11).

Cell Balancing – Timed Mode

Refer to "Timed Balance Mode" on page 27.

EXAMPLE: ACTIVATE BALANCING ON CELLS 2 AND 8 FOR 1 MINUTE.

Step 1. Write Balance Setup register: Set **Timed Balance mode**, Balance Status pointer, and turn off balance.

BMD = 10 (**Timed Balance mode**)
BWT = XXX
BSP = 0000 (Balance status pointer location 0)
BEN = 0 (BALANCING disabled)

BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX00 000X XX10

X = don't care

Step 2. Write Balance Status register: Set bits 1 and 7

BAL12:1 = 0000 1000 0010

BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0000 1000 0010

Step 3. Write balance timeout setting to the Watchdog/Balance Time register (page 2, address 6'h15, bits [13:7])

BTM6:1 = 0000011 (1 minute)

WATCHDOG/BALANCE TIME REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010101	00 0001 1XXX XXXX

X = don't care – the lower bits are the watchdog timeout value and should be set to a time longer than the balance time. A value of 111 1111 is suggested.

Step 4. Enable balancing using Balance Enable command

BALANCE ENABLE COMMAND

R/W	PAGE	ADDRESS	DATA
0	011	010000	00 0000

Or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX1X XXXX XXXX

The balance FETs attached to cells 2 and 8 turn on. The FETs turn off after 1 minute. Balancing may be stopped by resetting BEN or by sending the Balance Inhibit command.

Cell Balancing – Auto Mode

Refer to "Auto Balance Mode" on page 27.

BALANCE VALUE CALCULATION EXAMPLE

This example is based on a cell State of Charge (SOC) of 9360 coulombs, a target SOC of 8890 coulombs, a balancing leg impedance of 31Ω (30Ω resistor plus 1Ω FET on resistance) and a sampling time interval of 5 minutes (300 seconds).

The Balance Value is calculated using Equation 9.

$$B = \frac{8191}{5} \times (9360 - 8890) \times \frac{31}{300} = 79562 = 28'h00136CA \quad \text{(EQ. 9)}$$

The value 8191/5 is the scaling factor of the cell voltage measurement.

The value of 28'h00136CA is loaded to the required Cell Balance Register and the value 7'b0001111 (5 minutes) is loaded to the Balance Time bits in the Watchdog/Balance time register.

In this example, the total coulomb difference to be balanced is: 470 coulomb (9360 - 8890). At 3.3V/31Ω*300s = 31.9 coulomb per cycle, it takes about 15 cycles for the balancing to terminate.

AUTO BALANCE MODE CELL BALANCING EXAMPLE

The following describes a simple setup to demonstrate the **Auto Balance mode** cell balancing function of the ISL94212. Note that this balancing setup is not related to the balance value calculation in Equation 9.

Auto balance cells using the following criteria:

- Balance time = 20s
- Balance wait time (dead time between balancing cycles) = 8s
- Balancing disabled during cell measurements.
- Balance Values: See Table 25

TABLE 25. CELL BALANCE VALUES (HEX) FOR EACH CELL

CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12
28'h 406A	28'h 3E4D	28'h 0	28'h 292F	28'h 3E00	28'h 0	28'h 2903	28'h 3D06	28'h 0	28'h 151E	28'h 502	28'h 6D6

- Balance Status Register: Set up balance:
  Cells 1, 4, 7 and 10 on 1st cycle.
  Cells 3, 6, 9 and 12 on 2nd cycle.
  Cells 2, 5, 8 and 11 on 3rd cycle
  (See Table 26)

TABLE 26. BALANCE STATUS SETUP

BPS [3:0]	CELL 1	2	3	4	5	6	7	8	9	10	11	12
0000	Reserved for **Manual Balance mode** and **Timed Balance mode**											
0001	1	0	0	1	0	0	1	0	0	1	0	0
0010	0	0	1	0	0	1	0	0	1	0	0	1
0011	0	1	0	0	1	0	0	1	0	0	1	0

Step 1. Write Balance Value registers

BALANCE VALUE REGISTERS

R/$\overline{W}$	PAGE	ADDRESS	DATA (HEX)	CELL
1	010	100000	14'h006A	1
1	010	100001	14'h0001	
1	010	100010	14'h3E4D	2
1	010	100011	14'h0000	
1	010	100100	14'h0000	3
1	010	100101	14'h0000	
1	010	100110	14'h292F	4
1	010	100111	14'h0000	
1	010	101000	14'h3E00	5
1	010	101001	14'h0000	
1	010	101010	14'h0000	6
1	010	101011	14'h0000	
1	010	101100	14'h2903	7
1	010	101101	14'h0000	
1	010	101110	14'h3D06	8
1	010	101111	14'h0000	
1	010	110000	14'h0000	9
1	010	110001	14'h0000	
1	010	110010	14'h151E	10
1	010	110011	14'h0000	
1	010	110100	14'h0502	11
1	010	110101	14'h0000	
1	010	110110	14'h06D6	12
1	010	110111	14'h0000	

BALANCE VALUE REGISTERS (CELL1) - VALUE 28'h406A

6'20	B0107	B0106	B0105	B0104	B0103	B0102	B0101	B0100
	0	1	1	0	1	0	1	0
			B0113	B0112	B1011	B0110	B0109	B0108
			0	0	0	0	0	0
6'21	B0121	B0120	B0119	B0118	B0117	B0116	B0115	B0114
	0	0	0	0	0	0	0	1
			B0127	B0126	B0125	B0124	B0123	B0122
			0	0	0	0	0	0

Step 2. Write *BDDS* bit in *Device Setup* register (turn balancing functions off during measurement)

BDDS = 1

DEVICE SETUP REGISTER

R/$\overline{W}$	PAGE	ADDRESS	DATA
1	010	011001	XX XXXX 1XXX XXXX

X = don't care

Step 3. Write balance timeout setting to the Watchdog/Balance Time register: Balance timeout code = 0000001 (20 seconds)

BTM6:0 = 000 0001

BALANCE TIMEOUT REGISTER

R/$\overline{W}$	PAGE	ADDRESS	DATA
1	010	010101	00 0000 1XXX XXXX

X = don't care – the lower bits are the watchdog timeout value and should be set to a time longer than the balance time. A value 111 1111 is suggested.

Step 4. Set up Balance Status register (from Table 26 on page 64)

Step 4A. Write Balance Setup register: Set **Auto Balance mode**, set 8 second Balance wait time, and set balance off:

BMD = 11 (**Auto Balance mode**)
BWT = 100 (8 seconds)
BEN = 0 (Balancing disabled)

BALANCE SETUP REGISTER

R/$\overline{W}$	PAGE	ADDRESS	DATA
1	010	010011	XX XX0X XXX1 0011

X = don't care

Step 4B. Write Balance Setup register: Set Balance Status Pointer = 1

BSP = 0001 (Balance status pointer = 1)

BALANCE SETUP REGISTER

R/$\overline{W}$	PAGE	ADDRESS	DATA
1	010	010011	XX XXX0 001X XXXX

X = don't care

Step 4C. Write Balance Status register: Set bits 1, 4, 7 and 10

BAL12:1 = 0010 0100 1001

BALANCE STATUS REGISTER

R/$\overline{W}$	PAGE	ADDRESS	DATA
1	010	010100	XX 0010 0100 1001

Step 4D. Write Balance Setup register: Set Balance Status Pointer = 2

BSP = 0010 (Balance status pointer = 2)

BALANCE SETUP REGISTER

R/$\overline{W}$	PAGE	ADDRESS	DATA
1	010	010011	XX XXX0 010X XXXX

X = don't care

Step 4E. Write Balance Status register: Set bits 3, 6, 9 and 12

BAL12:1 = 1001 0010 0100

BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 1001 0010 0100

Step 4F. Write Balance Setup register: Set Balance Status Pointer = 3

BSP = 0011 (Balance status pointer = 3)

BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XXX0 011X XXXX

X = don't care

Step 4G. Write Balance Status register: Set bits 2, 5, 8 and 11

BAL12:1 = 0100 1001 0010

BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0100 1001 0010

Step 4H. Write *Balance Setup* register: Set Balance Status Pointer = 4

BSP = 0100 (Balance status pointer = 4)

BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XXX0 100X XXXX

X = don't care

Step 4I. Write Balance Status register: Set bits to all zero to set the end point for the instances.

BAL12:1 = 0000 0000 0000

BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0000 0000 0000

Step 5. Enable balancing using the Balance Enable command

BALANCE ENABLE COMMAND

R/W	PAGE	ADDRESS	DATA
0	011	010000	00 0000

Or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX1X XXXX XXXX

The balance FETs cycle through each instance of the Balance Status register in a loop, interposing the balance wait time between each instance. The measured voltage of each cell being balanced is subtracted from the balance value for that cell at the end of each balance status instance. The process continues until the Balance Value register for each cell contains zero.

Register Map

R/W + PAGE				BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE	ADDRESS	REGISTER NAME			BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0001		000000	V_{BAT} Voltage	VB7	VB6	VB5	VB4	VB3	VB2	VB1	VB0
						VB13	VB12	VB11	VB10	VB9	VB8
0001		000001	Cell 1 Voltage	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
						C1V13	C1V12	C1V11	C1V10	C1V9	C1V8
0001		000010	Cell 2 Voltage	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
						C2V13	C2V12	C2V11	C2V10	C2V9	C2V8
0001		000011	Cell 3 Voltage	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
						C3V13	C3V12	C3V11	C3V10	C3V9	C3V8
0001		000100	Cell 4 Voltage	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
						C4V13	C4V12	C4V11	C4V10	C4V9	C4V8
0001		000101	Cell 5 Voltage	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
						C5V13	C5V12	C5V11	C5V10	C5V9	C5V8

Register Map (Continued)

R/$\overline{W}$ + PAGE		ADDRESS	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE					BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0001		000110	Cell 6 Voltage	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
						C6V13	C6V12	C6V11	C6V10	C6V9	C6V8
0001		000111	Cell 7 Voltage	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
						C7V13	C7V12	C7V11	C7V10	C7V9	C7V8
0001		001000	Cell 8 Voltage	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
						C8V13	C8V12	C8V11	C8V10	C8V9	C8V8
0001		001001	Cell 9 Voltage	C9V7	C9V6	C9V5	C9V4	C9V3	C9V2	C9V1	C9V0
						C9V13	C9V12	C9V11	C9V10	C9V9	C9V8
0001		001010	Cell 10 Voltage	C10V7	C10V6	C10V5	C10V4	C10V3	C10V2	C10V1	C10V0
						C10V13	C10V12	C10V11	C10V10	C10V9	C10V8
0001		001011	Cell 11 Voltage	C11V7	C11V6	C11V5	C11V4	C11V3	C11V2	C11V1	C11V0
						C11V13	C11V12	C11V11	C11V10	C11V9	C11V8
0001		001100	Cell 12 Voltage	C12V7	C12V6	C12V5	C12V4	C12V3	C12V2	C12V1	C12V0
						C12V13	C12V12	C12V11	C12V10	C12V9	C12V8
0001		001111	All Cell Voltage Data	Daisy chain configuration only. This command returns all Page 1 data from address 6'h00 through 6'h0C in a single data stream.							
0001		010000	IC Temperature	ICT7	ICT6	ICT5	ICT4	ICT3	ICT2	ICT1	ICT0
						ICT13	ICT12	ICT11	ICT10	ICT9	ICT8
0001		010001	External Temperature Input 1 Voltage (ExT1 pin)	ET1V7	ET1V6	ET1V5	ET1V4	ET1V3	ET1V2	ET1V1	ET1V0
						ET1V13	ET1V12	ET1V11	ET1V10	ET1V9	ET1V8
0001		010010	External Temperature Input 2 Voltage (ExT2 pin)	ET2V7	ET2V6	ET2V5	ET2V4	ET2V3	ET2V2	ET2V1	ET2V0
						ET2V13	ET2V12	ET2V11	ET2V10	ET2V9	ET2V8
0001		010011	External Temperature Input 3 Voltage (ExT3 pin)	ET3V7	ET3V6	ET3V5	ET3V4	ET3V3	ET3V2	ET3V1	ET3V0
						ET3V13	ET3V12	ET3V11	ET3V10	ET3V9	ET3V8
0001		010100	External Temperature Input 4 Voltage (ExT4 pin)	ET4V7	ET4V6	ET4V5	ET4V4	ET4V3	ET4V2	ET4V1	ET4V0
						ET4V13	ET4V12	ET4V11	ET4V10	ET4V9	ET4V8
0001		010101	Secondary Reference Voltage	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0
						RV13	RV12	RV11	RV10	RV9	RV8
0001		010110	Scan Count					SCN3	SCN2	SCN1	SCN0
0001		011111	All Temperature Data	Daisy chain configuration only. This command returns all Page 1 data from address 6'h10 through 6'h16 in a single data stream.							
0010	1010	000000	Overvoltage Fault	OF8	OF7	OF6	OF5	OF4	OF3	OF2	OF1
								OF12	OF11	OF10	OF9
0010	1010	000001	Undervoltage Fault	UF8	UF7	UF6	UF5	UF4	UF3	UF2	UF1
								UF12	UF11	UF10	UF9
0010	1010	000010	Open Wire Fault	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0
							OC12	OC11	OC10	OC9	OC8

Register Map (Continued)

R/$\overline{W}$ + PAGE		ADDRESS	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE					BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0010	1010	000011	Fault Setup	TOT2	TOT1	TOT0	WSCN	SCN3	SCN2	SCN1	SCN0
							TTST4	TTST3	TTST2	TTST1	TTST0
0010	1010	000100	Fault Status	OW	UV	OV	OT	WDGF	OSC	0	0
						MUX	REG	REF	PAR	OVSS	OV_{BAT}
0010	1010	000101	Cell Setup	C8	C7	C6	C5	C4	C3	C2	C1
						FFSN	FFSP	C12	C11	C10	C9
0010	1010	000110	Over-temperature Fault				TFLT4	TFLT3	TFLT2	TFLT1	TFLT0
0010		001111	All Fault Data	Daisy Chain configuration only. This command returns all Page 2 data from address 6'h00 through 6'h06 in a single data stream.							
0010	1010	010000	Overvoltage Limit	OV7	OV6	OV5	OV4	OV3	OV2	OV1	OV0
						OV13	OV12	OV11	OV10	OV9	OV8
0010	1010	010001	Undervoltage Limit	UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0
						UV13	UV12	UV11	UV10	UV9	UV8
0010	1010	010010	External Temp Limit	ETL7	ETL6	ETL5	ETL4	ETL3	ETL2	ETL1	ETL0
						ETL13	ETL12	ETL11	ETL10	ETL9	ETL8
0010	1010	010011	Balance Setup	BSP2	BSP1	BSP0	BWT2	BWT1	BWT0	BMD1	BMD0
										BEN	BSP3
0010	1010	010100	Balance Status (Cells to Balance)	BAL8	BAL7	BAL6	BAL5	BAL4	BAL3	BAL2	BAL1
								BAL12	BAL11	BAL10	BAL9
0010	1010	010101	Watchdog/Balance Time	BTM0	WDG6	WDG5	WDG4	WDG3	WDG2	WDG1	WDG0
						BTM6	BTM5	BTM4	BTM3	BTM2	BTM1
0010	1010	010110	User Register	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0
						UR13	UR12	UR11	UR10	UR9	UR8
0010	1010	010111	User Register	UR21	UR20	UR19	UR18	UR17	UR16	UR15	UR14
						UR27	UR26	UR25	UR24	UR23	UR22
0010		011000	Comms Setup	SIZE3	SIZE2	SIZE1	SIZE0	ADDR3	ADDR2	ADDR1	ADDR0
								CRAT1	CRAT0	CSEL2	CSEL1
0010	1010	011001	Device Setup	BDDS	0	ISCN	SCAN	EOB	0	Pin 37	Pin 39
						WP5	WP4	WP3	WP2	WP1	WP0
0010		011010	Internal Temp Limit	ITL7	ITL6	ITL5	ITL4	ITL3	ITL2	ITL1	ITL0
						ITL13	ITL12	ITL11	ITL10	ITL9	ITL8
0010		011011	Serial Number 0	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
						SN13	SN12	SN11	SN10	SN9	SN8
0010		011100	Serial Number 1	SN21	SN20	SN19	SN18	SN17	SN16	SN15	SN14
						SN27	SN26	SN25	SN24	SN23	SN22
0010		011101	Trim Voltage	RESERVED							
						TV5	TV4	TV3	TV2	TV1	TV0

Register Map (Continued)

R/$\overline{W}$ + PAGE				BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE	ADDRESS	REGISTER NAME			BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0010		011111	All Setup Data	Daisy Chain configuration only. This command returns all Page 2 data from address 6'h10 through 6'h1D in a single data stream.							
0010	1010	100000	Cell 1 Balance Value 0	B0107	B0106	B0105	B0104	B0103	B0102	B0101	B0100
						B0113	B0112	B1011	B0110	B0109	B0108
0010	1010	100001	Cell 1 Balance Value 1	B0121	B0120	B0119	B0118	B0117	B0116	B0115	B0114
						B0127	B0126	B0125	B0124	B0123	B0122
0010	1010	100010	Cell 2 Balance Value 0	B0207	B0206	B0205	B0204	B0203	B0202	B0201	B0200
						B0213	B0212	B1011	B0210	B0209	B0208
0010	1010	100011	Cell 2 Balance Value 1	B0221	B0220	B0219	B0218	B0217	B0216	B0215	B0214
						B0227	B0226	B0225	B0224	B0223	B0222
		~	~	~							
0010	1010	110111	Cell 12 Balance Value 1	B1221	B1220	B1219	B1218	B1217	B1216	B1215	B1214
						B1227	B1226	B1225	B1224	B1223	B1222
0010		111000	Reference Coefficient C	RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0
						RCC13	RCC12	RCC11	RCC10	RCC9	RCC8
0010		111001	Reference Coefficient B	RCB7	RCB6	RCB5	RCB4	RCB3	RCB2	RCB1	RCB0
						RCB13	RCB12	RCB11	RCB10	RCB9	RCB8
0010		111010	Reference Coefficient A	RCA2	RCA1	RCA0	RESERVED				
						RCA8	RCA7	RCA6	RCA5	RCA4	RCA3
0010		111011	Cell Balance Enabled	CBEN8	CBEN7	CBEN6	CBEN5	CBEN4	CBEN3	BAL2	CBEN1
								CBEN12	CBEN11	CBEN10	CBEN9

Register Map (Continued)

R/$\overline{W}$ + PAGE				BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE	ADDRESS	REGISTER NAME			BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0011		000001	Scan Voltages								
0011		000010	Scan Temperatures								
0011		000011	Scan Mixed								
0011		000100	Scan Wires								
0011		000101	Scan All								
0011		000110	Scan Continuous								
0011		000111	Scan Inhibit								
0011		001000	Measure								
0011		001001	Identify								
0011		001010	Sleep								
0011		001011	NAK								
0011		001100	ACK								
0011		001110	Comms Failure								
0011		001111	Wakeup								
0011		010000	Balance Enable								
0011		010001	Balance Inhibit								
0011		010010	Reset								
0011		010011	Calc Register Checksum								
0011		010100	Check Register Checksum								
0100		111111	EEPROM MISR Data Register	14-bit MISR EEPROM checksum value. Programmed during test.							
0101		000000	MISR Calculated Checksum	14-bit shadow register MISR checksum value. Calculated when shadow registers are loaded from nonvolatile memory							

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
April 23, 2015	FN7938.1	Changed ground references in Figure 1 on page 1. Abs Max “Absolute Maximum Ratings” on page 7 changed the text in the ESD Ratings from Capacitive Discharge to Charge Device Model “Recommended Operating Conditions” on page 7 moved ExT1, ExT2, ExT3, ExT4, which had voltage range 0V to 3.6V to separate line with voltage range 0V to 2.5V. Added to “BASE” in “Pin Descriptions” on page 4, “Do not let this pin float.” Table 3 on page 24, Changed “Cell 0 Voltage” to “VBAT Voltage”. Changed “Fault Signal Filtering” on page 35 to add the comment in 2nd paragraph, “When a fault is detected, the *[TOT2:0]* bits should be rewritten.” Table 18 on page 36, changed in comments for “Read checksum value calculated by ISL94212” from: ...“cycling the EN pin or the host issuing a Reset command.” to: ...“cycling the EN pin followed by a host initiated Reset command, or simply the host issuing a Reset command.” Changed Section, “System Registers,” on page 39. Changed in 4th paragraph 1st sentence “when the EN pin is low” to “when the EN pin is toggled and the device receives a *Reset* Command”. Section, “Register Descriptions,” on page 40: Changed “Cell 0 Voltage” to “VBAT Voltage” and added voltage calculation equations. System Register description “TOT0, 1, 2” on page 42 added the comment, “This register must be rewritten following an error detection resulting from totalizer overflow.” Added to last sentence 2nd paragraph in Section, “Power Supplies,” on page 60, “The external pass transistor is required. Do not allow this pin to float.” Changed all pin name references to all caps. Updated Definitions for Shutdown Mode in “Power Modes” on page 21. Replaced “Measurement and Communication Timing” Section (pages 51 to 58 of previous revision) with new section “System Registers” on page 39
December 14, 2012	FN7938.0	Initial Release.

About Intersil

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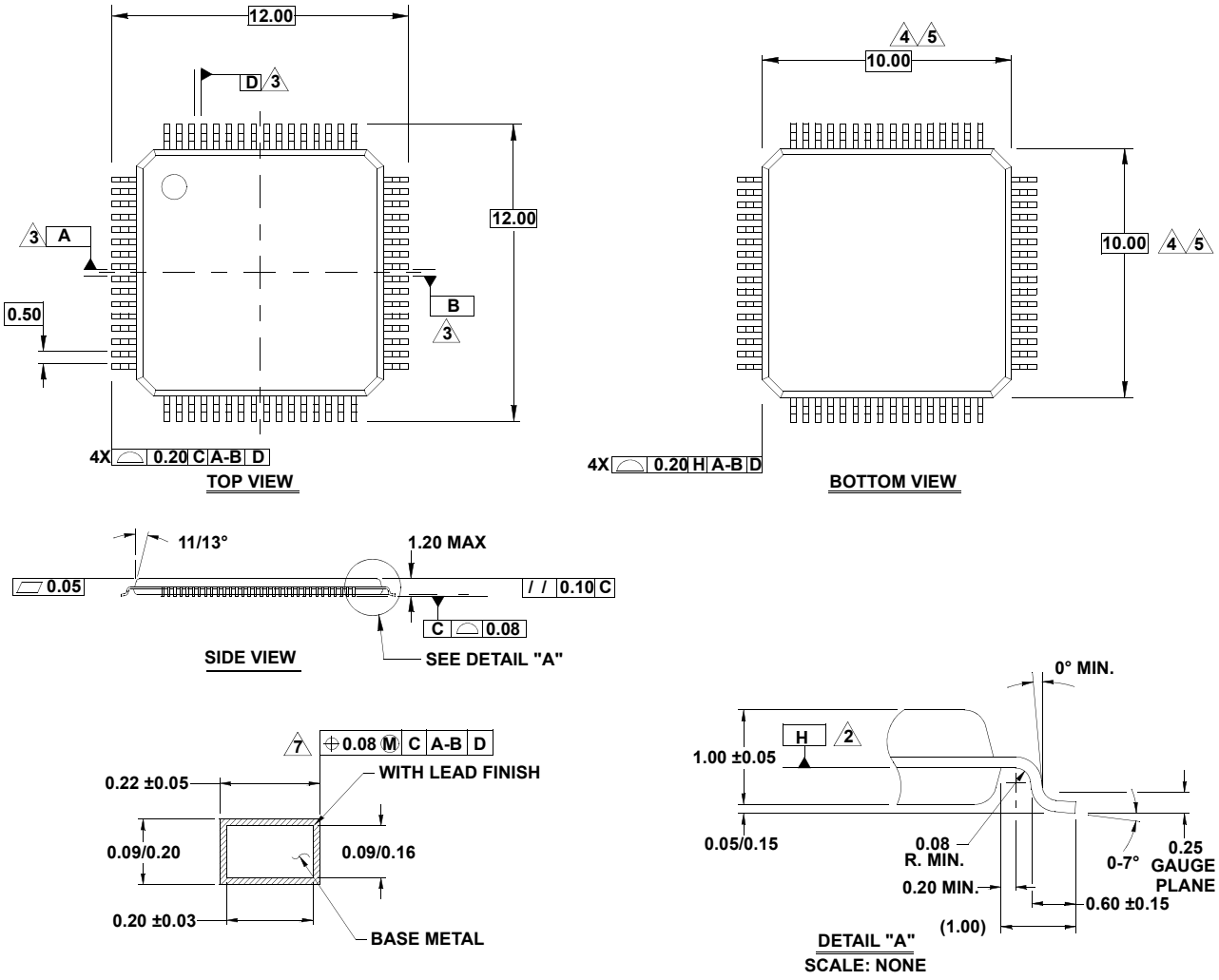
Package Outline Drawing
Q64.10x10D
64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

Rev 2, 9/12



NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.254mm.
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
7. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total at maximum material condition. Dambar cannot be located on the lower radius or the foot.
8. Controlling dimension: millimeter.
9. This outline conforms to JEDEC publication 95 registration MS-026, variation ACD.
10. Dimensions in ( ) are for reference only.