

# BVA518

## 5-4000 MHz DIGITAL VARIABLE GAIN AMPLIFIER



### Product Description

The BVA518 is a digitally controlled variable gain amplifier (DVGA) is featuring high linearity using the voltage 5V supply with a broadband frequency range of 5 to 4000 MHz.

The BVA518 integrates a high performance digital step attenuator and high performance InGaP/GaAs HBT MMIC amplifier. Amplifier is internally matched to 50 Ohms and uses a patented **temperature compensation circuit** to provide stable current over the operating temperature range without the need for external components and a patented **over voltage protection** circuit to protect a internal device. The BVA518 is designed for high linearity gain block applications that require excellent gain flatness and designed for use in 3G/4G wireless infrastructure and other high performance RF applications

Both stages are internally matched to 50 Ohms and It is easy to use with no external matching components required

A serial output port enables cascading with other serial controlled devices.

An integrated digital control interface supports both serial and parallel programming of the attenuation, including the capability to program an initial attenuation state at power-up. Covering a 31.5 dB attenuation range in 0.5 dB steps.

The BVA518 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application

Figure 2. Package Type

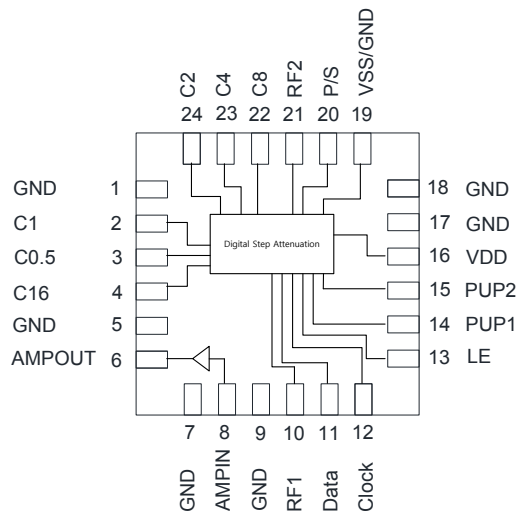


24-lead 4x4 mm QFN

### Device Features

- Small 24-Pin 4 x 4 mm QFN Package
- Integrate DSA to Amp Functionality
- Wide Power supply range of +2.7~5.5V(DSA)
- Single Fixed +5V supply (AMP)
- 5-4000MHZ Broadband Performance
- 19.1dB Gain at 1.9GHz
- 5.8dB Noise Figure at max gain setting
- 18.6dBm P1dB at 1.9GHz
- 32.2dBm OIP3 at 1.9GHz
- Patented temperature compensation
- Patented Over Voltage Protection Circuit
- No matching circuit needed
- Attenuation: 0.5 dB steps to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy(DSA to Amp)
  - ±(0.10 + 2% x Atten) @ 1 GHz
  - ±(0.15 + 2% x Atten) @ 2.2 GHz
  - ±(0.15 + 8% x Atten) @ 4 GHz
- 1.8V control logic compatible
- 105°C operating temperature
- Programming modes
  - Direct Parallel
  - Latched Parallel
  - Serial
- Unique power-up state selection

Figure 1. Functional Block Diagram



### Application

- 3G/4G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

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**Table 1. Electrical Specifications<sup>1</sup>**

Parameter		Condition	Min	Typ	Max	Unit
<b>Operational Frequency Range</b>			5		4000	MHz
<b>Gain</b>		Attenuation = 0dB, at 1900MHz		19.1		dB
<b>Attenuation Control range</b>		0.5dB step		31.5		dB
<b>Attenuation Step</b>				0.5		dB
<b>Attenuation Accuracy</b>	5MHz-1GHz	Any bit or bit combination			$\pm(0.10 + 2\%$ of atten setting)	dB
	>1GHz-2.2GHz				$\pm(0.15 + 2\%$ of atten setting)	
	>2.2GHz-4GHz				$\pm(0.15 + 8\%$ of atten setting)	
<b>Return loss (input or output port)</b>	1GHz-2.2GHz	Attenuation = 0dB	14.3	15.6		dB
	2.2GHz-4GHz		11.2	18.8		
<b>Output Power for 1dB Compression</b>		Attenuation = 0dB , at 1900MHz		18.6		dBm
<b>Output Third Order Intercept Point</b>		Attenuation = 0dB, at 1900MHz two tones at an output of 7 dBm per tone separated by 1 MHz.		32.2		dBm
<b>Noise Figure</b>		Attenuation = 0dB, at 1900MHz		5.8		dB
<b>Switching time</b>		50% CTRL to 90% or 10% RF		500	800	ns
<b>Supply voltage</b>		DSA	2.7		5.5	V
		AMP		5		V
<b>Supply Current</b>			63	73	83	mA
<b>Control Interface</b>		Serial / parallel mode		6		Bit
<b>Control Voltage</b>		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.6	V
<b>Impedance</b>				50		$\Omega$

<sup>1</sup> Device performance \_ measured on a BeRex Evaluation board at 25°C, 50  $\Omega$  system, VDD=+5V, measure on Evaluation Board (DSA to AMP)

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**Table 2. Typical RF Performance<sup>1</sup>**

Parameter	Frequency					Unit
	70 <sup>3</sup>	900	1900	2140	2700	
Gain	24.0	20.6	19.1	18.7	17.4	dB
S11	-13.0	-15.9	-16.5	-18	-24.6	dB
S22	-11.4	-16.6	-15.3	-14.8	-14.2	dB
OIP3 <sup>2</sup>	35.8	35.6	32.2	31.5	28.3	dBm
P1dB	18.1	19.9	18.6	18.1	16.4	dBm
Noise Figure	5.2	5.4	5.8	5.9	6.4	dB

<sup>1</sup> Device performance \_ measured on a BeRex evaluation board at 25°C, VDD=+5V,50 Ω system. measure on Evaluation Board (DSA to AMP)

<sup>2</sup> OIP3 \_ measured with two tones at an output of 7dBm per tone separated by 1 MHz.

<sup>3</sup> 70MHz measured with IF application circuit.(refer to table 10.)

**Table 3. Absolute Maximum Ratings**

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage(VCC)	Amp/DSA			6	V
Supply Current	Amp			160	mA
Digital input voltage		-0.3		3.6	V
Maximum input power	Amp/DSA			+23/+30	dBm
Operating Temperature	Amp/DSA	-40		85/105	°C
Storage Temperature		-55		155	°C
Junction Temperature			150		°C

Operation of this device above any of these parameters may result in permanent damage.



### Programming Options

#### Parallel/Serial Selection

Either a parallel or serial interface can be used to control the BVA518. The P/S bit provides this selection, with P/S = LOW selecting the parallel interface and P/S = HIGH selecting the serial interface.

#### Parallel Mode Interface

The parallel interface consists of six CMOS compatible control lines that select the desired attenuation state, as shown in *Table 4*.

The parallel interface timing requirements are defined by *Figure 4* (Parallel Interface Timing Diagram), *Table 7* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched* parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per *Figure 3*) to latch the new attenuation state into the device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for

Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by *Figure 3* (Serial Interface Timing Diagram) and *Table 6* (Serial Interface AC Characteristics).

#### Power-up Control Settings

The BVA518 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S = 1), the six control bits are set to whatever data is present on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S = 0) with LE = 0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in *Table 5* (Power-Up Truth Table, Parallel Mode).

**Table 4. Truth Table**

P/S	C16	C8	C4	C2	C1	C0.5	Attenuation state
0	0	0	0	0	0	0	Reference Loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: Not all 64 possible combinations of C0.5-C16 are shown in table

#### Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data,

**Table 5. Parallel PUP Truth Table**

P/S	LE	PUP2	PUP1	Attenuation state
0	0	0	0	Reference Loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31.5 dB
0	1	X	X	Defined by C0.5-C16

Note: Power up with LE = 1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active



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### Typical Performance Plot - BVA518 EVK - PCB(RF Circuit\*:500~4000MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 5.0V unless otherwise noted

Figure 5. WCDMA 4FA 2140 –60dBc

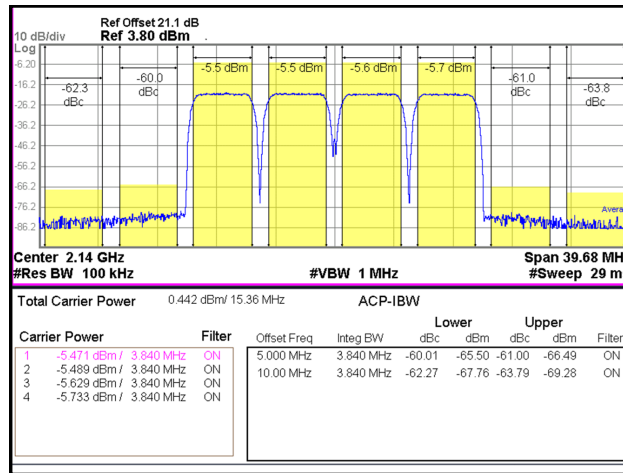


Figure 6. ACLR @3GPP 4FA WCDMA, 1-64DPCH, ±5MHz offset, 64-ch FWD 2140MHz

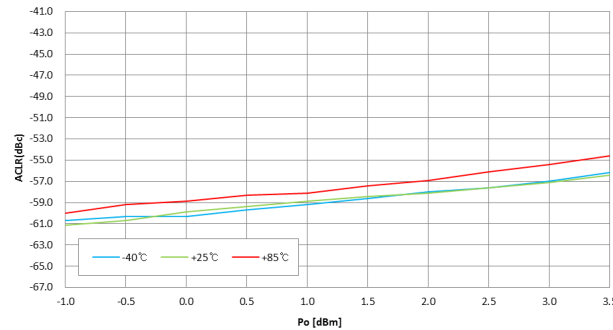


Figure 7. Device Performance Pin-Pout-Gain @900MHz

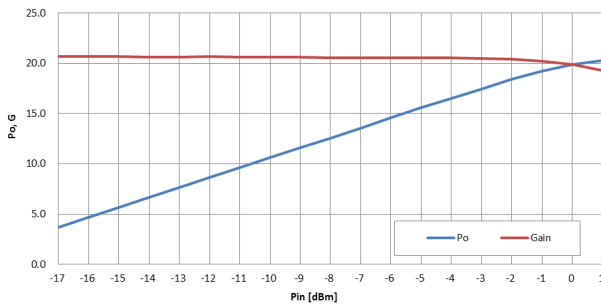
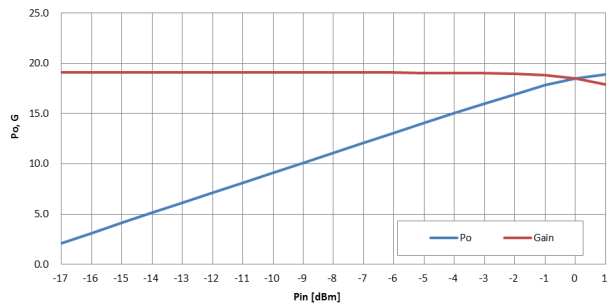


Figure 8. Device Performance Pin-Pout-Gain @1900MHz



\* RF Circuit application refer to Table 10.

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### Typical Performance Plot - BVA518 EVK - PCB(RF Circuit\*:500~4000MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 5.0V unless otherwise noted

Figure 9. Gain vs Frequency

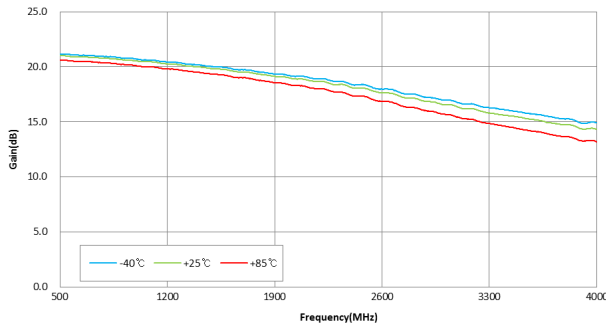


Figure 10. Gain vs Frequency @ Major Attenuation Steps

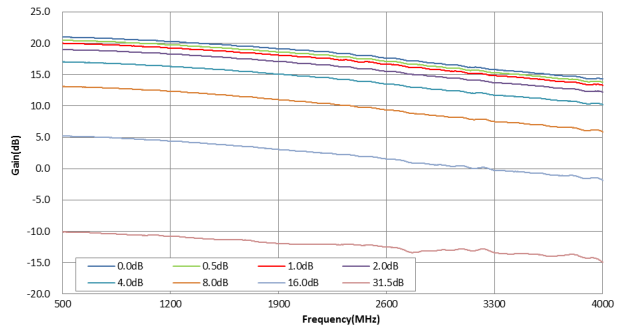


Figure 11. Input Return Loss vs Frequency

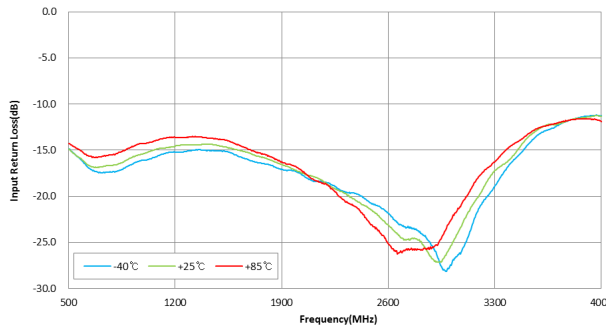
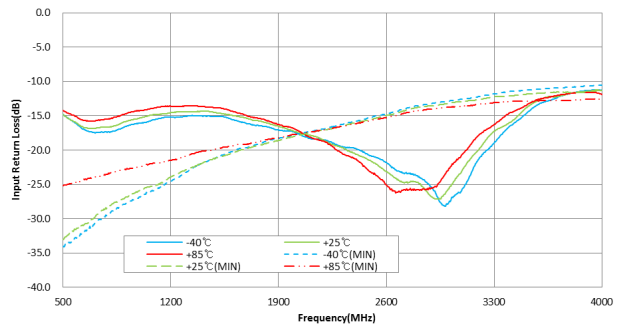


Figure 12. Input Return Loss vs Frequency @ Max Gain & Min Gain<sup>1</sup> State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

Figure 13. output Return Loss vs. Frequency

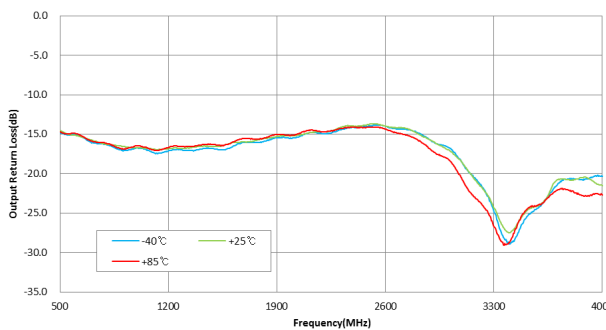
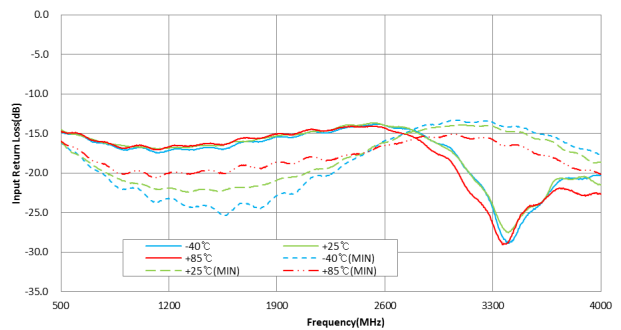


Figure 14. output Return Loss vs. Frequency @ Max Gain & Min Gain<sup>1</sup> State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

\* RF Circuit application refer to Table 10.

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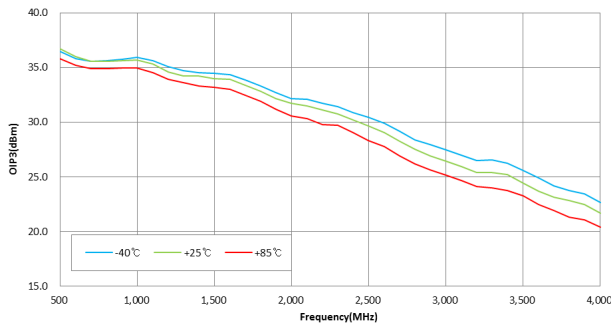


### Typical Performance Plot - BVA518 EVK - PCB(RF Circuit\*:500~4000MHz)

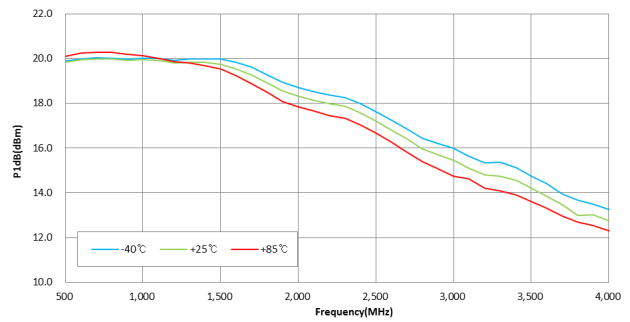
Typical Performance Data @ 25°C, Maximum gain state and VDD = 5.0V unless otherwise noted

**Figure 15. OIP3 vs Frequency**

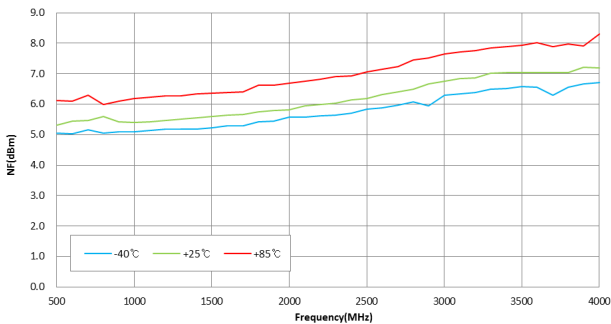
(2tones at an output of 7 dBm per tone separated by 1 MHz)



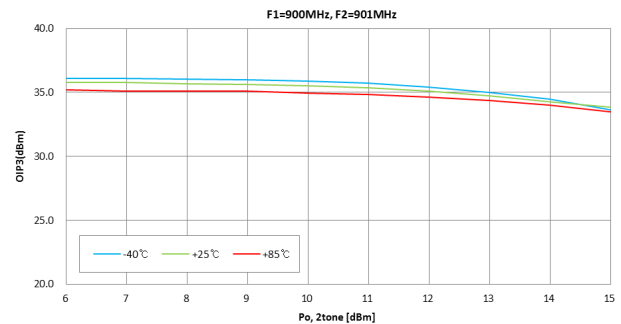
**Figure 16. P1dB vs Frequency**



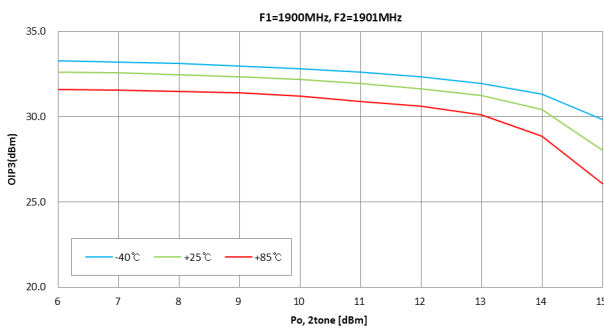
**Figure 17. Noise Figure vs Frequency**



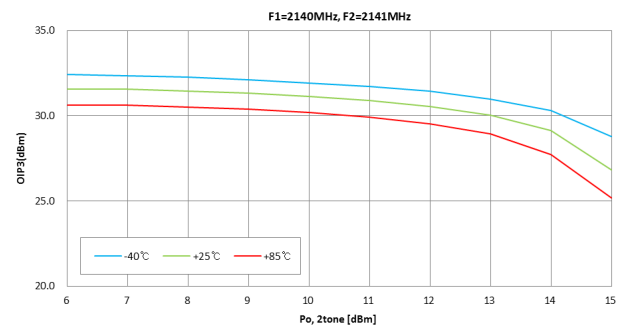
**Figure 18. OIP3 @900MHz vs Temperature**



**Figure 19. OIP3 @1900MHz vs Temperature**



**Figure 20. OIP3 @2140MHz vs Temperature**



\* RF Circuit application refer to Table 10.

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### Typical Performance Plot - BVA518 EVK - PCB(RF Circuit\*:500~4000MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 5.0V unless otherwise noted

Figure 21. Attenuation Error vs Frequency @ Major Attenuation Steps

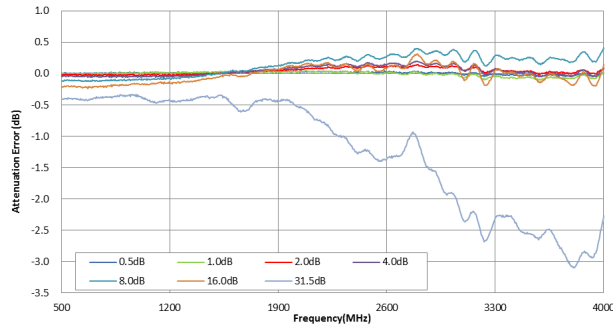


Figure 22. Attenuation Error vs Attenuation Setting

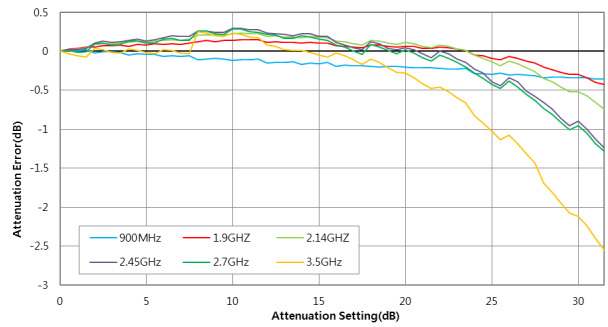


Figure 23. 0.5dB Step Attenuation vs Attenuation Setting

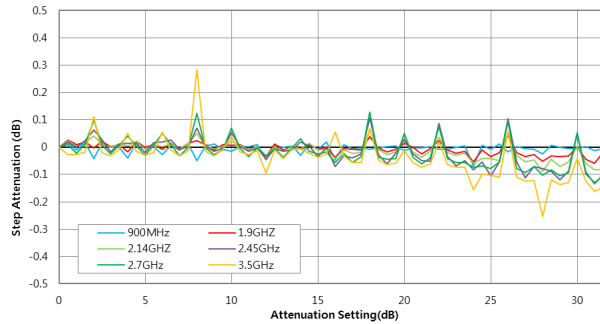


Figure 24. Attenuation Error @ 900MHz vs Temperature

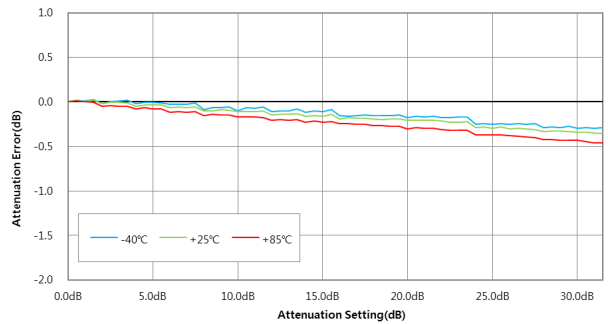


Figure 25. Attenuation Error @ 1.9GHz vs Temperature

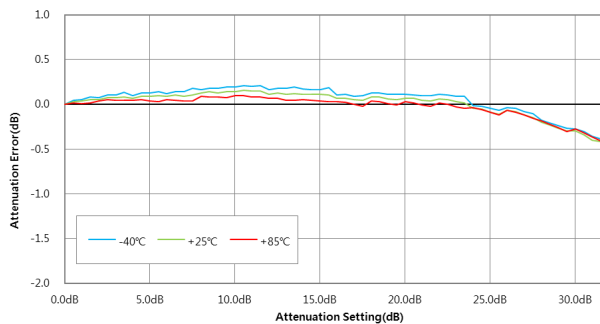
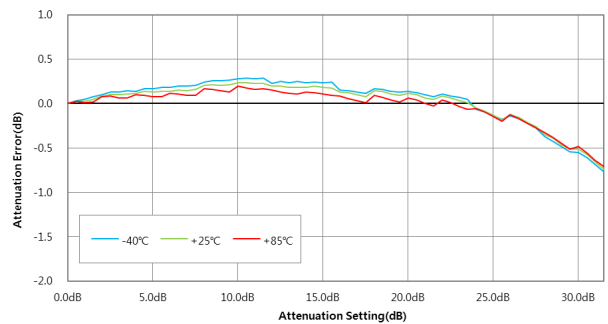


Figure 26. Attenuation Error @ 2.14GHz vs Temperature



\* RF Circuit application refer to Table 10.

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### Typical Performance Plot - BVA518 EVK - PCB(RF Circuit\*:500~4000MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 5.0V unless otherwise noted

Figure 27. Attenuation Error @ 2.7GHz vs Temperature

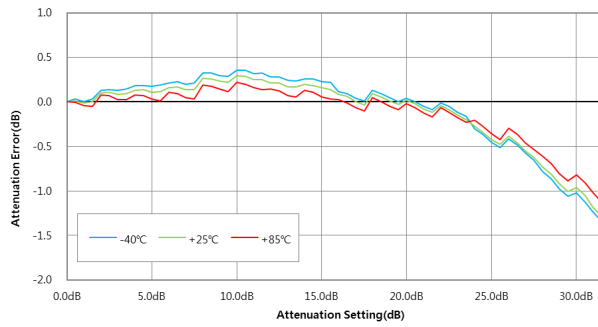
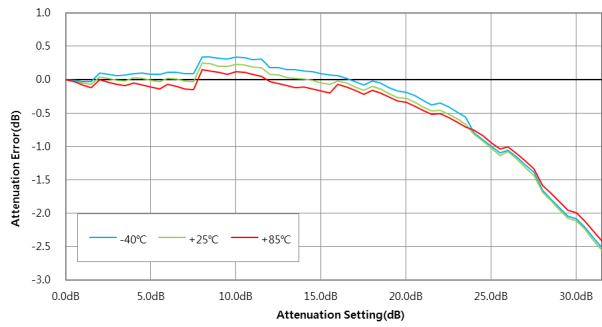


Figure 28. Attenuation Error @ 3.5GHz vs Temperature



\* RF Circuit application refer to Table 10.

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### Typical Performance Plot - BVA518 EVK - PCB(IF Circuit\*:5~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 5.0V unless otherwise noted

Figure 29. Gain vs Frequency

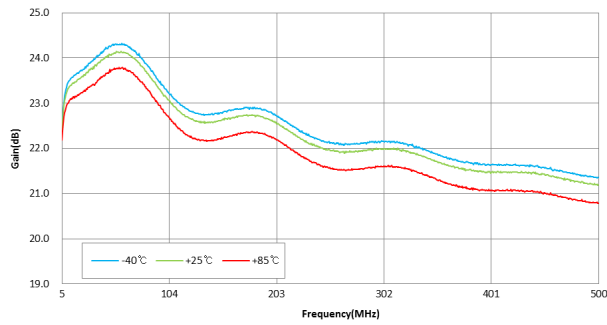


Figure 30. Gain vs Frequency @ Major Attenuation Steps

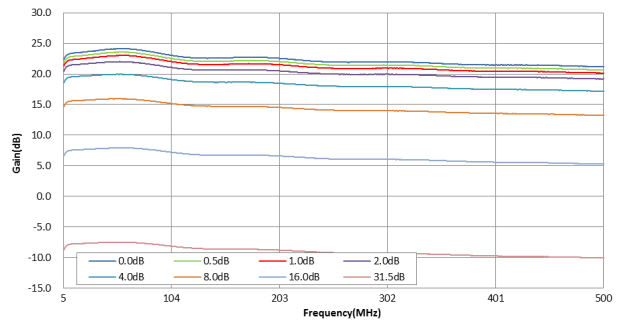


Figure 31. Input Return Loss vs Frequency

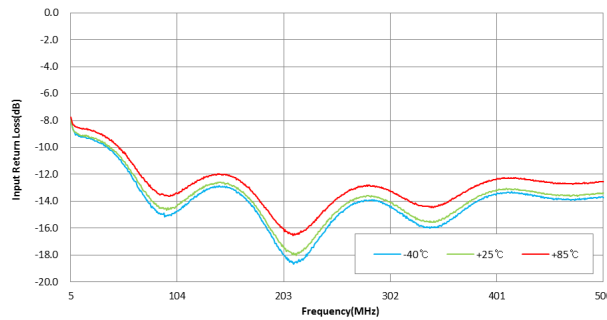
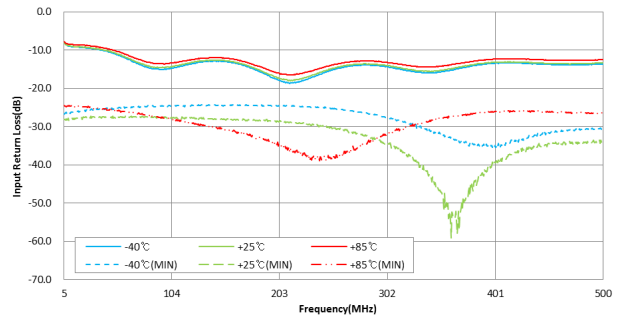


Figure 32. Input Return Loss vs Frequency @ Max Gain & Min Gain<sup>1</sup> State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

Figure 33. output Return Loss vs. Frequency

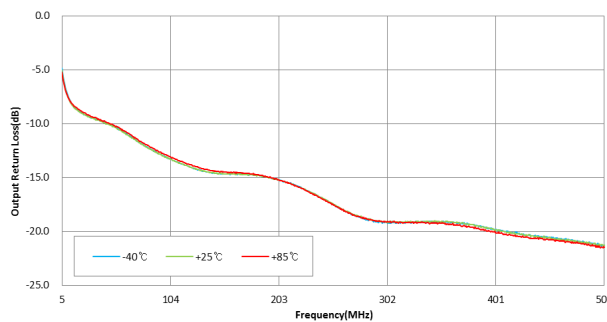
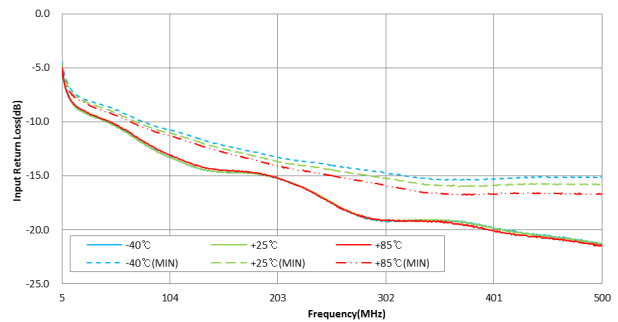


Figure 34. output Return Loss vs. Frequency @ Max Gain & Min Gain<sup>1</sup> State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

\* IF Circuit application refer to Table 10.

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### Typical Performance Plot - BVA518 EVK - PCB(IF Circuit\*:5~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 5.0V unless otherwise noted

Figure 35. OIP3 vs Frequency

(2tones at an output of 7 dBm per tone separated by 1 MHz)

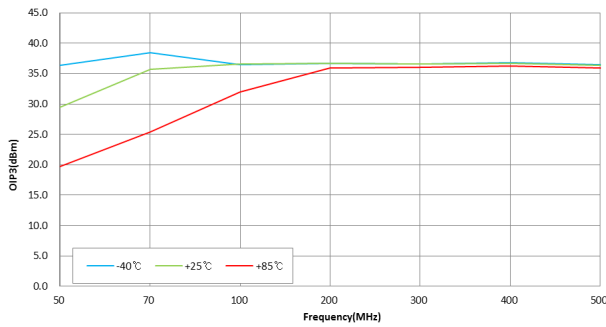


Figure 36. P1dB vs Frequency

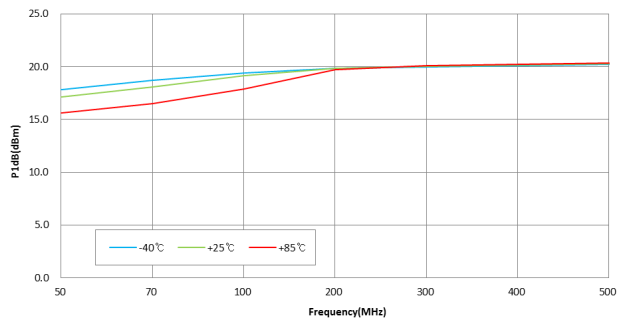


Figure 37. Noise Figure vs Frequency

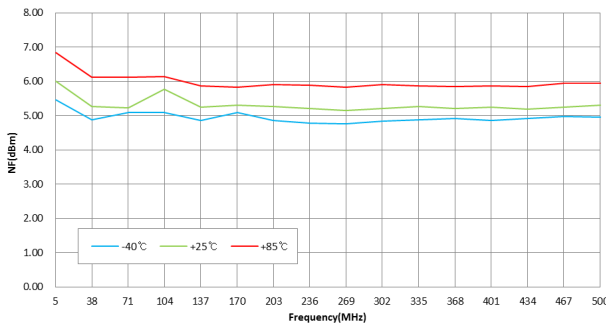


Figure 38. Attenuation Error vs Frequency @ Major Attenuation Steps

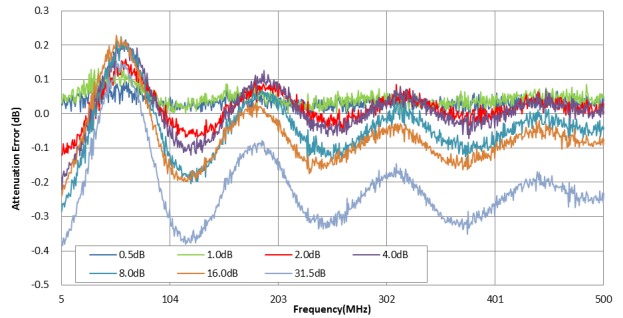


Figure 39. Attenuation Error vs Attenuation Setting

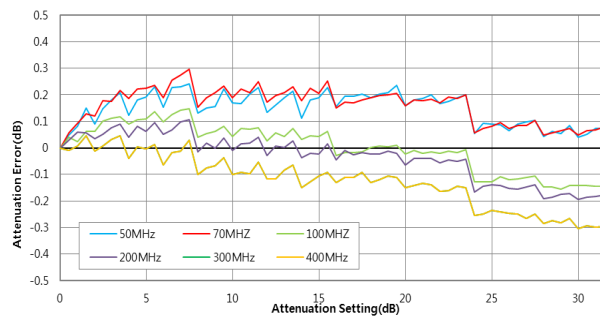
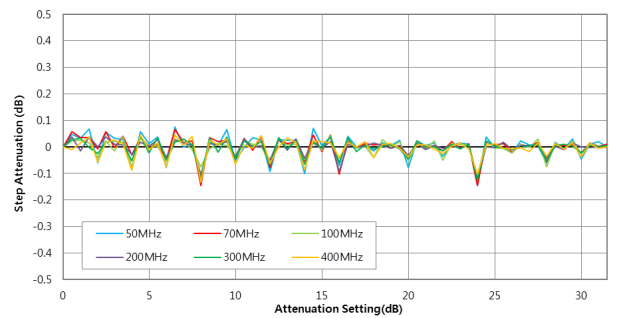


Figure 40. 0.5dB Step Attenuation vs Attenuation Setting



\* IF Circuit application refer to Table 10.

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### Typical Performance Plot - BVA518 EVK - PCB(IF Circuit\*:5~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 5.0V unless otherwise noted

Figure 41. Attenuation Error @ 30MHz vs Temperature

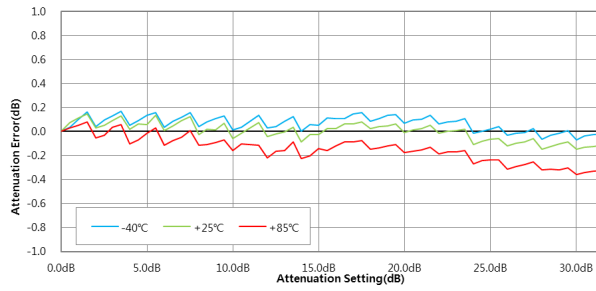


Figure 42. Attenuation Error @ 70MHz vs Temperature

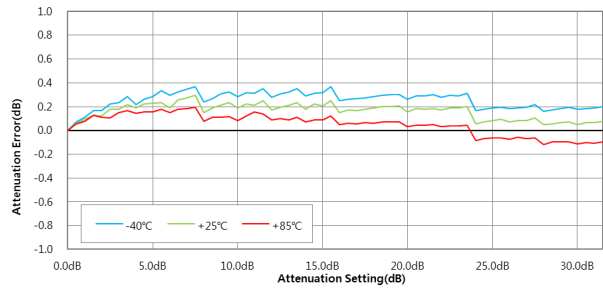


Figure 43. Attenuation Error @ 100MHz vs Temperature

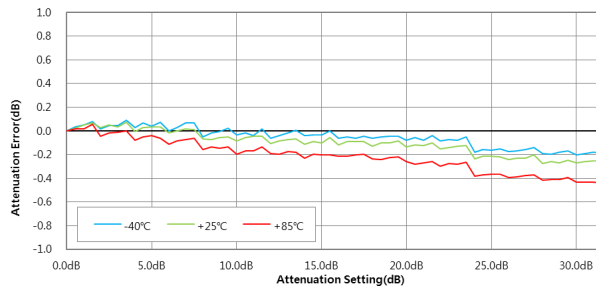


Figure 44. Attenuation Error @ 200MHz vs Temperature

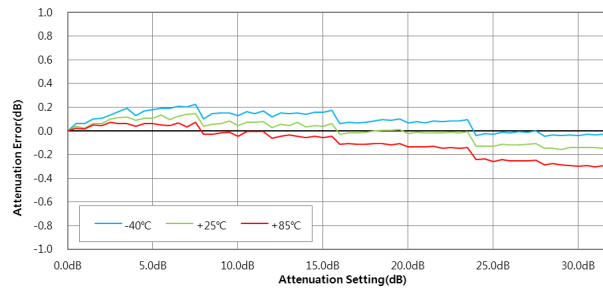


Figure 45. Attenuation Error @ 300MHz vs Temperature

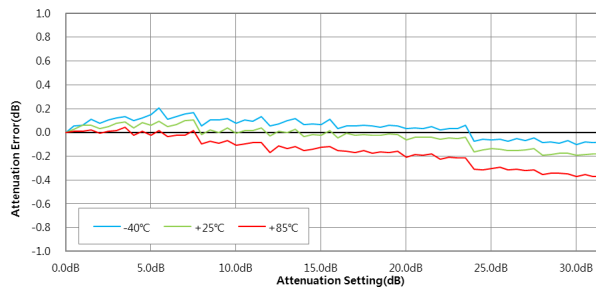
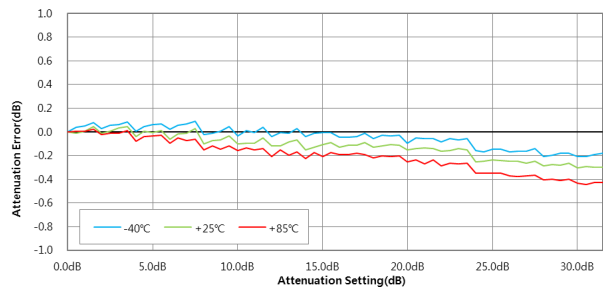


Figure 46. Attenuation Error @ 400MHz vs Temperature



\* IF Circuit application refer to Table 10.

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Figure 49. Evaluation Board Schematic

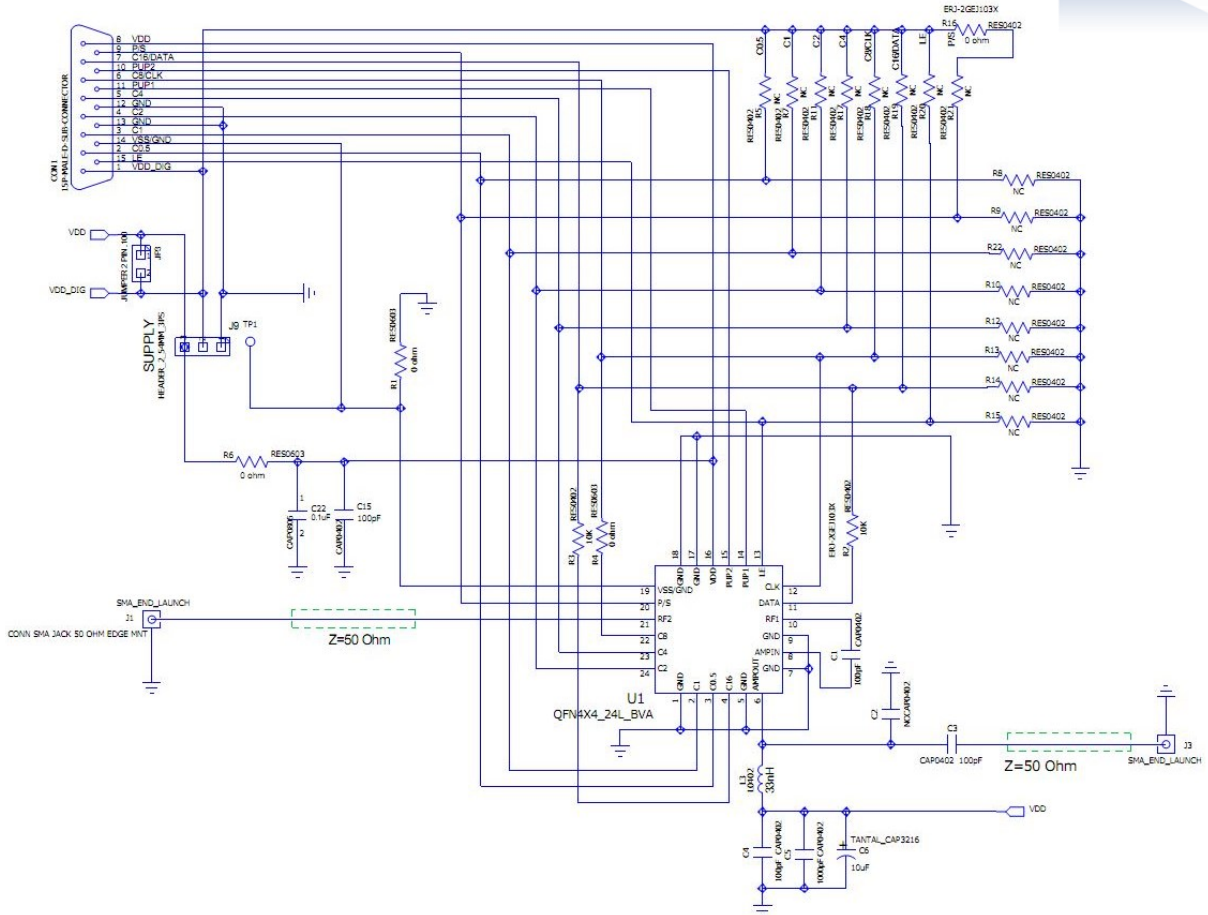


Table 10. Application Circuit

Application Circuit Values Example		
Freq.	IF Circuit 5~500MHz	RF Circuit 500MHz ~ 4GHz
C1/C3	10nF	100pF
L3(1005 Chip Ind)	2.7uH	33nH

Table 11. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Part Number	REMARK
1	C1,C3,C4,C15	4	CAP 0402 100pF J 50V	IF circuit refer to table 10
2	C5	1	CAP 0402 1000pF J 50V	
3	C2	1	CAP 0402 0.5pF C 50V	
4	C6	1	TANTAL 3216 10UF 16V	
5	C22	1	TANTAL 3216 0.1uF 35V	
7	L1	1	IND 1608 33nH	IF circuit refer to table 10
8	R2,R3	2	RES 1005 J 10K	
9	R1,R4,R6	3	RES 1608 J 0ohm	
20	CON1	1	15P-MALE-D-sub connector	
22	U1	1	QFN4X4_24L_BVA518	
23	J1,J3	2	SMA_END_LAUNCH	

Notice: Evaluation Board for Marketing Release was set to RF circuit application

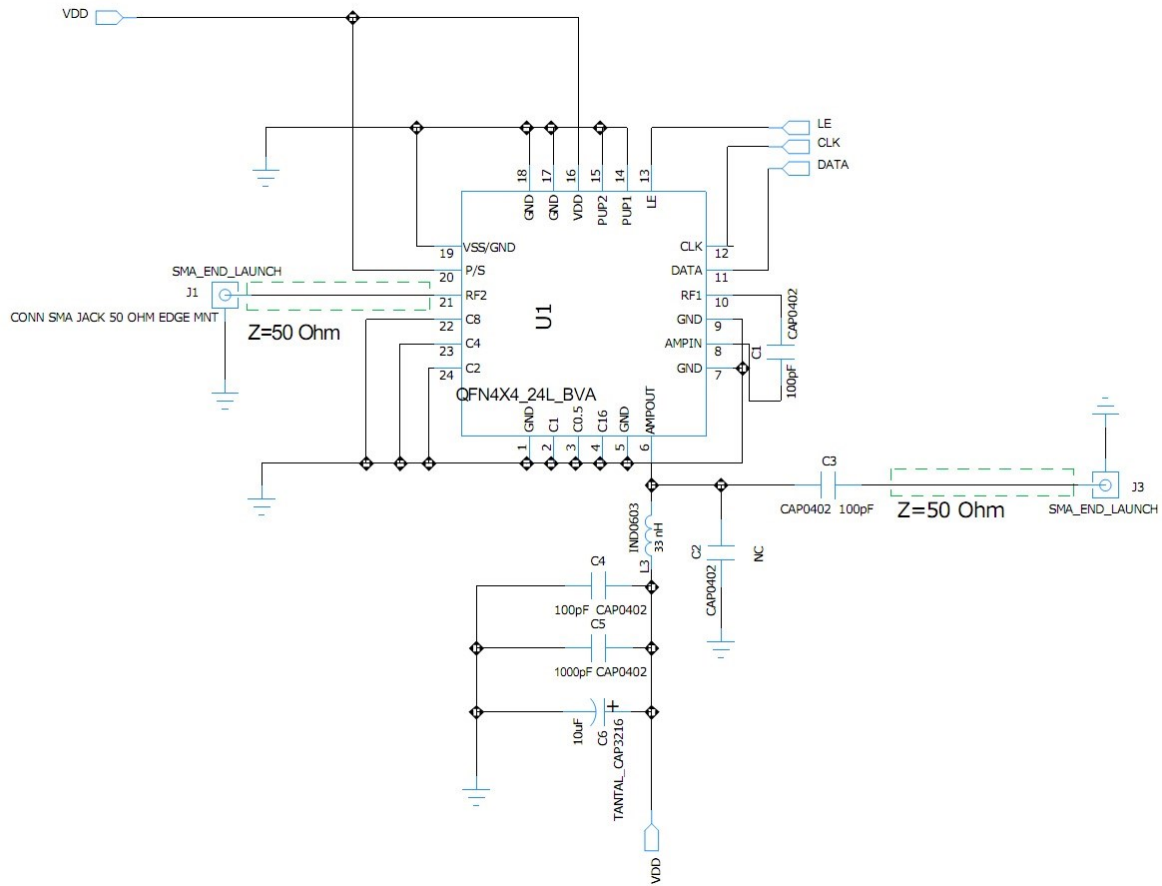
Preliminary Datasheet

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Figure 50. Application Circuit schematic  
(Use only Serial mode)



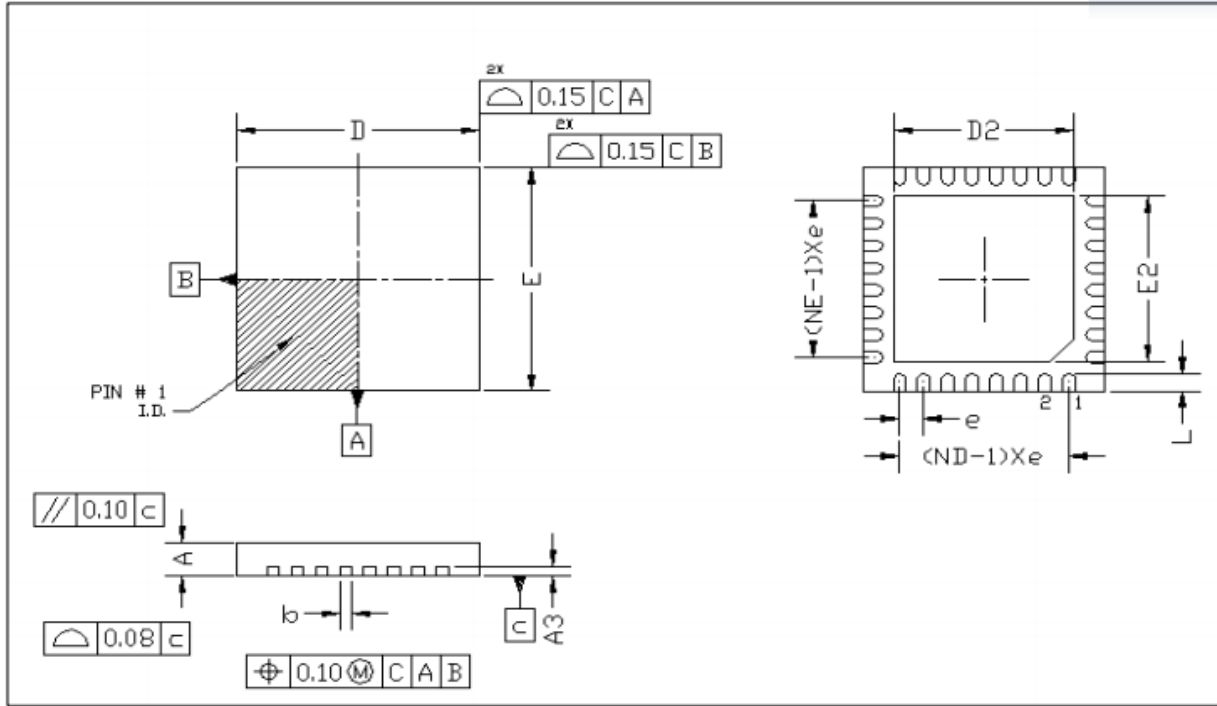
Notice: Evaluation Board for Marketing Release was set to RF circuit application

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Figure 51. Packing outline drawing



BODY		Lead/Pitch		Body		Lead		Thickness		PAD SIZE(MILS)		PAD SIZE(mm)		Remark
SIZE(D&E)	TYPE	COUNT	e	D2	E2	L	b	A	A3	X	Y	X	Y	
4X4	QFN	24	0.5	2.25	2.25	0.45	0.25	0.75/0.90	0.203Ref	98	98	2.49	2.49	

Figure 52. Package Marking



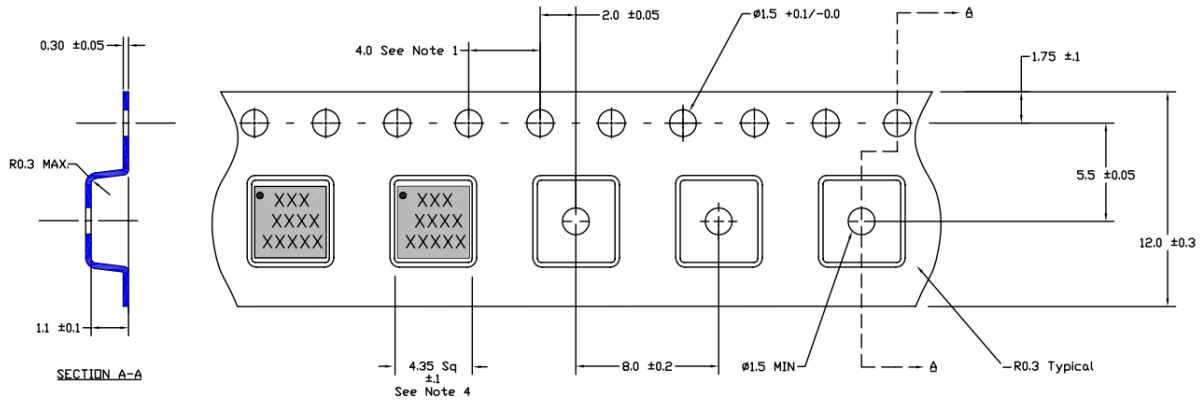
YY = Year, WW = Working Week, XX = Wafer No.

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Figure 53. Tape & Reel



Packaging information:

Tape Width (mm): 12 / Reel Size (inches): TBD

Device Cavity Pitch (mm): 8 / Devices Per Reel: TBD

## Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

## MSL / ESD Rating

ESD Rating:	Class 1C
Value:	Passes<2000V
Test:	Human Body Model(HBM)
Standard:	JEDEC Standard JESD22-A114B
MSL Rating:	Level 1 at +265°C convection reflow
Standard:	JEDEC Standard J-STD-020

## NATO CAGE code:

2	N	9	6	F
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