

BVA305

40-4000 MHz DIGITAL VARIABLE GAIN AMPLIFIER



Product Description

The BVA305 is a digitally controlled variable gain amplifier (DVGA) featuring high linearity using the voltage 3V supply with a broadband frequency range of 40 to 4000 MHz.

The BVA305 integrates a high performance digital step attenuator and a high linearity, broadband gain block, using the small package (4x4mm QFN package) and operating V_{DD} 3V voltage, and designed for use in 3G/4G wireless infrastructure and other high performance RF applications

Both stages are internally matched to 50 Ohms and it is easy to use with no external matching components required

A serial output port enables cascading with other serial controlled devices.

An integrated digital control interface supports both serial and parallel programming of the attenuation, including the capability to program an initial attenuation state at power-up. Covering a 31.5 dB attenuation range in 0.5 dB steps.

The BVA305 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application

Figure 1. Functional Block Diagram

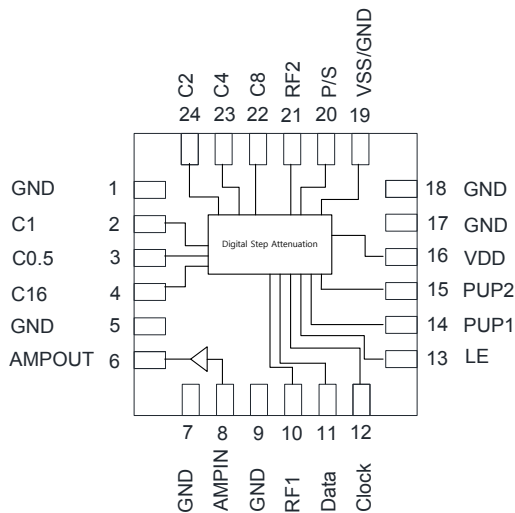
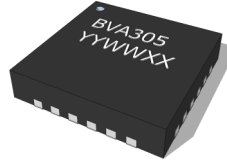


Figure 2. Package Type



24-lead 4x4 mm QFN

Device Features

- Small 24-Pin 4 x 4 mm QFN Package
- Integrate DSA to Amp Functionality
- Wide Power supply range of +2.7~5.5V(DSA)
- Single Fixed +3V supply(Amp)
- 40-4000MHZ Broadband Performance
- 13.8dB Gain at 2.14GHz
- 4dB Noise Figure at max gain setting
- 14.2dBm P1dB at 2.14GHz
- 27.6dBm OIP3 at 2.14GHz
- Single Fixed 3V supply
- No matching circuit needed
- Attenuation: 0.5 dB steps to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy(DSA to Amp)
 - ±(0.10 + 2% x Atten) @ 1 GHz
 - ±(0.15 + 2% x Atten) @ 2.2 GHz
 - ±(0.15 + 8% x Atten) @ 4 GHz
- 1.8V control logic compatible
- 105°C operating temperature
- Programming modes
 - Direct Parallel
 - Latched Parallel
 - Serial
- Unique power-up state selection

Application

- 3G/4G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

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Table 1. Electrical Specifications¹

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			40		4000	MHz
Gain		Attenuation = 0dB, at 1900MHz	13	14	15	dB
Attenuation Control range		0.5dB step		31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy	40MHz-1GHz	Any bit or bit combination			$\pm(0.10 + 2\%$ of atten setting)	dB
	>1GHz-2.2GHz				$\pm(0.15 + 2\%$ of atten setting)	
	>2.2GHz-4GHz				$\pm(0.15 + 8\%$ of atten setting)	
Return loss (input or output port)	1GHz-2.2GHz	Attenuation = 0dB	16	19		dB
	2.2GHz-4GHz		11	16		
Output Power for 1dB Compression		Attenuation = 0dB, at 1900MHz		14.8		dBm
Output Third Order Intercept Point		Attenuation = 0dB, at 1900MHz two tones at an output of 0 dBm per tone separated by 1 MHz.		28		dBm
Noise Figure		Attenuation = 0dB, at 1900MHz		4.1		dB
Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Supply voltage		DSA	2.7		5.5	V
		AMP		3		V
Supply Current			48	54	60	mA
Control Interface		Serial / parallel mode		6		Bit
Control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.6	V
Impedance				50		Ω

¹ Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+3V, measure on Evaluation Board (DSA to AMP)

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Table 2. Typical RF Performance¹

Parameter	Frequency					Unit
	70 ³	900	1900	2140	2650	
Gain	16.9	15.6	14.2	13.8	12.5	dB
S11	-15.3	-12.3	-15.6	-16.4	-17.3	dB
S22	-20.7	-15.5	-25.6	-18.7	-12.9	dB
OIP3 ²	32.3	31.3	28.0	27.6	25.5	dBm
P1dB	15.2	15.6	14.8	14.2	13.4	dBm
Noise Figure	3.4	3.6	4.1	4.2	5.1	dB

¹ Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+3V,50 Ω system. measure on Evaluation Board (DSA to AMP)

² OIP3 _ measured with two tones at an output of 0 dBm per tone separated by 1 MHz.

³ 70MHz measured with IF application circuit.(refer to table 10.)

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage(VCC)	Amp/DSA			3.6/5.5	V
Supply Current	Amp		110		mA
Digital input voltage		-0.3		3.6	V
Maximum input power	Amp/DSA			+12/+30	dBm
Operating Temperature	Amp/DSA	-40		85/105	°C
Storage Temperature		-55		150	°C
Junction Temperature			150		°C

Operation of this device above any of these parameters may result in permanent damage.



Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the BVA305. The P/S bit provides this selection, with P/S = LOW selecting the parallel interface and P/S = HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of six CMOS compatible control lines that select the desired attenuation state, as shown in *Table 4*.

The parallel interface timing requirements are defined by *Figure 4* (Parallel Interface Timing Diagram), *Table 7* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched* parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per *Figure 3*) to latch the new attenuation state into the device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for

Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by *Figure 3* (Serial Interface Timing Diagram) and *Table 6* (Serial Interface AC Characteristics).

Power-up Control Settings

The BVA305 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S = 1), the six control bits are set to whatever data is present on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S = 0) with LE = 0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in *Table 5* (Power-Up Truth Table, Parallel Mode).

Table 4. Truth Table

P/S	C16	C8	C4	C2	C1	C0.5	Attenuation state
0	0	0	0	0	0	0	Reference Loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: Not all 64 possible combinations of C0.5-C16 are shown in table

Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data,

Table 5. Parallel PUP Truth Table

P/S	LE	PUP2	PUP1	Attenuation state
0	0	0	0	Reference Loss
0	0	1	0	8 dB
0	0	0	1	16 dB
0	0	1	1	31.5 dB
0	1	X	X	Defined by C0.5-C16

Note: Power up with LE = 1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active

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Typical Performance Plot - BVA305 EVK - PCB(RF Circuit*:500~4000MHz)

Typical Performance Data @ 25°C and VDD = 3.0V unless otherwise noted and RF Circuit

Figure 5. Gain vs Frequency

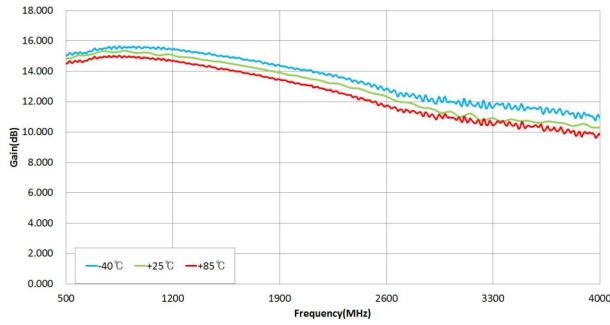


Figure 6. Gain vs Frequency @ Major Attenuation Steps

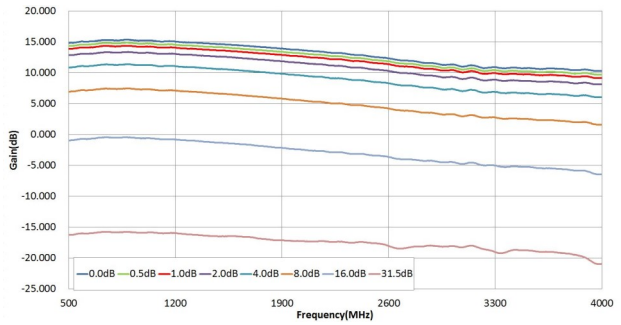


Figure 7. Input Return Loss vs Frequency

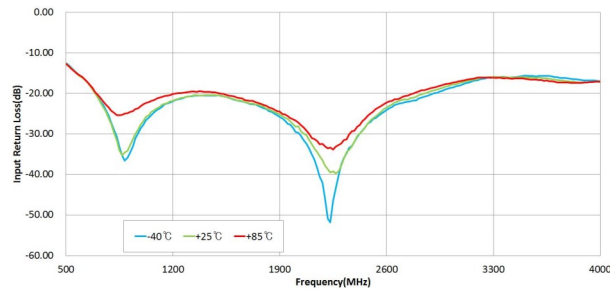
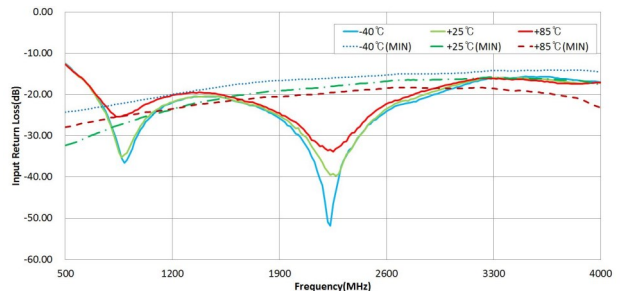


Figure 8. Input Return Loss vs Frequency @ Max Gain & Min¹ Gain State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

Figure 9. output Return Loss vs. Frequency

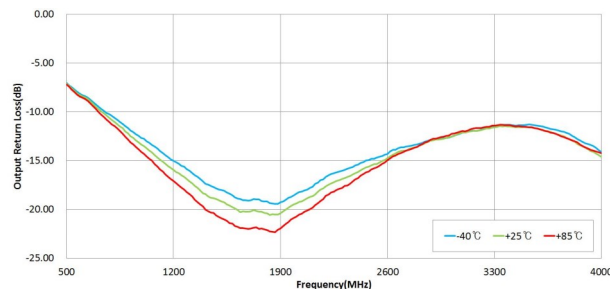
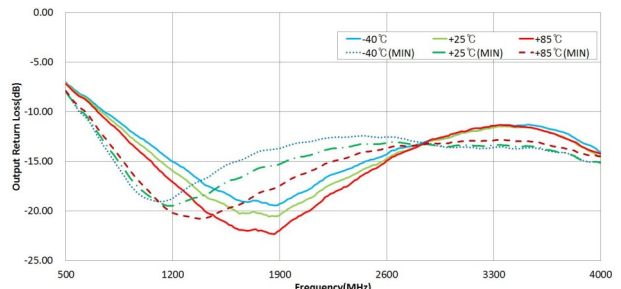


Figure 10. output Return Loss vs. Frequency @ Max Gain & Min Gain¹ State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

* RF Circuit application refer to Table 10.

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Typical Performance Plot - BVA305 EVK - PCB(RF Circuit*:500~4000MHz)

Typical Performance Data @ 25°C and VDD = 3.0V unless otherwise noted and RF Circuit

Figure 11. OIP3 vs Frequency

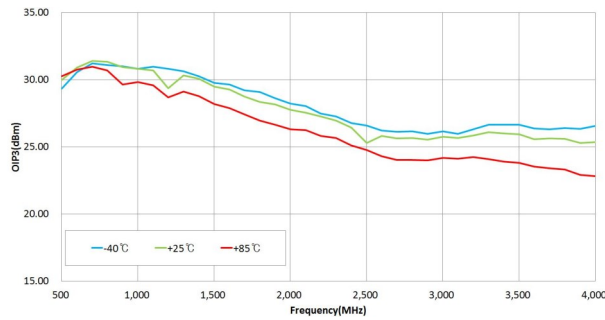


Figure 12. P1dB vs Frequency

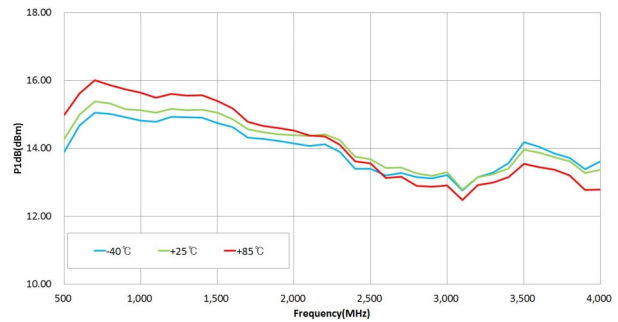


Figure 13. Noise Figure vs Frequency

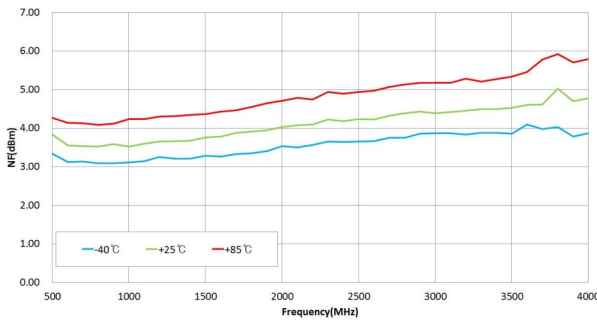


Figure 14. Attenuation Error vs Frequency @ Major Attenuation Steps

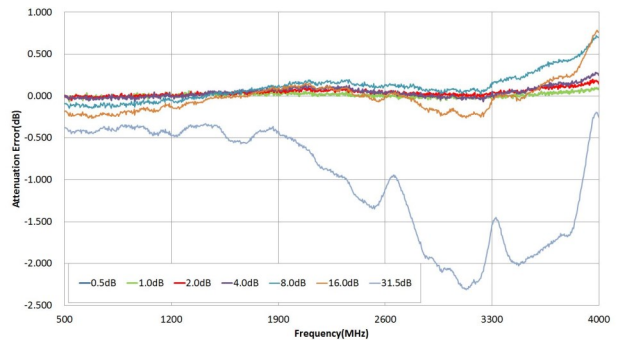


Figure 15. Attenuation Error vs Attenuation Setting

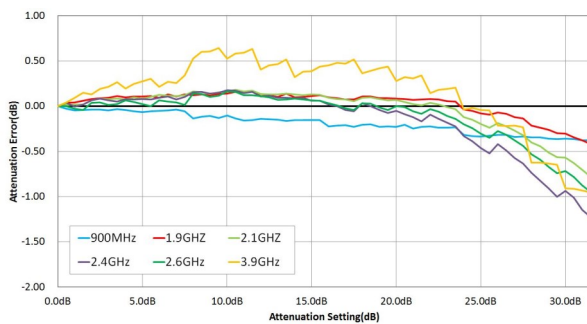
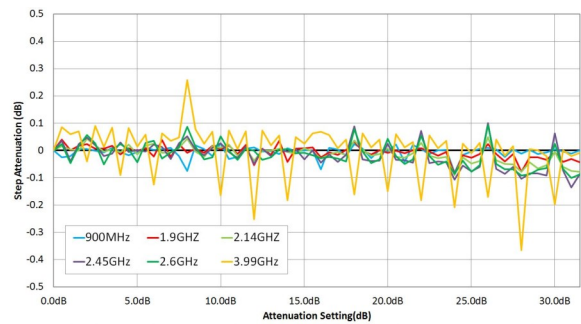


Figure 16. 0.5dB Step Attenuation vs Attenuation Setting



* RF Circuit application refer to Table 10.

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Typical Performance Plot - BVA305 EVK - PCB(RF Circuit*:500~4000MHz)

Typical Performance Data @ 25°and VDD = 3.0V unless otherwise noted and RF Circuit

Figure 17. Attenuation Error @ 900MHz vs Temperature

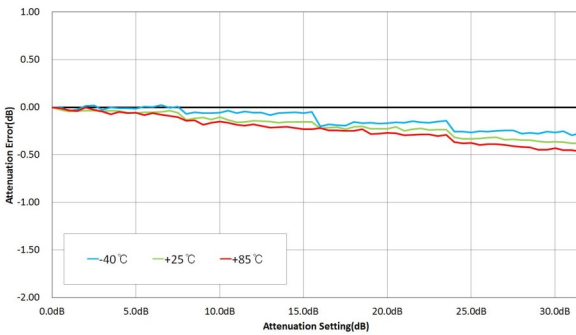


Figure 18. Attenuation Error @ 1.9GHz vs Temperature

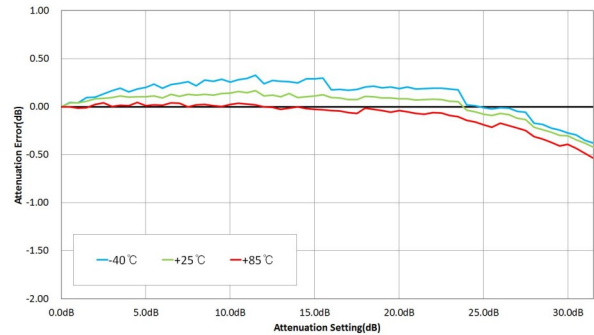


Figure 19. Attenuation Error @ 2.1GHz vs Temperature

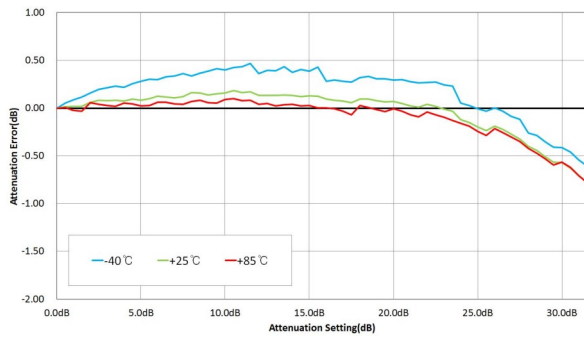


Figure 20. Attenuation Error @ 2.6GHz vs Temperature

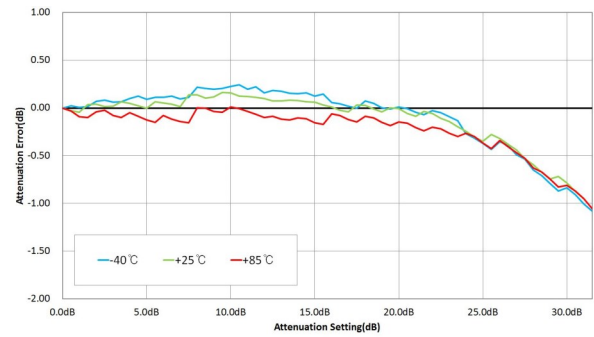
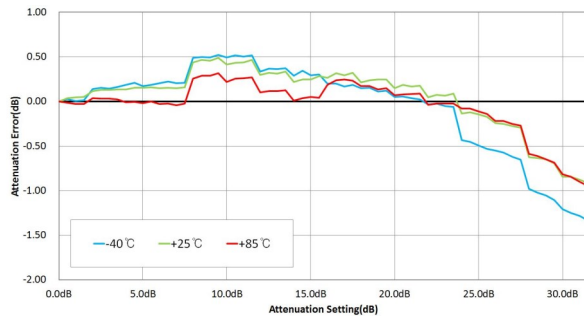


Figure 21. Attenuation Error @ 3.9GHz vs Temperature



* RF Circuit application refer to Table 10.

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Typical Performance Plot - BVA305 EVK - PCB(IF Circuit*:50~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted

Figure 22. Gain vs Frequency

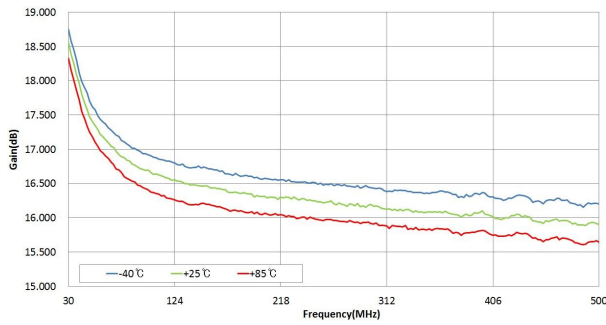


Figure 23. Gain vs Frequency @ Major Attenuation Steps

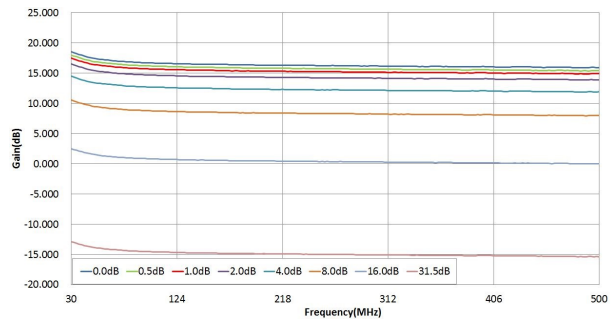


Figure 24. Input Return Loss vs Frequency

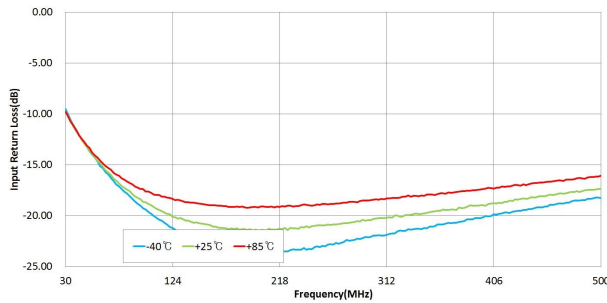
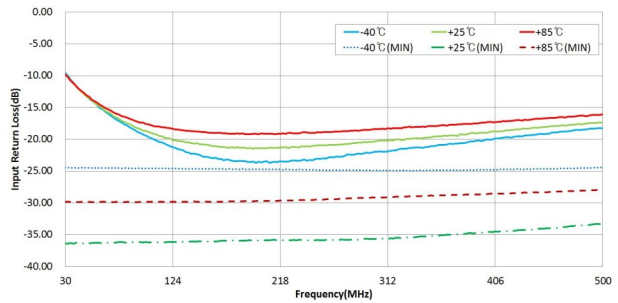


Figure 25. Input Return Loss vs Frequency @ Max Gain & Min Gain¹ State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

Figure 26. output Return Loss vs. Frequency

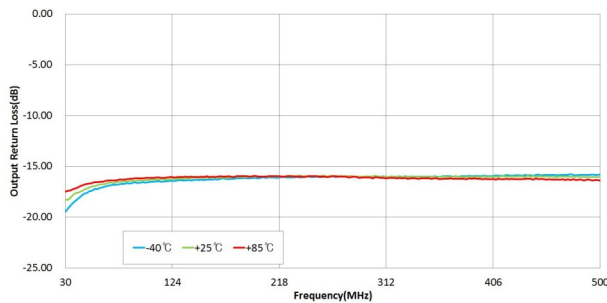
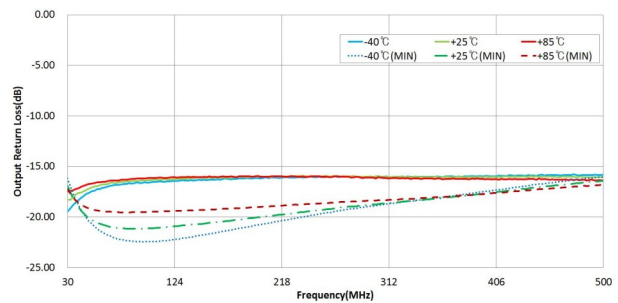


Figure 27. output Return Loss vs. Frequency @ Max Gain & Min Gain¹ State



Note: 1. Min Gain was measured in the state is set with attenuation 31.5dB

* RF Circuit application refer to Table 10.

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Typical Performance Plot - BVA305 EVK - PCB(IF Circuit*:50~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted

Figure 28. OIP3 vs Frequency

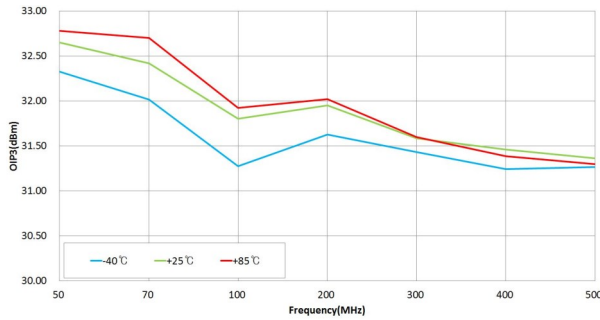


Figure 29. P1dB vs Frequency

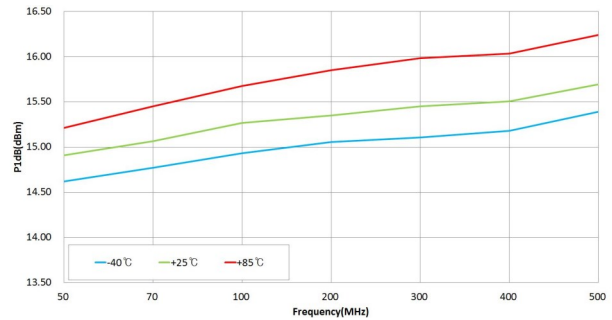


Figure 30. Noise Figure vs Frequency

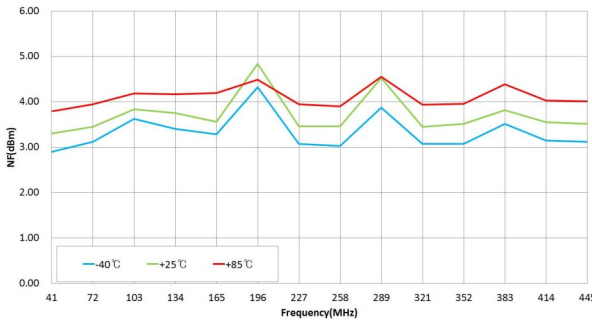


Figure 31. Attenuation Error vs Frequency @ Major Attenuation Steps

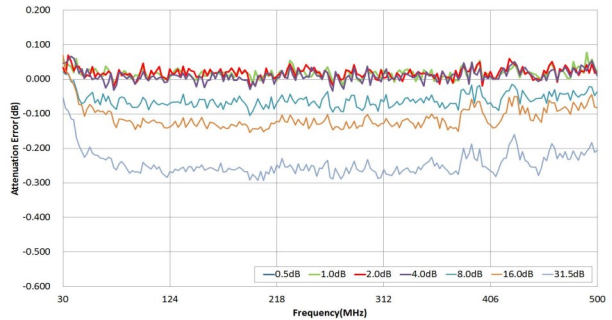


Figure 32. Attenuation Error vs Attenuation Setting

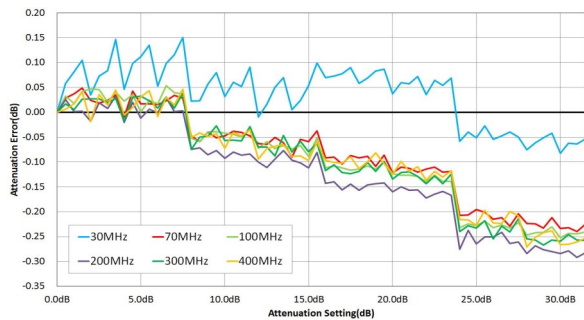
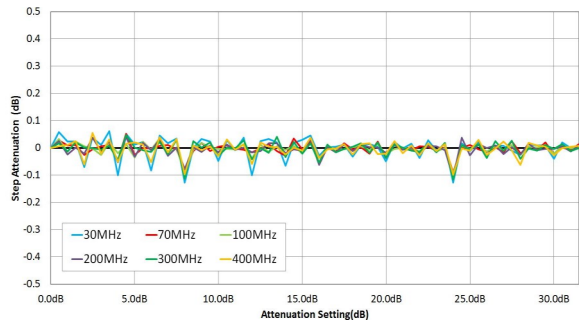


Figure 33. 0.5dB Step Attenuation vs Attenuation Setting



* IF Circuit application refer to Table 10.

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Typical Performance Plot - BVA305 EVK - PCB(IF Circuit*:50~500MHz)

Typical Performance Data @ 25°C, Maximum gain state and VDD = 3.0V unless otherwise noted

Figure 34. Attenuation Error @ 40MHz vs Temperature

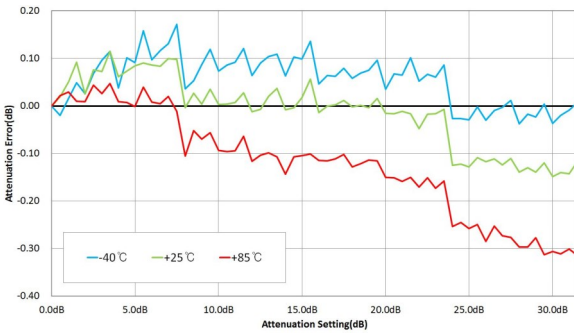


Figure 35. Attenuation Error @ 70MHz vs Temperature

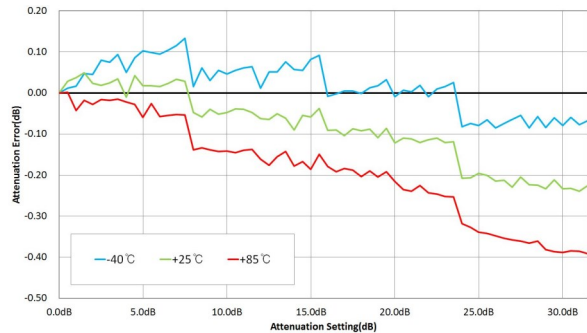


Figure 36. Attenuation Error @ 100MHz vs Temperature

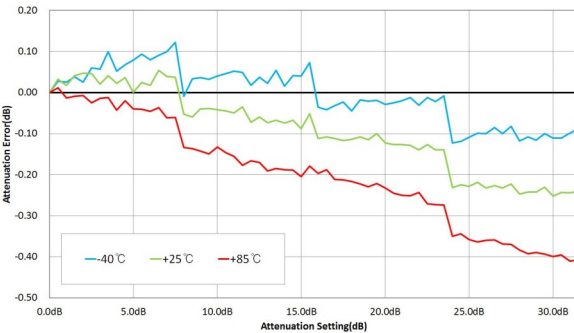


Figure 37. Attenuation Error @ 200MHz vs Temperature

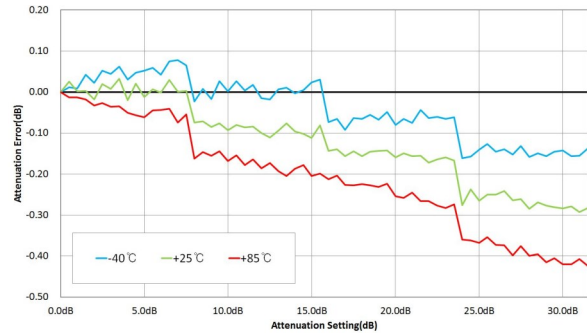


Figure 38. Attenuation Error @ 300MHz vs Temperature

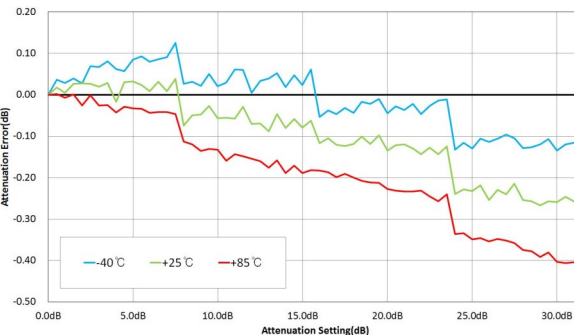
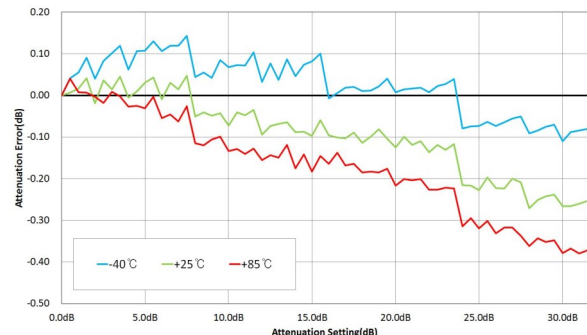


Figure 39. Attenuation Error @ 400MHz vs Temperature



* IF Circuit application refer to Table 10.

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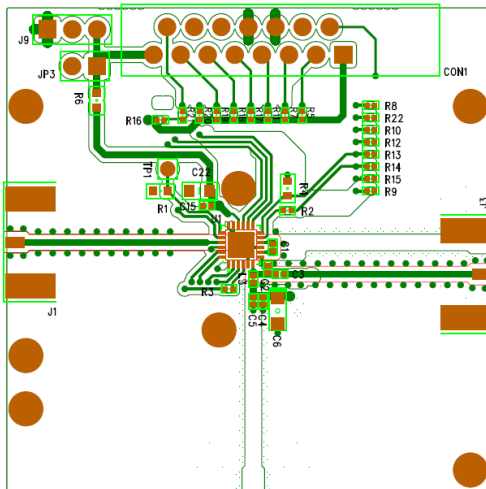


Evaluation Board PCB Information

Figure 40. Evaluation Board PCB Layer Information

	COPPER :1oz + 0.5oz (plating), Top Layer	↑
EM825B ER: 4.6~4.8	P.P : (0.2+0.06+0.06) TOTAL = 0.32mm	
	COPPER :1oz (GND), Inner Layer	↓
MTC Er:4.6	CORE : 0.73mm FINISH TICKNESS :1.55T	
	COPPER :1oz, Inner Layer	↓
EM825B Er:4.6~4.8	P.P : (0.2+0.06+0.06) TOTAL = 0.32mm	
	COPPER :1oz + 0.5oz (plating), Bottom Layer	

Figure 41. Evaluation Board PCB



* IF Circuit application refer to Table 10.

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Figure 42. Evaluation Board Schematic

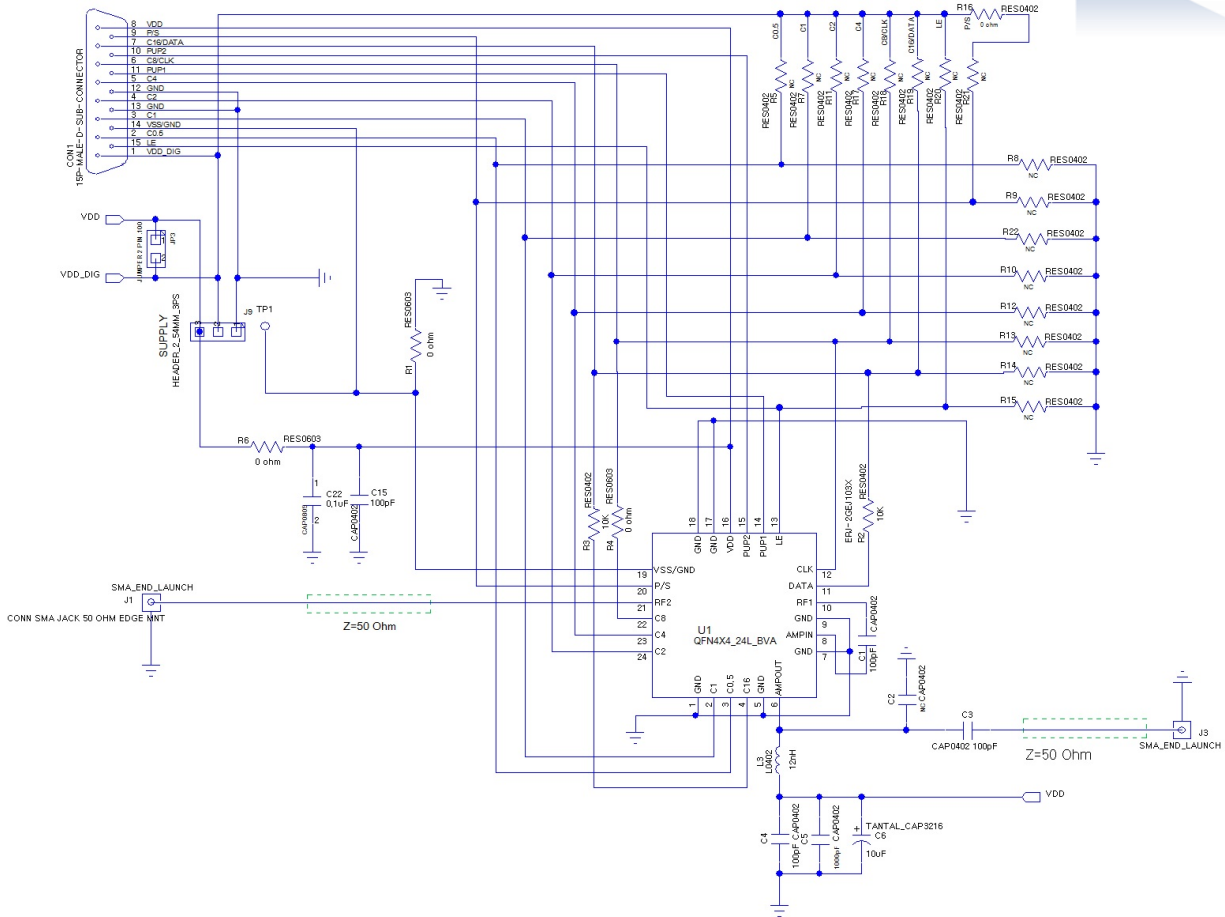


Table 10. Application Circuit

Application Circuit Values Example		
Freq.	IF Circuit 50~500MHz	RF Circuit 500MHz ~ 4GHz
C1/C3	2nF	100pF
L3(1005 Chip Ind)	820nH	12H

Table 11. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Part Number	REMARK
1	C1,C3,C4,C15	4	CAP 0402 100pF J 50V	IF circuit refer to table 10
2	C5	1	CAP 0402 1000pF J 50V	
3	C2	1	CAP 0402 0.5pF C 50V	
4	C6	1	TANTAL 3216 10UF 16V	
5	C22	1	TANTAL 3216 0.1uF 35V	
7	L1	1	IND 1608 56nH	IF circuit refer to table 10
8	R2,R3	2	RES 1005 J 10K	
9	R1,R4,R6	3	RES 1608 J 0ohm	
20	CON1	1	15P-MALE-D-sub connector	
22	U1	1	QFN4X4_24L_BVA303	
23	J1,J3	2	SMA_END_LAUNCH	

Notice: Evaluation Board for Marketing Release was set to RF circuit application

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