A Microchip Technology Company

FlashFlex MCU

SST89E54C / SST89E58C / SST89E516C

Advance Information

The SST89E54C, SST89E58C, and SST89E516C are members of the FlashFlex family of 8-bit micro controller products designed and manufactured with SST patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for customers. The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 micro-controller devices.

Features

- **8-bit 8051-Compatible Microcontroller (MCU) with Embedded SuperFlash Memory**
  - Fully Software Compatible
  - Development Toolset Compatible
  - Pin-for-Pin Package Compatible
- **SST89E5xC Operation**
  - 0 to 40 MHz at 5V
- **Total 512 Byte = 54C / 1KByte = 58C / 2KByte = 516C Internal RAM (256 Byte by default + 256/768/1792 Byte enabled by software)**
- **Single Block SuperFlash EEPROM**
  - SST89E/V54C: 16 KByte primary partition + 2 KByte secondary partition
  - SST89E/V58C: 32 KByte primary partition + 2 KByte secondary partition
  - SST89E/V516C: 64 KByte primary partition + 2 KByte secondary partition
  - Primary Partition is divided into Four Pages
  - Secondary Partition has One Page
  - In-System Programming (ISP)
  - In-Application Programming (IAP)
  - Small-Sector Architecture: 128-Byte Sector Size
- **Support External Address Range up to 64 KByte of Program and Data Memory**
- **Three 16-bit Timers/Counters**
- **I^2C Interface (1st and 2nd)**
- **Full-Duplex, Enhanced UART**
  - Framing error detection
  - Automatic address recognition
- **Eight Interrupt Sources at 4 Priority Levels**
- **Programmable Watchdog Timer (WDT)**
- **Programmable Counter Array (PCA)**
- **Four 8-bit I/O Ports (32 I/O pins) and one 4-bit port**
- **Second DPTR register**
- **Low EMI Mode (Inhibit ALE)**
- **SPI Serial Interface**
- **Standard 6 Clocks per cycle, the device has an option to halve the speed to 12 clocks per cycle**
- **TTL- and CMOS-Compatible Logic Levels**
- **Low Power Modes**
  - Power-down Mode with External Interrupt Wake-up
  - Idle Mode
- **Temperature Ranges:**
  - Commercial (0°C to +70°C)
    Industrial (-40°C to +85°C)
- **Packages Available**
  - 44-lead PLCC
  - 44-lead TQFP
- **All non-Pb (lead-free) devices are RoHS compliant**

Product Description

The SST89E54C, SST89E58C, and SST89E516C are members of the FlashFlex family of 8-bit micro controller products designed and manufactured with SST patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for customers. The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 micro-controller devices.

The SST89E54C/SST89E58C/SST89E516C comes with 18/34/66 KByte of on-chip flash EEPROM program memory which is divided into 2 independent program memory partitions. The primary partition occupies 16/8/4 KByte of internal program memory space and the secondary partition occupies 2 KByte of internal program memory space.

The flash memory can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and firmware for SST devices. During power-on reset, the devices can be configured as either a slave to an external host for source code storage or a master to an external host for an in-system programming (ISP) operation. The devices are designed to be programmed in-system on the printed circuit board for maximum flexibility. The device is pre-programmed with an example of the bootstrap loader (BSL) in memory, demonstrating initial user program code loading or subsequent user code updating via an ISP operation. The sample BSL is for the user's reference only; SST does not guarantee the sample BSL functionality. Chip-Erase operations will erase the pre-programmed sample code.

In addition to 18/34/66 KByte of SuperFlash EEPROM on-chip program memory and 512/1K/2K x8 bits of on-chip RAM, the devices can address up to 66 KByte and of external program memory and up to 64 KByte of external RAM.

SuperFlash, a highly-reliable patented SST technology, and memory cell architecture offer important advantages for designing and manufacturing flash EEPROMs. These advantages translate into significant cost and reliability benefits for customers.

Functional Blocks

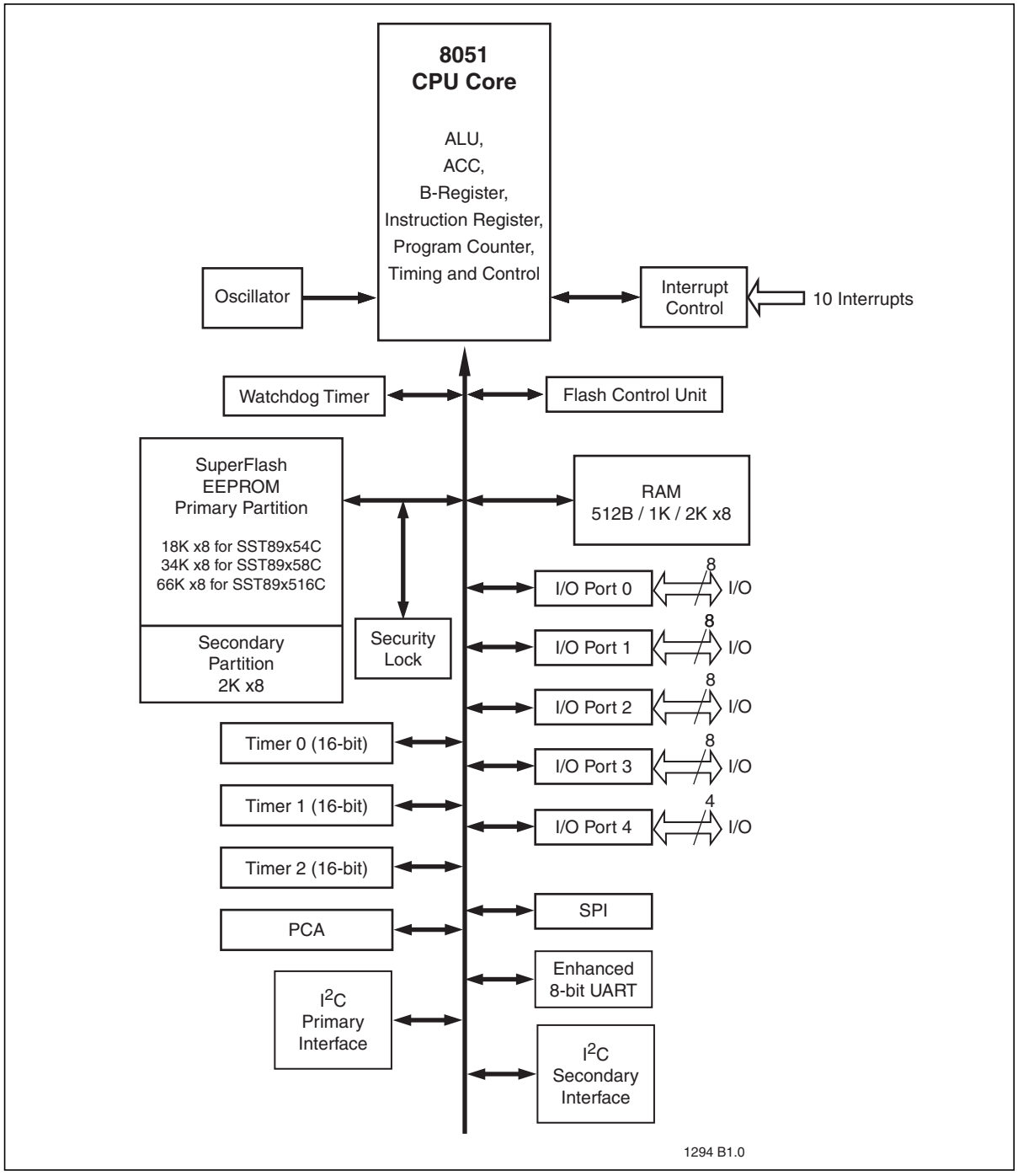

Figure 1: Functional Block Diagram

Pin Assignments

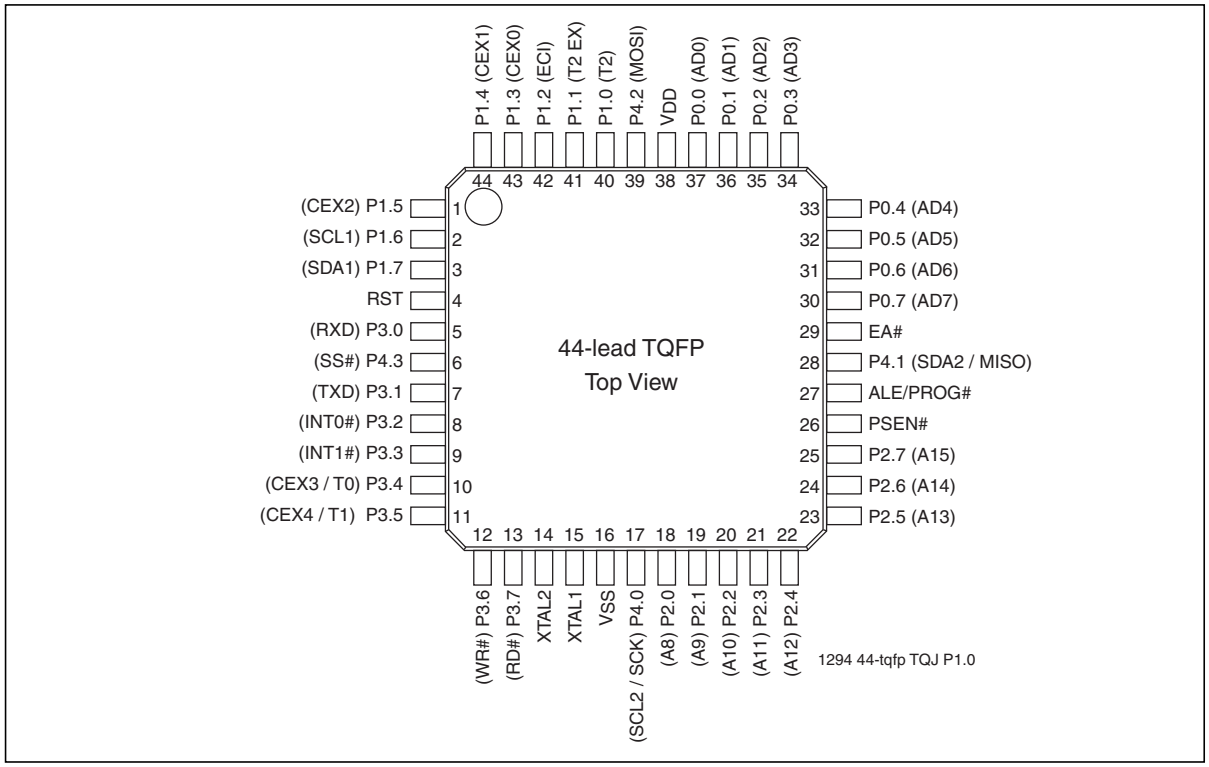

Figure 2: Pin Assignments for 44-lead TQFP

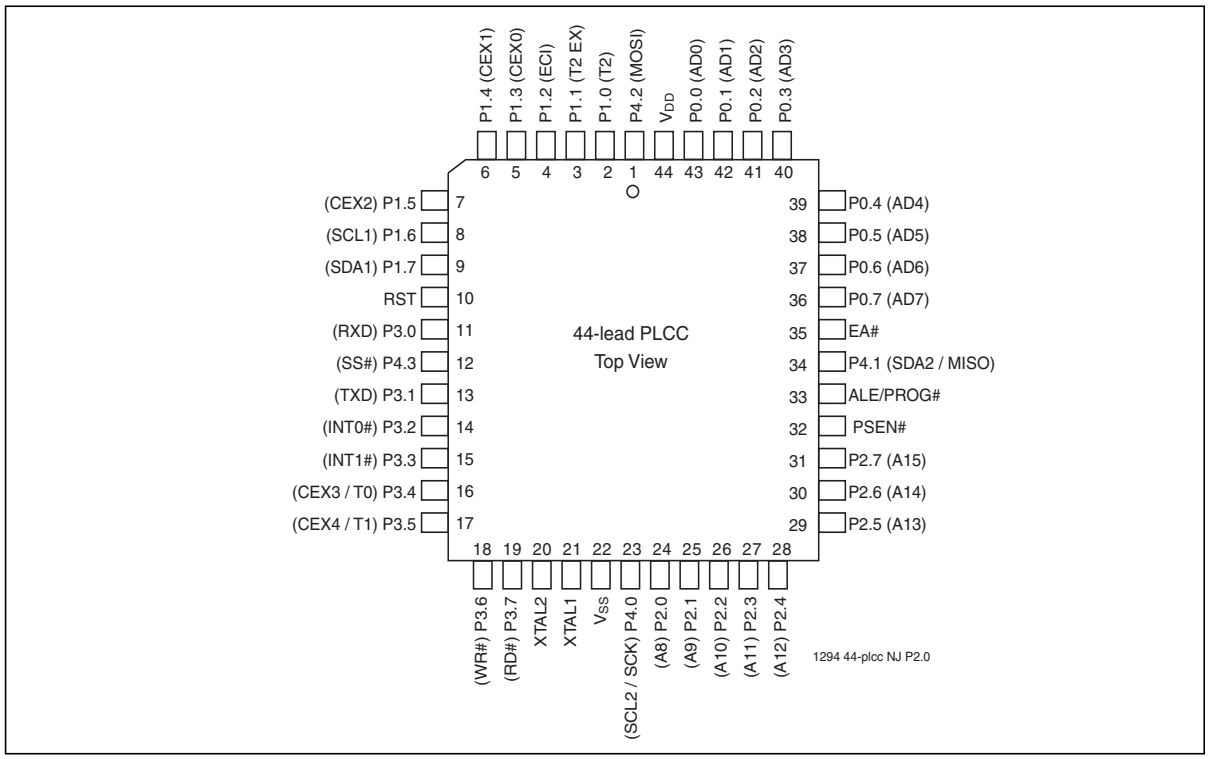

Figure 3: Pin Assignments for 44-lead PLCC

Pin Descriptions

Table 1: Pin Descriptions (1 of 3)

Symbol	Type[1]	Name and Functions
P0[7:0]	I/O	**Port 0:** Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. Port 0 also receives the code bytes during the external host mode programming, and outputs the code bytes during the external host mode verification. External pull-ups are required during program verification or as a general purpose I/O port.
P1[7:0]	I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, see Table 32) because of the internal pull-ups. P1[5, 6, 7] have high current drive of 16 mA. Port 1 also receives the low-order address byte during the external host mode programming and verification.
P1[0]	I/O	**T2:** External count input to Timer/Counter 2 or Clock-out from Timer/Counter 2
P1[1]	I	**T2EX:** Timer/Counter 2 capture/reload trigger and direction control
P1[2]	I	**ECI:** External Clock Input This signal is the external clock input for the PCA.

Table 1: Pin Descriptions (Continued) (2 of 3)

Symbol	Type[1]	Name and Functions
P1[3]	I/O	**CEX0:** Capture/Compare External I/O for PCA Module 0 Each capture/compare module connects to a Port 1 pin for external I/O. When not used by the PCA, this pin can handle standard I/O.
P1[4]	I/O	**CEX1:** Capture/Compare External I/O for PCA Module 1
P1[5]	I/O	**CEX2:** Capture/Compare External I/O for PCA Module 2
P1[6]	I/O	**SCL1:** Clock for I^2C - Primary
P1[7]	I/O	**SDA1** Data line for I^2C - Primary
P2[7:0]	I/O with internal pull-up	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, see Table 32) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to '1's. Port 2 also receives the high-order address byte during the external host mode programming and verification.
P3[7:0]	I/O with internal pull-up	**Port 3:** Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, see Table 32) because of the internal pull-ups. Port 3 also receives the high-order address byte during the external host mode programming and verification.
P3[0]	I	**RXD:** Universal Asynchronous Receiver/Transmitter (UART) - Receive input
P3[1]	O	**TXD:** UART - Transmit output
P3[2]	I	**INT0#:** External Interrupt 0 Input
P3[3]	I	**INT1#:** External Interrupt 1 Input
P3[4]	I	**T0:** External count input to Timer/Counter 0 **OR** **CEX3:** Capture/Compare External I/O for PCA module 3
P3[5]	I	**T1:** External count input to Timer/Counter 1 **OR** **CEX4:** Capture/Compare External I/O for PCA module 3
P3[6]	O	**WR#:** External Data Memory Write strobe
P3[7]	O	**RD#:** External Data Memory Read strobe
P4[3:0][2]	I/O with internal pull-ups	**Port 4:** Port 4 is a 4-bit bi-directional I/O port with internal pull-ups. The port 4 output buffers can drive LS TTL inputs. Port 4 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, port 4 pins that are externally pulled low will source current because of internal pull-ups. P4 is not bit-addressable.
P4[0]	I/O	**Port 4.0 SCK:** Master Clock output, slave clock input line for SPI. Bit 0 of port 4 **OR** **SCL2:** Clock for I^2C - secondary
P4[1]	I/O	**Port 4.1 M1SO:** Master input line, slave output line for SPI. Bit 1 of port 4 **OR** **SDA2:** Data line for I^2C - secondary
P4[2]	I/O	**Port 4.2 M0SI:** Master output line, slave input line for SPI. Bit 2 of port 4
P4[3]	I/O	**Port 4.3 SS#:** Slave port select input line for SPI. Bit 3 of port 4

Table 1: Pin Descriptions (Continued) (3 of 3)

Symbol	Type[1]	Name and Functions
PSEN#	I/O	**Program Store Enable:** PSEN# is the Read strobe to external program. When the device is executing from internal program memory, PSEN# is inactive (High). When the device is executing code from external program memory, PSEN# is activated twice each machine cycle, except that two PSEN# activations are skipped during each access to external data memory. A forced high-to-low input transition on the PSEN# pin while the RST input is continually held high for more than 10 machine cycles will cause the device to enter external host mode programming.
RST	I	**Reset:** While the oscillator is running, a "high" logic state on this pin for two machine cycles will reset the device. If the PSEN# pin is driven by a high-to-low input transition while the RST input pin is held "high," the device will enter the external host mode, otherwise the device will enter the normal operation mode.
EA#	I	**External Access Enable:** EA# must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. EA# must be strapped to V_{DD} for internal program execution. However, Disable-Extern-Boot (See Section , "Security Lock") will disable EA#, and program execution is only possible from internal program memory. The EA# pin can tolerate a high voltage[3] of 12V. (See Section , "Electrical Specification")
ALE/ PROG#	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input (PROG#) for flash programming. Normally the ALE[4] is emitted at a constant rate of 1/6 the crystal frequency[5] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to 1, ALE is disabled. (See "Auxiliary Register (AUXR)" in Section , "Special Function Registers")
NC	I/O	**No Connect**
XTAL1	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	I	**Power Supply**
V_{SS}	I	**Ground**

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1. I = Input; O = Output
2. Port 4 is not present on the PDIP and WQFN packages
3. It is not necessary to receive a 12V programming supply voltage during flash programming
4. ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3-50 KΩ to V_{DD}, e.g. for ALE pin.
5. For 6 clock mode, ALE is emitted at 1/3 of crystal frequency.

Memory Organization

The device has separate address spaces for program and data memory.

Program Flash Memory

There are two internal flash memory partitions in the device. The primary flash memory partition (Partition 0) has 66/34/18 KByte. The secondary flash memory partition (Partition 1) has 1 KByte. The total flash memory space of both partitions can be used as a contiguous code storage.

The 66/34/18 KByte primary flash partition is organized as 128/64/32 sectors, each sector consists of 128 Bytes. The primary partition is divided into four logical pages as shown in Figure 4, Figure 5 and Figure 6.

The 2K x8 secondary flash partition is organized as 8 sectors, each sector consists also of 128 Bytes.

For both partitions, the 7 least significant program address bits select the byte within the sector. The remainder of the program address bits select the sector within the partition.

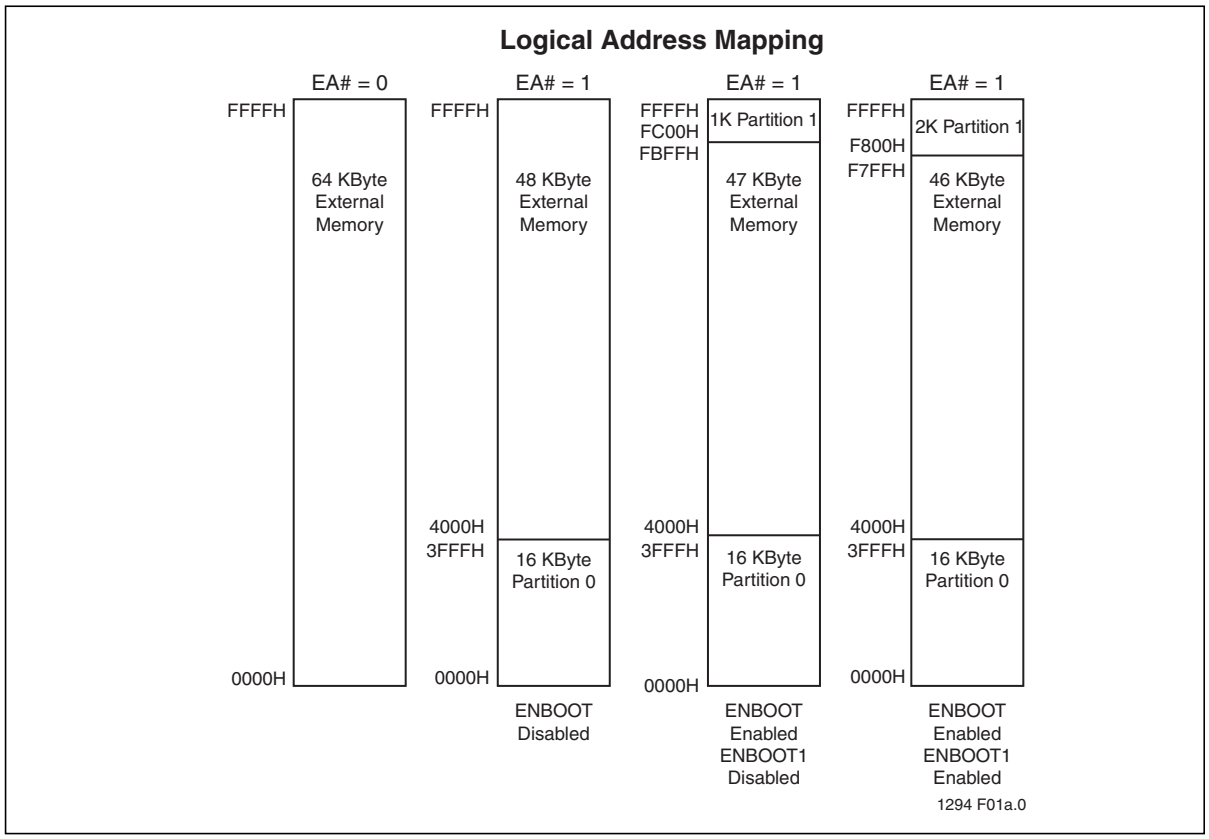

Figure 4: Program Memory Organization for SST89E54C

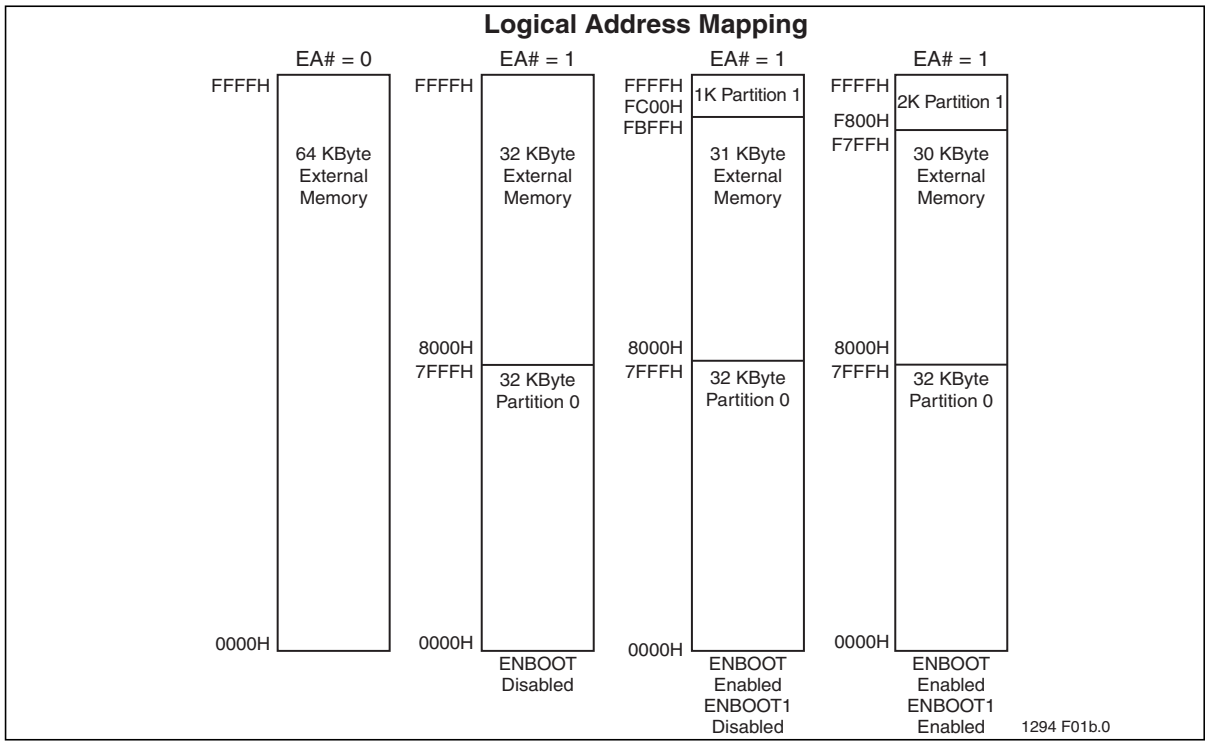

Figure 5: Program Memory Organization for SST89E58C

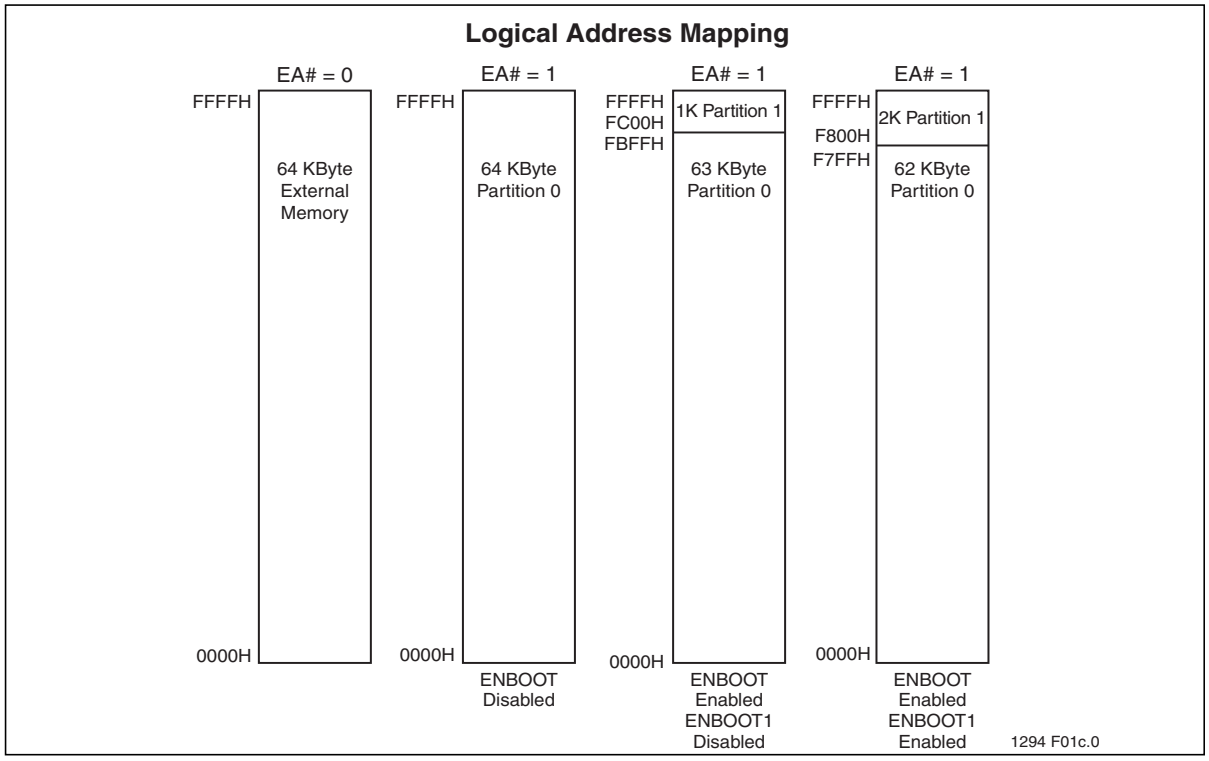

Figure 6: Program Memory Organization for SST89E516C

Data RAM Memory

The data RAM has 512 Bytes/1 KByte/2 KBytes of internal memory. The first 256 Bytes are available by default. The second 256/768/1792 Bytes are enabled by clearing the EXTRAM bit in the AUXR register. The RAM can be addressed up to 64 KByte for external data memory.

Expanded Data RAM Addressing

The SST89E/V5xC have the capability of 512 Bytes of RAM. See Figure 7.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 256/768/1792 Bytes (00H to FFH/00H to 2FFH/00H to 6FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit. (See “Auxiliary Register (AUXR)” in Section , “Special Function Registers”)

Since the upper 128 bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

When instructions access addresses in the upper 128 bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in “#data” is written to RAM location 90H rather than port 1.

Direct Access:

MOV90H, #data; write data to P1

Data in “#data” is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 256/768/1792 Bytes of memory is physically located on the chip and logically occupies the first 256/768/1792 bytes of external memory.

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 (WR#), P3.7 (RD#), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

MOVX@DPTR, A; DPTR contains 0A0H

DPTR points to 0A0H and data in "A" is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than FFH using the MOVX instruction will access external memory (0100H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX @DPTR generates a 16-bit address. This allows external addressing up the 64K. Port 2 provides the high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 - WR# and P3.7 - RD#) for external memory use. Table 2 shows external data memory RD#, WR# operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.

Table 2: External Data Memory RD#, WR# with EXTRAM bit (Typical Example[1])

	MOVX @DPTR, A or MOVX A, @DPTR		**MOVX @Ri, A or MOVX A, @Ri**
AUXR	**ADDR < 0100H**	**ADDR >= 0100H**	**ADDR = Any**
EXTRAM = 0	RD# / WR# not asserted	RD# / WR# asserted	RD# / WR# not asserted[2]
EXTRAM = 1	RD# / WR# asserted	RD# / WR# asserted	RD# / WR# asserted

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1. The table addresses will differ for each part—SST89E54C, SST89E58C, and SST89E516C.
2. Access limited to ERAM address within 0 to 0FFH.

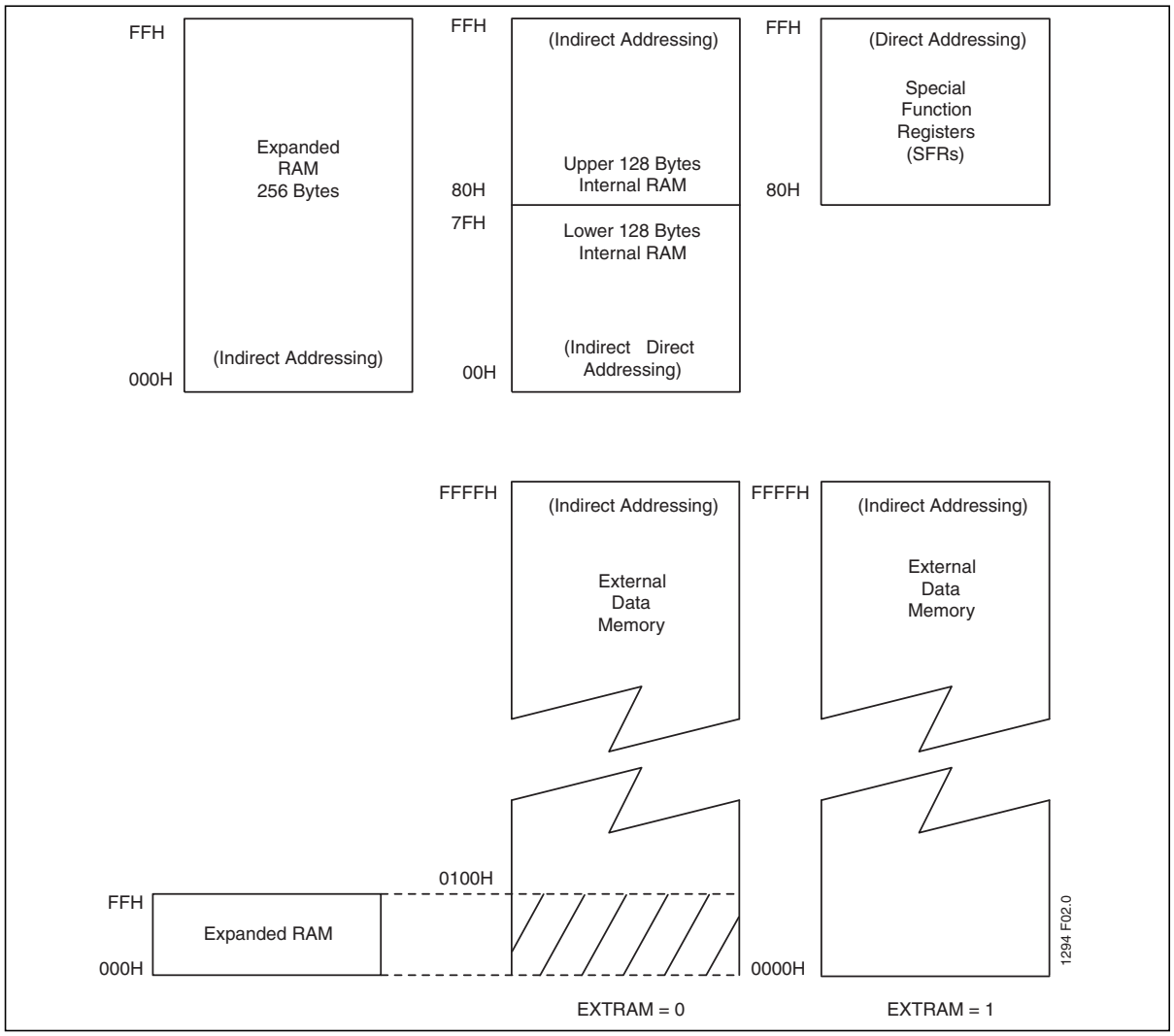

Figure 7: Internal and External Data Memory Structure

Dual Data Pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS=0, DPTR0 is selected; when DPS=1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1. (See Figure 8)

Special Function Registers

Most of the unique features of the FlashFlex micro controller family are controlled by bits in special function registers (SFRs) located in the SFR memory map shown in Table 3. Individual descriptions of each SFR are provided and reset values indicated in Tables 4 to 8.

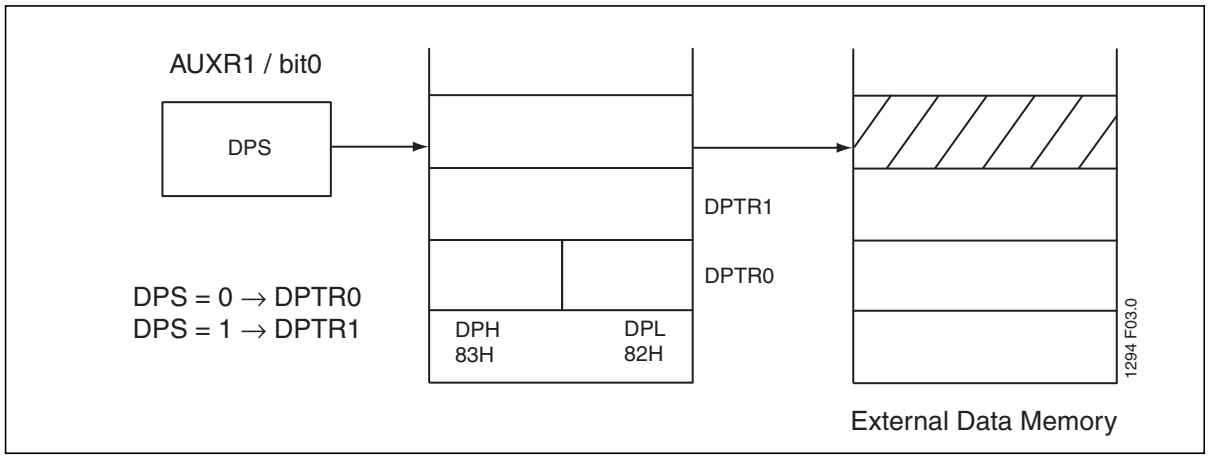

Figure 8: Dual Data Pointer Organization

Table 3: FlashFlex SFR Memory Map

	8 BYTES								
F8H	S2CON	CH	CCAP0H	CCAP1H	CCAP2H	CCAP3H	CCAP4H		FFH
F0H	B								F7H
E8H	IEN1	CL	CCAP0L	CCAP1L	CCAP2L	CCAP3L	CCAP4L		EFH
E0H	ACC	S2STA	S2DAT	S2ADR					E7H
D8H	S1CON	S1STA	S1DAT	S1ADR					DFH
D0H	PSW					SPCR			D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	CCON	CMOD	CCAPM0	CCAPM1	CCAPM2	CCAPM3	CCAPM4		C7H
B8H	IP	SADEN							BFH
B0H	P3	SFCF	SFCM	SFAL	SFAH		SFST	IPH	B7H
A8H	IEN0	SADDR	SPSR						AFH
A0H	P2	P4	AUXR1				WDTRST		A7H
98H	S0CON	S0BUF							9FH
90H	P1	IP1	IP1H						97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1	AUXR		8FH
80H	P0	SP	DPL	DPH			SPDR	PCON	87H

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Table 4: CPU related SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B[1]	B Register	F0H	B[7:0]								00H
PSW[1]	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IEN0[1]	Interrupt Enable	A8H	EA	EC	ES1	ES0	ET1	EX1	ET0	EX0	00H
IEN1[1]	Interrupt Enable A	E8H	-	-	-	-	-	ES3	ES2	ET2	xxxxx000b
IP	Interrupt Priority Reg	B8H	PT2	PPC	PS1	PS0	PT1	PX1	PT0	PX0	00000000b
IPH	Interrupt Priority Reg High	B7H	PT2H	PPCH	PS1H	PS0H	PT1H	PX1H	PT0H	PX0H	00000000b
IPI	Interrupt Priority Reg A	91H	-		-	-	-	-	PS3	PS2	xxxxxx00b
IPIH	Interrupt Priority Reg A High	92H	-		-	-	-	-	PS3H	PS2H	xxxxxx00b
PCON	Power Control	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL	00x10000b
AUXR	Auxiliary Reg	8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxx10b
AUXR1	Auxiliary Reg 1	A2H	-	-	ENBOOT	-	GF2	0	-	DPS	xxxx00x0b

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1. Bit Addressable SFRs

Table 5: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB					LSB			Reset Value
SFCF	SuperFlash Configuration	B1H	IAP Command Status	IAP/ ISP	-	ENBOOT 1	-	SFST_SEL			10x00000b
SFCM	SuperFlash Command	B2H	-	FCM[6:0]							00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register A_7 to A_0 (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register A_{15} to A_8 (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H SFST_SEL= 0H	Manufacturer's ID								15H
		SFST_SEL= 1H	Device ID0 (F7H indicates Device ID1 is real ID)								
		SFST_SEL= 2H	Device ID1								
		SFST_SEL= 3H	Boot Vector								
		SFST_SEL= 4H	Status Byte_N	-	-	-	12 Cycle Mode_N	LB3_N	LB2_N	LB1_N	1xxx1111b

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Table 6: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB	Reset Value
WDTRST		A6H		00H

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Table 7: TIMER/COUNTER SFR

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
TMOD	Timer/Counter Mode Control	89H	Timer 1				Timer 0				00H
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON[1]	Timer/Counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TH0	Timer 0 MSB	8CH	TH0[7:0]								00H
TL0	Timer 0 LSB	8AH	TL0[7:0]								00H
TH1	Timer 1 MSB	8DH	TH1[7:0]								00H
TL1	Timer 1 LSB	8BH	TL1[7:0]								00H
T2CON[1]	Timer/Counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H
T2MOD#	Timer 2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b
TH2	Timer 2 MSB	CDH	TH2[7:0]								00H
TL2	Timer 2 LSB	CCH	TL2[7:0]								00H
RCAP2H	Timer 2 Capture MSB	CBH	RCAP2H[7:0]								00H
RCAP2L	Timer 2 Capture LSB	CAH	RCAP2L[7:0]								00H

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1. Bit Addressable SFRs

Table 8: Interface SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
S0BUF	Serial Data Buffer	99H	SBUF[7:0]								Indeterminate
S0CON[1]	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SADDR	Slave Address	A9H	SADDR[7:0]								00H
SADEN	Slave Address Mask	B9H	SADEN[7:0]								00H
SPCR	SPI Control Register	D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04H
SPSR	SPI Status Register	AAH	SPIF	WCOL							00H
SPDR	SPI Data Register	86H	SPDR[7:0]								00H
S1CON	I^2C 1 Control	D8H	CR2_1	ENS1_1	STA_1	ST0_1	S1_1	AA_1	CR1_1	CR0_1	00H
S1STA	I^2C 1 Status	D9H	SC4_1	SC3_1	SC2_1	SC1_1	SC0_1	0	0	0	F8H
S1DAT	I^2C 1 Data	DAH	S1DAT[7:0]								00H
S1ADR	I^2C 1 Address	DBH	Slave Address							GC_1	00H
S2CON	I^2C 1 Control	F8H	CR2_2	ENS1_2	STA_2	ST0_2	S1_2	AA_2	CR1_2	CR0_2	00H
S2STA	I^2C 1 Status	E1H	SC4_2	SC3_2	SC2_2	SC1_2	SC0_2	0	0	0	F8H
S2DAT	I^2C 1 Data	E2H	S2DAT[7:0]								00H
S2ADR	I2C 1 Address	E3H	Slave Address							GC_2	00H
P0[1]	Port 0	80H	P0[7:]								FFH
P1[1]	Port 1	90H	-	-	-	-	-	-	T2EX	T2	FFH
P2[1]	Port 2	A0H	P0[7:]								FFH
P3[1]	Port 3	B0H	RD#	WR#	T1	T0	INT1#	INT0#	TXD	RXD	FFH

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1. Bit Addressable SFRs

Table 9: PCA SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
CH CL	PCA Timer/Counter	F9H E9H	CH[7:0] CL[7:0]								00H 00H
CCON[1]	PCA Timer/Counter Control Register	C0H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000b
CMOD	PCA Timer/Counter Mode Register	C1H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000b
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]								00H
CCAP0L		EAH	CCAP0L[7:0]								00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]								00H
CCAP1L		EBH	CCAP1L[7:0]								00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]								00H
CCAP2L		ECH	CCAP2L[7:0]								00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]								00H
CCAP3L		EDH	CCAP3L[7:0]								00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]								00H
CCAP4L		EEH	CCAP4L[7:0]								00H
CCAPM0	PCA Compare/Capture Module Mode Registers	C2H	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	x0000000b
CCAPM1		C3H	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	x0000000b
CCAPM2		C4H	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	x0000000b
CCAPM3		C5H	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	x0000000b
CCAPM4		C6H	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	x0000000b

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1. Bit Addressable SFRs

SuperFlash Configuration Register (SFCF)

Location	7	6	5	4	3	2	1	0	Reset Value
B1H	IAP Command Status	IAP/ISP Enable	-	ENBOOT 1	-	SFST_SEL			10x00000b

Symbol	Function
IAP Command Status	If the IAP command is executed successfully, it is set to 1 bit/binary one by the hardware. It is reset by the hardware if SFCM is written by software.
IAP/ISP Enable	IAP/ISP Enable Bit 0: Disable IAP/ISP commands (Commands will be ignored) 1: Enable all IAP/ISP (default enable) commands
ENBOOT1	0: Any instruction code fetch from address 62K to 63K will read from Partition 0 for 516C and from external memory for 54C and 58C 1: Any instruction code fetch from address 62K-63K will read from Lower 1K of Partition 1
SFST_SEL	Provide index to read back information when read to SFST register is executed (See , “SuperFlash Status Register (SFST) (Read Only Register)” on page 20 for detailed settings)

SuperFlash Command Register (SFCM)

Location	7	6	5	4	3	2	1	0	Reset Value
B2H	-	FCM6	FCM5	FCM4	FCM3	FCM2	FCM1	FCM0	00H

Symbol	Function
-	Reserved
FCM[6:0]	Flash operation command 000_0001b Chip-Erase 000_1011b Sector-Erase 000_1101b Partition0-Erase 000_1100b Byte-Verify[1] 000_1110b Byte-Program 000_0011b Prog Lock Bit 1/2/3 000_1000b Prog-12-Cycles mode/status byte 000_1001b prog Boot Vector/Erase Boot Vector and Status Byte All other combinations are not implemented, and reserved for future use. Before writing the command to the registers, the application code needs to put the correct value on SFAL, SFAH, and SFDT if necessary.

SuperFlash Address Registers (SFAL)

Location	7	6	5	4	3	2	1	0	Reset Value
B3H	SuperFlash Low Order Byte Address Register								00H

Symbol	Function
SFAL	Mailbox register for interfacing with flash memory block. (Low order address register)

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00H

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register)

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00H

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block. (Data register)

SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SuperFlash Status Register								15H

Symbol	Function
SFST	This is a read-only register. The read-back value is indexed by SFST_SEL in the SuperFlash Configuration Register (SFCF) SFST_SEL= 0H: Manufacturer's ID 1H: Device ID0 = F7H 2H: Device ID1 = Device ID (Refer to Table 10 on page 31) 3H: Boot Vector 4H: Page-Security bit setting 5H: Chip-Level Security bit setting and Boot Options

Interrupt Enable (IEN0)

Location	7	6	5	4	3	2	1	0	Reset Value
A8H	EA	EC	ES1	ES	ET1	EX1	ET0	EX0	00H

Symbol	Function
EA	Global Interrupt Enable 0 = Disable 1 = Enable
EC	PCA Interrupt Enable
ES1	I^2C 1 Interrupt Enable
ES	Serial Interrupt Enable
ET1	Timer 1 Interrupt Enable
EX1	External 1 Interrupt Enable
ET0	Timer 0 Interrupt Enable
EX0	External 0 Interrupt Enable

Interrupt Enable A (IEN1)

Location	7	6	5	4	3	2	1	0	Reset Value
E8H	-	-	-	-	-	ES3	ES2	ET2	xxxxx000b

Symbol	Function
ET2	Timer 2 Interrupt Enable
ES2	I^2C 2 Interrupt Enable
ES3	SPI Enable

Interrupt Priority (IP)

Location	7	6	5	4	3	2	1	0	Reset Value
B8H	PT2	PPC	PSI	PS	PT1	PX1	PT0	PX0	00000000b

Symbol	Function
PT2	Timer 2 Interrupt priority bit
PPC	PCA Interrupt priority bit
PSI	I^2C 1 Interrupt priority bit
PS	Serial Port Interrupt priority bit
PT1	Timer 1 Interrupt priority bit
PX1	External Interrupt 1 priority bit
PT0	Timer 0 Interrupt priority bit
PX0	External Interrupt 0 priority bit

Interrupt Priority High (IPH)

Location	7	6	5	4	3	2	1	0	Reset Value
B7H	PT2H	PPCH	PS1H	PSH	PT1H	PX1H	PT0H	PX0H	00000000b

Symbol	Function
PT2H	Timer 2 Interrupt priority bit high
PPCH	PCA Interrupt priority bit high
PS1H	I^2C 1 Interrupt priority bit high
PSH	Serial Port Interrupt priority bit high
PT1H	Timer 1 Interrupt priority bit high
PX1H	External Interrupt 1 priority bit high
PT0H	Timer 0 Interrupt priority bit high
PX0H	External Interrupt 0 priority bit high

Interrupt Priority (IPI)

Location	7	6	5	4	3	2	1	0	Reset Value
91H	-	-	-	-	-		PS3	PS2	xxxxxx00b

Symbol	Function
PS2	I^2C 2 Interrupt priority bit
PS3	SPI Interrupt priority bit

Interrupt Priority High (IPIH)

Location	7	6	5	4	3	2	1	0	Reset Value
92H	-	-	-	-	-	-	PS3H	PS2H	xxxxxx00b

Symbol	Function
PS2H	I^2C 2 Interrupt priority bit high
PS3H	SPI Interrupt priority bit high

Auxiliary Register (AUXR)

Location	7	6	5	4	3	2	1	0	Reset Value
8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxx10b

Symbol	Function
EXTRAM	Internal/External RAM access 0: Internal Expanded RAM access within range of 00H to FFH using MOVX @Ri / @DPTR. Beyond 100H, the MCU always accesses external data memory For details, refer to Section , “Expanded Data RAM Addressing” 1: External data memory access
AO	Disable/Enable ALE 0: ALE is emitted at a constant rate of 1/3 the oscillator frequency in 6 clock mode, 1/6 f_{OSC} in 12 clock mode 1: ALE is active only during a MOVX or MOVC instruction

Auxiliary Register 1 (AUXR1)

Location	7	6	5	4	3	2	1	0	Reset Value
A2H	-	-	ENBOOT	-	GF2	0	-	DPS	xx0x00x0b

Symbol	Function
ENBOOT	0: Any instruction code fetch from address 62K to 63K will read from Block 0 for 516C and from external memory for 54C and 58C 1: Any instruction code fetch from address 62K-63K will read from Upper 1K of Block 1
GF2	General purpose user-defined flag
DPS	DPTR registers select bit 0: DPTR0 is selected 1: DPTR1 is selected

Watchdog Timer Control Register (WDTRST)

Location	7	6	5	4	3	2	1	0	Reset Value
A6H	-	-	-	-	-	-	-	-	00000000b

Symbol	Function
-	Reserved

I²C 1 Control Register (S1CON)

Location	7	6	5	4	3	2	1	0	Reset Value
D8H	CR2_1	ENS1_1	STA_1	ST0_1	S1_1	AA_1	CR1_1	CR0_1	00H

Symbol	Function
CR2_1	Clock rate Bit
ENS1_1	I²C 1 Enable Bit
STA_1	Start Flag
ST0_1	Stop Flag
S1_1	Serial Interrupt Flag
AA_1	Assert Acknowledge Flag
CR1_1	Clock rate Bit
CR0_1	Clock Rate Bit

I²C 2 Control Register (S2CON)

Location	7	6	5	4	3	2	1	0	Reset Value
F8H	CR2_2	ENS1_2	STA_2	ST0_2	S1_2	AA_2	CR1_2	CR0_2	00H

Symbol	Function
CR2_2	Clock rate Bit
ENS1_2	I²C 1 Enable Bit
STA_2	Start Flag
ST0_2	Stop Flag
S1_2	Serial Interrupt Flag
AA_2	Assert Acknowledge Flag
CR1_2	Clock Rate Bit
CR0_2	Clock Rate Bit

I²C 1 Status Register (S1STA)

Location	7	6	5	4	3	2	1	0	Reset Value
D9H	SC4_1	SC3_1	SC2_1	SC1_1	SC0_1	0	0	0	F8H

Symbol	Function
S1STA	This is a read-only SFR. The five most significant bits contain the status code. The three least significant bits are always 0.

I²C 2 Status Register (S2STA)

Location	7	6	5	4	3	2	1	0	Reset Value
E1H	SC4_2	SC3_2	SC2_2	SC1_2	SC0_2	0	0	0	F8H

Symbol	Function
S2STA	This is a read-only SFR. The five most significant bits contain the status code. The three least significant bits are always 0.

I²C 1 Data Register (S1DAT)

Location	7	6	5	4	3	2	1	0	Reset Value
DAH	S1DAT[7:0]								00H

I²C 2 Data Register (S2DAT)

Location	7	6	5	4	3	2	1	0	Reset Value
E2H	S2DAT[7:0]								00H

I²C 1 Address Register 1 (S1ADR)

Location	7	6	5	4	3	2	1	0	Reset Value
D8H	Slave Address							GC_1	00H

I²C 2 Data Register (S2ADR)

Location	7	6	5	4	3	2	1	0	Reset Value
E3H	Slave Address							GC_2	00H

PCA Timer/Counter Control Register[1] (CCON)

Location	7	6	5	4	3	2	1	0	Reset Value
C0H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000b

1. Bit addressable

Symbol	Function
CF	PCA Counter Overflow Flag Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software, but can only cleared by software.
CR	PCA Counter Run control bit Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

PCA Timer/Counter Mode Register[1] (CMOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C1H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000b

1. Not bit addressable

Symbol	Function
CIDL	Counter Idle Control: 0: Programs the PCA Counter to continue functioning during idle mode 1: Programs the PCA Counter to be gated off during idle
WDTE	Watchdog Timer Enable: 0: Disables Watchdog timer function on PCA module 4 1: Enables Watchdog timer function on PCA module 4
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
CPS1	PCA Count Pulse Select bit 1
CPS0	PCA Count Pulse Select bit 2

CPS1	CPS0	Selected PCA Input[1]	
0	0	0	Internal clock, f_{OSC}/6 in 6 clock mode (f_{OSC}/12 in 12 clock mode)
0	1	1	Internal clock, f_{OSC}/2 in 6 clock mode (f_{OSC}/4 in 12 clock mode)
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P1.2 pin
			(max. rate = f_{OSC}/4 in 6 clock mode, f_{OSC}/8 in 12 clock mode)

1. f_{OSC} = oscillator frequency

ECF	PCA Enable Counter Overflow interrupt: 0: Disables the CF bit in CCON 1: Enables CF bit in CCON to generate an interrupt

PCA Compare/Capture Module Mode Register[1] (CCAPMn)

Location	7	6	5	4	3	2	1	0	Reset Value
C2H	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	x0000000b
C3H	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	x0000000b
C4H	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	x0000000b
C5H	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	x0000000b
C6H	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	x0000000b

1. Not bit addressable

Symbol	Function
-	Not implemented, reserved for future use. **Note:** User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
ECOMn	Enable Comparator 0: Disables the comparator function 1: Enables the comparator function
CAPPn	Capture Positive 0: Disables positive edge capture on CEX[4:0] 1: Enables positive edge capture on CEX[4:0]
CAPNn	Capture Negative 0: Disables negative edge capture on CEX[4:0] 1: Enables negative edge capture on CEX[4:0]
MATn	Match: Set ECOM[4:0] and MAT[4:0] to implement the software timer mode 0: Disables software timer mode 1: A match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle 0: Disables toggle function 1: A match of the PCA counter with this module’s compare/capture register causes the the CEXn pin to toggle.
PWMn	Pulse Width Modulation mode 0: Disables PWM mode 1: Enables CEXn pin to be used as a pulse width modulated output
ECCFn	Enable CCF Interrupt 0: Disables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request. 1: Enables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request.

SPI Control Register (SPCR)

Location	7	6	5	4	3	2	1	0	Reset Value
D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	00H

Symbol	Function
SPIE	If both SPIE and ES are set to one, SPI interrupts are enabled.
SPE	SPI enable bit. 0: Disables SPI. 1: Enables SPI and connects SS#, MOSI, MISO, and SCK to pins P1.4, P1.5, P1.6, P1.7.
DORD	Data Transmission Order. 0: MSB first in data transmission. 1: LSB first in data transmission.
MSTR	Master/Slave select. 0: Selects Slave mode. 1: Selects Master mode.
CPOL	Clock Polarity 0: SCK is low when idle (Active High). 1: SCK is high when idle (Active Low).
CPHA	Clock Phase control bit. 0: Shift triggered on the leading edge of the clock. 1: Shift triggered on the trailing edge of the clock.
SPR1, SPR0	SPI Clock Rate Select bits. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, f_{OSC}, is as follows:

SPR1	SPR0	SCK = f_{OSC} divided by
0	0	4
0	1	16
1	0	64
1	1	128

SPI Status Register (SPSR)

Location	7	6	5	4	3	2	1	0	Reset Value
AAH	SPIF	WCOL	-	-	-	-	-	-	00xxxxxxb

Symbol	Function
SPIF	SPI Interrupt Flag. Upon completion of data transfer, this bit is set to 1. If SPIE =1 and ES =1, an interrupt is then generated. This bit is cleared by software.
WCOL	Write Collision Flag. Set if the SPI data register is written to during data transfer. This bit is cleared by software.

SPI Data Register (SPDR)

Location	7	6	5	4	3	2	1	0	Reset Value
86H	SPDR[7:0]								00H

Power Control Register (PCON)

Location	7	6	5	4	3	2	1	0	Reset Value
87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL	00x10000b

Symbol	Function
SMOD1	Double Baud rate bit. If SMOD1 = 1, Timer 1 is used to generate the baud rate, and the serial port is used in modes 1, 2, and 3.
SMOD0	FE/SM0 Selection bit. 0: SCON[7] = SM0 1: SCON[7] = FE,
POF	Power-on reset status bit, this bit will not be affected by any other reset. POF should be cleared by software. 0: No Power-on reset. 1: Power-on reset occurred
GF1	General-purpose flag bit.
GF0	General-purpose flag bit.
PD	Power-down bit, this bit is cleared by hardware after exiting from power-down mode. 0: Power-down mode is not activated. 1: Activates Power-down mode.
IDL	Idle mode bit, this bit is cleared by hardware after exiting from idle mode. 0: Idle mode is not activated. 1: Activates idle mode.

Serial Port Control Register (S0CON)

Location	7	6	5	4	3	2	1	0	Reset Value
98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00000000 b

Symbol	Function
FE	Set SMOD0 = 1 to access FE bit. 0: No framing error 1: Framing Error. Set by receiver when an invalid stop bit is detected. This bit needs to be cleared by software.
SM0	SMOD0 = 0 to access SM0 bit. Serial Port Mode Bit 0
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate[1]
0	0	0	Shift Register	f_{OSC}/6 (6 clock mode) or f_{OSC}/12 (12 clock mode)
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	f_{OSC}/32 or f_{OSC}/16 (6 clock mode) or f_{OSC}/64 or f_{OSC}/32 (12 clock mode)
1	1	3	9-bit UART	Variable

1. f_{OSC} = oscillator frequency

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a given or broadcast address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be 0.
REN	Enables serial reception. 0: to disable reception. 1: to enable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission, Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Timer/Counter 2 Control Register (T2CON)

Location	7	6	5	4	3	2	1	0	Reset Value
C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflow to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2#	Timer or counter select (Timer 2) 0: Internal timer (OSC/6 in 6 clock mode, OSC/12 in 12 clock mode) 1: External event counter (falling edge triggered)
CP/RL2#	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timer/Counter 2 Mode Control (T2MOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b

Symbol	Function
-	Not implemented, reserved for future use. **Note:** User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

Flash Memory Programming

The device internal flash memory can be programmed or erased using In-Application Programming (IAP).

Product Identification

The Read-ID command accesses the Signature Bytes that identify the device and the manufacturer as SST. External programmers primarily use these Signature Bytes in the selection of programming algorithms.

Table 10: Product Identification

	Address	Data
Manufacturer's ID	30H	15H
Device ID	31H	C2H
Device ID (extended)		
SST89E54C	32H	90H
SST89E58C	32H	91H
SST89E516C	32H	92H

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In-Application Programming

The IAP/ISP functions are issued via the SST mail box scheme. Detailed flash block operations are performed by the flash control unit. While the flash control executes IAP commands, the CPU is on hold since there is only one physical flash block in the SST89x5xC devices. When IAP commands finish, the CPU can resume execution of the application code. So the application code needs to turn off the interrupt or turn off the peripheral modules before it issues IAP commands since the CPU cannot respond to the interrupt or poll the SFR status.

The IAP supports the following commands:

1. Chip-Erase
2. Partition0-Erase
3. Sector-Erase
4. Byte-Program
5. Byte-Verify
6. PROG-Status Byte
7. PROG-Boot Vector
8. PROG-LB-1/-2/-3 (LB = Lock Bit)
9. PROG-12-Cycles-Mode
10. Erase-Status-Byte-and-Boot-Vector

Table 11: IAP Commands

Operation	SFCM [6:0]	SFAH	SFAL	SFDT
Chip-Erase	01H	X	X	55H
Partition0-Erase	0DH	X	X	AAH
Sector-Erase	0BH	AH	AL	A5H
Byte-Program	0EH	AH	AL	DI
Byte-Verify (Read)	0CH	AH	AL	DO
PROG-Boot-Vector	09H	F0H	X	DI
PROG-Status-Byte	08H	E0H	X	X
PROG-LB1	03H	90H	X	X
PROG-LB2	03H	91H	X	X
PROG-LB3	03H	92H	X	X
PROG-12-Cycles-Mode	03H	93H	X	X
Erase-Status-Byte-and-Boot-Vector	03H	C0H	X	X

T11.0 1294

Chip-Erase

Chip-Erase IAP command will erase Partition 0 and Partition 1, code flash memory, erase the non-volatile RAM (NVR) sector 1, and set the LB status bit to 0.

Partition0-Erase

Partition0-Erase IAP command will erase Partition 0 code flash memory, erase the NVR sector 1, and set the LB status bit to 0.

Erase Status Byte and Boot Vector

This command sets the Status Byte and Boot Vector to 1.

IAP Command Sequence

In order to protect the flash during the power-off condition, the application needs to write a special, sequential command sequence to the SFCM SFR address before issuing a valid IAP command.

First, the application needs to write 0FH, second, A6H or 59H (depending on the targeted block), then the IAP command.

Table 12: Command Sequence Table

IAP Commands	Valid 2nd Sequence	Target Memory	Address Range
Sector-Erase Byte-Program Byte-Verify	59H	Partition 1	0-2K
	A6H	Partition 0	0-64K (SST89E516C) 0-32K (SST89E58C) 0-16K (SST89E54C)
Other IAP Commands	A6H/59H	NVR or Partition 0 or Whole Flash Space	N/A

T12.0 1294

In-System Programming

The bootstrap loader (BSL) is located in Partition 1 and cannot be accessed unless the SFR AUXR1 (Address = A2H), Bit 5 is enabled. The default value of this bit after reset is 0 unless the Status byte is programmed or the PSEN# is pulled low, ALE is high and EA# is high at the falling edge of the reset.

Normal Mode

After power-on, the hardware checks the Status byte. If the Status byte is set to 0, the value of the boot vector is used as the high byte of the program counter (PC) starting address, the lower byte of PC will be 00H. If the Status byte is set to 1, the PC will start from address 0. The boot vector factory setting is FCH and the Status byte factory default setting is 0.

Hardware Enter Mode

The user can hold PSEN# low, ALE and EA# is high at the falling edge of reset. This is the same effect as having a programmed NVR Status Byte.

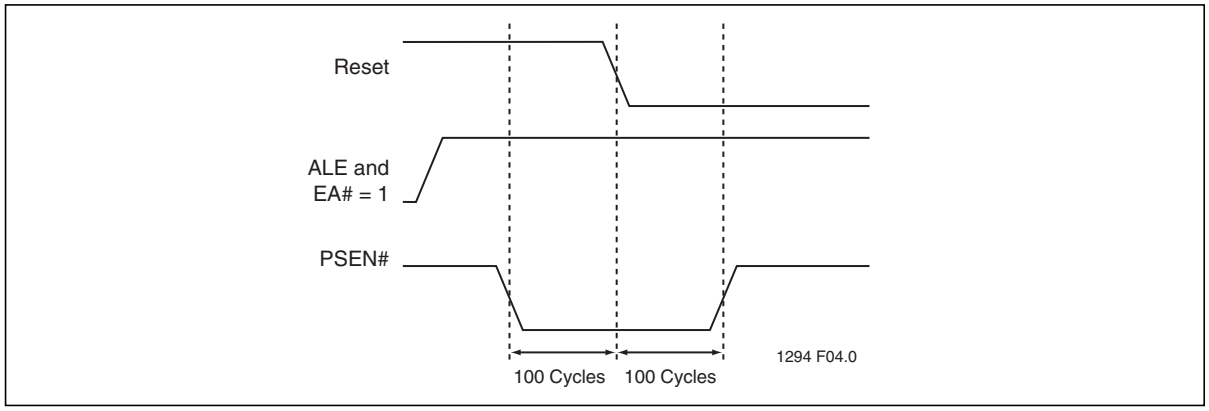

Figure 9: Hardware Active Mode/ISP Entry Mode

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 7 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 13: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

T13.0 25096

1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 14: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

T14.0 25096

1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

Table 15: Timer/Counter 2

	Mode	T2CON	
		Internal Control[1]	External Control[2]
Used as Timer	16-bit Auto-Reload	00H	08H
	16-bit Capture	01H	09H
	Baud rate generator receive and transmit same baud rate	34H	36H
	Receive only	24H	26H
	Transmit only	14H	16H
Used as Counter	16-bit Auto-Reload	02H	0AH
	16-bit Capture	03H	0BH

T15.0 25096

1. Capture/Reload occurs only on timer/counter overflow.
2. Capture/Reload occurs on timer/counter overflow and a 1 to 0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generating mode.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency (61 Hz to 4 MHz in 12 clock mode).

To configure Timer/Counter 2 as a clock generator, bit
C/#T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H, RCAP2L})}$$

n =2 (in 6 clock mode)
4 (in 12 clock mode)

Where (RCAP2H, RCAP2L) = the contents of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will not be the same.

Serial I/O

Full-Duplex, Enhanced UART

The device serial I/O port is a full-duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The UART has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) SFR is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.

Framing Error Detection

Framing Error Detection is a feature, which allows the receiving controller to check for valid stop bits in modes 1, 2, or 3. Missing stops bits can be caused by noise in serial lines or from simultaneous transmission by two CPUs.

Framing Error Detection is selected by going to the PCON register and changing SMOD0 = 1 (see Figure 10). If a stop bit is missing, the Framing Error bit (FE) will be set. Software may examine the FE bit after each reception to check for data errors. After the FE bit has been set, it can only be cleared by software. Valid stop bits do not clear FE. When FE is enabled, RI rises on the stop bit, instead of the last data bit (see Figure 11 and Figure 12).

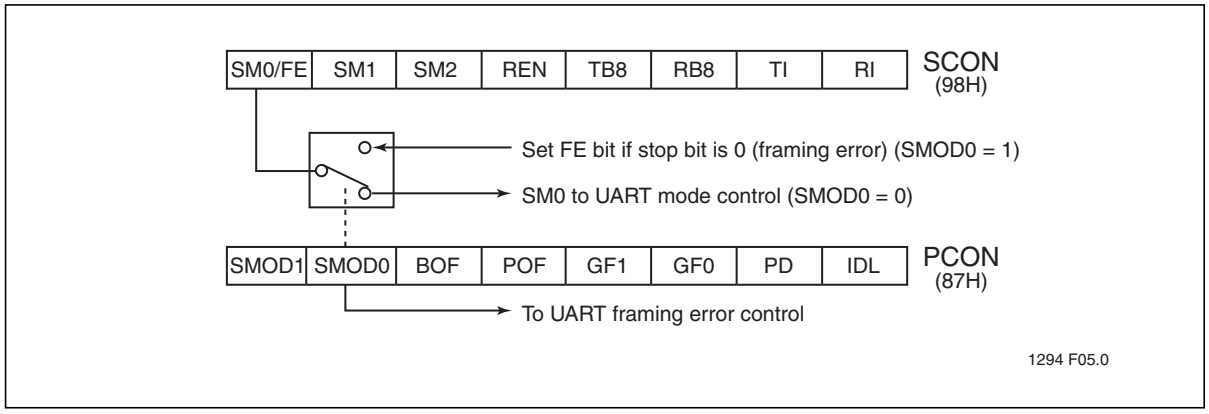

Figure 10: Framing Error Block Diagram

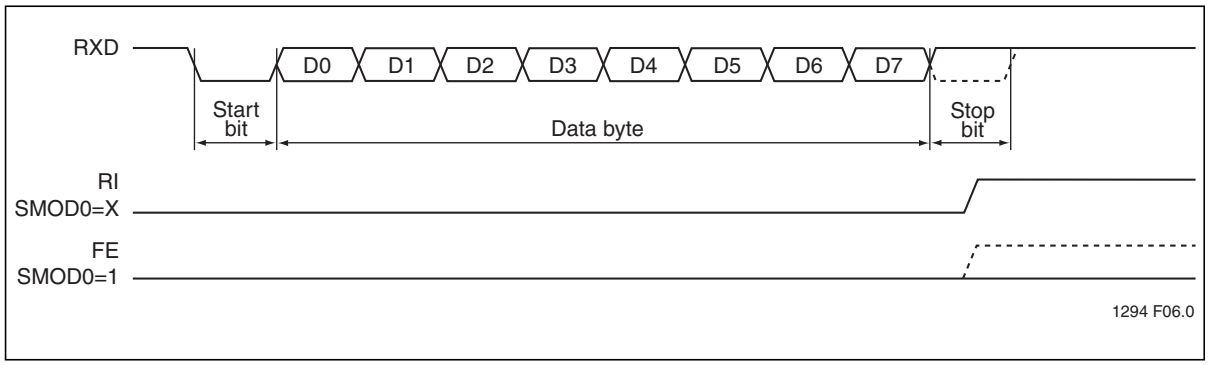

Figure 11: UART Timings in Mode 1

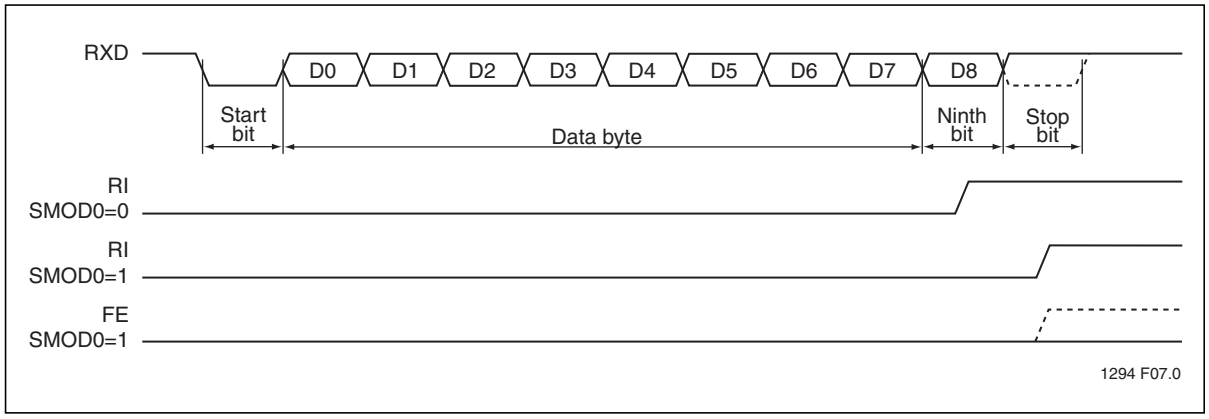

Figure 12: UART Timings in Modes 2 and 3

Automatic Address Recognition

Automatic Address Recognition (AAR) helps to reduce the time and power required to communicate with multiple serial devices. Each device shares the same serial link, but has its own address. In this configuration, a device is only interrupted when it receives its own address, thus eliminating the software overhead to compare addresses.

This same feature helps to save power because it can be used in conjunction with idle mode to reduce the system's overall power consumption. AAR allows the other slaves to remain in idle mode while only one is interrupted. By limiting the number of interruptions, the total current draw on the system is reduced.

There are two ways to communicate with slaves: a group of them at once, or all of them at once. To communicate with a group of slaves, the master sends out an address called the given address. To communicate with all the slaves, the master sends out an address called the "broadcast" address.

AAR can be configured as mode 2 or 3 (9-bit modes) and setting the SM2 bit in SCON. Each slave has its own SM2 bit set waiting for an address byte (9th bit = 1). The Receive Interrupt (RI) flag will only be set when the received byte matches either the given address or the broadcast address. Next, the slave then clears its SM2 bit to enable reception of the data bytes (9th bit = 0) from the master. When the 9th bit = 1, the master is sending an address. When the 9th bit = 0, the master is sending actual data.

If mode 1 is used, the stop bit takes the place of the 9th bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit. Note that mode 0 cannot be used. Setting SM2 bit in the SCON register in mode 0 will have no effect.

Each slave's individual address is specified by SFR SADDR. SFR SADEN is a mask byte that defines "don't care" bits to form the given address when combined with SADDR. See the example below:

Slave 1

SADDR = 1111 0001
SADEN = 1111 1010
GIVEN = 1111 0X0X

Slave 2

SADDR = 1111 0011
SADEN = 1111 1001
GIVEN = 1111 0XX1

Using the Given Address to Select Slaves

Any bits masked off by a 0 from SADEN become a "don't care" bit for the given address. Any bit masked off by a 1, becomes ANDED with SADDR. The "don't cares" provide flexibility in the user-defined addresses to address more slaves when using the given address.

Shown in the example above, Slave 1 has been given an address of 1111 0001 (SADDR). The SADEN byte has been used to mask off bits to a given address to allow more combinations of selecting Slave 1 and Slave 2. In this case for the given addresses, the last bit (LSB) of Slave 1 is a "don't care" and the last bit of Slave 2 is a 1. To communicate with Slave 1 and Slave 2, the master would need to send an address with the last bit equal to 1 (e.g. 1111 0001) since Slave 1's last bit is a don't care and Slave 2's last bit has to be a 1. To communicate with Slave 1 alone, the master would send an address with the last bit equal to 0 (e.g. 1111 0000), since Slave 2's last bit is a 1. See the table below for other possible combinations.

Select Slave 1 Only		
Slave 1	**Given Address**	**Possible Addresses**
	1111 0X0X	1111 0000 1111 0100

Select Slave 2 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 0XX1	1111 0111 1111 0011

Select Slaves 1 and 2	
Slaves 1 and 2	**Possible Addresses**
	1111 0001 1111 0101

If the user added a third slave such as the example below:

Slave 3

SADDR	=	1111	1001
SADEN	=	1111	0101
GIVEN	=	1111	X0X1

Select Slave 3 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 X0X1	1111 1011 1111 1001

The user could use the possible addresses above to select slave 3 only. Another combination could be to select slave 2 and 3 only as shown below.

Select Slaves 2 and 3 Only	
Slaves 2 and 3	**Possible Addresses**
	1111 0011

More than one slave may have the same SADDR address as well, and a given address could be used to modify the address so that it is unique.

Using the Broadcast Address to Select Slaves

Using the broadcast address, the master can communicate with all the slaves at once. It is formed by performing a logical OR of SADDR and SADEN with 0s in the result treated as “don’t cares”.

Slave 1

1111 0001	=	SADDR
+1111 1010	=	SADEN
1111 1X11	=	Broadcast

“Don’t cares” allow for a wider range in defining the broadcast address, but in most cases, the broadcast address will be FFH.

On reset, SADDR and SADEN are “0”. This produces an given address of all “don’t cares” as well as a broadcast address of all “don’t cares.” This effectively disables Automatic Addressing mode and allows the micro controller to function as a standard 8051, which does not make use of this feature.

Serial Peripheral Interface

SPI Features

- Master or slave operation
- 10 MHz bit frequency (max)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write collision flag protection (WCOL)
- Wake up from idle mode (slave mode only)

SPI Description

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the SST89E/V5xC and peripheral devices or between several SST89E/V5xC devices.

Figure 13 shows the correspondence between master and slave SPI devices. The SCK pin is the clock output and input for the master and slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin on the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPIF flag is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the Serial Port Interrupt Enable bit (ES) are both set.

An external master drives the Slave Select input pin, SS#/P1[4], low to select the SPI module as a slave. If SS#/P1[4] has not been driven low, then the slave SPI unit is not active and the MOSI/P1[5] port can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock. Figures 14 and 15 show the four possible combinations of these two bits.

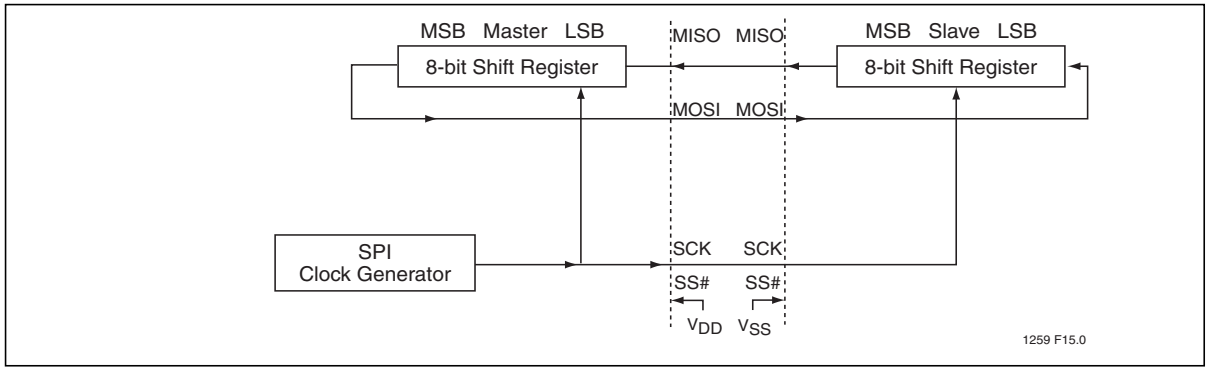

Figure 13: SPI Master-slave Interconnection

SPI Transfer Formats

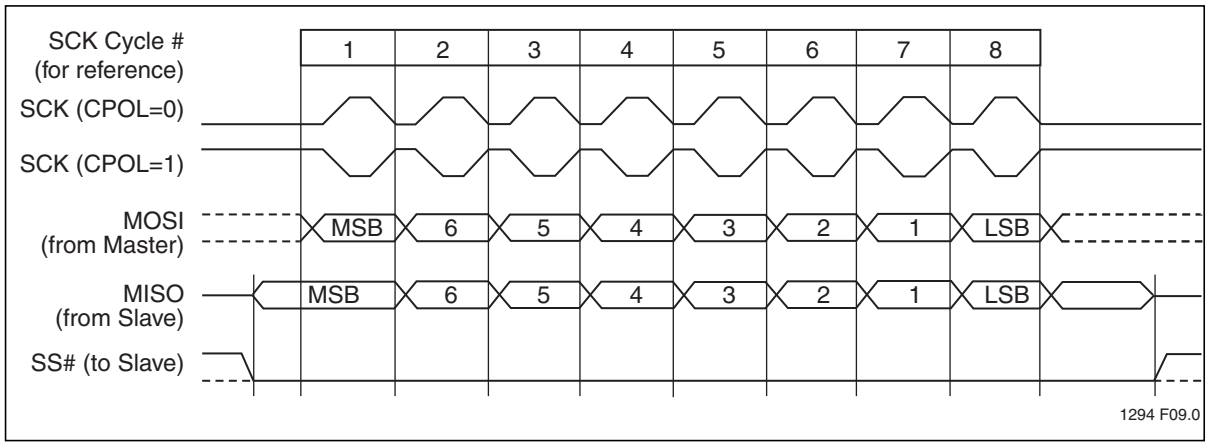

Figure 14: SPI Transfer Format with CPHA = 0

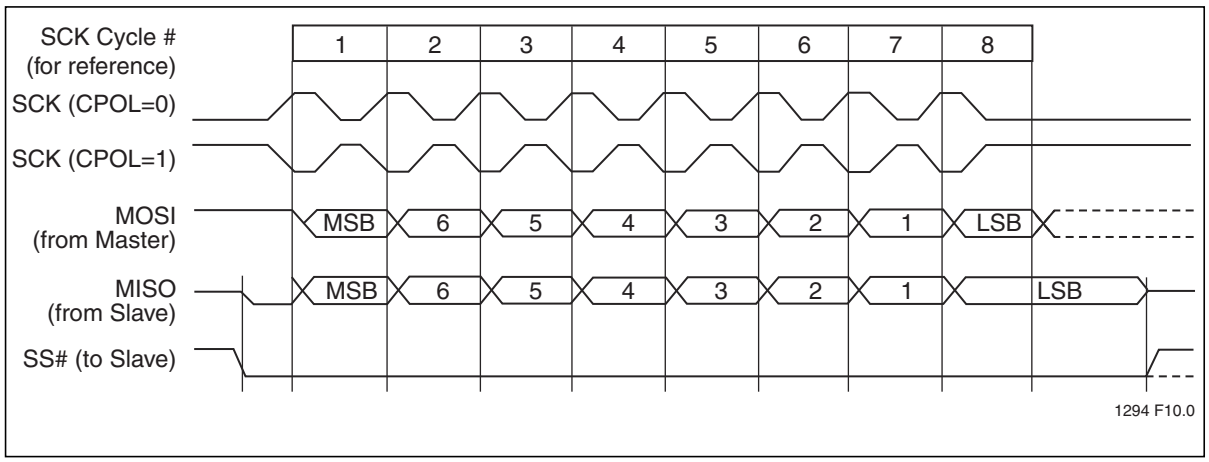

Figure 15: SPI Transfer Format with CPHA = 1

I²C Serial Communication (SIO1)

Introduction

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Bi-directional data transfer between masters and slaves
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C bus may be used for test and diagnostic purposes

A typical I²C bus configuration is shown in Figure 6.7 and Figure 6.8 shows how data transfer is accomplished on the bus.

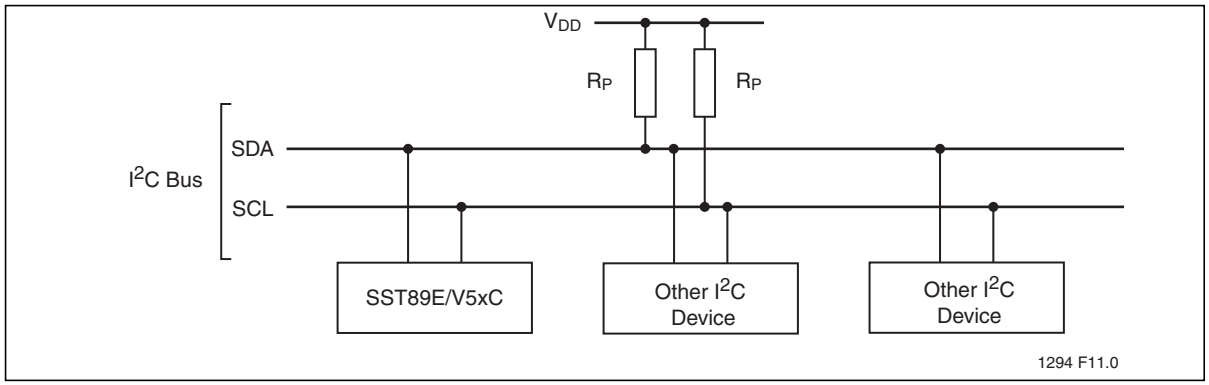

Figure 16: Typical I²C Bus Configuration

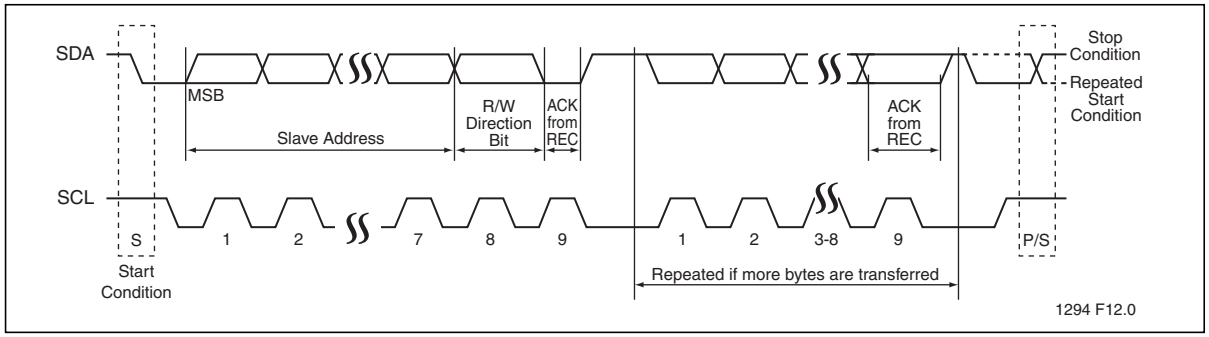

Figure 17: Data Transfer on the I²C Bus

Modes of Operation

The on-chip I^2C logic provides a serial interface that meets the I^2C bus specs and supports all transfer modes, except low speed mode, from and to the I^2C bus. The SIO1 logic may operate in the follow for modes.

Master Transmitter Mode

The serial data output through P1.7/SDA1 while P1.6/SCL1 supplies the serial clock. The first transmitted byte contains the slave address of the receiving device (7 bits) and the data direction bit. In this mode, the data direction bit (R/W) will be logic 0, and we say that a 'W' is transmitted. Thus, the first byte transmitted is SLA+W. Send data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

Master Receiver Mode

The first transmitted byte contains the slave address of the transmitting device (7 bits) and the data direction bit. In this mode, the data direction bit (R/W) will be logic 1, and we say that an "R" is transmitted. Thus, the first byte transmitted is SLA+R. Serial data is received via P1.7/SDA1 while P1.6/SCL1 outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

Slave Receiver Mode

Serial data and the serial clock are received through P1.7/SDA1 and P1.6/SCL1. After each byte is received, and acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

Slave Transmitter Mode

The first byte is received and handled as in the Slave Receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via P1.7/SDA1 while the serial clock is input through P1.6/SCL1. START and STOP conditions are recognized as the beginning and end of a serial transfer.

In a given application, SIO1 may operate as a master and as a slave. In the Slave mode, the SIO1 hardware looks for its own slave address and the general call address. If one of these addresses is detected, an interrupt is requested. When the microcontroller wishes to become the bus master, the hardware waits until the bus is free before the Master mode is entered so that a possible slave action is not interrupted. If bus arbitration is lost in the Master mode, SIO1 switches to the Slave mode immediately and can detect its own slave address in the same serial transfer.

SIO1 Implementation and Operation

Figure 6.9 shows how the on-chip I^2C bus interface is implemented. Details can be seen in Appendix A.

I²C Interfaces

This device will include two I²C interfaces. Both interfaces will be identical except for the SFR addresses and I/O pins associated with each interface.

Primary I²C Interface

The primary I²C interface will use the S1 register sets (S1CON). These register addresses are identical to that used in Philips byte-wide two wire devices including the P89C66x series.The primary I²C interface will use open drain port pins P1.6 and P1.7 for SCL1 and SDA1, respectively.

Secondary I²C Interface

The secondary I²C interface will use the S2 register sets (S2CON). The secondary I²C interface will use standard quasi bi-directional port pins P4.0 and P4.1 for SCL2 and SDA2, respectively. The secondary I²C interface will have its enable bit, ES2, located in IEN1.1. Its priority will be controlled by bits PS2 and PS2H in locations IP1.0 and IP1H.0, respectively.

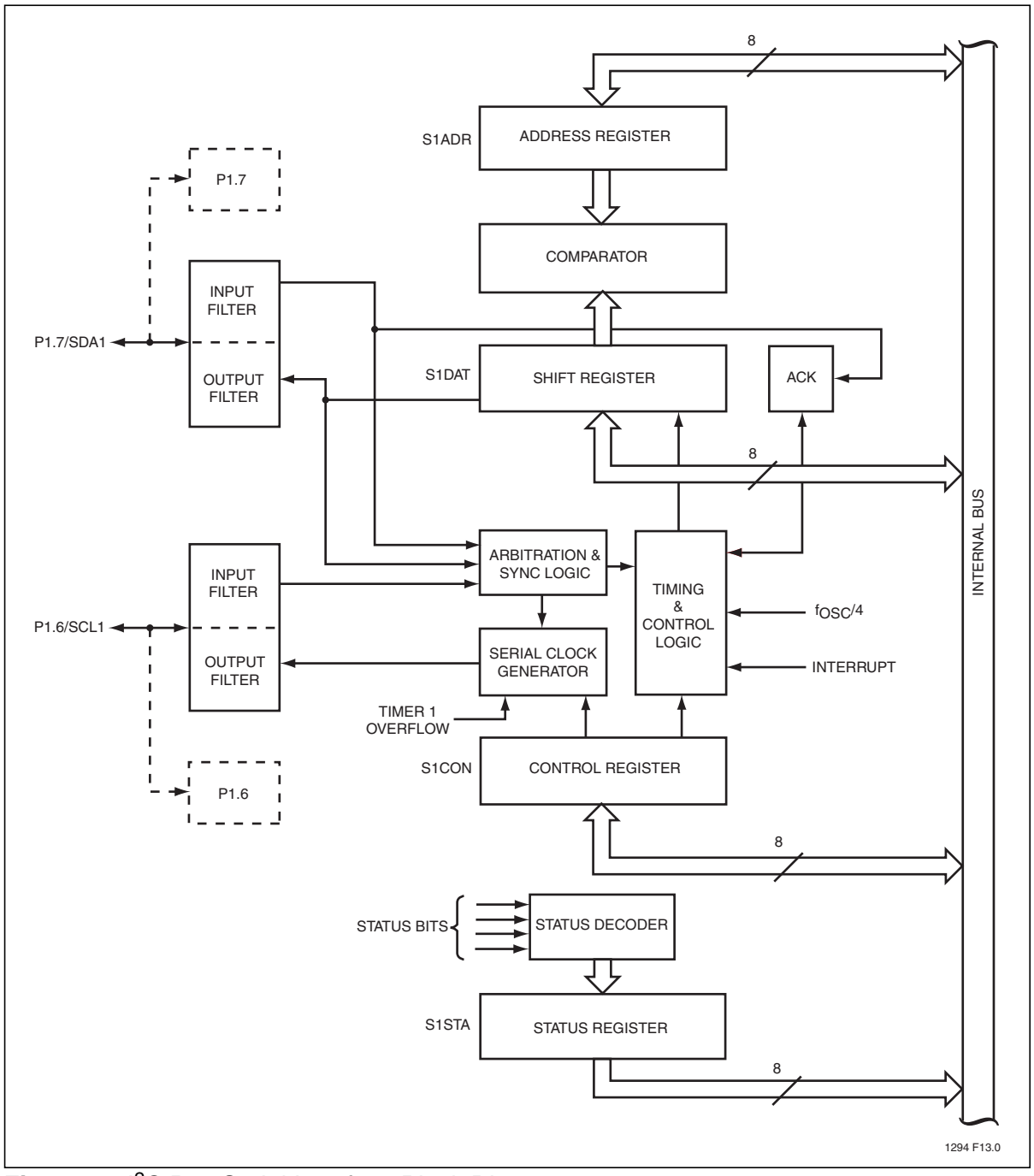

Figure 18: I^2C Bus Serial Interface Block Diagram

Watchdog timer

Hardware Watchdog Timer

The WDT is intended as a recovery method in situations when the CPU encounters software errors. The WDT consists of a 14-bit counter and the write-only WatchDog Timer reset (WDTRST) SFR.

After hardware reset, the WDT is disabled. To enable it, commands must be written to the WDTRST SFR. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. There is no way to disable the WDT except though hardware reset.

Using the WDT

The WDT is enabled or serviced by writing 01EH and 0E1H, in sequence, to the WDTRST (SFR location 0A6H). Once enabled, the WDT counter will increment every machine cycle while the oscillator is running. The 14-bit counter value cannot be read or written. The counter overflows when it reaches 16383 (3FFFH) and then it drives an output reset HIGH pulse at the RST pin. The RESET pulse duration is 98 x T_{OSC} (6 clock mode; 196 in 12 clock mode), where $T_{OSC} = 1/f_{OSC}$.

To make the best use of the WDT, it should be serviced in those sections of code that will be periodically executed within the time required to prevent a WDT overflow.

Note: The WDT counter will be on hold while IAP commands are executed.

Programmable Counter Array

The Programmable Counter Array (PCA) is a special 16-bit timer that has five 16-bit capture/compare modules. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. The 5th module can be programmed as a Watchdog timer in addition to the other four modes. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1[4] (CEX1), module 2 to P1[5] (CEX2), module 3 to P3[4] (CEX3), and module 4 to P3[5] (CEX4). PCA configuration is shown in Figure 19.

PCA Overview

PCA provides more timing capabilities with less CPU intervention than the standard timer/counter. Its advantages include reduced software overhead and improved accuracy.

The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/capture modules. Figure 19 shows a block diagram of the PCA. External events associated with modules are shared with corresponding Port 1 pins. Modules not using the port pins can still be used for standard I/O.

Each of the five modules can be programmed in any of the following modes:

- Rising and/or falling edge capture
- Software timer
- High speed output
- Watchdog timer (Module 4 only)
- Pulse Width Modulator (PWM)

PCA Timer/Counter

The PCA timer is a free-running 16-bit timer consisting of registers CH and CL (the high and low bytes of the count values). The PCA timer is common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, Timer 0 overflow, or the input on the ECI pin (P1.2). The timer/counter source is determined from the CPS1 and CPS0 bits in the CMOD SFR as shown in Table 16. See also “PCA Timer/Counter Mode Register (CMOD)” on page 25.

Table 16: PCA Timer/Counter Source

CPS1	CPS0	12 Clock Mode	6 Clock Mode
0	0	f_{OSC} /12	f_{OSC} /6
0	1	f_{OSC} /4	f_{OSC} /2
1	0	Timer 0 overflow	Timer 0 overflow
1	1	External clock at ECI pin (maximum rate = f_{OSC} /8)	External clock at ECI pin (maximum rate = f_{OSC} /4)

T16.0 25096

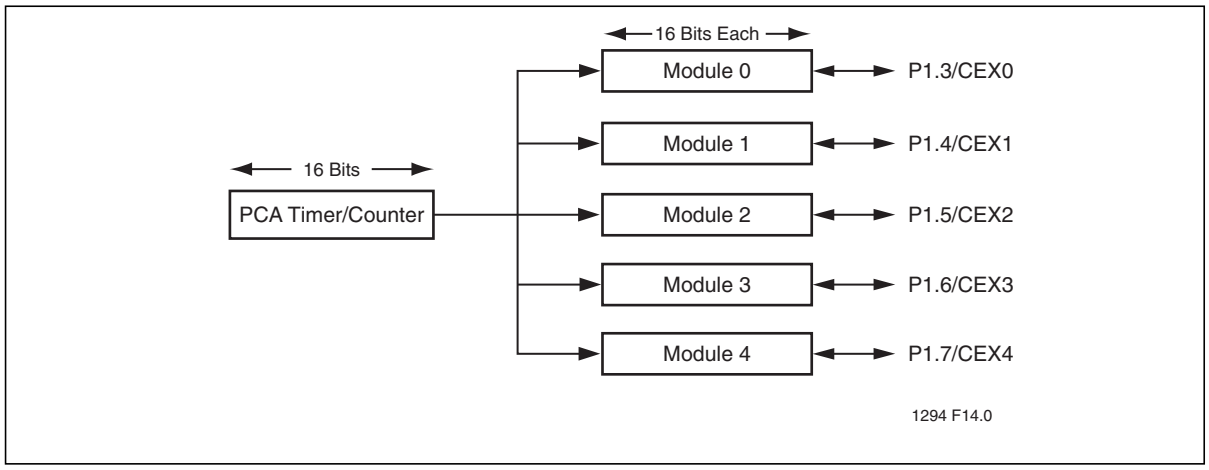

Figure 19: PCA Timer/Counter and Compare/Capture Modules

The table below summarizes various clock inputs at two common frequencies.

Table 17: PCA Timer/Counter Inputs

PCA Timer/Counter Mode	Clock Increments	
	12 MHz	16 MHz
Mode 0: $f_{OSC}/12$	1 µsec	0.75 µsec
Mode 1:	330 nsec	250 nsec
Mode 2: Timer 0 Overflows[1]		
Timer 0 programmed in:		
8-bit mode	256 µsec	192 µsec
16-bit mode	65 msec	49 µsec
8-bit auto-reload	1 to 255 µsec	0.75 to 191 µsec
Mode 3: External Input MAX	0.66 µsec	0.50 µsec

T17.0 25096

1. In Mode 2, the overflow interrupt for Timer 0 does not need to be enabled.

CMOD's four possible timer modes with and without the overflow interrupt enabled are shown below. This list assumes that PCA will be left running during idle mode.

Table 18: CMOD Values

PCA Count Pulse Selected	CMOD Value	
	Without Interrupt Enabled	With Interrupt Enabled
Internal clock, $f_{OSC}/12$	00H	01H
Internal clock, $f_{OSC}/4$	02H	03H
Timer 0 overflow	04H	05H
External clock at P1.2	06H	07H

T18.0 25096

The CCON register is associated with all PCA timer functions. It contains run control bits and flags for the PCA timer (CF) and all modules. To run the PCA the CR bit (CCON.6) must be set by software. Clearing the bit, will turn off PCA. When the PCA counter overflows, the CF (CCON.7) will be set, and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Each module has its own timer interrupt or capture interrupt flag (CCF0 for module 0, CCF4 for module 4, etc.). They are set when either a match or capture occurs. These flags can only be cleared by software. See “PCA Timer/Counter Control Register (CCON)” on page 24.

Compare/Capture Modules

Each PCA module has an associated SFR with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. Refer to “PCA Compare/Capture Module Mode Register (CCAPMn)” on page 26 for details. The registers each contain 7 bits which are used to control the mode each module will operate in. The ECCF bit (CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on module) will enable the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set, causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module’s capture/compare register. When there is a match between the PCA counter and the module’s capture/compare register, the MATn (CCAPMn.3) and the CCFn bit in the CCON register to be set.

Bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine whether the capture input will be active on a positive edge or negative edge. The CAPN bit enables the negative edge that a capture input will be active on, and the CAPP bit enables the positive edge. When both bits are set, both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set, enables the comparator function. Table 20 shows the CCAPMn settings for the various PCA functions.

There are two additional register associated with each of the PCA modules: CCAPnH and CCAPnL. They are registers that hold the 16-bit count value when a capture occurs or a compare occurs. When a module is used in PWM mode, these registers are used to control the duty cycle of the output. See Figure 19.

Table 19: PCA High and Low Register Compare/Capture Modules

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB	RESET Value
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]	00H
CCAP0L		EAH	CCAP0L[7:0]	00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]	00H
CCAP1L		EBH	CCAP1L[7:0]	00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]	00H
CCAP2L		ECH	CCAP2L[7:0]	00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]	00H
CCAP3L		EDH	CCAP3L[7:0]	00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]	00H
CCAP4L		EEH	CCAP4L[7:0]	00H

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Table 20: PCA Module Modes

Without Interrupt enabled								
-[1]	ECOMy[2]	CAPPy[2]	CAPNy[2]	MATy[2]	TOGy[2]	PWMy[2]	ECCFy[2]	Module Code
-	0	0	0	0	0	0	0	No Operation
-	0	1	0	0	0	0	0	16-bit capture on positive-edge trigger at CEX[4:0]
-	0	0	1	0	0	0	0	16-bit capture on negative-edge trigger at CEX[4:0]
-	0	1	1	0	0	0	0	16-bit capture on positive/negative-edge trigger at CEX[4:0]
-	1	0	0	1	0	0	0	Compare: software timer
-	1	0	0	1	1	0	0	Compare: high-speed output
-	1	0	0	0	0	1	0	Compare: 8-bit PWM
-	1	0	0	1	0 or 1[3]	0	0	Compare: PCA WDT (CCAPM4 only)[4]

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1. User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
2. y = 0, 1, 2, 3, 4
3. A 0 disables toggle function. A 1 enables toggle function on CEX[4:0] pin.
4. For PCA WDT mode, also set the WDTE bit in the CMOD register to enable the reset output signal.

Table 21: PCA Module Modes

With Interrupt enabled								
-[1]	ECOMy[2]	CAPPy[2]	CAPNy[2]	MATy[2]	TOGy[2]	PWMy[2]	ECCFy[2]	Module Code
-	0	1	0	0	0	0	1	16-bit capture on positive-edge trigger at CEX[4:0]
-	0	0	1	0	0	0	1	16-bit capture on negative-edge trigger at CEX[4:0]
-	0	1	1	0	0	0	1	16-bit capture on positive/negative-edge trigger at CEX[4:0]
-	1	0	0	1	0	0	1	Compare: software timer
-	1	0	0	1	1	0	1	Compare: high-speed output
-	1	0	0	0	0	1	X[3]	Compare: 8-bit PWM
-	1	0	0	1	0 or 1[4]	0	X[5]	Compare: PCA WDT (CCAPM4 only)[6]

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1. User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
2. y = 0, 1, 2, 3, 4
3. No PCA interrupt is needed to generate the PWM.
4. A 0 disables toggle function. A 1 enables toggle function on CEX[4:0] pin.
5. Enabling an interrupt for the Watchdog timer would defeat the purpose of the Watchdog timer.
6. For PCA WDT mode, also set the WDTE bit in the CMOD register to enable the reset output signal.

Capture Mode

Capture mode is used to capture the PCA timer/counter value into a module's capture registers (CCAPnH and CCAPnL). The capture will occur on a positive edge, negative edge, or both on the corresponding module's pin. To use one of the PCA modules in the capture mode, either one or both the CCAPM bits CAPN and CAPP for that module must be set. When a valid transition occurs on the CEX pin corresponding to the module used, the PCA hardware loads the 16-bit value of the PCA counter register (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set, then an interrupt will be generated. In the interrupt service routine, the 16-bit capture value must be saved in RAM before the next event capture occurs. If a subsequent capture occurred, the original capture values would be lost. After flag event flag has been set by hardware, the user must clear the flag in software. See Figure 20.

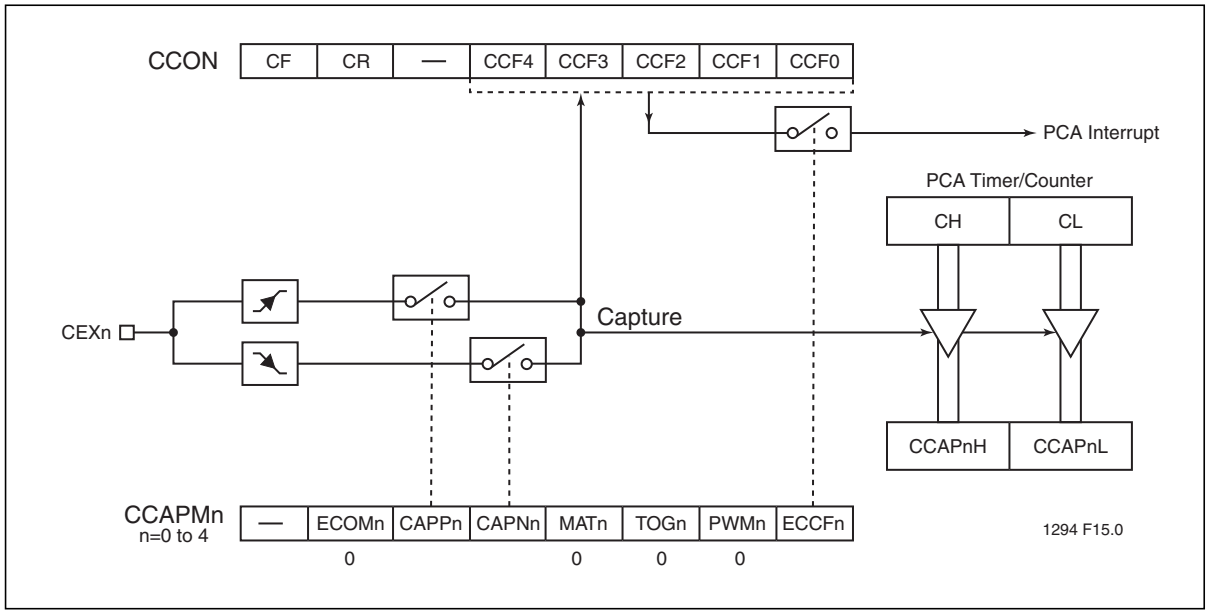

Figure 20: PCA Capture Mode

16-Bit Software Timer Mode

The 16-bit software timer mode is used to trigger interrupt routines, which must occur at periodic intervals. It is setup by setting both the ECOM and MAT bits in the module's CCAPMn register. The PCA timer will be compared to the module's capture registers (CCAPnL and CCAPnH) and when a match occurs, an interrupt will occur, if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

If necessary, a new 16-bit compare value can be loaded into CCAPnH and CCAPnL during the interrupt routine. The user should be aware that the hardware temporarily disables the comparator function while these registers are being updated so that an invalid match will not occur. Thus, it is recommended that the user write to the low byte first (CCAPnL) to disable the comparator, then write to the high byte (CCAPnH) to re-enable it. If any updates to the registers are done, the user may want to hold off any interrupts from occurring by clearing the EA# bit. See Figure 21.

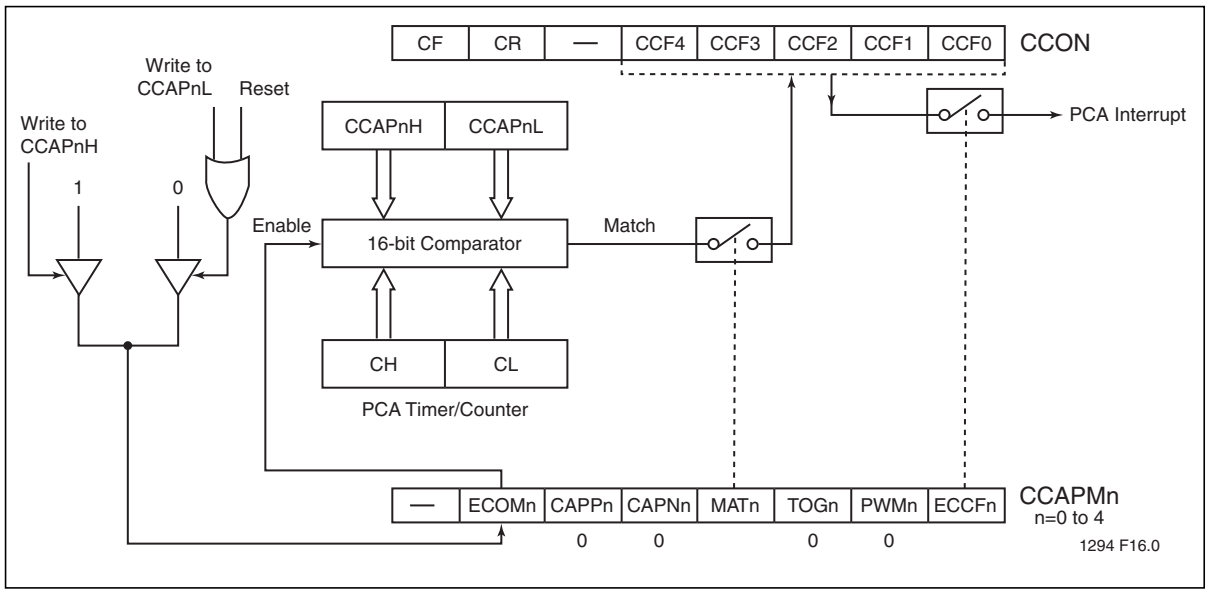

Figure 21: PCA Compare Mode (Software Timer)

High Speed Output Mode

The high speed output mode is used to toggle a port pin when a match occurs between the PCA timer and the preloaded value in the compare registers. In this mode, the CEX output pin (on port 1) associated with the PCA module will toggle every time there is a match between the PCA counter (CH and CL) and the capture registers (CCAPnH and CCAPnL). To activate this mode, the user must set TOG, MAT, and ECOM bits in the module's CCAPMn SFR.

High speed output mode is much more accurate than toggling pins since the toggle occurs before branching to an interrupt. In this case, interrupt latency will not affect the accuracy of the output. When using high speed output, using an interrupt is optional. Only if the user wishes to change the time for the next toggle is it necessary to update the compare registers. Otherwise, the next toggle will occur when the PCA timer rolls over and matches the last compare value. See Figure 22.

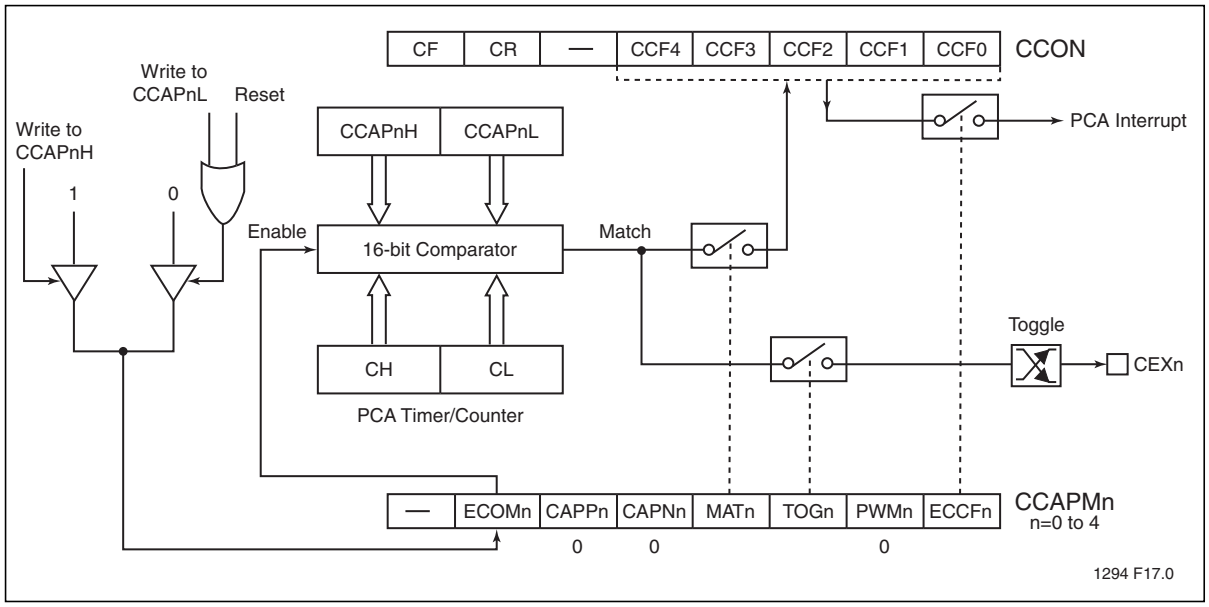

Figure 22: PCA High Speed Output Mode

Pulse Width Modulator

The Pulse Width Modulator (PWM) mode is used to generate 8-bit PWMs by comparing the low byte of the PCA timer (CL) with the low byte of the compare register (CCAPnL). When CL < CCAPnL the output is low. When CL ≥ CCAPnL the output is high. To activate this mode, the user must set the PWM and ECOM bits in the module's CCAPMn SFR. See Figure 23 and Table 22.

In PWM mode, the frequency of the output depends on the source for the PCA timer. Since there is only one set of CH and CL registers, all modules share the PCA timer and frequency. Duty cycle of the output is controlled by the value loaded into the high byte (CCAPnH). Since writes to the CCAPnH register are asynchronous, a new value written to the high byte will not be shifted into CCAPnL for comparison until the next period of the output (when CL rolls over from 255 to 00).

To calculate values for CCAPnH for any duty cycle, use the following equation:

CCAPnH = 256(1 - Duty Cycle)

where CCAPnH is an 8-bit integer and Duty Cycle is a fraction.

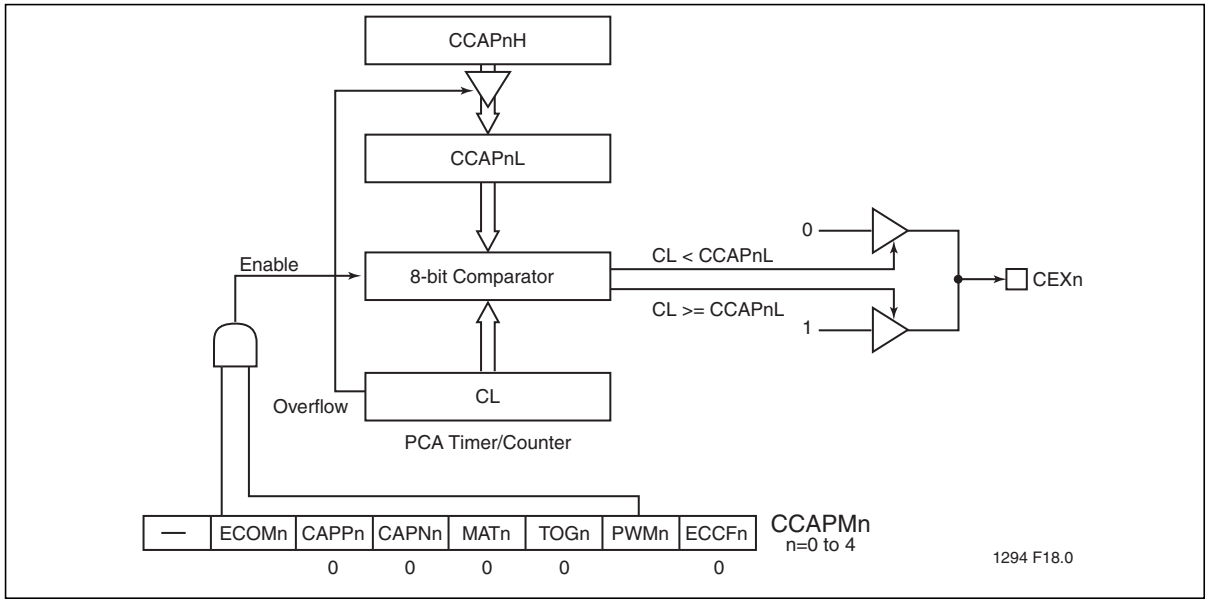

Figure 23: PCA Pulse Width Modulator Mode

Table 22: Pulse Width Modulator Frequencies

PCA Timer Mode	PWM Frequency	
	12 MHz	**16 MHz**
1/12 Oscillator Frequency	3.9 KHz	5.2 KHz
1/4 Oscillator Frequency	11.8 KHz	15.6 KHz
Timer 0 Overflow:		
8-bit	15.5 Hz	20.3 Hz
16-bit	0.06 Hz	0.08 Hz
8-bit Auto-Reload	3.9 KHz to 15.3 Hz	5.2 KHz to 20.3 Hz
External Input (Max)	5.9 KHz	7.8 KHz

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Watchdog Timer

The Watchdog Timer mode is used to improve reliability in the system without increasing chip count (See Figure 24). Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. It can also be used to prevent a software deadlock. If during the execution of the user's code, there is a deadlock, the Watchdog timer will time out and an internal reset will occur. Only module 4 can be programmed as a Watchdog timer (but still can be programmed to other modes if the Watchdog timer is not used).

To use the Watchdog timer, the user pre-loads a 16-bit value in the compare register. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the Watchdog timer by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the Watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most application the first solution is the best option.

Use the code below to initialize the Watchdog timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the Watchdog routine below.

```
;===========================================
Init_Watchdog:
    MOVCCAPM4, #4CH; Module 4 in compare mode
    MOVCCAP4L, #0FFH; Write to low byte first
    MOVCCAP4H, #0FFH; Before PCA timer counts up
            ; to FFFF Hex, these compare
            ; values must be changed.
    ORLCMOD, #40H; Set the WDTE bit to enable the
            ; watchdog timer without
            ; changing the other bits in
            ; CMOD
;===========================================
;Main program goes here, but call WATCHDOG periodically.
;===========================================
WATCHDOG:
    CLR EA; Hold off interrupts
    MOVCCAP4L, #00; Next compare value is within
    MOVCCAP4H, CH; 65,535 counts of the
            ; current PCA
    SETBEA; timer value
    RET
;===========================================
```

This routine should not be part of an interrupt service routine. If the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program of the PCA timer.

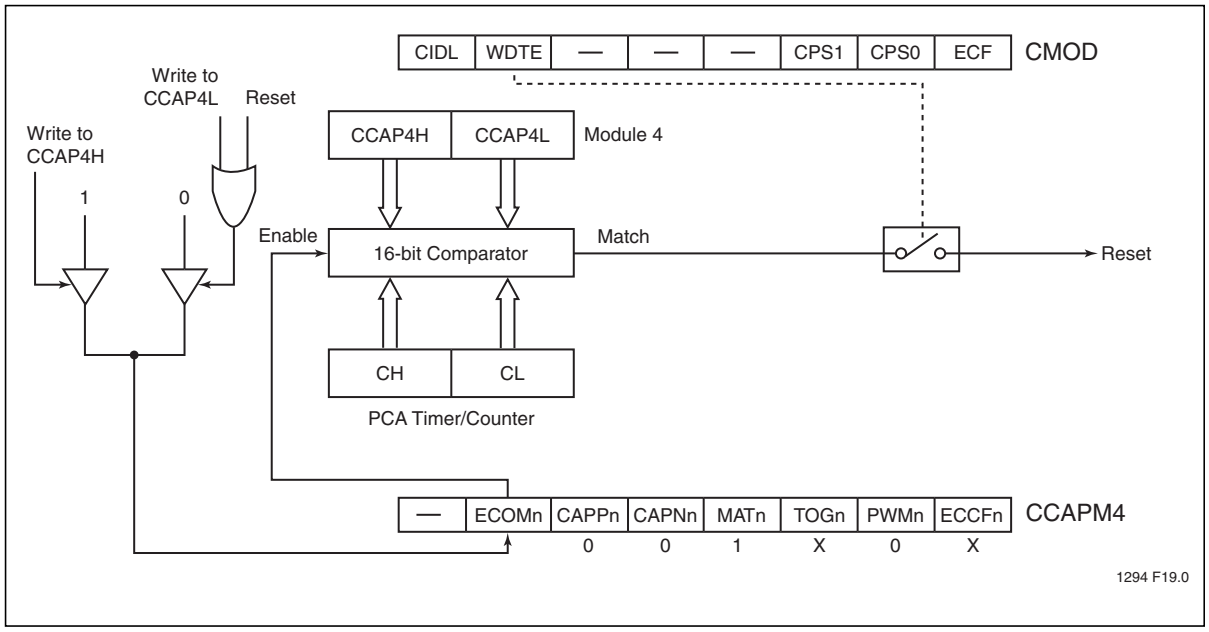

Figure 24: PCA Watchdog Timer (Module 4 only)

Security Lock

Chip-Level Security Lock

The SSTE/V895xC use three flash bits for security setting and each bit actually acts independently.

Security Bit	Protection Scheme
LB1	All the External Host mode commands are disabled except Read-ID, Byte-Verify, Partition0-Erase, Chip-Erase, Partition Selection, and security bit programming commands
LB2	Verify memory is disabled in External Host mode
LB3	External execution is disabled

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Default Security

MOVC command is always disabled if it is executed from External Code Memory and Targeting Internal Code Memory without any LB programmed. If one byte of the MOVC instruction resides in external memory, this command will also be disabled. The READ BACK value is 00H if this command is blocked.

Security Bit 1 (LB1)

If the NVR bit LB1 has been programmed, only Read-ID, Verify, Partition Selection, Partition0-Erase, Chip-Erase and security bit programming commands are allowed in the External Host mode (parallel programming mode). For the IAP/ISP mode, the hardware only needs to provide the LB bits status and let the firmware control it.

Security Bit 2 (LB2)

If the NVR bit LB2 has been programmed, the flash code memory verify command will be disabled in the External Host mode (parallel programming mode). Any attempt to read the user code in the External Host mode will return a value of 55H. For the IAP/ISP mode, the hardware will only need to provide the LB bits status and let the firmware control it. Once this bit is set, the E-Hook will be disabled.

Security Bit 3 (LB3)

If the NVR bit LB3 has been programmed, the MCU will ignore the EA# pin and fetch the code from internal flash memory. All code fetched from external code memory (SST89E54C/58C/516C) will become 00H (NOP command).

EA# Pin Security

The EA# pin value is latched at the falling edge of the external reset. See Figure 25.

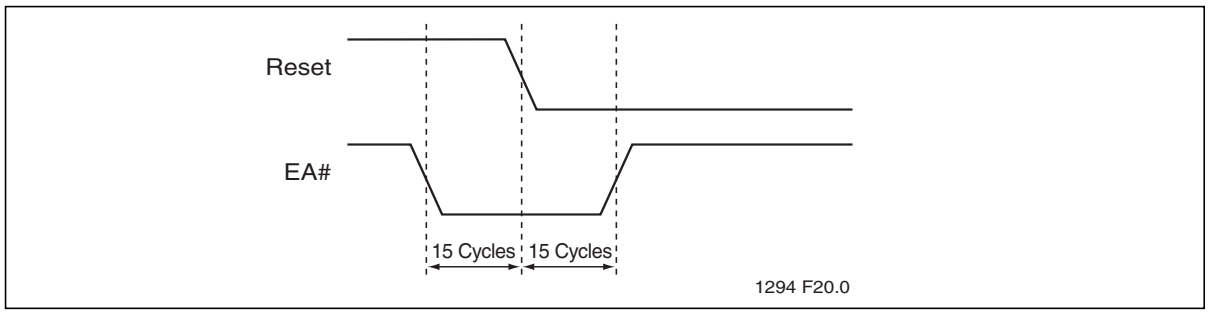

Figure 25: Latching the EA# Pin

Reset Mode

Reset

A system reset initializes the MCU and begins program execution at program memory location 0000H or the boot vector address. The reset input for the device is the RST pin. In order to reset the device (See Figure 26), a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE and PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform a proper reset. This level must not be affected by external element. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power up are indeterminate. Following reset, all Special Function Registers (SFR) return to their reset values outlined in Tables 4 to 9.

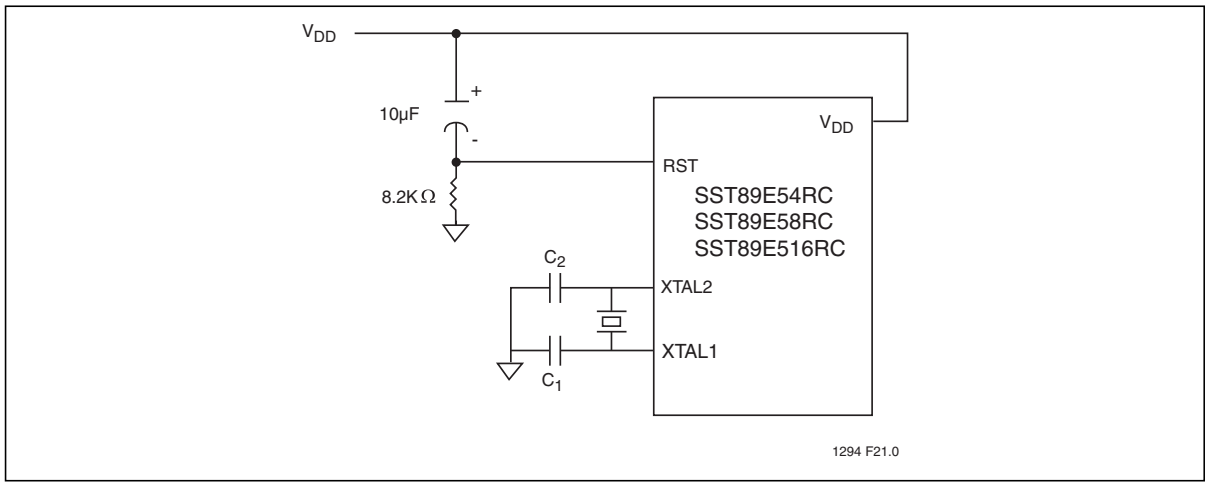

Figure 26: Power-on Reset Circuit

Boot Sequence

Normal Mode

After Power-on, the hardware checks the Status byte. (See Figure 27) If the Status byte is programmed, the value of the boot vector is used as the high byte of the program counter (PC) starting address, the lower byte of PC will be 00H. if the Status Byte is un-programmed, the PC will start from address 0. The boot vector factory default setting is FCH and the status byte factory default setting is programmed.

Hardware Enter Mode

The user can hold PSEN# low, ALE and EA# high at the falling edge of reset. This is the same effect as having a programmed NVR Status byte.

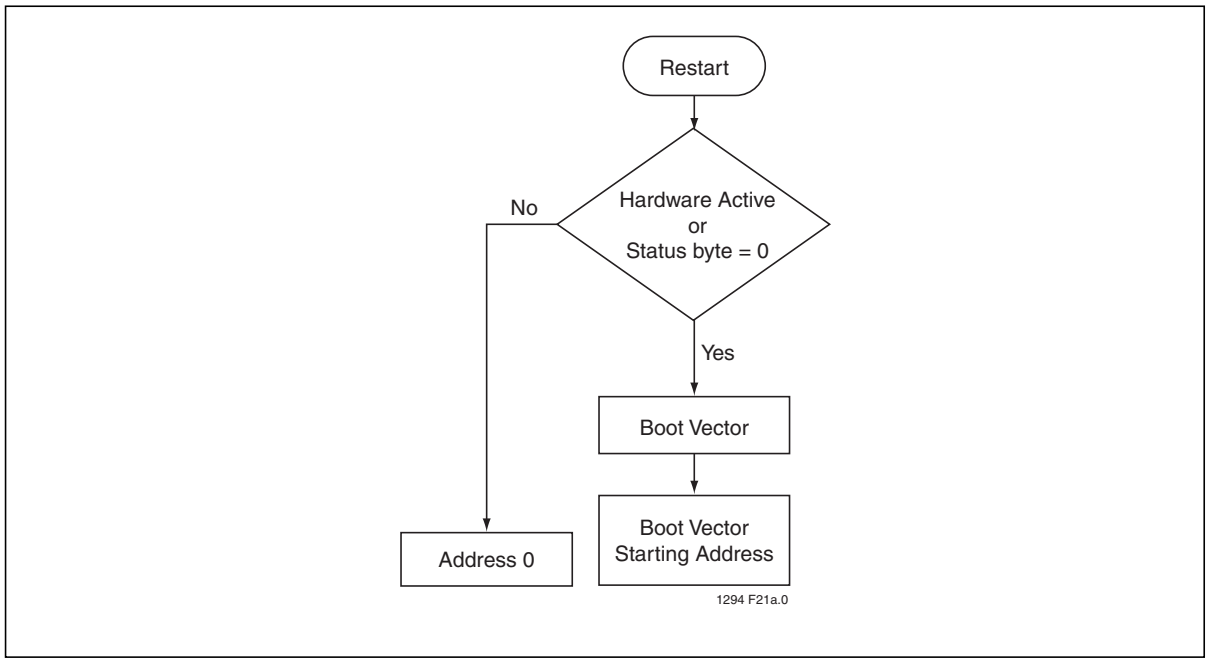

Figure 27: Boot Sequence Flow Chart

Interrupt Priority and Polling Sequence

The device supports eight interrupt sources under four-level priority scheme. Table 23 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector. See Figure 28.

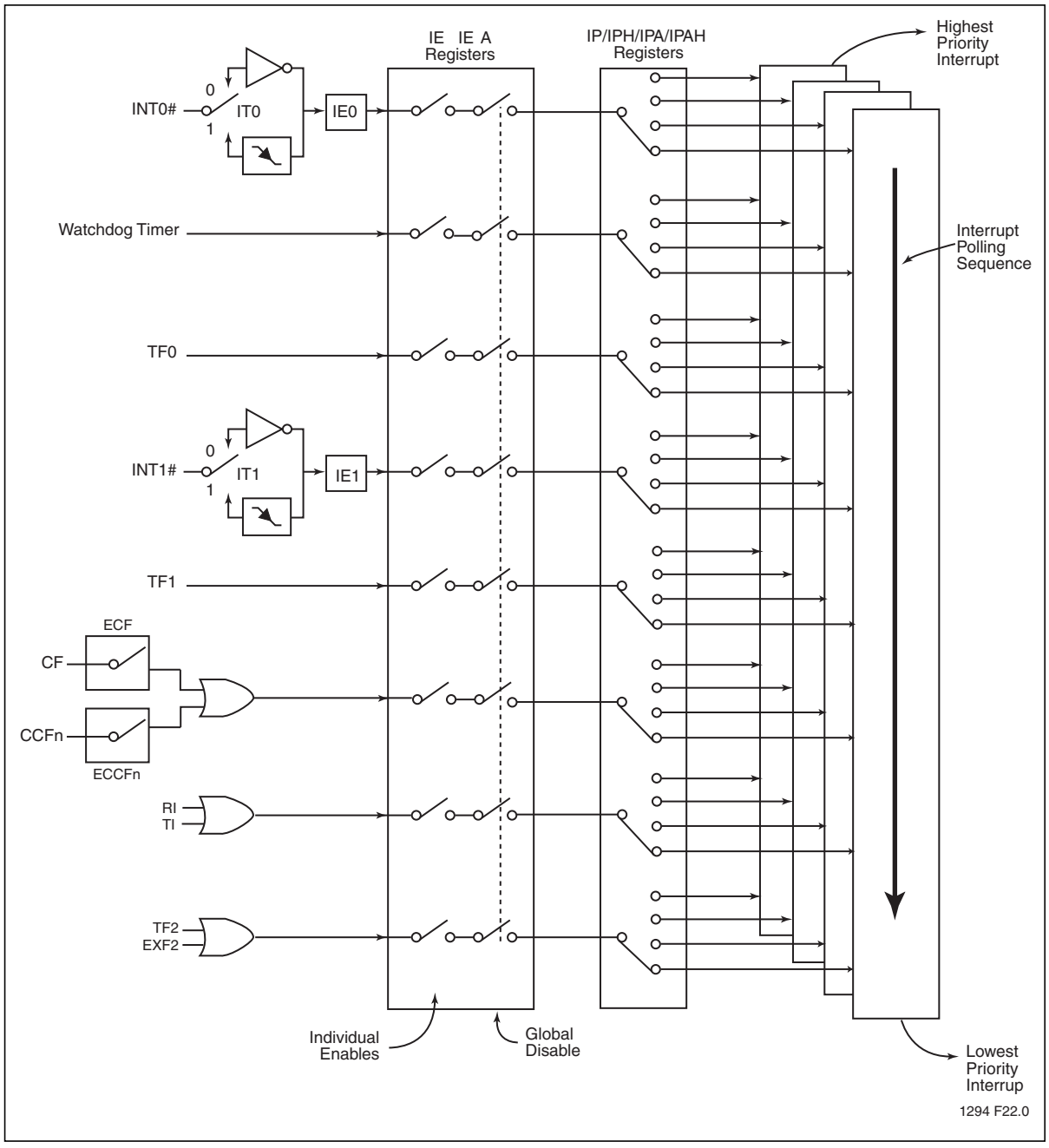

Figure 28: Interrupt Sequence

Table 23: Interrupt Table

Description	Interrupt Flag	Vector Address	Interrupt Enable	Interrupt Priority	Service Priority	Wake-Up Power-down
Ext. Int0	IE0	0003H	EX0	PX0/H	1(highest)	yes
I^2C 1 Vector	S1_1	002BH	ES1	PS1/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
Ext. Int1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
UART	TI/RI	0023H	ES	PS/H	6	no
T2	TF2, EXF2	003BH	ET2	PT2/H	7	no
PCA	CF/CCFn	0033H	EC	PPC/H	8	no
SPI Interrupt Vector	SPIF	004BH	ES3	PS3/H	9	no
I^2C 2 Vector	S1_2	0043H	ES2	PS2/H	10	no

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Power-Saving Modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and power-down, see Table 24.

Idle Mode

Idle mode is entered setting the IDL bit in the PCON register. In idle mode, the program counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits idle mode through either a system interrupt or a hardware reset. Exiting idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the idle mode. A hardware reset starts the device similar to a power-on reset.

Power-down Mode

The power-down mode is entered by setting the PD bit in the PCON register. In the power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 4.5V.

The device exits power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal restored to logic $V_{IH,}$ the interrupt service routine program execution resumes beginning at the instruction immediately following the instruction which invoked power-down mode. A hardware reset starts the device similar to power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

Table 24: Power Saving Modes

Mode	Initiated by	State of MCU	Exited by
Idle	Software (Set IDL bit in PCON) MOV PCON, #01H;	• CLK is running. • Interrupts, serial port and timers/counters are active. • Program Counter is stopped. • ALE and PSEN# signals at a HIGH level during Idle. • All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked idle mode. A user could consider placing two or three NOP instructions after the instruction that invokes idle mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Power-down	Software (Set PD bit in PCON) MOV PCON, #02H;	• CLK is stopped. • On-chip SRAM and SFR data is maintained. • ALE and PSEN# signals at a LOW level during power - down. • External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked power-down mode. A user could consider placing two or three NOP instructions after the instruction that invokes power-down mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.

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System Clock and Clock Options

Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 29 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 25, shows the typical values for C1 and C2 vs. crystal type for various frequencies

Table 25: Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

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More specific information about on-chip oscillator design can be found in the **FlashFlex Oscillator Circuit Design Considerations** application note.

Clock Halving Option

By default, the device runs at 6 clocks per machine cycle (x1 mode). The device has a clock halving option to reduce speed to 12 clocks per machine cycle. Please refer to Table 26 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 11 for the IAP mode enabling command (When set, the Enable-Clock-Double_i bit in the SFST register will indicate 6-clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

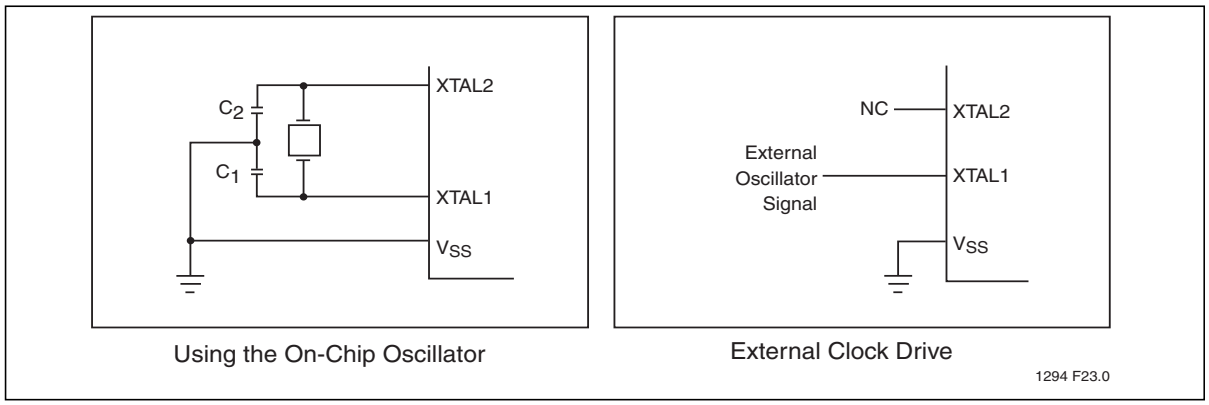

Figure 29: Oscillator Characteristics

Table 26: Clock Halving Features

Device	Standard Mode (x1)		Clock Half Mode (x2)	
	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)
SST89E5xC	6	20	12	40

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Electrical Specification

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature. . . . . -65°C to +150°C
Voltage on EA# Pin to V_{SS}. . . . . -0.5V to +14.0V
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} . . . . . -1.0V to V_{DD}+1.0V
Maximum I_{OL} per I/O for All Other Pins 15mA
Package Power Dissipation Capability (T_A = 25°C). 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature[1] . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

(Based on package heat transfer limitations, not device power consumption.

Note: This specification contains preliminary information on new products in production. The specifications are subject to change without notice.

Table 27: Operating Range

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V_{DD}	Supply Voltage			
	SST89E5xC	4.5	5.5	V
f_{OSC}	Oscillator Frequency			
	SST89E5xC	0	40	MHz
	Oscillator Frequency for In-Application programming			
	SST89E5xC	.25	40	MHz

T27.1 25096

Table 28: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T28.0 25096

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 29: AC Conditions of Test[1]

Input Rise/Fall Time	Output Load
10 ns	C_L = 100 pF

T29.1 25096

1. See Figures 36 and 38

Table 30: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T30.2 25096

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

Table 31: Pin Impedance (VDD=3.3V, TA=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF
L_{PIN}[2]	Pin Inductance		20 nH

T31.4 25096

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI spec.

DC Electrical Characteristics

Table 32: DC Characteristics for SST89E5xC: T_A = -40°C to +85°C; V_{DD} = 4.5-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	4.5 < V_{DD} < 5.5	-0.5	0.2V_{DD} - 0.1	V
V_{IH}	Input High Voltage	4.5 < V_{DD} < 5.5	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	4.5 < V_{DD} < 5.5	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 4.5V I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 4.5V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 4.5V I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 4.5V I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{Li}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
I_{L2}	Input leakage current, P1.6/SCL1, P41.7SDA1	0V < VI < 6V 0V < V_{DD} < 5.5v		10	µA
R_{RST}	RST Pull-down Resistor		40	225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current				
	IAP Mode @ 40 MHz			88	mA
	Active Mode @ 40 MHz			50	mA
	Idle Mode@ 40 MHz			42	mA
	Power-down Mode (min. V_{DD} = 4.5V)	T_A = 0°C to +70°C		80	µA
		T_A = -40°C to +85°C		90	µA

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1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port:26mA
   Maximum I_{OL} total for all outputs:71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE and PSEN#= 100pF, load capacitance for all other outputs = 80 pF.
4. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
5. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. Pin capacitance is characterized but not tested. EA# is 25pF (max).

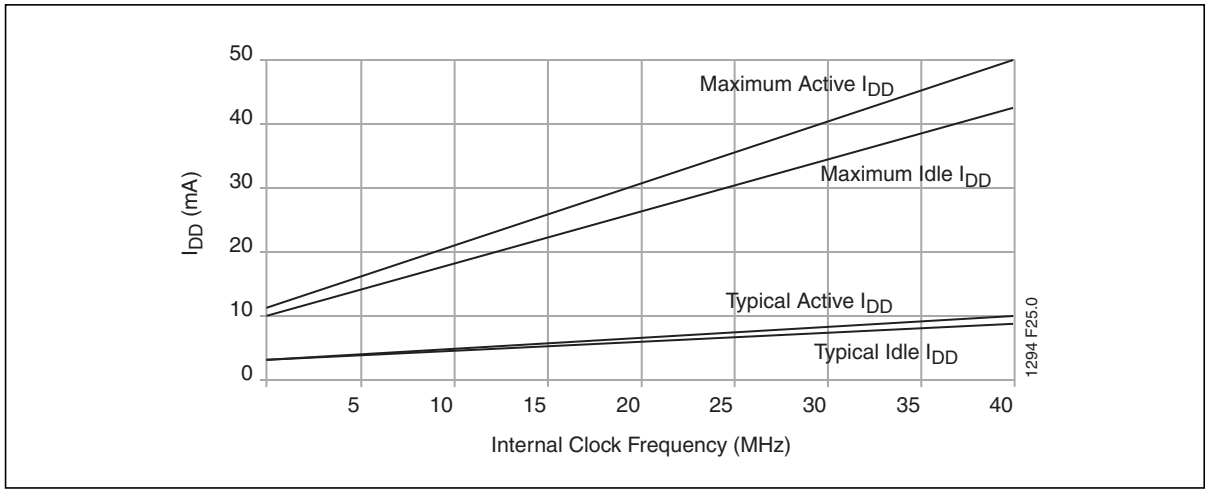

Figure 30: I_{DD} vs. Frequency (SST89E5xC)

AC Electrical Characteristics

AC Characteristics:

(Over Operating Conditions: Load Capacitance for Port 0, ALE, and PSEN# = 100pF; Load Capacitance for All Other Outputs = 80pF)

Table 33: AC Electrical Characteristics T_A = -40°C to +85°C, 4.5-5.5V@40MHz, V_{SS} = 0V

		Oscillator				
		40 MHz (x1 Mode) 20 MHz (x2 Mode)[1]		Variable		Units
Symbol	Parameter	Min	Max	Min	Max	
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	40	0	40	MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	20	0	20	MHz
T_{LHLL}	ALE Pulse Width	35		$2T_{CLCL}$ - 15		ns
T_{AVLL}	Address Valid to ALE Low	10		T_{CLCL} - 15 (5V)		ns
T_{LLAX}	Address Hold After ALE Low	10		T_{CLCL} - 15 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In		55		$4T_{CLCL}$ - 45 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low	10		T_{CLCL} - 15 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	60		$3T_{CLCL}$ - 15 (5V)		ns
T_{PLIV}	PSEN# Low to Valid Instr In		25		$3T_{CLCL}$ - 50 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#			0		ns
T_{PXIZ}	Input Instr Float After PSEN#		10		T_{CLCL} - 15 (5V)	ns
T_{PXAV}	PSEN# to Address valid	17		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In		65		$5T_{CLCL}$ - 60 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10	ns
T_{RLRH}	RD# Pulse Width	120		$6T_{CLCL}$ - 30 (5V)		ns
T_{WLWH}	Write Pulse Width (WE#)	120		$6T_{CLCL}$ - 30 (5V)		ns
T_{RLDV}	RD# Low to Valid Data In		75		$5T_{CLCL}$ - 50 (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		ns
T_{RHDZ}	Data Float After RD#		38		$2T_{CLCL}$ - 12 (5V)	ns
T_{LLDV}	ALE Low to Valid Data In		150		$8T_{CLCL}$ - 50 (5V)	ns
T_{AVDV}	Address to Valid Data In		150		$9T_{CLCL}$ - 75 (5V)	ns
T_{LLWL}	ALE Low to RD# or WR# Low	60	90	$3T_{CLCL}$ - 15 (5V)	$3T_{CLCL}$ + 15 (5V)	ns
T_{AVWL}	Address to RD# or WR# Low	70		$4T_{CLCL}$ - 30 (5V)		ns
T_{QVWX}	Data Valid to WR# High to Low Transition		5	T_{CLCL} - 20		ns
T_{WHQX}	Data Hold After WR#	5		T_{CLCL} - 20 (5V)		ns
T_{QVWH}	Data Valid to WR# High	125		$7T_{CLCL}$ - 50 (5V)		ns
T_{RLAZ}	RD# Low to Address Float		0		0	ns
T_{WHLH}	RD# to WR# High to ALE High	10	40	T_{CLCL} - 15 (5V)	T_{CLCL} + 15 (5V)	ns

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1. Calculated values are for x1 Mode only

Explanation of Symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW or ALE
P: PSEN#
Q: Output data
R: RD# signal
T: Time
V: Valid
W: WR# signal
X: No longer a valid logic level
Z: High Impedance (Float)

For example:

- T_{AVLL} = Time from Address Valid to ALE Low
- T_{LLPL} = Time from ALE Low to PSEN# Low

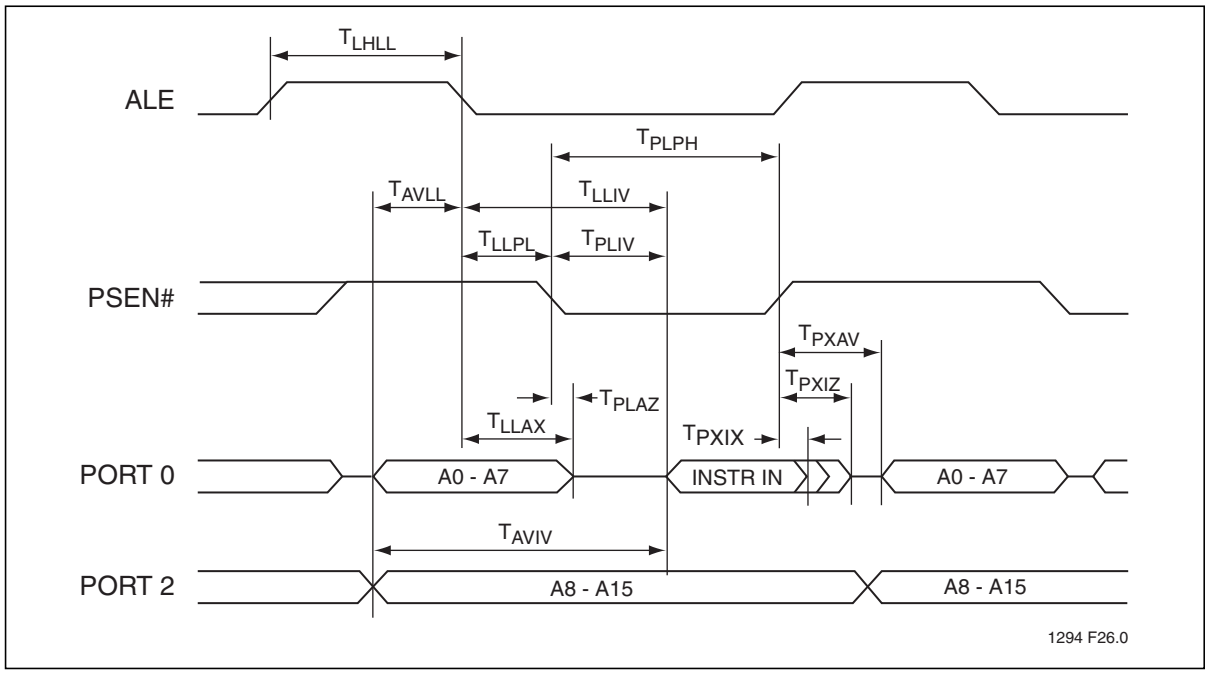

Figure 31: External Program Memory Read Cycle

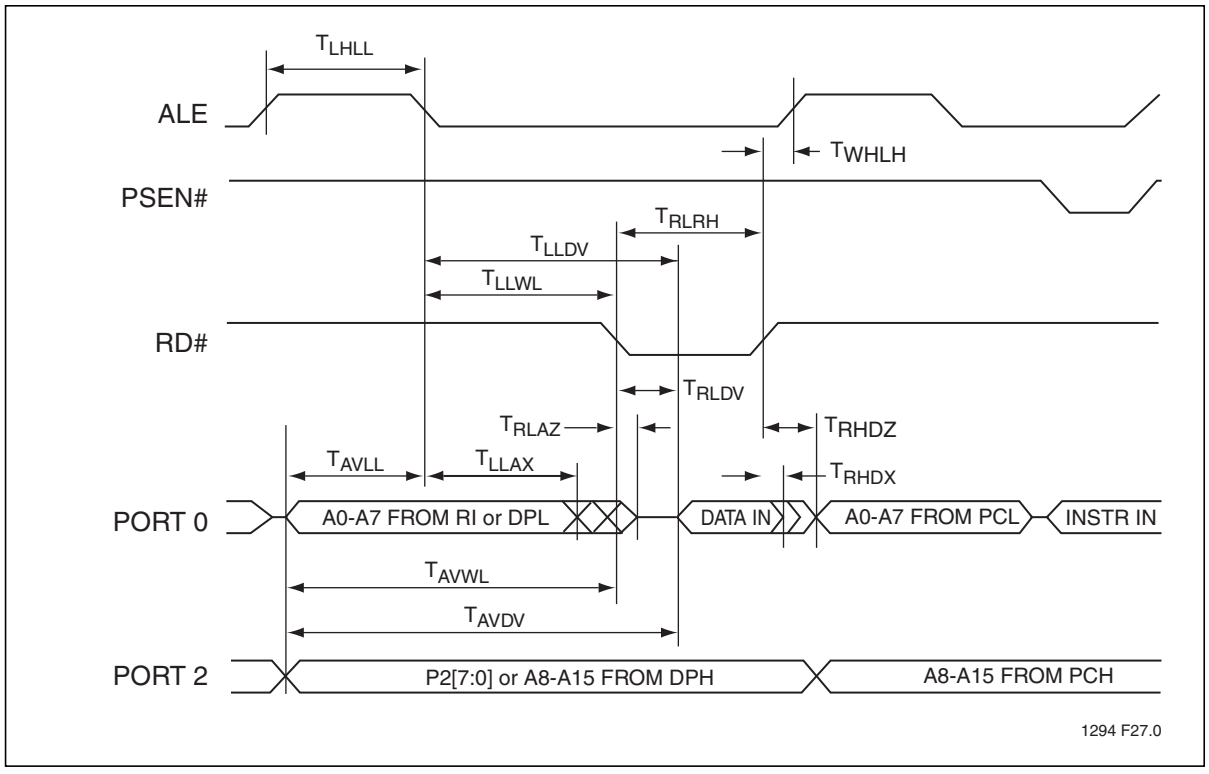

Figure 32: External Data Memory Read Cycle

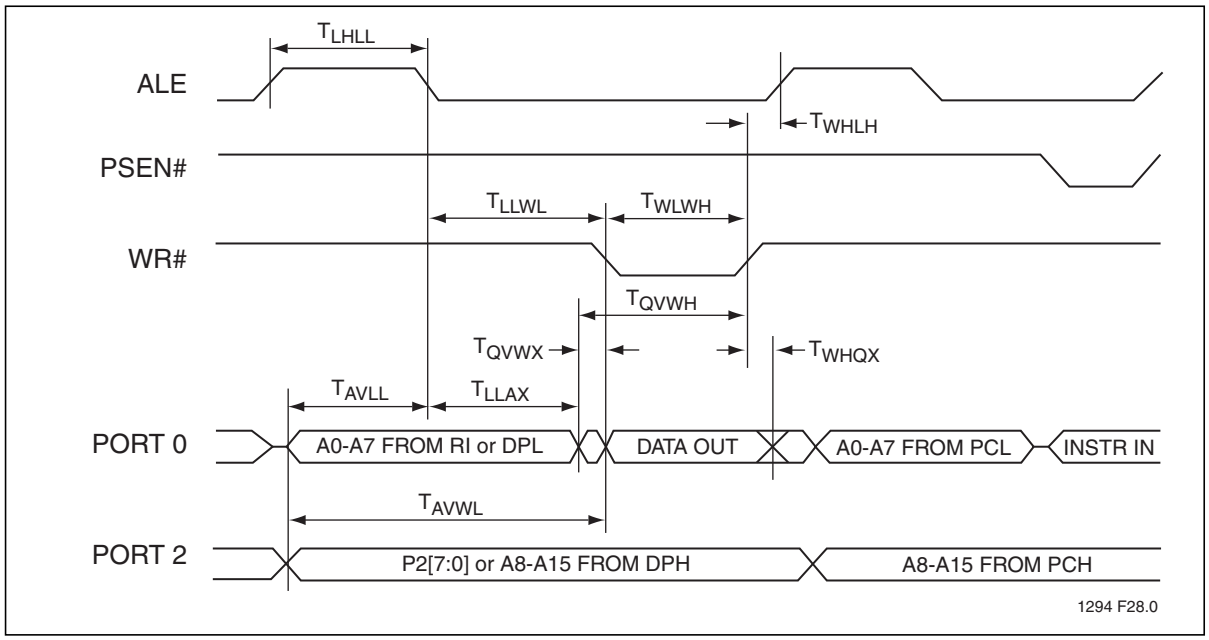

Figure 33: External Data Memory Write Cycle

Table 34: External Clock Drive

Symbol	Parameter	Oscillator				Units
		40MHz		Variable		
		Min	Max	Min	Max	
$1/T_{CLCL}$	Oscillator Frequency			0	40	MHz
T_{CLCL}		25				ns
T_{CHCX}	High Time	8.75		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCX}	Low Time	8.75		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCH}	Rise Time		10			ns
T_{CHCL}	Fall Time		10			ns

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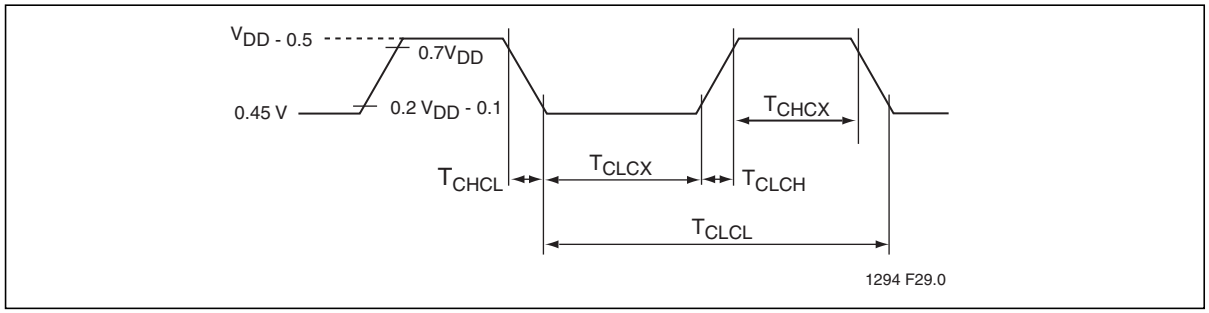

Figure 34: External Clock Drive Waveform

Table 35: Serial Port Timing

Symbol	Parameter	Oscillator				Units
		40MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	0.3		$12T_{CLCL}$		µs
T_{QVXH}	Output Data Setup to Clock Rising Edge	117		$10T_{CLCL}$ - 133		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge			$2T_{CLCL}$ - 117		ns
		0		$2T_{CLCL}$ - 50		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		117		$10T_{CLCL}$ - 133	ns

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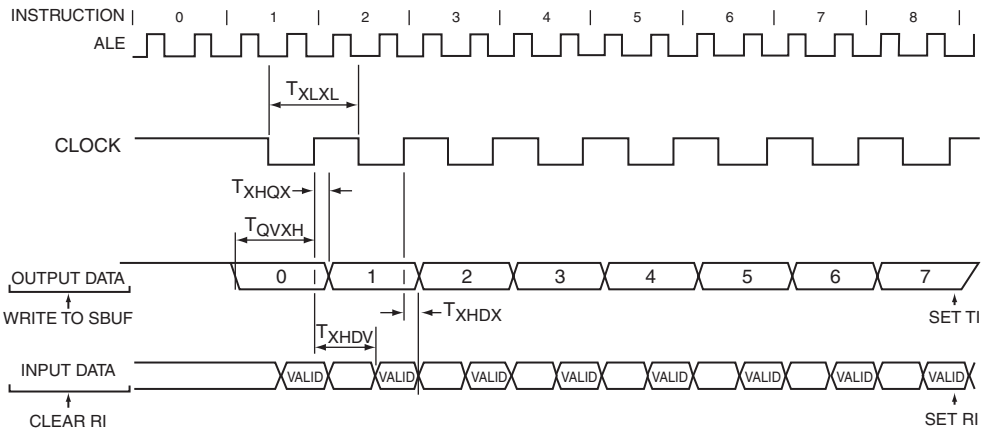
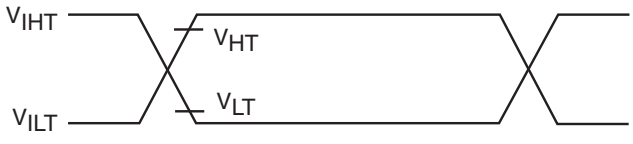


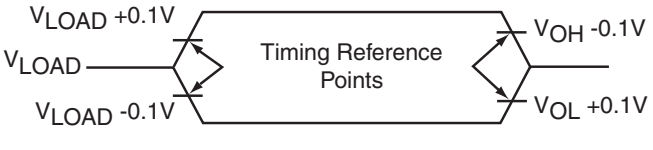
Figure 35: Shift Register Mode Timing Waveforms



AC Inputs during testing are driven at V_{IHT} (V_{DD} -0.5V) for Logic 1 and V_{ILT} (0.45V) for a Logic 0 . Measurement reference points for inputs and outputs are at V_{HT} (0.2V_{DD} + 0.9) and V_{LT} (0.2V_{DD} - 0.1)

Note: V_{HT}- V_{HIGH} Test
V_{LT}- V_{LOW} Test
V_{IHT}-V_{INPUT} HIGH Test
V_{ILT}- V_{INPUT} LOW Test

Figure 36: AC Testing Input/Output Test Waveform



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ± 20mA.

Figure 37: Float Waveform

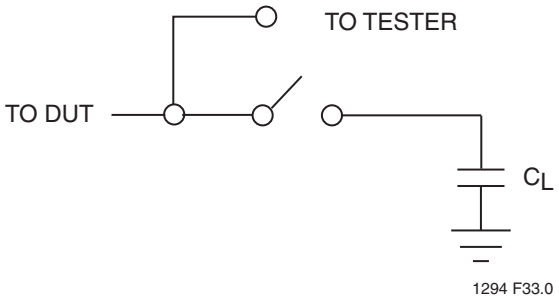
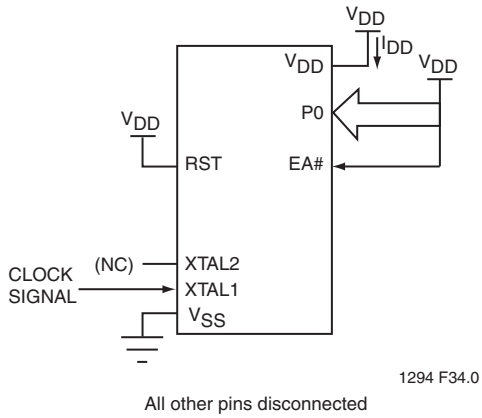


Figure 38: A Test Load Example



All other pins disconnected

Figure 39: I_{DD} Test Condition, Active Mode

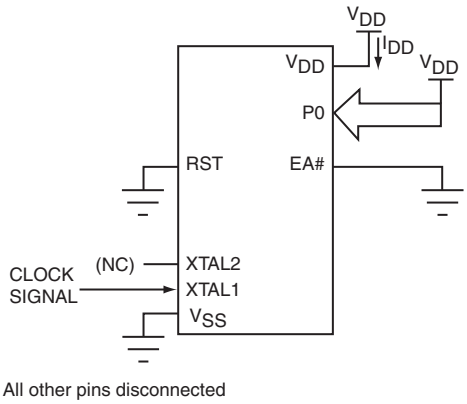


Figure 40: I_{DD} Test Condition, Idle Mode

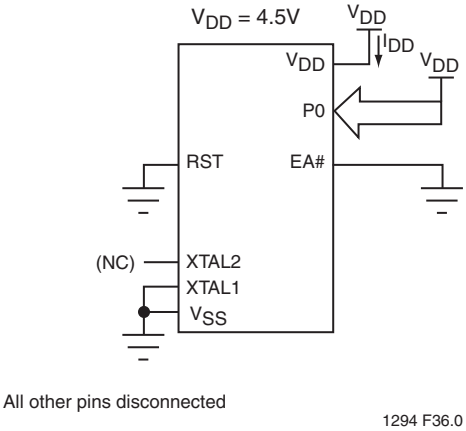


Figure 41: I_{DD} Test Condition, Power-down Mode

Table 36: Flash Memory Programming/Verification Parameters[1]

Parameter[2]	Max	Units
Chip-Erase Time	350	ms
Block-Erase Time	300	ms
Sector-Erase Time	30	ms
Byte-Program Time[3]	100	µs
Re-map or Security bit Program Time	100	µs

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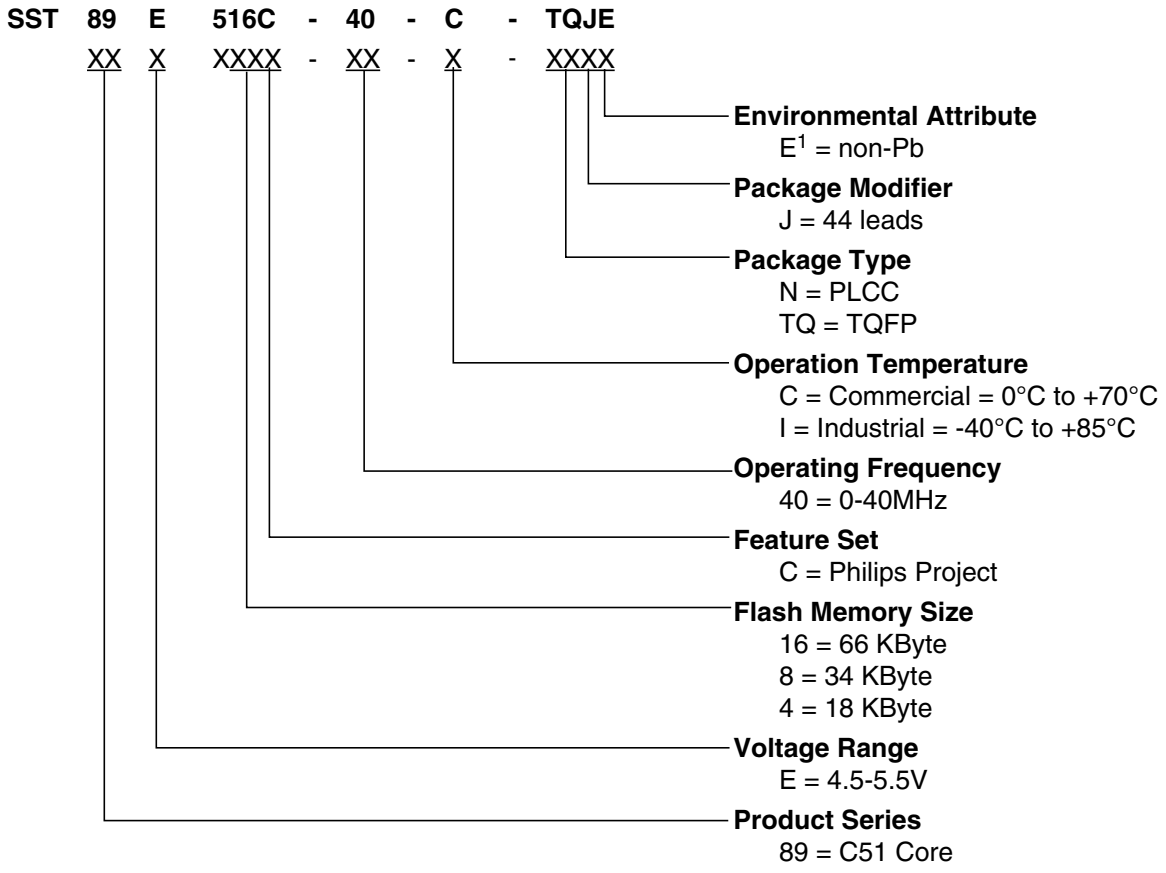
1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.

Product ordering information



1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

Valid Combinations

Valid combinations for SST89E54C

SST89E54C-40-C-NJE	SST89E54C-40-C-TQJE
SST89E54C-40-I-NJE	SST89E54C-40-I-TQJE

Valid combinations for SST89E58C

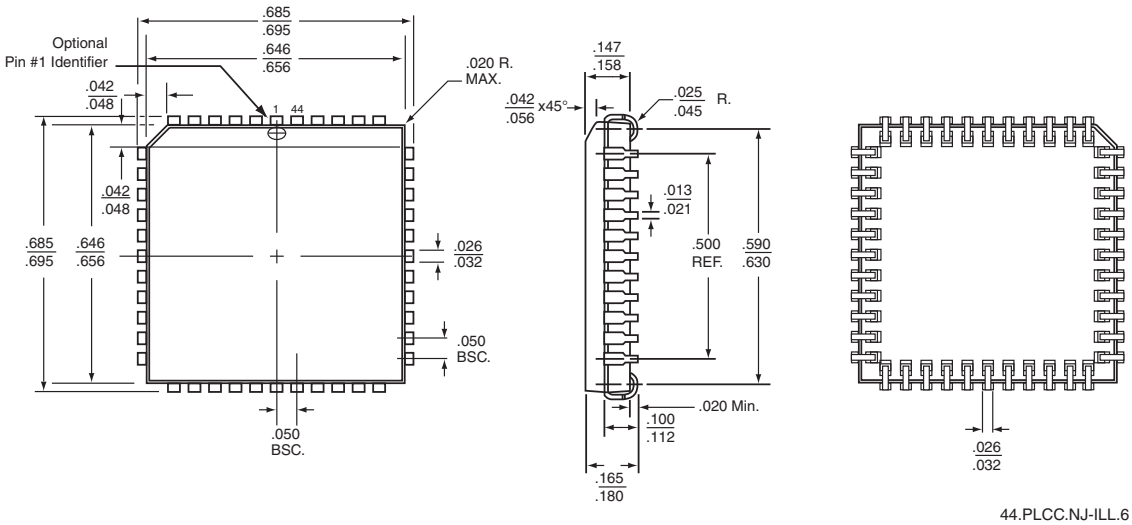
SST89E58C-40-C-NJE	SST89E58C-40-C-TQJE
SST89E58C-40-I-NJE	SST89E58C-40-I-TQJE

Valid combinations for SST89E516C

SST89E516C-40-C-NJE	SST89E516C-40-C-TQJE
SST89E516C-40-I-NJE	SST89E516C-40-I-TQJE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Packaging Diagrams



Note: 1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
= JEDEC min is .650; SST min is *less*stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: ± 4 mils.

Figure 42: 44-Lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NJ

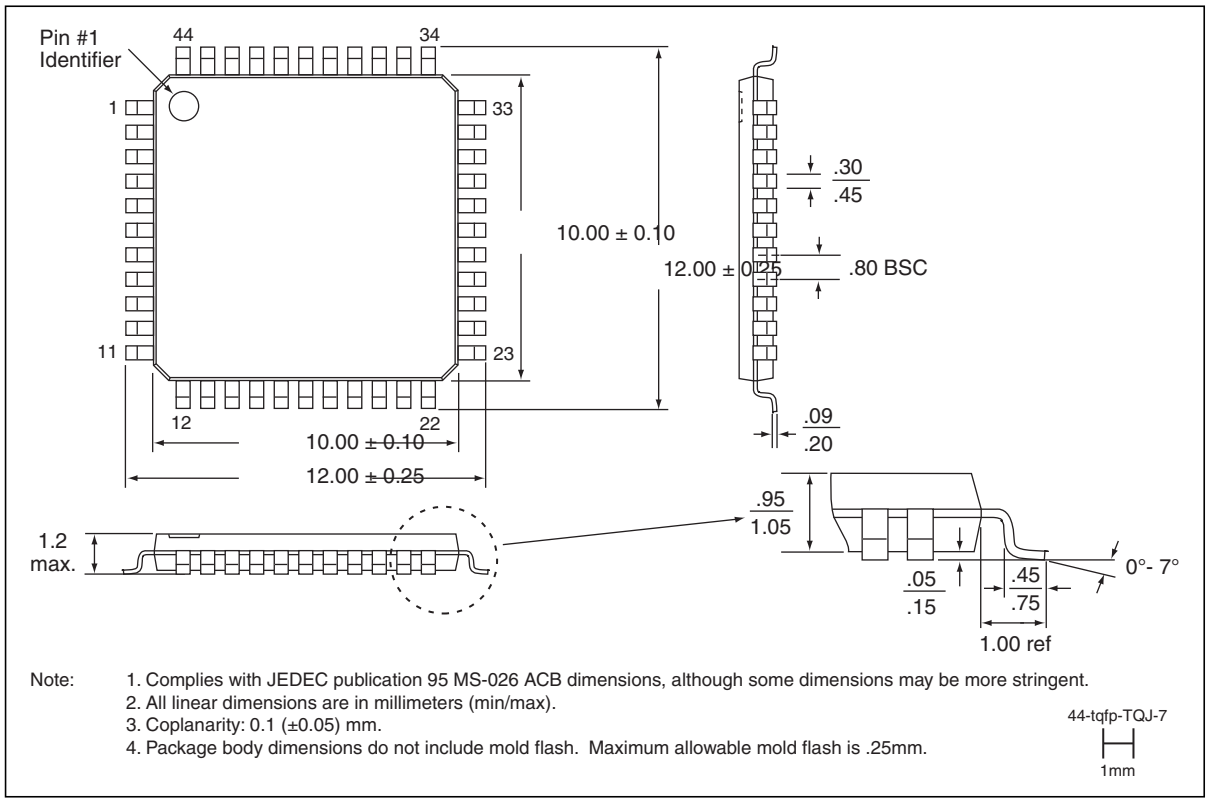


Figure 43: 44-Lead Thin Quad Flat Pack (TQFP)
SST Package Code: TQJ

Table 37: Revision History

Revision	Description	Date
00	• Initial Release of data sheet • Removed 3V version and Pb packages	Jan 2006
01	• Changed B798H, B797H, B3B0H, and B3AFH to FC00H, FBFFH, FB00H, and F7FFH in Figure 4, Figure 5, and Figure 6 • Edited SFCF Register page 19 • Edited SFCM Register page 19 • Changed Clock Doubling Option to “Clock Halving Option” on page 66 • Edited Table 26 on page 67 • Removed “Individual Page Security Lock” from Features on page 1 • Edited SFST last row in Table 5 on page 15 • Removed 12MHz Min/Max from Table 34 on page 75 and Table 35 on page 76 • Changed Block to Partition globally. • Changed FlashFlex51 to FlashFlex globally. • In Features under Single Block SuperFlash EEPROM, changed 18 KByte to 16 KByte, 34 KByte to 32 KByte, and 66 KByte to 64 KByte on page 1. • In Features, deleted “Three High Current Port 1 Pins” page 1. • Changed 512 x8 bits to 512/1K/2K x8 bits on page 2. • Changes 256 Bytes to 1792/768/256 Bytes in four places on page 10. • In Table 2, added footnote. • Edited Table 4, CPU related SFRs • Edited Table 5, changed reset value of SFCF and SFST. • Edited Table 6, changed reset value of WDTRST. • Edited “SuperFlash Configuration Register (SFCF)” , changed reset value. • Edited “SuperFlash Command Register (SFCM)” , removed note. • Edited “SuperFlash Status Register (SFST) (Read Only Register)” , changed reset value. • Edited “Interrupt Priority (IP)” , changed reset value • Edited “Interrupt Priority High (IPH)” , changed reset value • Edited “Interrupt Priority (IPI)” , changed reset value • Edited “Interrupt Priority High (IPIH)” , changed reset value • Edited “Auxiliary Register 1 (AUXR1)” , added ENBOOT symbol and function. • Edited “PCA Compare/Capture Module Mode Register (CCAPMn)” , changed all reset values. • Added Partition Selection Command and changed the External Host mode value from FFH to 55H on page 59. • Edited table Table 23 • Removed Maximum I_{OL} per I/O Pins P1.5, P1.6, P1.7 on page 68 • Edited Table 32, removed V_{OL}. • Changed SRAM power-down voltage from 2.0V to 4.5V in “Power-down Mode” on page 64, in Table 32, and in Figure 41.	Apr 2007
A	• Applied new document format • Release document under letter revision system • Updated spec number from S71294 to DS25096	Nov 2011

ISBN:978-1-61341-774-4

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