rfHCS362G/362F

KEELOQ® Code Hopping Encoder with UHF ASK/FSK Transmitter

General

- Combination KEELOQ® encoder and synthesized UHF ASK/FSK transmitter in a single package
- Operates on a single lithium coin cell
  - <200 nA typical standby current
  - 4.8 to 11.5 mA transmit current
  - 2.2 to 5.5V operation
- Integrated solution with minimum external parts
- Separate pin-outs for KEELOQ encoder and RF transmitter provides for design flexibility

Code Hopping Encoder

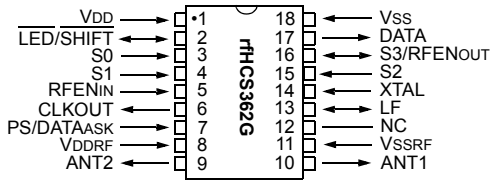
- Programmable minimum code word completion
- Battery low signal transmitted to receiver with programmable threshold
- Non-volatile EEPROM storage of synchronization data
- Easy to use EEPROM programming interface
- PWM or Manchester modulation
- Selectable encoder data rate 417 to 3334 bps
- On-chip tunable encoder oscillator
- RF Enable output for transmitter control
- Button inputs have internal pull-down resistors
- Elapsed time and button queuing options
- Current limiting on $\overline{\text{LED}}$ output
- 2-bit CRC for error detection

UHF ASK/FSK Transmitter

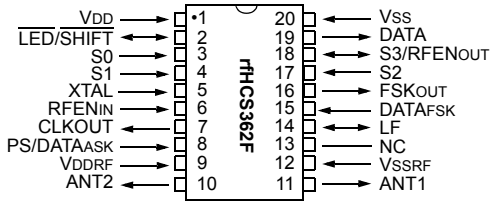
- Conforms to US FCC Part 15.231 regulations and European ERC 70-03E and EN 300 220-1 requirements
- VCO phase locked to quartz crystal reference; allows narrow receiver bandwidth to maximize range and interference immunity
- Crystal frequency divide by 4 output (CLKOUT)
- Transmit frequency range (310 – 440 MHz) set by Crystal frequency
- ASK Modulation
- FSK Modulation through crystal pulling (rfHCS362F)
- Adjustable output power: -12 dBm to +2 dBm
- Differential output configurable for single or double ended loop antenna
- Automatic power amplifier inhibit until PLL lock

Pin Diagrams

SOIC



SSOP



Security

- Programmable 28/32-bit serial number
- Two programmable 64-bit encryption keys
- Programmable 60-bit seed
- Each 69-bit transmission is unique with 32 bits of hopping code
- Encryption keys are read protected

Applications

- Automotive Remote Keyless Entry (RKE) systems
- Automotive alarm systems
- Automotive immobilizers
- Community gate and garage door openers
- Identity tokens with usage counters
- Burglar alarm systems
- Building access

Device	Features		
	Encrypt Keys	Encoding	Transmitter
rfHCS362AG	2 x 64	PWM/MAN	ASK
rfHCS362AF	2 x 64	PWM/MAN	ASK/FSK

1.0 GENERAL DESCRIPTION

The rfHCS362G/362F is a code hopping encoder plus UHF transmitter designed for secure wireless command and control systems. The rfHCS362G/362F utilizes the KEELOQ® code hopping technology which incorporates high security in a small package outline at a low cost to make this device well suited for unidirectional remote keyless entry systems and access control systems.

The rfHCS362G/362F combines a 32-bit hopping code generated by a nonlinear encryption algorithm with a 28/32-bit serial number and 9/5 status bits to create a 69-bit transmission stream. The length of the transmission strongly resists the threat of code scanning. The code hopping mechanism makes each transmission unique, thus rendering code capture and resend (code grabbing) schemes virtually useless.

The encryption key, serial number and configuration data are stored in an EEPROM array which is not accessible via any external connection. The EEPROM data is programmable but read protected. The data can be verified only after an automatic erase and programming operation. This protects against attempts to gain access to keys or manipulate synchronization values. The rfHCS362G/362F provides an easy to use serial interface for programming the necessary keys, system parameters and configuration data.

The transmitter is a fully integrated UHF ASK/FSK transmitter consisting of crystal oscillator, Phase-Locked Loop (PLL), open-collector differential-output Power Amplifier (PA), and mode control logic. External components consist of bypass capacitors, crystal, and PLL loop filter. There are no internal electrical connections between the encoder and the transmitter. The encoder oscillator is independent from the transmitter crystal oscillator.

The rfHCS362G is capable of Amplitude Shift Keying (ASK) modulation by turning the PA on and off. The rfHCS362F is capable of ASK or Frequency Shift Keying (FSK) modulation by employing an internal FSK switch to pull the transmitter crystal via a second load capacitor.

The rfHCS362G/362F is a single channel device. The transmit frequency is fixed and set by an external reference crystal. Transmit frequencies in the range of 310 to 440 MHz can be selected. Output drive is an open-collector differential amplifier. The differential output is well suited for loop antennas. Output power is adjustable from +2 dBm to -12 dBm in six discrete steps.

The rfHCS362G/362F are radio frequency (RF) emitting devices. Wireless RF devices are governed by a country's regulating agency. For example, in the United States it is the Federal Communications Committee (FCC) and in Europe it is the European Conference of Postal and Telecommunications Administrations (CEPT). It is the responsibility of the designer to ensure that their end product conforms to rules and regulations of the country of use and/or sale.

RF devices require correct board level implementation in order to meet regulatory requirements. Layout considerations are given in Section 6.0 UHF ASK/FSK Transmitter.

1.1 Important Terms

The following is a list of key terms used throughout this data sheet. For additional information on KEELOQ and Code Hopping refer to Technical Brief 3 (TB003).

- **RKE** - Remote Keyless Entry
- **Button Status** - Indicates what button input(s) activated the transmission. Encompasses the 4 button status bits S3, S2, S1 and S0 (Figure 3-6).
- **Code Hopping** - A method by which a code, viewed externally to the system, appears to change unpredictably each time it is transmitted.
- **Code word** - A block of data that is repeatedly transmitted upon button activation (Figure 3-6).
- **Transmission** - A data stream consisting of repeating code words (Figure 10-1).
- **Encryption key** - A unique and secret 64-bit number used to encrypt and decrypt data. In a symmetrical block cipher such as the KEELOQ algorithm, the encryption and decryption keys are equal and will be referred to generally as the encryption key.
- **Encoder** - A device that generates and encodes data.
- **Encryption Algorithm** - A recipe whereby data is scrambled using a encryption key. The data can only be interpreted by the respective decryption algorithm using the same encryption key.
- **Decoder** - A device that decodes data received from an encoder.
- **Decryption algorithm** - A recipe whereby data scrambled by an encryption algorithm can be unscrambled using the same encryption key.
- **Learn** – Learning involves the receiver calculating the transmitter's appropriate encryption key, decrypting the received hopping code and storing the serial number, synchronization counter value and encryption key in EEPROM. The KEELOQ product family facilitates several learning strategies to be implemented on the decoder. The following are examples of what can be done.
  - **Simple Learning**
    The receiver uses a fixed encryption key, common to all components of all systems by the same manufacturer, to decrypt the received code word's encrypted portion.

- **Normal Learning**
  The receiver uses information transmitted during normal operation to derive the encryption key and decrypt the received code word's encrypted portion.
- **Secure Learn**
  The transmitter is activated through a special button combination to transmit a stored 60-bit seed value used to generate the transmitter's encryption key. The receiver uses this seed value to derive the same encryption key and decrypt the received code word's encrypted portion.

- **Manufacturer's code** – A unique and secret 64-bit number used to generate unique encoder encryption keys. Each encoder is programmed with a encryption key that is a function of the manufacturer's code. Each decoder is programmed with the manufacturer code itself.

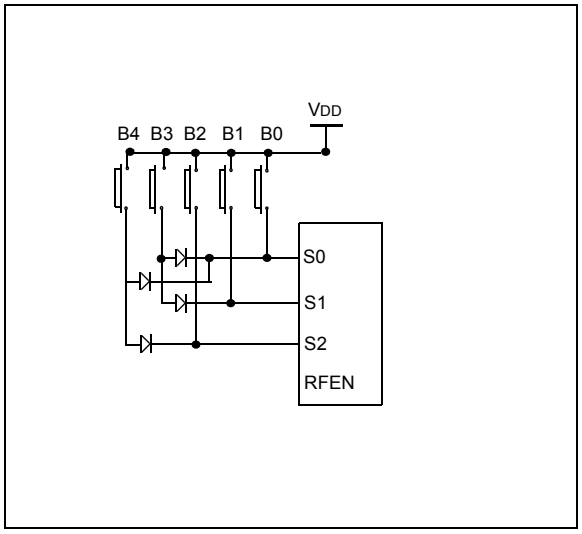
1.2 Applications

The rfHCS362G/362F is suited for secure wireless remote control applications. The EEPROM technology makes customizing application programs (transmitter codes, appliance settings, etc.) extremely fast and convenient. The small footprint packages are suitable for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the rfHCS362G/362F very versatile. Typical application circuits are shown in Figure 1-5 and Figure 1-6.

Most low-end keyless entry transmitters are given a fixed identification code that is transmitted every time a button is pushed. The number of unique identification codes in a low-end system is usually a relatively small number. These shortcomings provide an opportunity for a sophisticated thief to create a device that 'grabs' a transmission and retransmits it later, or a device that quickly 'scans' all possible identification codes until the correct one is found.

The rfHCS362G/362F, on the other hand, employs the KEELOQ code hopping technology coupled with a transmission length of 66 bits to virtually eliminate the use of code 'grabbing' or code 'scanning'. The high security level of the rfHCS362G/362F is based on patented technology. A block cipher based on a block length of 32 bits and a key length of 64 bits is used. The algorithm obscures the information in such a way that even if the transmission information (before coding) differs by only one bit from that of the previous transmission, the next coded transmission will be completely different. Statistically, if only one bit in the 32-bit string of information changes, approximately 50 percent of the coded transmission bits will change.

FIGURE 1-1: ADDITIONAL BUTTON INPUTS



Up to 7 button inputs can be implemented making them look like a binary value to the 3 Sx inputs. This is done with switching diodes as shown in Figure 1-1. The disadvantage is that simultaneously pressed buttons now appear as if a single button is pressed.

The rfHCS362G/362F has a small EEPROM array which must be loaded with several parameters before use. These are most often programmed by the manufacturer at the time of production. The most important of these are:

- A 28-bit serial number, typically unique for every encoder
- An encryption key
- An initial 16-bit synchronization value
- A 16-bit configuration value

The encryption key generation typically inputs the transmitter serial number and 64-bit manufacturer's code into the key generation algorithm (Figure 1-2). The manufacturer's code is chosen by the system manufacturer and must be carefully controlled as it is a pivotal part of the overall system security.

The 16-bit synchronization counter is the basis behind the transmitted code word changing for each transmission; it increments each time a button is pressed. Due to the code hopping algorithm's complexity, each increment of the synchronization value results in about 50% of the bits changing in the transmitted code word.

Figure 1-3 shows how the key values in EEPROM are used in the encoder. Once the encoder detects a button press, it reads the button inputs and updates the synchronization counter. The synchronization counter and encryption key are input to the encryption algorithm and the output is 32 bits of encrypted information. This data will change with every button press, its value appearing externally to 'randomly hop around', hence it is referred to as the hopping portion of the code word. The 32-bit hopping code is combined with the button information and serial number to form the code word transmitted to the receiver. The code word format is explained in greater detail in Section 3.1.

A receiver may use any type of controller as a decoder, but it is typically a microcontroller with compatible firmware that allows the decoder to operate in conjunction with an rfHCS362G/362F based transmitter. Section 7.0 provides detail on integrating the rfHCS362G/362F into a system.

A transmitter must first be 'learned' by the receiver before its use is allowed in the system. Learning includes calculating the transmitter's appropriate encryption key, decrypting the received hopping code and storing the serial number, synchronization counter value and encryption key in EEPROM.

In normal operation, each received message of valid format is evaluated. The serial number is used to determine if it is from a learned transmitter. If from a learned transmitter, the message is decrypted and the synchronization counter is verified. Finally, the button status is checked to see what operation is requested. Figure 1-4 shows the relationship between some of the values stored by the receiver and the values received from the transmitter.

FIGURE 1-2: CREATION AND STORAGE OF ENCRYPTION KEY DURING PRODUCTION

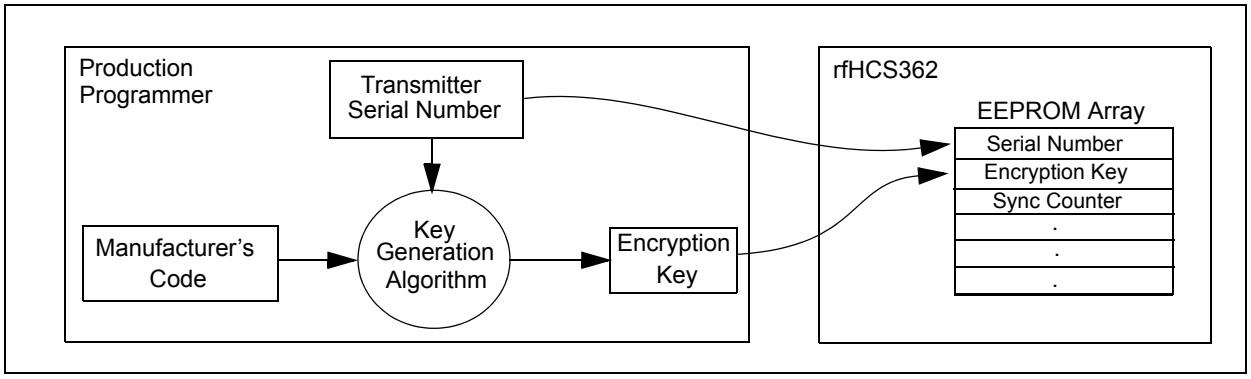


FIGURE 1-3: BUILDING THE TRANSMITTED CODE WORD (ENCODER)

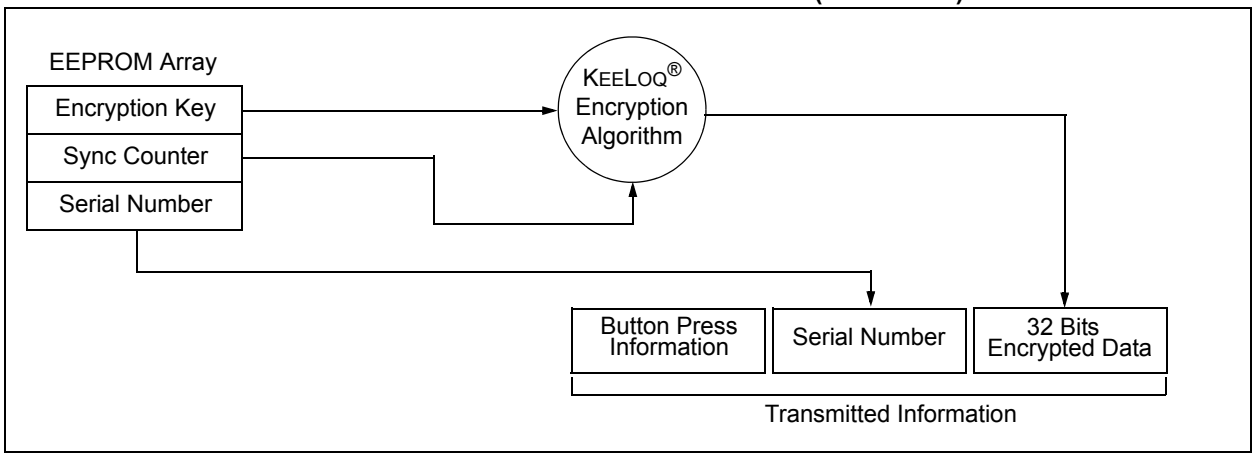
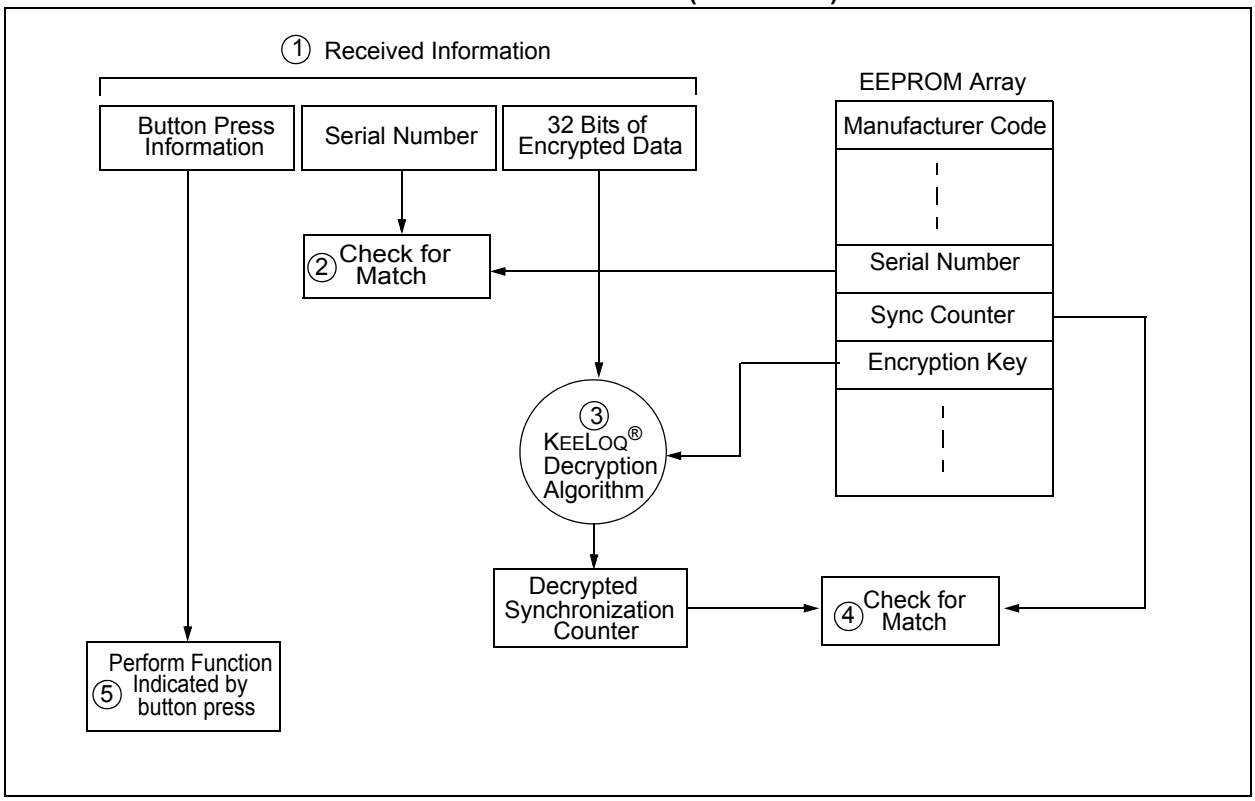


FIGURE 1-4: BASIC OPERATION OF RECEIVER (DECODER)



NOTE: Circled numbers indicate the order of execution.

FIGURE 1-5: ASK EXAMPLE APPLICATIONS CIRCUIT

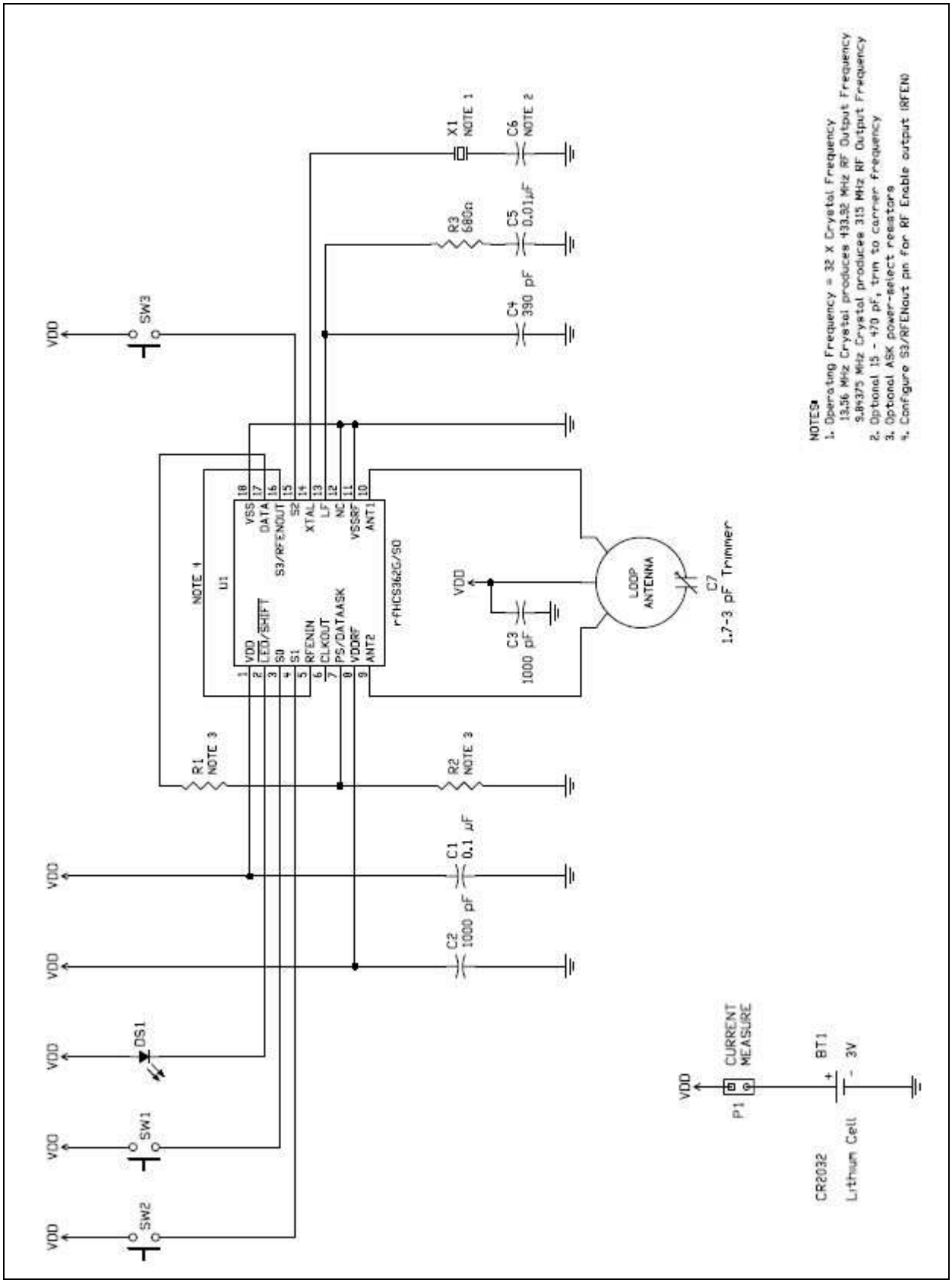
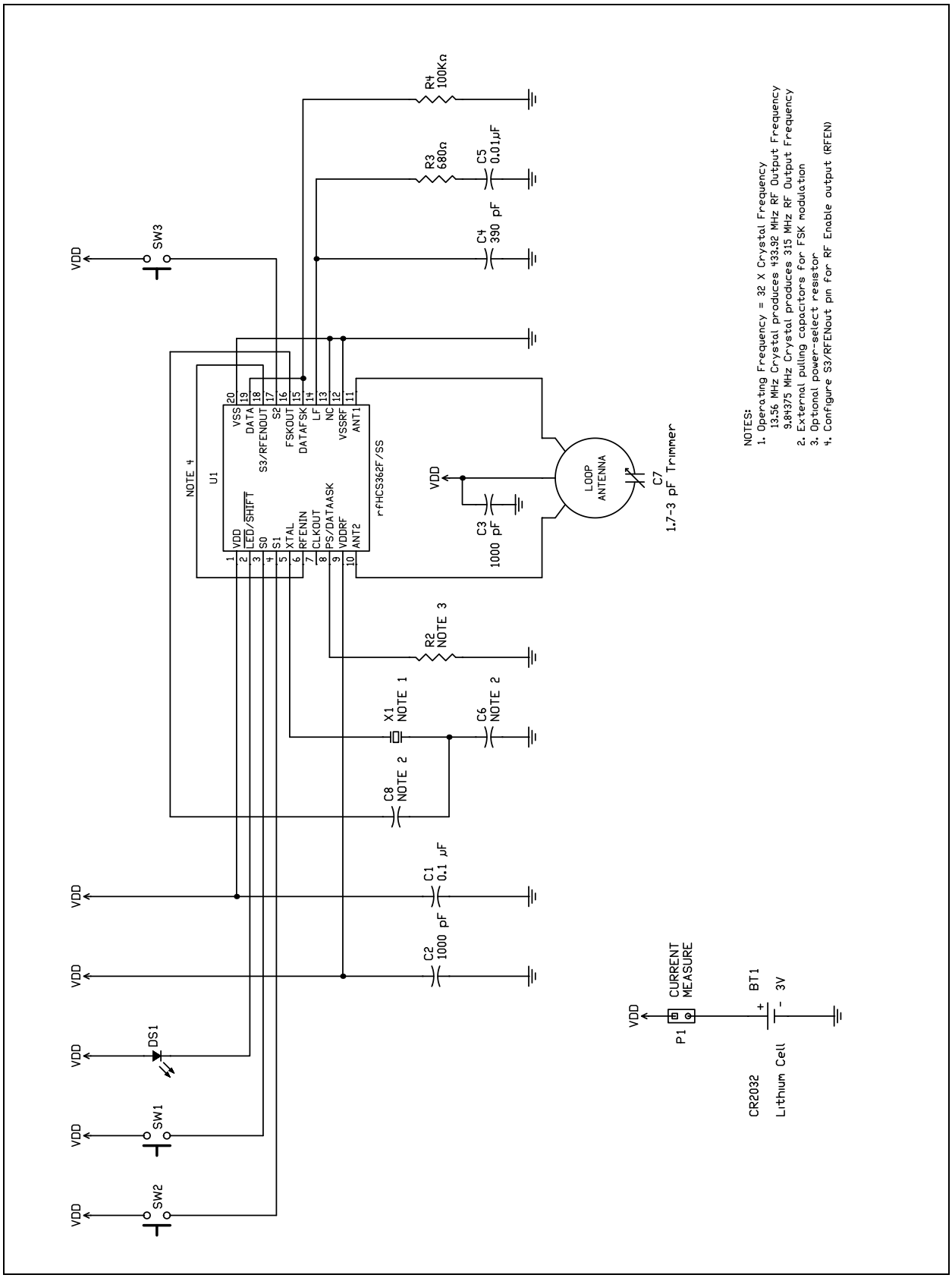


FIGURE 1-6: FSK EXAMPLE APPLICATIONS CIRCUIT

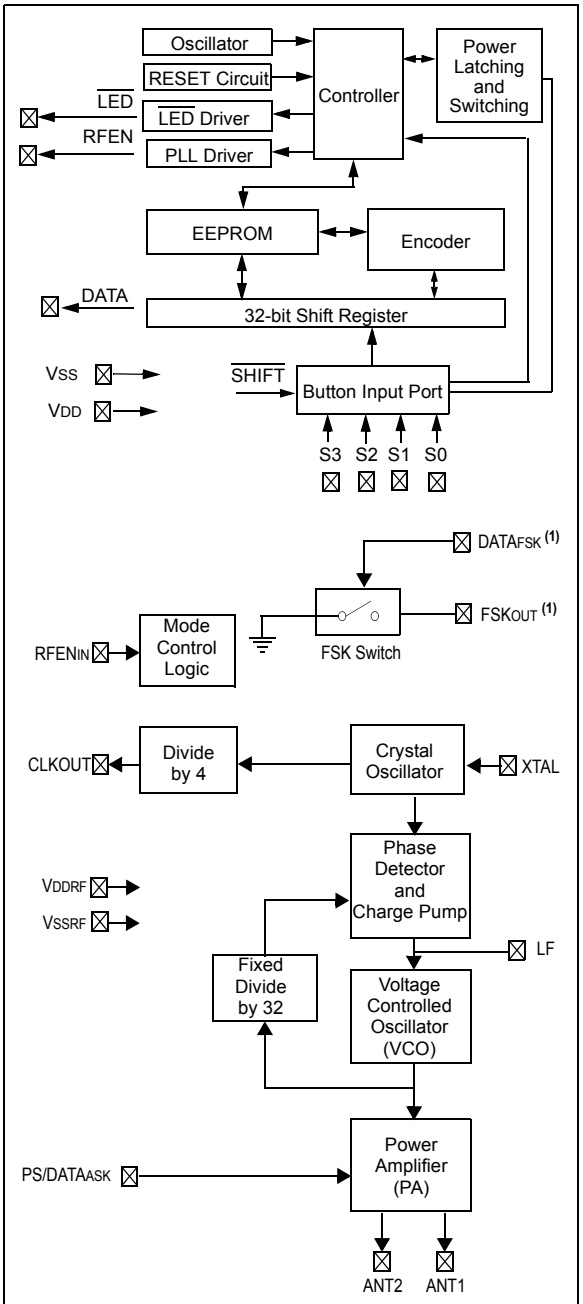


2.0 DEVICE DESCRIPTION

The block diagram in Figure 2-1 shows the internal configuration with the top half representing the encoder and the bottom half the UHF transmitter. Note that connections between the encoder and transmitter are made external to the device for more versability.

Typical application circuits are shown in Figure 1-5 and Figure 1-6. The rfHCS362G/362F requires only the addition of push button switches and few external components for use as a transmitter in your security application. See Table 2-1 for pinout description. Figure 2-2 shows the device I/O circuits.

FIGURE 2-1: rfHCS362 BLOCK DIAGRAM



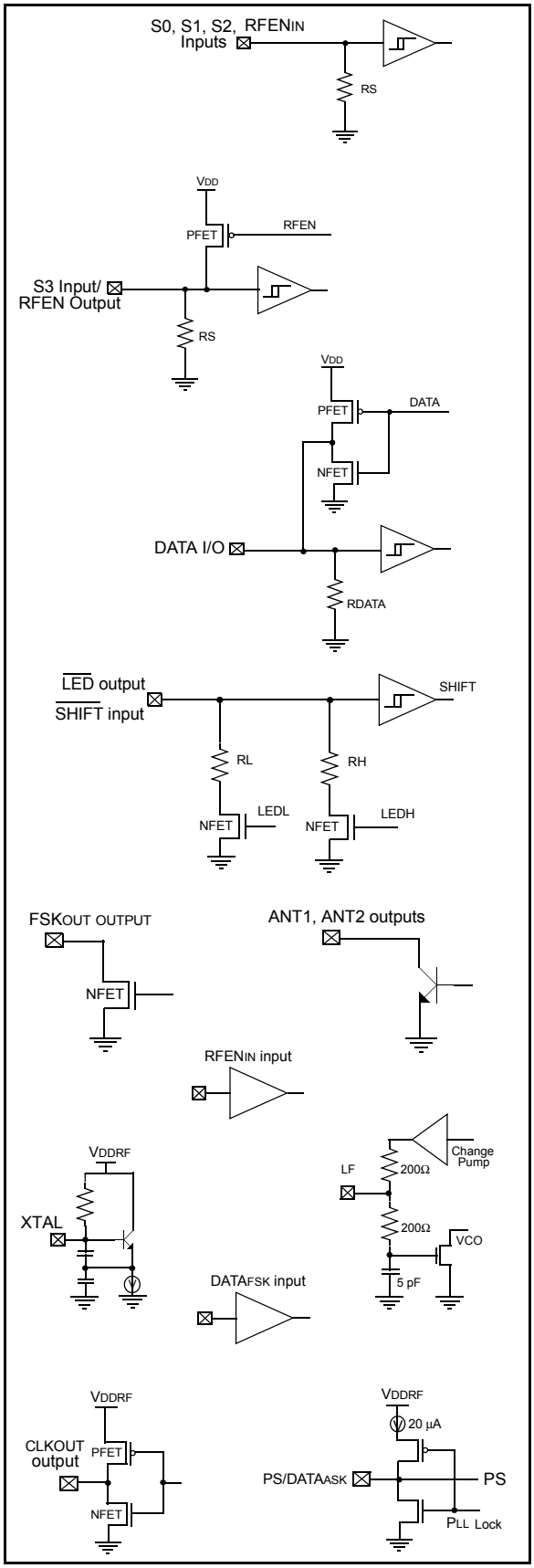
Note 1: rfHCS362F only.

TABLE 2-1: rfHCS362G/362F PINOUT DESCRIPTION

Name	SOIC Pin #	SSOP Pin #	I/O/P Type	Description
ANT1	10	11	O	Antenna connection to differential power amplifier output, open collector.
ANT2	9	10	O	Antenna connection to differential power amplifier output, open collector.
CLKOUT	6	7	O	Clock output.
DATA	17	19	I/O	Encoder data output pin or serial programming.
$DATA_{FSK}$	—	15	I	FSK data input.
FSK_{OUT}	—	16	O	FSK crystal pulling output.
$\overline{LED}/\overline{SHIFT}$	2	2	I/O	Current limited LED driver. Input sampled before LED driven.
LF	13	14	—	External loop filter connection. Common node of charge pump output and VCO tuning input.
$PS/DATA_{ASK}$	7	8	I	Power select and ASK data input.
$RFEN_{IN}$	5	6	I	Transmitter and CLKOUT enable. Internal pull-down.
S0	3	3	I	Switch input 0 with internal pull-down.
S1	4	4	I	Switch input 1 with internal pull-down.
S2	15	17	I	Switch input 2 with internal pull-down or Schmitt Trigger clock input during serial programming.
S3/RFEN	16	18	I/O	Switch input 3 with internal pull-down or RF enable output as selected by RFEN option in configuration word SEED_3.
V_{DD}	1	1	P	Positive supply for encoder
V_{DDRF}	8	9	P	Positive supply for transmitter.
V_{SS}	18	20	P	Ground reference for encoder
V_{SSRF}	11	12	P	Ground reference for transmitter.
XTAL	14	5	I	Transmitter crystal connection to Colpitts type crystal oscillator.

Legend: I = input, O = output, I/O = input/output, P = power

FIGURE 2-2: I/O CIRCUITS



2.1 Encoder Architectural Overview

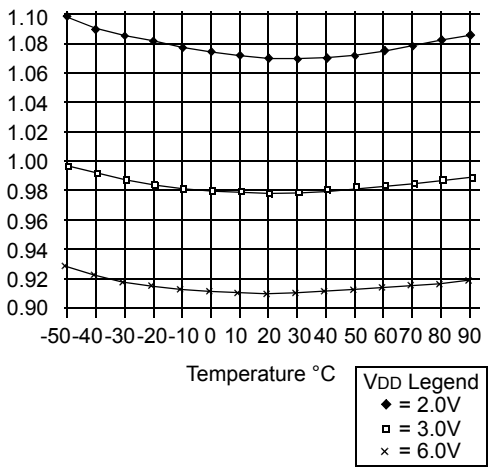
2.1.1 ONBOARD EEPROM

The rfHCS362G/362F has an onboard nonvolatile EEPROM which is used to store user programmable data. The data can be programmed at the time of production and includes the security-related information such as encoder keys, serial numbers, discrimination and seed values. All the security related options are read protected. The rfHCS362G/362F has built-in protection against counter corruption. Before every EEPROM write, the internal circuitry also ensures that the high voltage required to write to the EEPROM is at an acceptable level.

2.1.2 INTERNAL RC OSCILLATOR

The rfHCS362G/362F has an onboard RC oscillator that controls all the logic output timing characteristics. The oscillator frequency varies within ±10% of the nominal value (once calibrated over a voltage range of 2V – 3.5V or 3.5V – 6.3V). All the timing values specified in this document are subject to the oscillator variation.

FIGURE 2-3: TYPICAL rfHCS362G/362F NORMALIZED OSCILLATOR PERIOD VS. TEMPERATURE



Note: Values are for calibrated oscillator

2.1.3 LOW VOLTAGE DETECTOR

A low battery voltage detector onboard the rfHCS362G/362F can indicate when the operating voltage drops below a predetermined value. There are eight options available depending on the VLOW[0..2] configuration options. The options provided are:

000 - 2.0V	100 - 4.0V
001 - 2.1V	101 - 4.2V
010 - 2.2V	110 - 4.4V
011 - 2.3V	111 - 4.6V

FIGURE 2-4: rfHCS362 VLOW DETECTOR (TYPICAL)

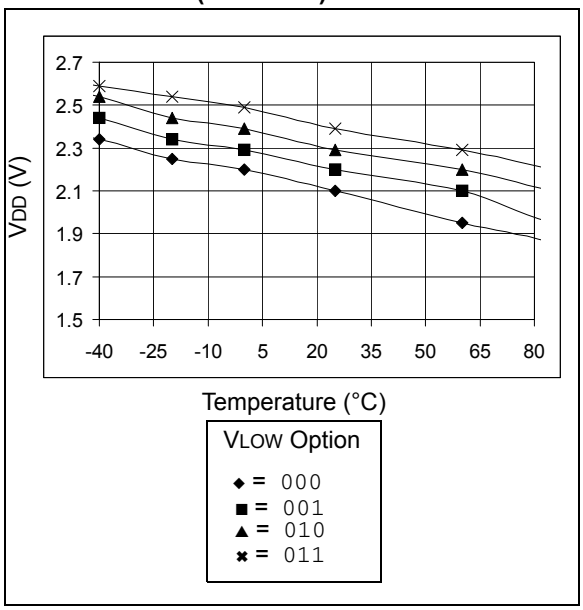
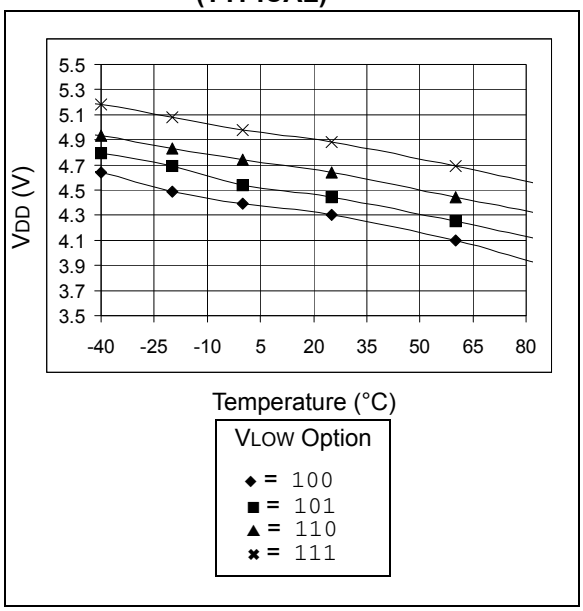


FIGURE 2-5: rfHCS362 VLOW DETECTOR (TYPICAL)



The output of the low voltage detector is transmitted in each code word, so the decoder can give an indication to the user that the transmitter battery is low. Operation of the LED changes as well to further indicate that the battery is low and needs replacing.

3.0 ENCODER OPERATION

The rfHCS362G/362F will wake-up upon detecting a switch closure and then delay for switch debounce (Figure 3-1). The synchronization information, fixed information and switch information will be encrypted to form the hopping code. The encrypted or hopping code portion of the transmission will change every time a button is pressed, even if the same button is pushed again. Keeping a button pressed for a long time will result in the same code word being transmitted until the button is released or time-out occurs.

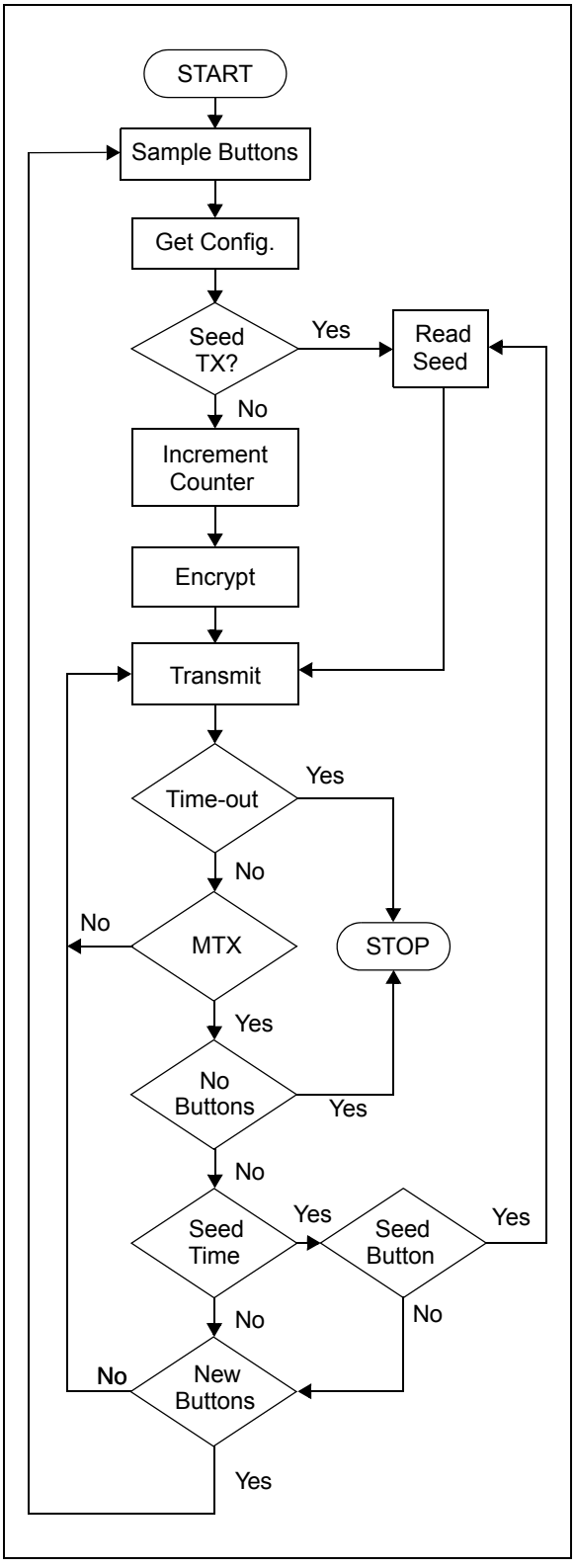
The time-out time can be selected with the time-out (TIMOUT[0..1]) configuration option. This option allows the time-out to be disabled or set to 0.8 s, 3.2 s or 25.6 s. When a time-out occurs, the device will go into SLEEP mode to protect the battery from draining when a button gets stuck.

If in the transmit process, and a new button is pressed, the current code word will be aborted. A new code word will be transmitted and the time-out counter will RESET. If all the buttons are released, the minimum code words will be completed. The minimum code words can be set to 1, 2, 4 or 8 using the Minimum Code Words (MTX[0..1]) configuration option. If the time for transmitting the minimum code words is longer than the time-out time, the device will not complete the minimum code words.

Note:	If multiple buttons are pressed and one is released, it will not have any effect on the code word. If no buttons remain pressed the minimum code words will be completed and the power-down will occur.

A code that has been transmitted will not occur again for more than 64K transmissions. This will provide more than 18 years of typical use before a code is repeated based on 10 operations per day. Overflow information programmed into the encoder can be used by the decoder to extend the number of unique transmissions to more than 192K.

FIGURE 3-1: BASIC FLOW DIAGRAM OF THE DEVICE OPERATION



3.1 Transmission Modulation Format

The rfHCS362 transmission is made up of several code words. Each code word consists of a preamble, a header and data (see Figure 3-2).

The code words are separated by a **Guard Time** that can be set to 0 ms, 6.4 ms, 25.6 ms or 76.8 ms with the Guard Time Select (GUARD[0..1]) configuration option. All other timing specifications for the modulation formats are based on a basic timing element (TE). This **Timing Element** can be set to 100 µs, 200 µs, 400 µs or 800 µs with the Baud Rate Select (BSEL[0..1]) configuration option. The **Header Time** can be set to 3 TE or 10 TE with the Header Select (HEADER) configuration option.

There are two different modulation formats available on the rfHCS362 that can be set using the Modulation Select (MOD) configuration option:

- Pulse Width Modulation (PWM)
- Manchester Encoding

Modulation formats are shown in Figure 3-3 and Figure 3-4. Code word data formats are shown in Figure 3-6.

FIGURE 3-2: CODE WORD TRANSMISSION SEQUENCE

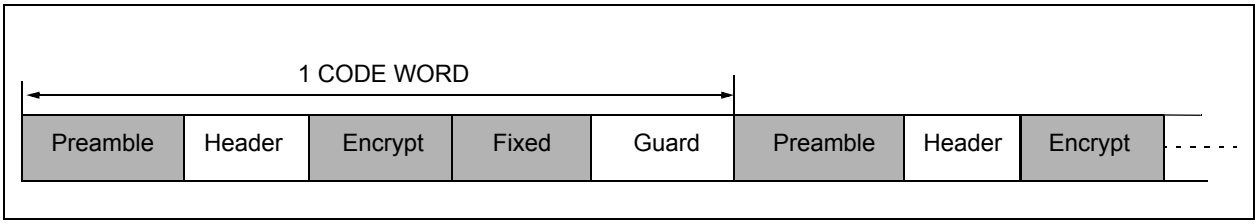


FIGURE 3-3: PULSE WIDTH MODULATION TRANSMISSION FORMAT

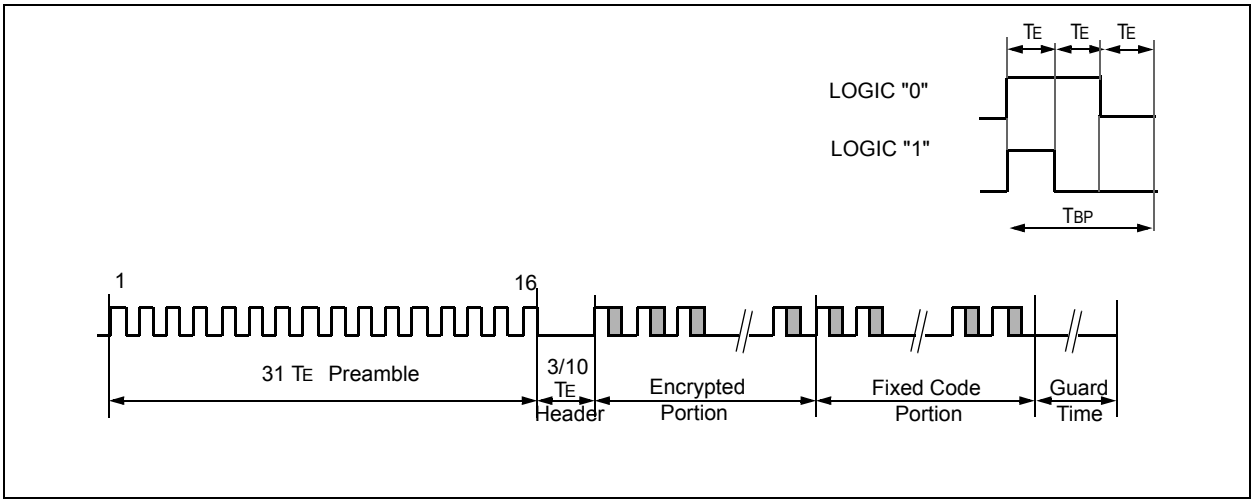
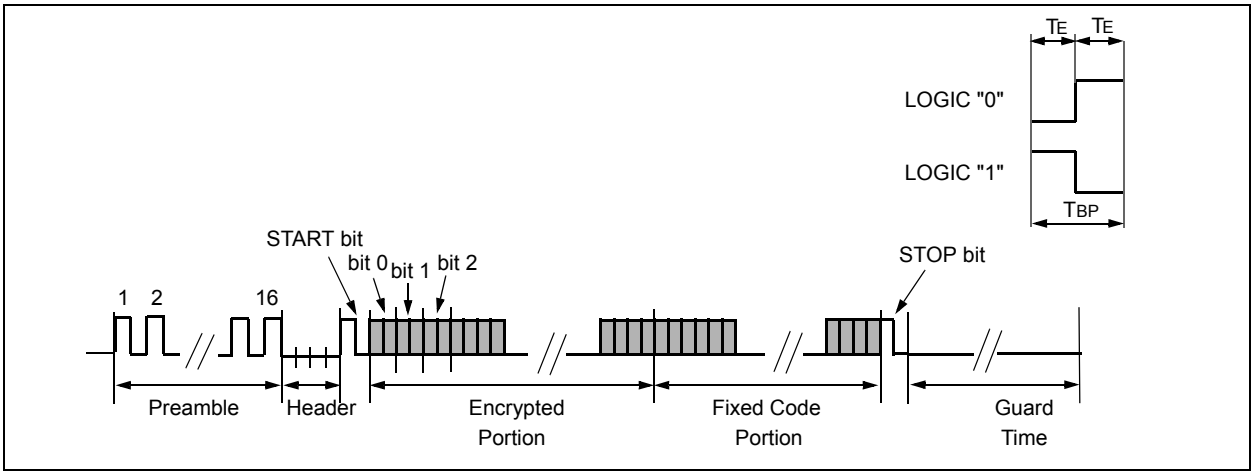


FIGURE 3-4: MANCHESTER TRANSMISSION FORMAT



3.1.1 CODE HOPPING DATA

The hopping portion is calculated by encrypting the counter, discrimination value and function code with the Encoder Key (KEY). The counter is 16 bits wide. The discrimination value is 10 bits wide. There are 2 counter overflow bits (OVR) that are cleared when the counter wraps to 0. The rest of the 32 bits are made up of the function code also known as the button inputs.

3.1.2 FIXED CODE DATA

The 32 bits of fixed code consist of 28 bits of the serial number (SER) and another copy of the function code. This can be changed to contain the whole 32-bit serial number with the Extended Serial Number (XSER) configuration option.

3.1.3 MINIMUM CODE WORDS

MTX[0..1] configuration bits selects the minimum number of code words that will be transmitted. If the button is released after 1.6 s (or greater) and MTX code words have been transmitted, the code word being transmitted will be terminated. The possible values are:

00 - 1

01 - 2

10 - 4

11 - 8

3.1.4 STATUS INFORMATION

The status bits will always contain the output of the Low Voltage detector (VLOW), the Cyclic Redundancy Check (CRC) bits (or TIME bits depending on CTSEL) and the Button Queue information.

3.1.4.1 Low Voltage Detector Status (VLOW)

The output of the low voltage detector is transmitted with each code word. If VDD drops below the selected voltage, a logic '1' will be transmitted. The output of the detector is sampled before each code word is transmitted.

3.1.4.2 Button Queue Information (QUEUE)

The queue bits indicate a button combination was pressed again within 2 s after releasing the previous activation. Queuing or repeated pressing of the same buttons (or button combination) is detected by the rfHCS362 button debouncing circuitry.

The Queue bits are added as the last two bits of the standard code word. The queue bits are a 2-bit counter that does not wrap. The counter value starts at '00b' and is incremented if a button is pushed within 2 s of the previous button press. The current code word is terminated when the buttons are queued. This allows additional functionality for repeated button presses.

The button inputs are sampled every 6.4 ms during this 2 s period.

00 - first activation
01 - second activation
10 - third activation
11 - from fourth activation on

3.1.4.3 Time BITS

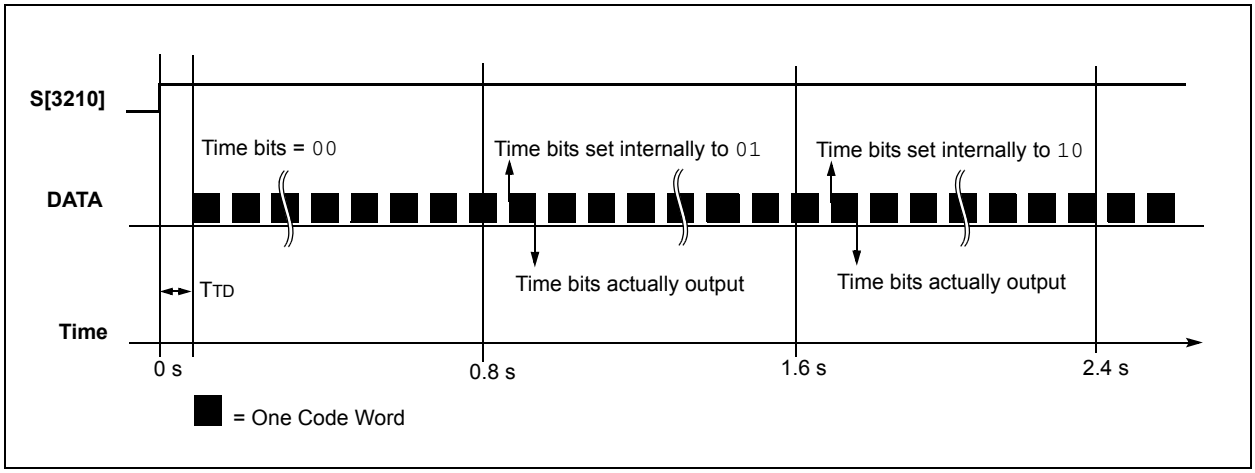
The time bits (Figure 3-5) indicate the duration that the inputs were activated:

00 - immediate
01 - after 0.8 s
10 - after 1.6 s
11 - after 2.4 s

The TIME bits are incremented every 0.8 s and will not wrap once it reaches '11'.

Time information is alternative to the CRC bits availability and is selected by the CTSEL configuration bit.

FIGURE 3-5: TIME BITS OPERATION



3.1.4.4 Cyclic Redundancy Check (CRC)

The CRC bits are calculated on the 65 previously transmitted bits. The decoder can use the CRC bits to check the data integrity before processing starts. The CRC can detect all single bit errors and 66% of double bit errors. The CRC is computed as follows:

EQUATION 3-1: CRC Calculation

$$CRC[1]_{n+1} = CRC[0]_n \oplus Di_n$$

and

$$CRC[0]_{n+1} = (CRC[0]_n \oplus Di_n) \oplus CRC[1]_n$$

with

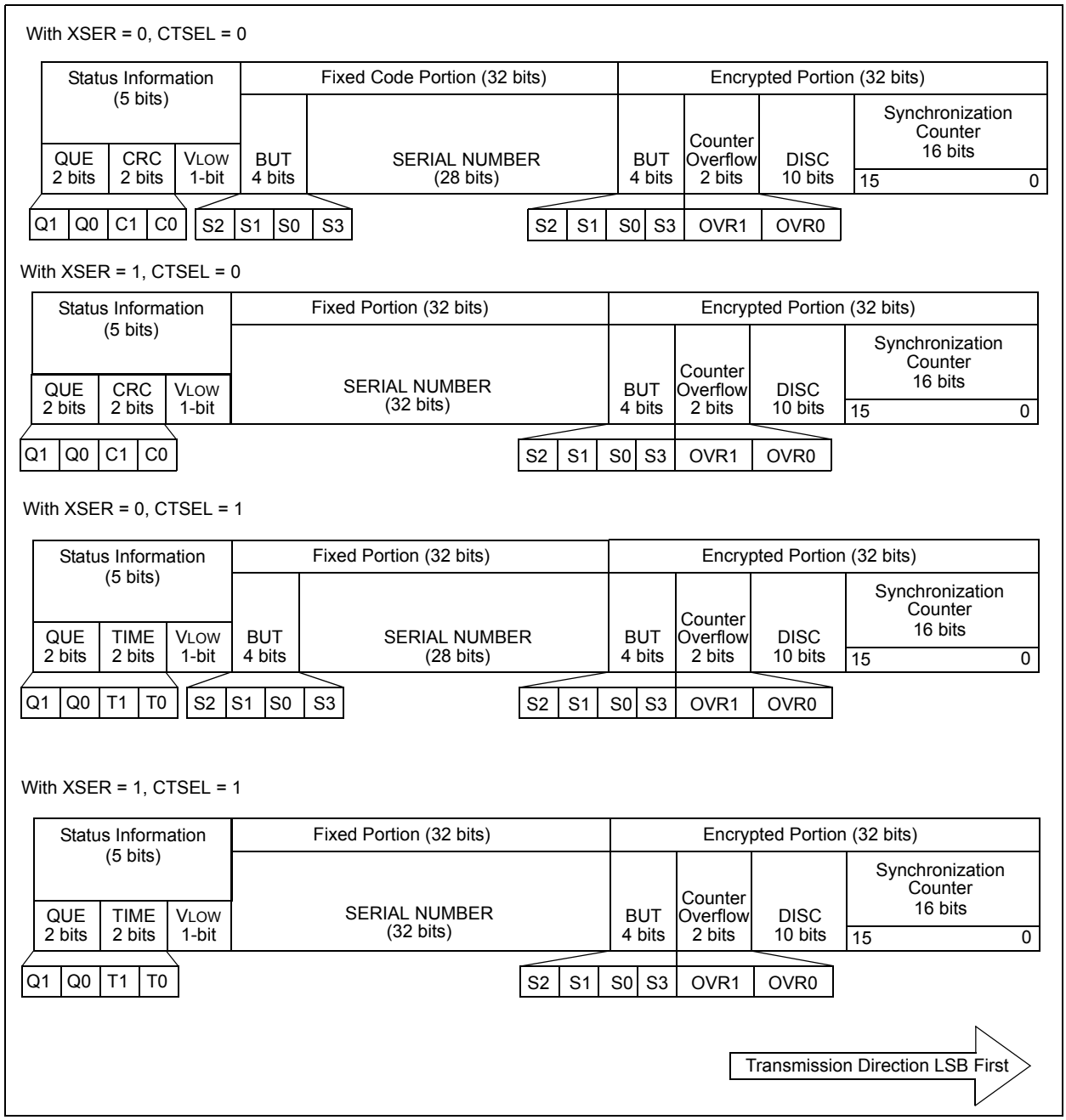
$$CRC[1,\ 0]_0 = 0$$

and Di_n the nth transmission bit $0 \leq n \leq 64$

Warning: The CRC may be wrong when the battery voltage is near the selected VLOW trip point. This may happen because VLOW is sampled twice each transmission, once for the CRC calculation and once when VLOW is transmitted. VDD tends to move slightly during a transmission which could lead to a different value for VLOW being used for the CRC calculation and the transmission.

Work around: If the CRC is incorrect, recalculate for the opposite value of VLOW.

FIGURE 3-6: CODE WORD DATA FORMAT

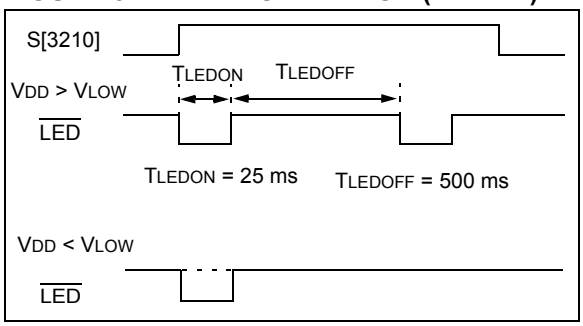


3.2 $\overline{\text{LED}}$ Output

The $\overline{\text{LED}}$ pin will be driven LOW periodically while the rfHCS362 is transmitting data to power an external LED.

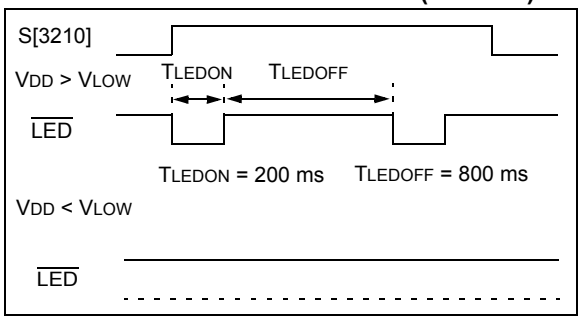
The duty cycle (T_{LEDON}/T_{LEDOFF}) can be selected between two possible values by the configuration option (LED).

FIGURE 3-7: LED OPERATION (LED = 1)



The same configuration option determines whether when the V_{DD} Voltage drops below the selected V_{LOW} trip point the LED will blink only once or stop blinking.

FIGURE 3-8: LED OPERATION (LED = 0)



Note: When the rfHCS362 encoder is used as a Dual Encoder the $\overline{\text{LED}}$ pin is used as a $\overline{\text{SHIFT}}$ input (Figure 3-9). In such a configuration the LED is always ON during transmission. To keep power consumption low, it is recommended to use a series resistor of relatively high value. V_{LOW} information is not available when using the second Encryption Key.

3.3 Dual Encoder Operation

The rfHCS362G/362F contains two encryption keys (for example derived from two different Manufacturer's Codes), but only one Serial Number, one set of Discrimination bits, one 16-bit Synchronization Counter and a single 60-bit Seed value. For this reason the rfHCS362G/362F can be used as an encoder in multiple (two) applications as far as they share the same configuration: transmission format, baud rate, header and guard settings. The SHIFT input pin (multiplexed with the LED output) is used to select between the two encryption keys.

A logic 1 on the $\overline{\text{SHIFT}}$ input pin selects the first encryption key.

A logic 0 on the $\overline{\text{SHIFT}}$ input pin will select the second encryption key.

FIGURE 3-9: USING DUAL ENCODER OPERATION

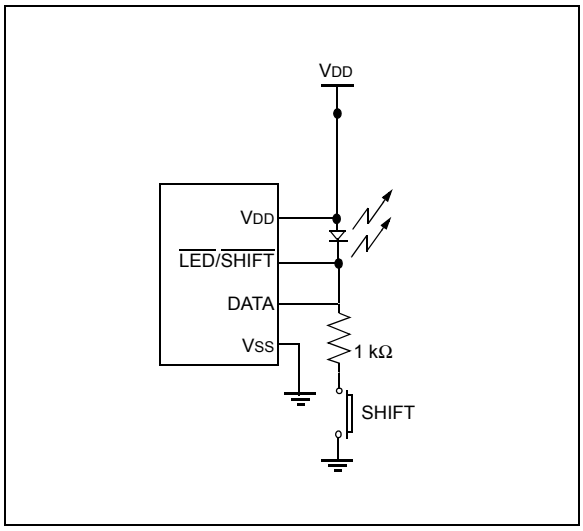
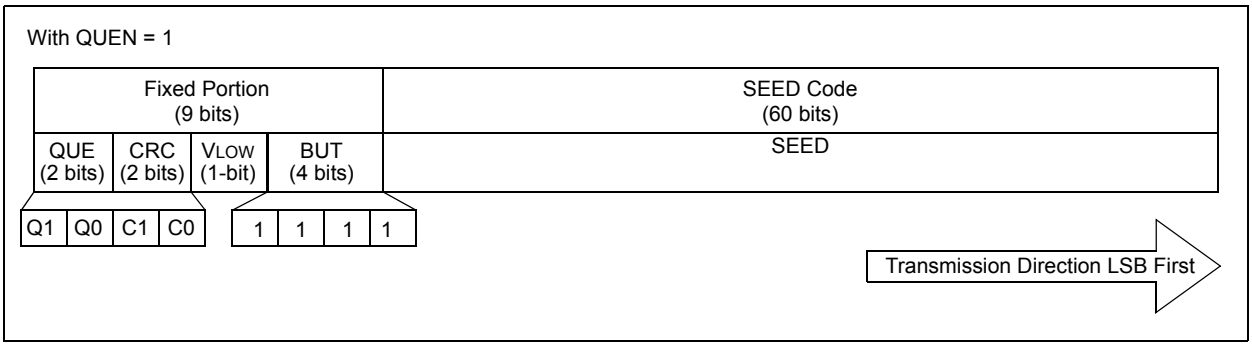


FIGURE 3-10: SEED CODE WORD FORMAT



3.4 Seed Code Word Data Format

A seed transmission transmits a unencrypted code word that consists of 60 bits of fixed data that is stored in the EEPROM. This can be used for secure learning of encoders or whenever a fixed code transmission is required. The seed code word further contains the function code and the status information (VLOW, CRC and QUEUE) as configured for normal code hopping code words. The seed code word format is shown in Figure 3-10. The function code for seed code words is always '1111b'.

Seed code words can be configured as follows:

- Enabled permanently.
- Disabled permanently.
- Enabled until the synchronization counter is greater than 7Fh, this configuration is often referred to as **Limited Seed**.
- The time before the seed code word is transmitted can be set to 1.6 s or 3.2 s, this configuration is often referred to as **Delayed Seed**. When this option is selected, the rfHCS362 will transmit a code hopping code word for 1.6 s or 3.2 s, before the seed code word is transmitted.

3.4.1 SEED OPTIONS

The button combination (S[3210]) for transmitting a Seed code word can be selected with the Seed and SeedC (SEED[0..1] and SEEDC) configuration options as shown in Table 3-1 and Table 3-2:

TABLE 3-1: SEED OPTIONS (SEEDC = 0)

SEED	Seed S[3210]	1.6 s Delayed Seed S[3210]
00	–	–
01	0101*	0001*
10	0101	0001
11	0101	–
Note:	*Limited Seed	

TABLE 3-2: SEED OPTIONS (SEEDC = 1)

SEED	Seed S[3210]	3.2 s Delayed Seed S[3210]
00	–	–
01	1001*	0011*
10	1001	0011
11	1001	–
Note:	*Limited Seed	

Example A): Selecting SEEDC = 1 and SEED = 11: makes SEED transmission available every time the combination of buttons S3 and S0 is pressed simultaneously, but Delayed Seed mode is not available.

Example B): Selecting SEEDC = 0 and SEED = 01: makes SEED transmission available only for a limited time (only up to 128 times). The combination of buttons S2 and S0 produces an immediate transmission of the SEED code. Pressing and holding for more than 1.6 seconds the S0 button alone produces the SEED code word transmission (Delayed Seed).

3.5 RF Enable and Transmitter Interface

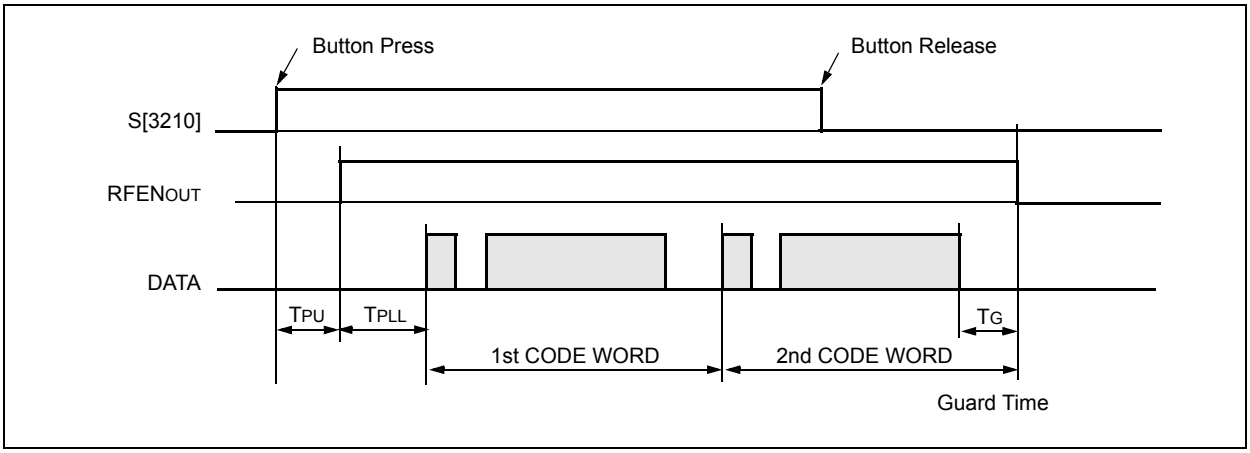
The S3/RFENOUT pin of the rfHCS362 can be configured to function as an RF Enable output signal. This is selected by the RF Enable Output (RFEN) configuration option as described in Section 4.5.13. When enabled, this pin will be driven HIGH before data is transmitted through the DATA pin.

The RFENOUT and DATA pins are synchronized to interface with the transmitter. Figure 3-11 shows the start-up sequence. A button is debounced and the EEPROM counter advanced during the power-up delay (TPU). Then the RFENOUT pin goes high to enable the transmitter. The DATA output is delayed to give the transmitter crystal oscillator and PLL time to startup (TPLL). The RFENOUT signal will go LOW one guard time after the end of the last code word.

When the RF Enable output is selected, the S3 pin can still be used as a button input. However, only minimum code words will be transmitted. An alternative solution for more than three push buttons can be the switching diode circuit described in Section 1.2.

In typical implementations of the rfHCS362G/362F, the encoder RFENOUT pin is connected to the transmitter RFENIN pin.

FIGURE 3-11: PLL INTERFACE



4.0 EEPROM MEMORY ORGANIZATION

The rfHCS362G/362F contains 288 bits (18 x 16-bit words) of EEPROM memory (Table 4-1). This EEPROM array is used to store the encryption key information and synchronization value. Further descriptions of the memory array is given in the following sections.

TABLE 4-1: EEPROM MEMORY MAP

Word Address	Field	Description
0	KEY1_0	64-bit Encryption Key1 (Word 0) LSB
1	KEY1_1	64-bit Encryption Key1 (Word 1)
2	KEY1_2	64-bit Encryption Key1 (Word 2)
3	KEY1_3	64-bit Encryption Key1 (Word 3) MSB
4	KEY2_0	64-bit Encryption Key2 (Word 0) LSB
5	KEY2_1	64-bit Encryption Key2 (Word 1)
6	KEY2_2	64-bit Encryption Key2 (Word 2)
7	KEY2_3	64-bit Encryption Key2 (Word 3) MSB
8	SEED_0	Seed value (Word 0) LSB
9	SEED_1	Seed value (Word 1)
10	SEED_2	Seed value (Word 2)
11	SEED_3	Seed value (Word 3) MSB
12	CONFIG_0	Configuration Word (Word 0)
13	CONFIG_1	Configuration Word (Word 1)
14	SERIAL_0	Serial Number (Word 0) LSB
15	SERIAL_1	Serial Number (Word 1) MSB
16	SYNC	Synchronization counter
17	RES	Reserved – Set to zero

4.1 KEY_0 - KEY_3 (64-bit Encryption Key)

The 64-bit encryption key is used to create the encrypted message. This key is calculated and programmed during production using a key generation algorithm. The key generation algorithm may be different from the KEELOQ algorithm. Inputs to the key generation algorithm are typically the transmitter's serial number and the 64-bit manufacturer's code. While the key generation algorithm supplied from Microchip is the typical method used, a user may elect to create their own method of key generation.

4.2 SYNC (Synchronization Counter)

This is the 16-bit synchronization value that is used to create the hopping code for transmission. This value will be incremented after every transmission.

4.3 SEED_0, SEED_1, SEED_2, and SEED 3 (Seed Word)

This is the four word (60 bits) seed code that will be transmitted when seed transmission is selected. This allows the system designer to implement the secure learn feature or use this fixed code word as part of a different key generation/tracking process or purely as a fixed code transmission.

Note: Upper four Significant bits of SEED_3 contains extra configuration information (see Table 4-5).

4.4 SERIAL_0, SERIAL_1 (Encoder Serial Number)

SERIAL_0 and SERIAL_1 are the lower and upper words of the device serial number, respectively. There are 32 bits allocated for the serial number and a selectable configuration bit determines whether 32 or 28 bits will be transmitted. The serial number is meant to be unique for every transmitter.

TABLE 4-2: CONFIG_0

Bit Address	Field	Description	Values
0	OSC_0	Oscillator adjust	0000 - nominal 1000 - fastest 0111 - slowest
1	OSC_1		
2	OSC_2		
3	OSC_3		
4	VLOW_0	VLOW select	nominal values 000 - 2.0V 100 - 4.0V 001 - 2.1V 101 - 4.2V 010 - 2.2V 110 - 4.4V 011 - 2.3V 111 - 4.6V
5	VLOW_1		
6	VLOW_2		
7	BSEL_0	Bit rate select	00 - TE = 100 µs 01 - TE = 200 µs 10 - TE = 400 µs 11 - TE = 800 µs
8	BSEL_1		
9	MTX_0	Minimum number of code words	00 - 1 01 - 2 10 - 4 11 - 8
10	MTX_1		
11	GUARD_0	Guard time select	00 - 0 ms (1 TE) 01 - 6.4 ms + 2 TE 10 - 25.6 ms + 2 TE 11 - 76.8 ms + 2 TE
12	GUARD_1		
13	TIMOUT_0	Time-out select	00 - No Time-out 01 - 0.8 s to 0.8 s + 1 code word 10 - 3.2 s to 3.2 s + 1 code word 11 - 25.6 s to 25.6 s + 1 code word
14	TIMOUT_1		
15	CTSEL	CTSEL	0 = TIME bits 1 = CRC bits

4.5 Configuration Words

There are 36 configuration bits stored in the EEPROM array. They are used by the device to determine transmission speed, format, delays and Guard times. They are grouped in three Configuration Words: CONFIG_0, CONFIG_1 and the upper nybble of the SEED_3 word. A description of each of the bits follows this section.

4.5.1 OSC

The internal oscillator can be tuned to ±10%. (0000 selects the nominal value, 1000 the fastest value and 0111 the slowest). When programming the device, it is the programmer's responsibility to determine the optimal calibration value.

4.5.2 VLOW[0..2]

The low voltage threshold can be programmed to be any of the values shown in Table 4-2.

4.5.3 BSEL[0..1]

The basic timing element TE, determines the actual transmission Baud Rate. This translates to different code word lengths depending on the encoding format selected (Manchester or PWM), the Header length selection and the Guard time selection, from approximately 40 ms up to 220 ms. Refer to Table 4-2 for bit rate configuration. Refer to Figure 10-3 through Figure 10-6 for code word timing.

4.5.4 MTX[0..1]

MTX selects the minimum number of code words that will be transmitted. A minimum of 1, 2, 4 or 8 code words will be transmitted.

Note:	If MTX and BSEL settings in combination require a transmission sequence to exceed the TIMOUT setting, TIMOUT will take priority.

TABLE 4-3: CONFIG_1

Bit Address	Field	Description	Values
0	DISC_0	Discrimination bits	DISC[9:0]
1	DISC_1		
2	DISC_2		
...	...		
8	DISC_8		
9	DISC_9		
10	OVR_0	Overflow	OVR[1:0]
11	OVR_1		
12	XSER	Extended Serial Number	0 - Disable 1 - Enable
13	SEEDC	Seed Control	0 = Seed transmission on: S[3210] = 0001 (delay 1.6 s) S[3210] = 0101 (immediate) 1 = Seed transmission on: S[3210] = 0011 (delay 3.2 s) S[3210] = 1001 (immediate)
14	SEED_0	Seed options	00 - No Seed 01 - Limited Seed (Permanent and Delayed) 10 - Permanent and Delayed Seed 11 - Permanent Seed only
15	SEED_1		

4.5.5 GUARD

The Guard time between code words can be set to 0 ms, 6.4 ms, 25.6 ms and 76.8 ms. If during a series of code words, the output changes from Hopping Code to Seed the Guard time will increase by 3 x TE.

4.5.6 TIMOUT[0..1]

The transmission time-out can be set to 0.8 s, 3.2 s, 25.6 s or no time-out. After the time-out period, the encoder will stop transmission and enter a low power Shutdown mode.

4.5.7 DISC[0..9]

The discrimination bits are used to validate the decrypted code word. The discrimination value is typically programmed with the 10 Least Significant bits of the serial number or a fixed value.

4.5.8 OVR[0..1]

The automatically incrementing synchronization counter is at the core of generating the varying code. Since the counter is limited to 16 bits, it overflows after 65536 increments, after which the code hopping sequence repeats. In practice, this allows 20+ operations per day for ten years before repeating the sequence. In addition, two overflow bits allow the sequence to be extended further. The feature is enabled by setting to logical “1” the two overflow bits OVL0 and OVL1. The overflow bits form part of the encrypted transmission, and therefore can be examined by receiver firmware. Table 4-4 shows how the overflow bits act when they are set to one during initial device configuration.

TABLE 4-4:

Sync. Counter	OVL0	OVL1
No overflow 0-FFFFH	1	1
First overflow 2nd 0-FFFFH	0	1
Second overflow Third 0-FFFFH	0	0
Subsequent overflows	0	0

As can be seen from the table, the counter is effectively extended by one bit, that is OVL0. In addition, OVL1 provides indication of the second counter overflow. After the second overflow, OVL0 and OVL1 remain zero, providing permanent evidence of the first and second overflow events.

4.5.9 XSER

If XSER is enabled a 32-bit serial number is transmitted. If XSER is disabled a 28-bit serial number and a 4-bit function code are transmitted.

4.5.10 SEED[0..1]

The seed value which is transmitted on key combinations (0011) and (1001) can be disabled, enabled or enabled for a limited number of transmissions determined by the initial counter value.

In limited Seed mode, the device will output the seed if the sync counter (Section 4.2) is from 00hex to 7Fhex. For a counter higher than 7F, a normal hopping code will be output.

Note:	Whenever a SEED code word is output, the 4 function bits (Figure 3-10) will be set to all ones [1,1,1,1].

4.5.11 SEEDC

SEEDC selects between seed transmission on 0001 and 0101 (SEEDC = 0) and 0011 and 1001 (SEEDC = 1). The delay before seed transmission is 1.6 s for (SEEDC = 0) and 3.2 s for (SEEDC = 1).

TABLE 4-5: SEED_3

Bit Address	Field	Description	Values
0	SEED_48	Seed Most Significant word	—
1	SEED_49		
2	SEED_50		
...	...		
9	SEED_57		
10	SEED_58		
11	SEED_59		
12	LED	LED output timing	0 = V_{BOT}>V_{LOW} LED blink 200/800 ms V_{BOT}<V_{LOW} LED not blinking 1 = V_{BOT}>V_{LOW} LED blink 25/500 ms V_{BOT}<V_{LOW} LED blink once
13	MOD	Modulation Format	0 = PWM 1 = MANCHESTER
14	RFEN	RF Enable/S3 multiplexing	0 - Enabled (S3 only sensed 2 seconds after the last button is released) 1 - Disabled (S3 same as other S inputs)
15	HEADER	PWM Header Length	0 = short Header, T_H = 3 x T_E 1 = standard Header, T_H = 10 x T_E

4.5.12 HEADER

When PWM mode is selected the header length (low time between preamble and data bits start) can be set to 10 x TE or 3 x TE. The 10 x TE mode is recommended for compatibility with previous KEELOQ encoder models. In Manchester mode, the header length is fixed and set to 4 x TE.

4.5.13 RFEN

RFEN selects whether the RFEN output is enabled or disabled. If enabled, S3 is only sampled 2 s after the last button is released and at the start of the first transmission. If disabled S3 functions the same as the other S inputs. For typical implementation of the rfHCS362G/362F the RFEN bit = 0.

4.6 SYNCHRONOUS MODE

In Synchronous mode, the code word can be clocked out on DATA using S2 as a clock. To enter Synchronous mode, S2 must be taken HIGH and then DATA and S0 or S1 are taken HIGH. After Synchronous mode is entered, DATA and S2 must be taken LOW. The data is clocked out on DATA on every falling edge of S2. Auto-shutoff timer is not disabled in Synchronous mode. Refer to Figure 4-1 and Figure 4-2.

FIGURE 4-1: SYNCHRONOUS TRANSMISSION MODE

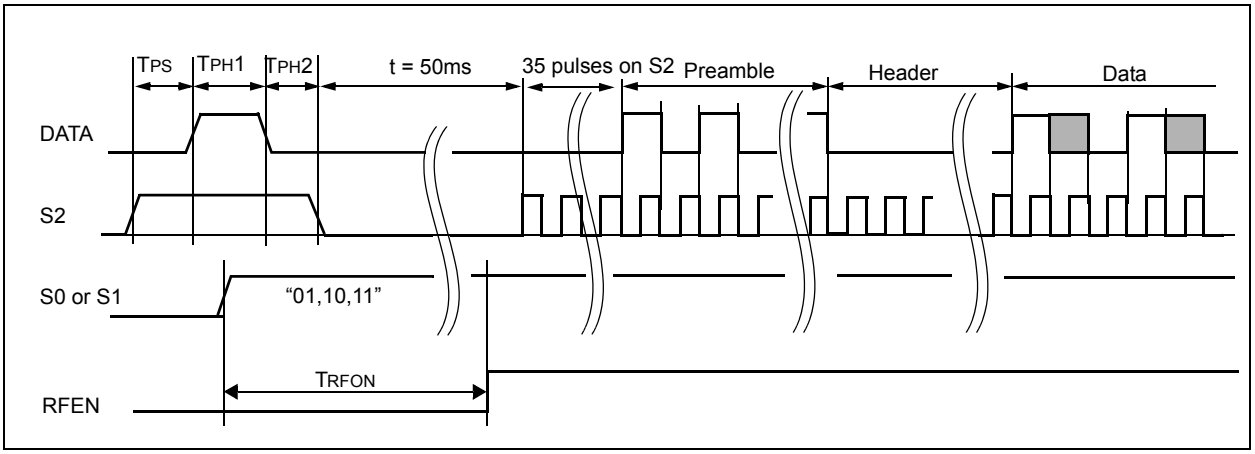
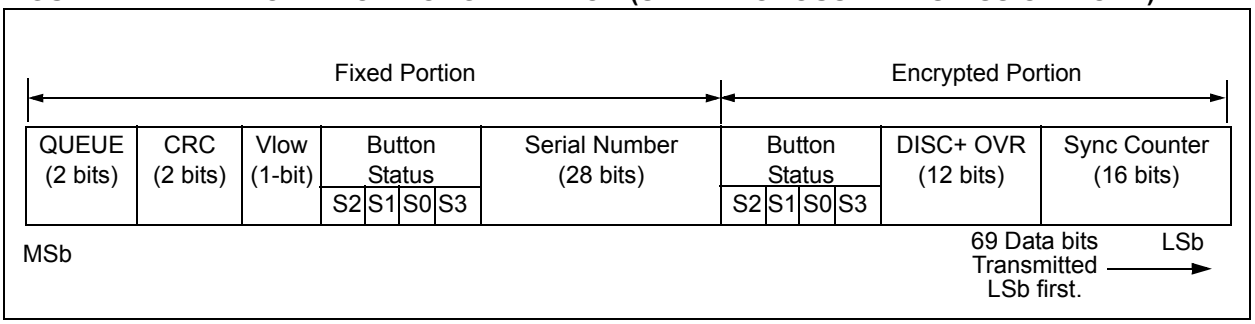


FIGURE 4-2: CODE WORD ORGANIZATION (SYNCHRONOUS TRANSMISSION MODE)



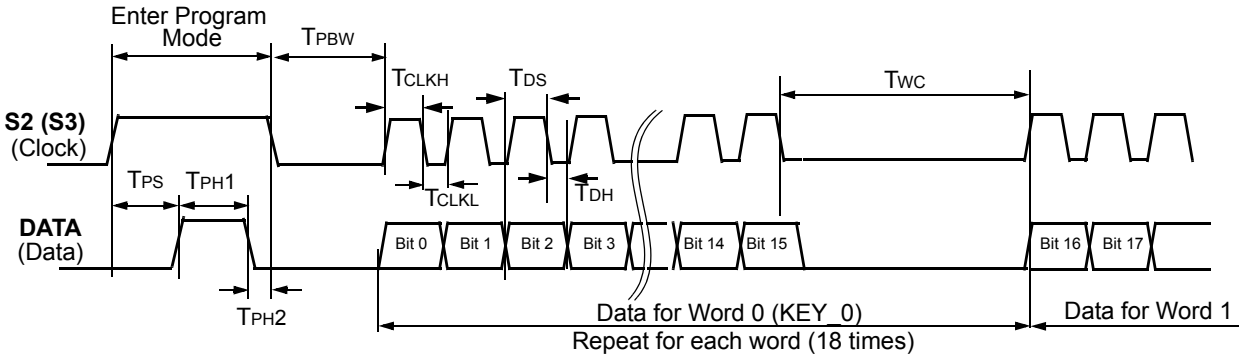
5.0 PROGRAMMING THE rfHCS362G/362F

When using the rfHCS362G/362F in a system, the user will have to program some parameters into the device, including the serial number and the secret key before it can be used. The programming cycle allows the user to input all 288 bits in a serial data stream, which are then stored internally in EEPROM. Programming will be initiated by forcing the DATA line HIGH, after the S2 line has been held HIGH for the appropriate length of time (Table 10-3 and Figure 5-1). After the Program mode is entered, a delay must be provided to the device for the automatic bulk write cycle to complete. This will write all locations in the EEPROM to an all zeros pattern including the OSC calibration bits.

The device can then be programmed by clocking in 16 bits at a time, using S2 as the clock line and DATA as the data in-line. After each 16-bit word is loaded, a programming delay is required for the internal program cycle to complete. This delay can take up to Twc. At the end of the programming cycle, the device can be verified (Figure 5-2) by reading back the EEPROM. Reading is done by clocking the S2 line and reading the data bits on DATA. For security reasons, it is not possible to execute a Verify function without first programming the EEPROM. **A Verify operation can only be done once, immediately following the Program cycle**.

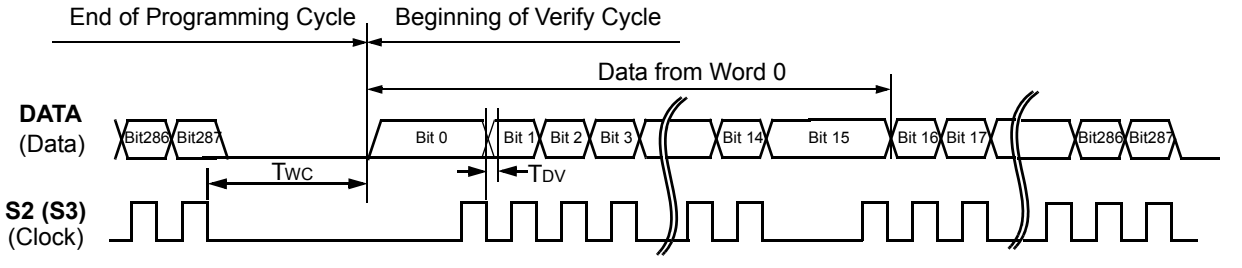
Note:	To ensure that the device does not accidentally enter Programming mode, DATA should never be pulled high by the circuit connected to it. Special care should be taken when driving circuits other than the RFENIN.

FIGURE 5-1: PROGRAMMING WAVEFORMS



Note 1: Unused button inputs to be held to ground during the entire programming sequence.
2: The VDD pin must be taken to ground after a Program/Verify cycle.

FIGURE 5-2: VERIFY WAVEFORMS



Note: If a Verify operation is to be done, then it must immediately follow the Program cycle.

6.0 UHF ASK/FSK TRANSMITTER

6.1 Transmitter Operation

The transmitter is a fully integrated UHF ASK/FSK transmitter consisting of crystal oscillator, Phase-Locked Loop (PLL), open-collector differential-output Power Amplifier (PA), and mode control logic. External components consist of bypass capacitors, crystal, and PLL loop filter. The rfHCS362G is capable of Amplitude Shift Keying (ASK) modulation. The rfHCS362F is capable of ASK or Frequency Shift Keying (FSK) modulation by employing an internal FSK switch to pull the transmitter crystal via a second load capacitor.

Figure 2-1 shows the internal structure of the transmitter. Transmitter connections are independent from the encoder to provide for maximum design flexibility. Example application circuits for ASK or FSK modulation are presented in Section 1.2.

The rfHCS362G/362F are radio frequency (RF) emitting devices. Wireless RF devices are governed by a country's regulating agency. For example, in the United States it is the Federal Communications Committee (FCC) and in Europe it is the European Conference of Postal and Telecommunications Administrations (CEPT). It is the responsibility of the designer to ensure that their end product conforms to rules and regulations of the country of use and/or sale.

RF devices require correct board level implementation in order to meet regulatory requirements. Layout considerations are listed at the end of each subsection. It is best to place a ground plane on the PCB to reduce radio frequency emissions and cross talk.

6.2 Supply Voltage (V_{DDRF}, V_{SSRF})

Pins V_{DDRF} and V_{SSRF} supply power and ground respectively to the transmitter. These power pins are separate from power supply pins V_{DD} and V_{SS} to the encoder.

Layout Considerations - Provide low impedance power and ground traces to minimize spurious emissions. A two-sided PCB with a ground plane on the bottom layer is highly recommended. Separate bypass capacitors should be connected as close as possible to each of the supply pins V_{DD} and V_{DDRF}. Connect V_{SS} and V_{SSRF} to the ground plane using separate PCB vias. Do not share a PCB via with multiple ground traces.

6.3 Crystal Oscillator

The transmitter crystal oscillator is a Colpitts oscillator that provides the reference frequency to the PLL. It is independent from the encoder oscillator. An external crystal or AC coupled reference signal is connected to the XTAL pin. The transmit frequency is fixed and determined by the crystal frequency according to the formula:

$$f_{transmit} = f_{XTAL} \times 32$$

Due to the flexible selection of transmit frequency, the resulting crystal frequency may not be a standard off-the-shelf value. Therefore, for some carrier frequencies the designer will have to consult a crystal manufacturer and have a custom crystal manufactured. Crystal parameters are listed in Table 6-1. For background information on crystal selection see Application Note AN588, PIC® Microcontroller Oscillator Design Guide, and AN826 Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PIC MCU Devices.

The crystal oscillator start time (t_{on}) is listed in Table 10-7, Transmitter AC Characteristics.

TABLE 6-1: CRYSTAL PARAMETERS

Sym	Characteristic	Min	Max	Units	Conditions
f_{XTAL}	Crystal Frequency	9.69	15	MHz	Parallel Resonant Mode
C_L	Load Capacitance	10	15	pF	
C_O	Shunt Capacitance	—	7	pF	
ESR	Equivalent Series Resistance	—	60	Ω	
These values are for design guidance only.					

6.3.1 CRYSTAL OSCILLATOR ASK OPERATION

The rfHCS362G/362F crystal oscillator can be configured for ASK operation. Figure 6-1 shows an example ASK circuit.

Capacitor C1 trims the crystal load capacitance to the desired circuit load capacitance and places the crystal on the desired frequency.

FIGURE 6-1: EXAMPLE ASK EXTERNAL CRYSTAL CIRCUIT

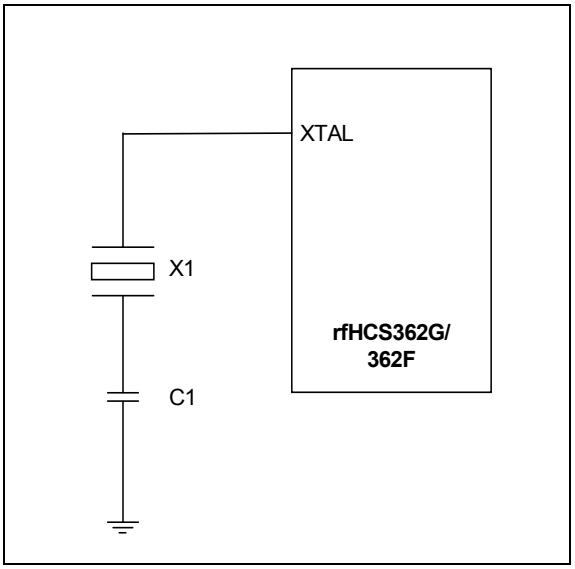


TABLE 6-2: XTAL OSC APPROXIMATE FREQ. VS. CAPACITANCE (ASK MODE) (1)

C1	Predicted Frequency (MHz)	PPM from 13.55 MHz	Transmit Frequency (MHz) (32 * f_{XTAL})
22 pF	13.551438	+106	433.646
39 pF	13.550563	+42	433.618
100 pF	13.549844	-12	433.595
150 pF	13.549672	-24	433.5895
470 pF	13.549548	-33	433.5856
1000 pF	13.549344	-48	433.579

Note 1: Standard Operating Conditions (unless otherwise stated) T_A = 25°C, RF_{EN} = 1, V_{DDRF} = 3V, f_{XTAL} = 13.55 MHz

6.3.2 CRYSTAL OSCILLATOR FSK OPERATION

The rfHCS362F crystal oscillator can be configured for FSK operation. Figure 6-2 shows an example FSK circuit. Capacitors C1 and C2 achieve FSK modulation by pulling the crystal. When DATAFSK = 1, FSKOUT is high-impedance effectively coupling only capacitor C1 to the crystal and the resulting transmit frequency equals fMAX. When DATAFSK = 0, FSKOUT is grounded to VSSRF and will parallel capacitor C2 with C1. The resulting transmit frequency will equal fMIN.

Selecting the appropriate values for C1 and C2 sets the center frequency and frequency deviation. Capacitor C1 sets fMAX and capacitors C1 and C2 in parallel set fMIN. The graph in Figure 6-3 illustrates this relationship. The transmit center frequency f_C is defined as:

$$f_c = \frac{f_{max} + f_{min}}{2}$$

The frequency deviation of the transmit frequency is defined as:

$$\Delta f = \frac{f_{max} - f_{min}}{2}$$

Layout considerations - Avoid parallel traces in order to reduce circuit stray capacitance. Keep traces as short as possible. Isolate components to prevent coupling. Use ground traces to isolate signals.

TABLE 6-3: TYPICAL TRANSMIT CENTER FREQUENCY AND FREQUENCY DEVIATION (FSK MODE) (1)

	C2 = 1000 pF	C2 = 100 pF	C2 = 47 pF
C1 (pF)	Freq (MHz) / Dev (kHz)	Freq (MHz) / Dev (kHz)	Freq (MHz) / Dev (kHz)
22	433.612 / 34	433.619 / 27	433.625 / 21
33	433.604 / 25	433.610 / 19	433.614 / 14
39	433.598 / 20	433.604 / 14	433.608 / 10
47	433.596 / 17	433.601 / 11.5	433.604 / 8
68	433.593 / 13	433.598 / 9	433.600 / 5.5
100	433.587 / 8	—	—

Note 1: Standard Operating Conditions (unless otherwise stated) TA = 25°C, RFEN = 1, VDDRF = 3V, fXTAL = 13.55 MHz

FIGURE 6-2: EXAMPLE FSK EXTERNAL CRYSTAL CIRCUIT

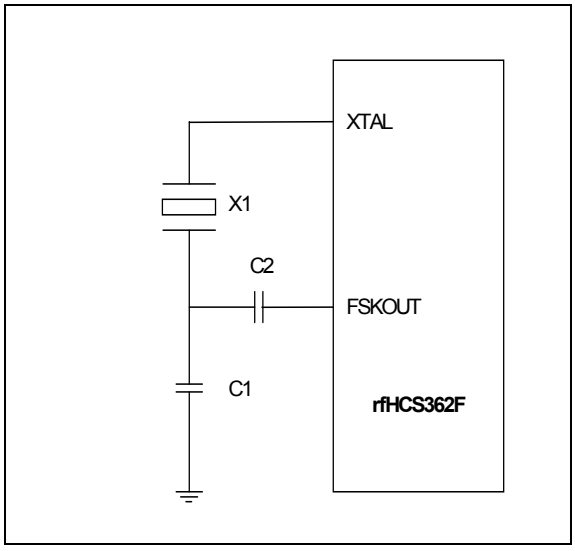
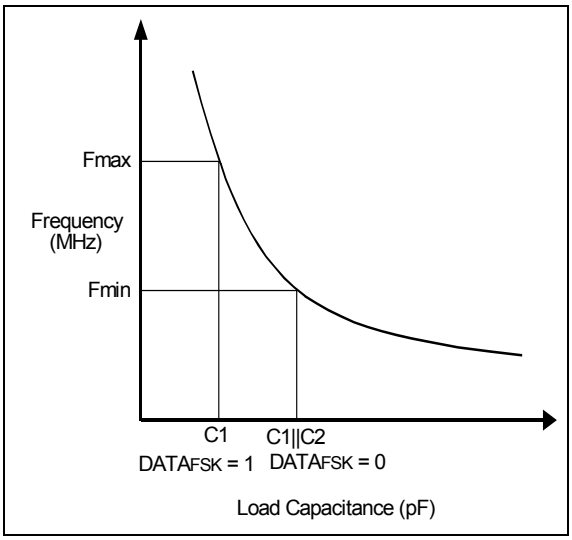


FIGURE 6-3: LOAD CAPACITANCE VERSUS CHANGE IN TRANSMITTED FREQUENCY



6.4 Clock Output (CLKOUT)

The crystal oscillator feeds a divide-by-four circuit that provides a clock output at the CLKOUT pin. CLKOUT is slew-rate limited in order to keep spurious signal emissions as low as possible. The voltage swing (V_{CLKOUT}) depends on the capacitive loading (C_{LOAD}) on the CLKOUT pin (2 V_{PP} at 5 pF).

Layout considerations - Shield each side of the clock output trace with ground traces to isolate the CLKOUT signal and reduce coupling.

6.5 Phase-Locked Loop (PLL)

The PLL consists of a Phase-frequency Detector (PFD), charge pump, Voltage-controlled Oscillator (VCO), and fixed divide-by-32 divider. An external loop filter is connected to pin LF. The loop filter controls the dynamic behavior of the PLL, primarily lock time and spur levels. The application determines the loop filter requirements.

The rfHCS362 employs a charge pump PLL that offers many advantages over the classical voltage phase detector PLL: infinite pull-in range and zero steady state phase error. The charge pump PLL allows the use of passive loop filters that are lower cost and minimize noise. Charge pump PLLs have reduced flicker noise thus limiting phase noise. Many of the classical texts on PLLs do not cover this type of PLL, however, today this is the most common type of PLL. This data sheet briefly covers the general terms and design requirements for the rfPIC. Detailed PLL design and operation is beyond the scope of this data sheet. For more information, the designer is referred to "*PLL Performance, Simulation, and Design*," Second Edition by Dean Banerjee ISBN 0970820704. Banerjee covers charge pump PLLs and loop filter selection.

The loop filter has a major impact on lock time and spur levels. Lock time is the time it takes the PLL to lock on frequency. When the PLL is first powered on or is changing frequencies, no data can be transmitted. Lock time must be considered before data transmission can begin. In addition to PLL lock time, the designer must take into account the crystal oscillator start time of approximately 1 ms. See Section 6.3 for more information about the crystal oscillator. Reference spurs occur at the carrier frequency plus and minus integer multiples of the reference frequency. Phase noise refers to noise generated by the PLL. Spur levels and phase noise can increase the signal to noise ratio (SNR) of the system and mask or degrade the transmitted signal.

The first order effect on PLL performance is loop bandwidth. Loop bandwidth (ω_L) is defined as the point where the open loop phase transfer function equals 0 dB. Selecting a small loop bandwidth results in lower spur levels but slower lock time. Selecting a larger loop bandwidth results in a faster lock time but higher spur levels.

Second order effects on PLL performance is Phase margin (ϕ) and Damping factor (ζ). Phase margin is a measure of PLL stability. Choosing a phase margin that is too low will result in PLL instability. Choosing a higher phase margin results in less ringing and faster lock time at the expense of higher spur levels. Loop filters are typically designed for a total phase margin between 30 and 70 degrees. The aim of the designer is to choose a loop bandwidth and phase margin that gives the fastest possible lock time and meets the spur level requirements of the application.

Damping factor governs the second order transient response that determines the shape of the exponential envelope of the natural frequency. The natural frequency, also called ringing frequency, is the frequency of the VCO steering voltage as the PLL settles. Lock time is proportional to damping factor and inversely proportional to loop bandwidth.

The application determines the loop filter component requirements. For example, if the transmit frequency selected is near band edges or restricted bands, spur levels must be reduced to meet regulatory requirements. However, this will be at the expense of lock time. For an FSK application, a larger damping factor ($\cong$ 1.0) is desired so that there is less overshoot in the keying of FSK. For an ASK application, a damping factor = 0.707 results in less settling time and near optimum noise performance.

Figure 6-4 shows an example passive second order loop filter circuit. Table 6-4 gives example loop filter values for a crystal frequency of 13.56 MHz and transmit frequency of 433.92 MHz. Table 6-5 gives example loop filter values for a crystal frequency of 9.84375 MHz and transmit frequency of 315 MHz.

Layout considerations - Keep traces short and place loop filter components as close as possible to the LF pin.

FIGURE 6-4: EXAMPLE LOOP FILTER CIRCUIT

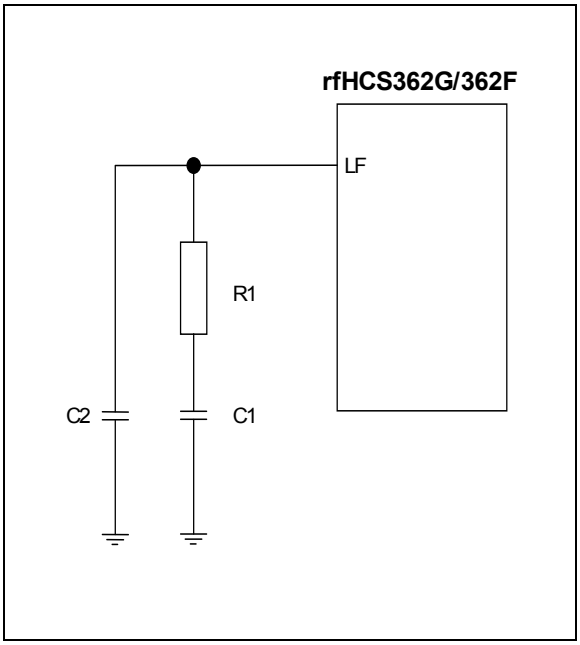


TABLE 6-4: EXAMPLE LOOP FILTER VALUES FOR TRANSMIT FREQUENCY = 433.92 MHz (1)

C1	C2	R1	Loop BW	Fn (natural freq in Hz)	Phase Margin (not counting sampling delay)	2nd Order damping factor	Calculated Lock Time
0.01 uF	390 pF	680	165 kHz	64 kHz	65 deg	1.37	47 µs
3900 pF	100 pF	1.5K	360 kHz	103 kHz	63 deg	1.89	29 µs
1500 pF	47 pF	2.7K	610 kHz	166 kHz	55 deg	2.10	18 µs
1000 pF	18 pF	4.7K	1.05 MHz	203 kHz	50 deg	3.0	15 µs
Note 1: Standard Operating Conditions (unless otherwise stated) T_A = 25°C, RF_{EN} = 1, V_{DDRF} = 3V.							

TABLE 6-5: EXAMPLE LOOP FILTER VALUES FOR TRANSMIT FREQUENCY = 315 MHz (1)

C1	C2	R1	Loop BW	Fn (natural freq in Hz)	Phase Margin (not counting sampling delay)	2nd Order damping factor	Calculated Lock Time
3900 pF	390 pF	680	190 kHz	112 kHz	55 deg	0.94	27 µs
3900 pF	680 pF	680	175 kHz	112 kHz	47 deg	0.94	27 µs
3900 pF	1000 pF	680	155 kHz	112 kHz	39 deg	0.94	27 µs
Note 1: Standard Operating Conditions (unless otherwise stated) T_A = 25°C, RF_{EN} = 1, V_{DDRF} = 3V.							

6.6 Power Amplifier

The PLL output feeds the power amplifier (PA). The open-collector differential output (ANT1, ANT2) can be used to drive a loop antenna directly or converted to single-ended output via an impenance matching network or balanced-to-unbalanced (balun) transformer. Pins ANT1 and ANT2 are open-collector outputs and must be pulled-up to VDDRF through the load.

The differential output of the PA should be matched to an impedance of 800 to 1000 Ω. Failure to match the impedance may cause excessive spurious and harmonic emissions. For more information see Application Note AN831, Matching Small Loop Antennas to rfPIC Devices.

The transmit output power can be adjusted in six discrete steps from +2 dBm to -12 dBm by varying the voltage (VPS) at the PS/DATAASK pin. Figure 6-5 shows an example voltage divider network for ASK operation and Figure 6-6 for FSK operation.

For FSK operation, the PS/DATAASK pin only serves as a Power Select (PS) pin. An internal 20 µA current source pushes current through the PS/DATAASK pin resulting in a voltage drop across resistor R2 at the VPS level selected for transmitter output power. VPS selects the PA bias current. Higher transmit power will draw higher current.

For ASK operation, the function of the PS/DATAASK pin is to turn the Power Amplifier (PA) on and off. Resistors R1 and R2 form a voltage divider network to apply voltage VPS for the selected transmitter output power. If maximum transmitter output is desired, the output of a GP0 pin can be connected directly to PS/DATAASK.

Table 6-6 lists typical values for R1 and R2 for both the ASK and FSK modes.

.

Note: PS/DATAASK is driven low when RFENIN = 0. Make sure external circuitry on PS/DATAASK does not conflict by driving the pin high. The encoder DATA output works because it is low if RFENOUT is low

FIGURE 6-5: EXAMPLE ASK POWER SELECT CIRCUIT

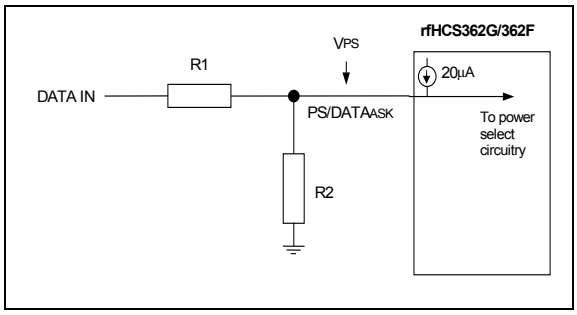


FIGURE 6-6: EXAMPLE FSK POWER SELECT CIRCUIT

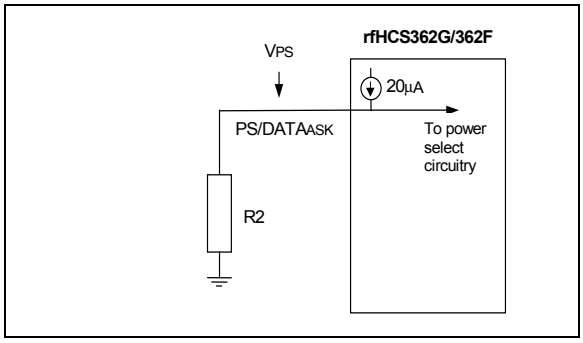


TABLE 6-6: POWER SELECT (1)

Transmitter Output Power (dBm)	Transmitter Operating Current (mA)	Power Select (PS) Voltage VPS (Volts) (2)	ASK		FSK
			R1 (Ω)	R2 (Ω) (3)	R2 (Ω)
+2	11.5	≥2.0	2400	4700	≥75K
-1	8.6	1.2	6800	4700	56K
-4	7.3	0.9	11K	4700	47K
-7	6.2	0.7	15K	4700	39K
-10	5.3	0.5	24K	4700	27K
-12	4.8	0.3	43K	4700	15K
-60	<4.8	<0.1	OPEN	4700	4700

Note 1: Standard Operating Conditions (unless otherwise stated) T_A = 25°C, RF_{EN} = 1, V_{DDRF} = 3V, $f_{TRANSMIT}$ = 433.92 MHz

2: V_{PS} is actual voltage on PS/$DATA_{ASK}$ pin.

3: The Power Select circuitry contains an internal 20 μA current source. To ensure that the transmitter output power is at the minimum when transmitting a $DATA_{ASK}$ = 0 (V_{SSRF}), select the value of resistor R2 such that the voltage drop across it is less than 0.1 volts.

6.7 Mode Control Logic

The mode control logic pin RFENIN controls the operation of the transmitter (Table 6-7). When RFENIN goes high, the crystal oscillator starts up. The voltage on the LF pin ramps up proportionally to the RF frequency. The PLL can lock onto the frequency faster than the starting up crystal can stabilize. When the LF pin reaches 0.8V, the RF frequency is close to locked on the crystal frequency. This initiates a 150 microsecond delay to ensure that the PLL settles. After the delay, the PS/DATAASK bias current and power amplifier are enabled to start transmitting.

When RFENIN goes low, the transmitter goes into low power Standby mode. The power amplifier is disabled, the crystal oscillator stops, and the PS/DATAASK pin is driven low. This will be a conflict if other circuitry drives the PS/DATAASK pin high while RFENIN is low. The encoder DATA pin is typically the only connection to PS/DATAASK and it always drives DATA low before RFENOUT goes low.

For most applications the RFENIN pin is connected directly to the RFENOUT pin. The RFENIN pin has an internal pull-down resistor.

TABLE 6-7: RFENIN PIN STATES

RFEN	Description
0	Transmitter and CLKOUT in Standby
1	Transmitter and CLKOUT enabled

7.0 INTEGRATING THE rfHCS362G/362F INTO THE SYSTEM

Use of the rfHCS362G/362F in a system requires a compatible decoder. This decoder is typically a microcontroller with compatible firmware. Microchip will provide (via a license agreement) firmware routines that accept transmissions from the rfHCS362G/362F and decrypt the hopping code portion of the data stream. These routines provide system designers the means to develop their own decoding system.

7.1 Learning a Transmitter to a Receiver

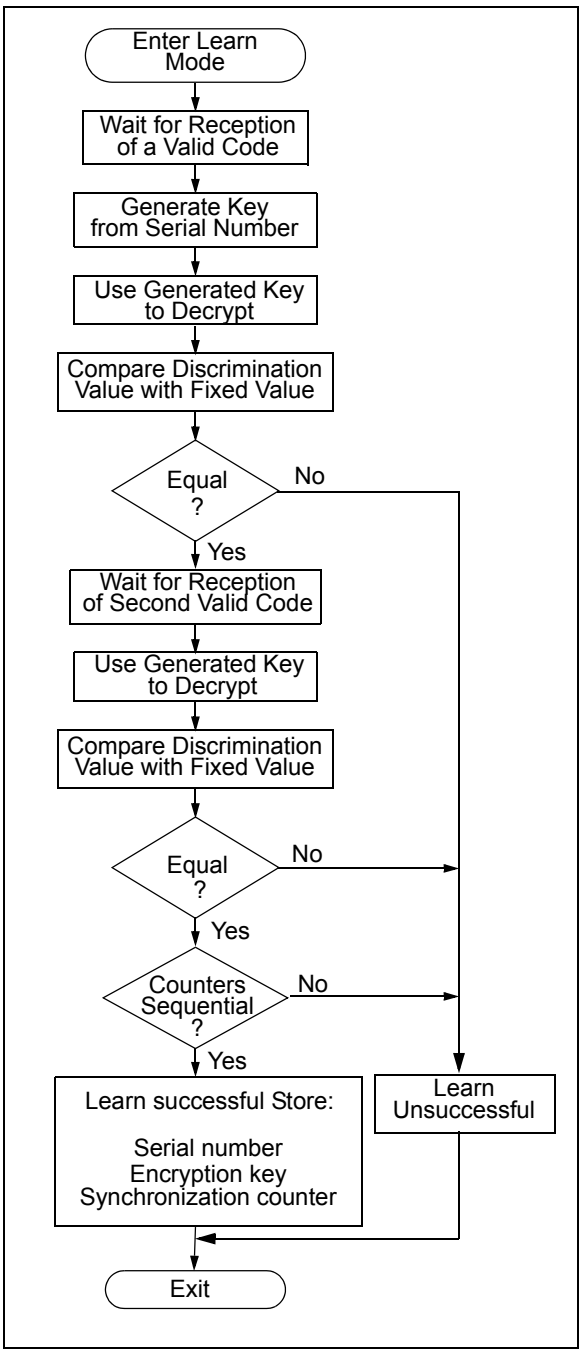
A transmitter must first be 'learned' by a decoder before its use is allowed in the system. Several learning strategies are possible, Figure 7-1 details a typical learn sequence. Core to each, the decoder must minimally store each learned transmitter's serial number and current synchronization counter value in EEPROM. Additionally, the decoder typically stores each transmitter's unique encryption key. The maximum number of learned transmitters will therefore be relative to the available EEPROM.

A transmitter's serial number is transmitted in the clear but the synchronization counter only exists in the code word's encrypted portion. The decoder obtains the counter value by decrypting using the same key used to encrypt the information. The KEELOQ algorithm is a symmetrical block cipher so the encryption and decryption keys are identical and referred to generally as the encryption key. The encoder receives its encryption key during manufacturing. The decoder is programmed with the ability to generate an encryption key as well as all but one required input to the key generation routine; typically the transmitter's serial number.

Figure 7-1 summarizes a typical learn sequence. The decoder receives and authenticates a first transmission; first button press. Authentication involves generating the appropriate encryption key, decrypting, validating the correct key usage via the discrimination bits and buffering the counter value. A second transmission is received and authenticated. A final check verifies the counter values were sequential; consecutive button presses. If the learn sequence is successfully complete, the decoder stores the learned transmitter's serial number, current synchronization counter value and appropriate encryption key. From now on the encryption key will be retrieved from EEPROM during normal operation instead of recalculating it for each transmission received.

Certain learning strategies have been patented and care must be taken not to infringe.

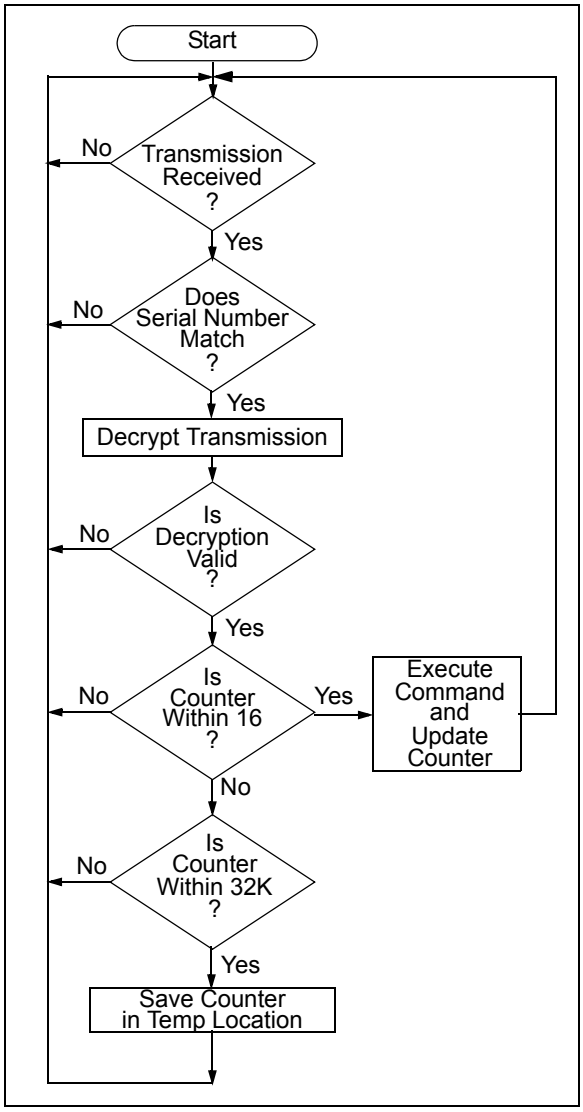
FIGURE 7-1: TYPICAL LEARN SEQUENCE



7.2 Decoder Operation

Figure 7-2 summarizes normal decoder operation. The decoder waits until a transmission is received. The received serial number is compared to the EEPROM table of learned transmitters to first determine if this transmitter's use is allowed in the system. If from a learned transmitter, the transmission is decrypted using the stored encryption key and authenticated via the discrimination bits for appropriate encryption key usage. If the decryption was valid the synchronization value is evaluated.

FIGURE 7-2: TYPICAL DECODER OPERATION



7.3 Synchronization with Decoder (Evaluating the Counter)

The KEELOQ technology patent scope includes a sophisticated synchronization technique that does not require the calculation and storage of future codes. The technique securely blocks invalid transmissions while providing transparent resynchronization to transmitters inadvertently activated away from the receiver.

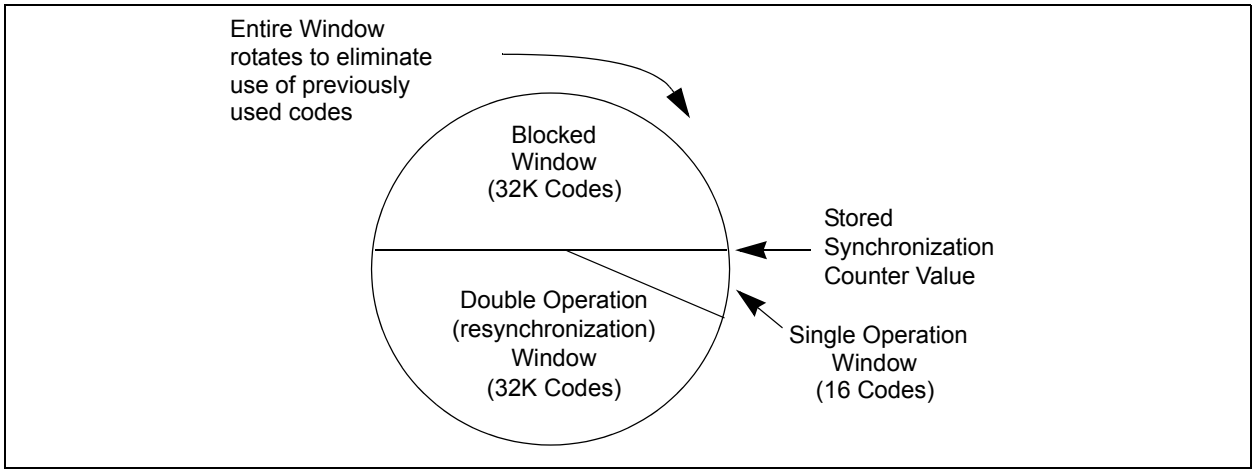
Figure 7-3 shows a 3-partition, rotating synchronization window. The size of each window is optional but the technique is fundamental. Each time a transmission is authenticated, the intended function is executed and the transmission's synchronization counter value is stored in EEPROM. From the currently stored counter value there is an initial "Single Operation" forward window of 16 codes. If the difference between a received synchronization counter and the last stored counter is within 16, the intended function will be executed on the single button press and the new synchronization counter will be stored. Storing the new synchronization counter value effectively rotates the entire synchronization window.

A "Double Operation" (resynchronization) window further exists from the Single Operation window up to 32K codes forward of the currently stored counter value. It is referred to as "Double Operation" because a transmission with synchronization counter value in this window will require an additional, sequential counter transmission prior to executing the intended function. Upon receiving the sequential transmission the decoder executes the intended function and stores the synchronization counter value. This resynchronization occurs transparently to the user as it is human nature to press the button a second time if the first was unsuccessful.

The third window is a "Blocked Window" ranging from the double operation window to the currently stored synchronization counter value. Any transmission with synchronization counter value within this window will be ignored. This window excludes previously used, perhaps code-grabbed transmissions from accessing the system.

Note:	The synchronization method described in this section is only a typical implementation and because it is usually implemented in firmware, it can be altered to fit the needs of a particular system.

FIGURE 7-3: SYNCHRONIZATION WINDOW



8.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

8.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

8.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

8.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

8.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

8.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

8.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

8.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

8.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

8.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

8.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

8.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

8.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

8.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

9.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Ambient Temperature under bias ..... -40°C to +85°C

Storage Temperature ..... -40°C to +125°C

Total Power Dissipation(1) ..... 700 mW

Absolute Maximum Ratings Encoder

Voltage on V_{DD} with respect to V_{SS} ..... -0.3 to +6.6V

Max. Output Current sunk by any I/O pin ..... 20 mA

Max. Output Current sourced by any I/O pin ..... 20 mA

Voltage on all other Encoder pins with respect to V_{SS} ..... -0.3 V to (V_{DD} + 0.3V)

Absolute Maximum Ratings Transmitter

Voltage on V_{DDRF} with respect to V_{SSRF} ..... -0.3 to +7.0V

Max. Voltage on $RFEN_{IN}$ and $DATA_{FSK}$ pins with respect to V_{SSRF} ..... -0.3 to (V_{DDRF} +0.3V)

Max. Current into $RFEN_{IN}$ and $DATA_{FSK}$ pins ..... -1.0 to 1.0 mA

Note 1: Power Dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum\{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL}) + V_{DDRF} \times \{I_{DDRF} - \sum I_{OHRF}\} + \sum\{(V_{DDRF}-V_{OHRF}) \times I_{OHRF}\}$$

†NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.0 DC CHARACTERISTICS

TABLE 10-1: ENCODER DC CHARACTERISTICS

Industrial (I): T_{AMB} = -40 °C to +85 °C						
		2.0V < V_{DD} < 6.3				
Parameter	**Sym.**	**Min.**	**Typ.(1)**	**Max.**	**Unit**	**Conditions**
Operating current (avg.)	I_{CC}	—	0.3	1.2	mA	V_{DD} = 6.3V
Standby current	I_{CCS}	—	0.1	1.0	μA	V_{DD} = 6.3V
High level Input voltage	V_{IH}	0.65 V_{DD}	—	V_{DD} + 0.3	V	V_{DD} = 2.0V
Low level input voltage	V_{IL}	-0.3	—	0.15 V_{DD}	V	V_{DD} = 2.0V
High level output voltage	V_{OH}	0.7 V_{DD} 0.7 V_{DD}	—	—	V	I_{OH} = -1.0 mA, V_{DD} = 2.0V I_{OH} = -2.0 mA, V_{DD} = 6.3V
Low level output voltage	V_{OL}	—	—	0.15 V_{DD} 0.15 V_{DD}	V	I_{OL} = 1.0 mA, V_{DD} = 2.0V I_{OL} = 2.0 mA, V_{DD} = 6.3V
RFEN pin high drive	I_{RFEN}	0.5 1.0	1 2.5	3.0 5.0	mA	V_{RFEN} = 1.4V V_{DD} = 2.0V V_{RFEN} = 4.4V V_{DD} = 6.3V
$\overline{LED}$ sink current	I_{LEDL} I_{LEDH}	1.0 2.0	3.5 4.5	6.0 7.0	mA mA	V_{LED} = 1.5V, V_{DD} = 3.0V V_{LED} = 1.5V, V_{DD} = 6.3V
Pull-down Resistance; S0-S3	R_{S0-3}	40	60	80	KΩ	V_{DD} = 4.0V
Pull-down Resistance; PWM	R_{PWM}	80	120	160	KΩ	V_{DD} = 4.0V

Note 1: Typical values are at 25 °C.

FIGURE 10-1: POWER-UP AND TRANSMIT TIMING

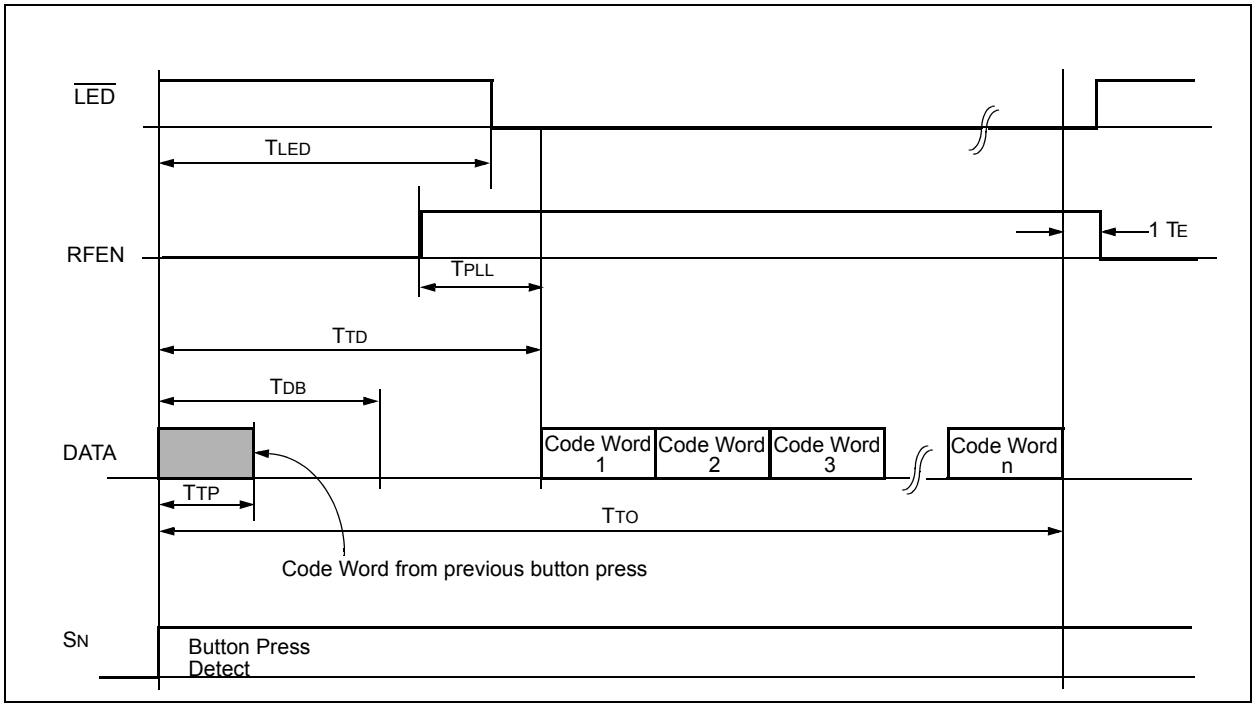


TABLE 10-2: POWER-UP AND TRANSMIT TIMING REQUIREMENTS(3)

VDD = +2.0 to 6.3V Industrial(I):TAMB = -40 °C to +85 °C						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Remarks**
Transmit delay from button detect	TTD	26	30	40	ms	**(Note 1)**
Debounce delay	TDB	18	20	22	ms	—
Auto-shutoff time-out period (TIMO=10)	TTO	23.4	25.6	28.16	s	**(Note 2)**
Button press to RFEN	TPU	20	26	38	ms	—
RFEN to code word	TPLL	2	4	6	ms	—
LED on after key press	TLED	25	—	45	ms	—
Time to terminate code word from previous button press	TTP	—	—	10 ms	—	—

Note 1: Transmit delay maximum value if the previous transmission was successfully transmitted.
2: The Auto-shutoff time-out period is not tested.
3: These values are characterized but not tested

TABLE 10-3: PROGRAMMING/VERIFY TIMING REQUIREMENTS

V_{DD} = 5.0 ± 10% 25°C ± 5°C						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Remarks**
Program mode setup time	T_{PS}	3.5	—	4.5	ms	
Hold time 1	T_{PH1}	3.5	—	—	ms	
Hold time 2	T_{PH2}	50	—	—	µs	
Bulk Write time	T_{PBW}	4.0	—	—	ms	
Program delay time	T_{PROG}	4.0	—	—	ms	
Program cycle time	T_{WC}	50	—	—	ms	
Clock low time	T_{CLKL}	50	—	—	µs	
Clock high time	T_{CLKH}	50	—	—	µs	
Data setup time	T_{DS}	0	—	—	µs	
Data hold time	T_{DH}	30	—		µs	
Data out valid time	T_{DV}	—	—	30	µs	

FIGURE 10-2: PWM DATA FORMAT (MOD = 0)

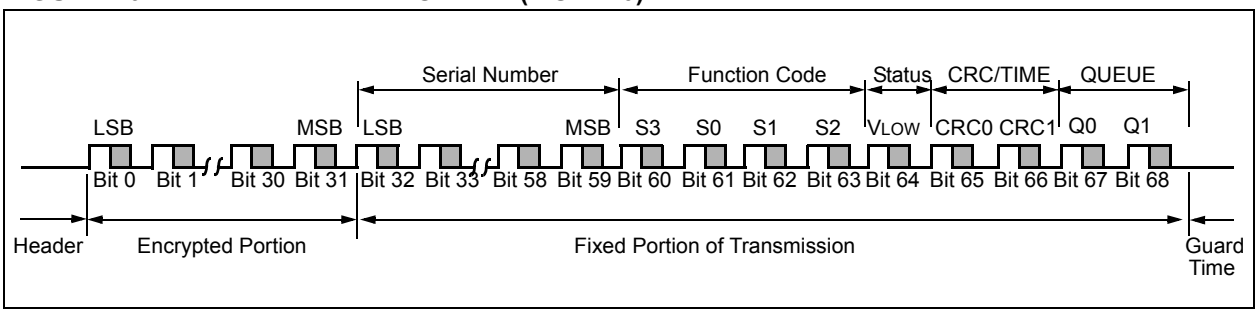


FIGURE 10-3: PWM FORMAT SUMMARY (MOD=0)

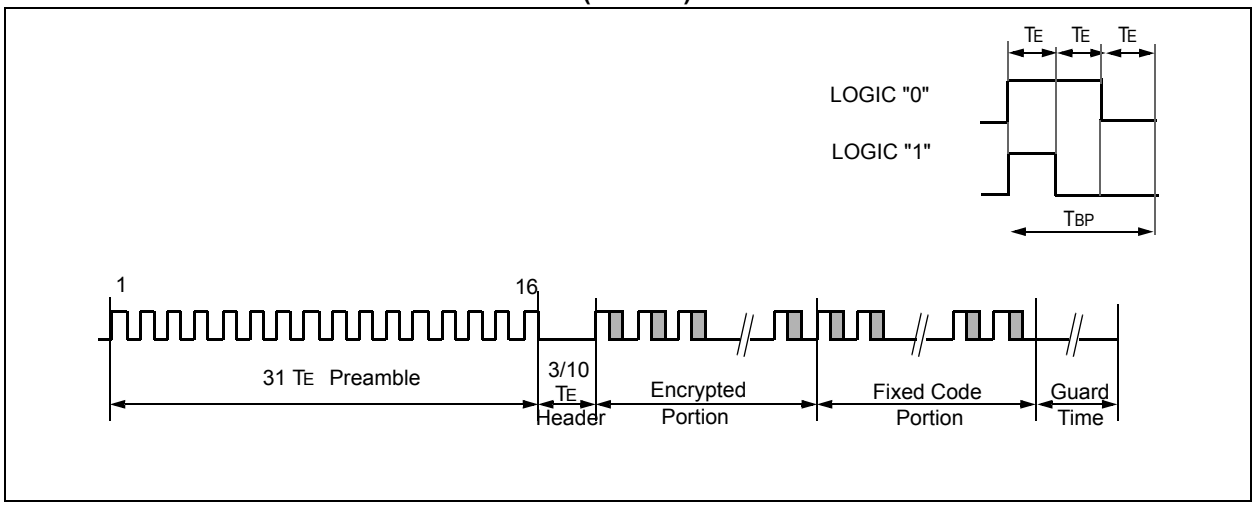


FIGURE 10-4: PWM PREAMBLE/HEADER FORMAT (MOD=0)

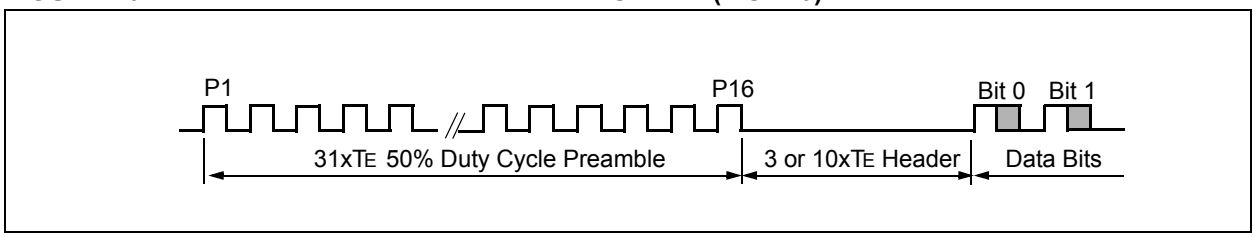


TABLE 10-4: CODE WORD TRANSMISSION TIMING PARAMETERS – PWM MODE(1,3)

VDD = +2.0V to 6.3V Industrial (I): TAMB = -40 °C to +85 °C		BSEL Value				
		11	10	01	00	
Symbol	Characteristic	Typical	Typical	Typical	Typical	Units
TE	Basic pulse element	800	400	200	100	µs
TBP	Bit width	3	3	3	3	TE
TP	Preamble duration	31	31	31	31	TE
TH	Header duration(4)	10	10	10	10	TE
TC	Data duration	207	207	207	207	TE
TG	Guard time(2)	27.2	26.4	26	25.8	ms
—	Total transmit time	220	122	74	50	ms
—	Data Rate	417	833	1667	3334	bps

Note 1: The timing parameters are not tested but derived from the oscillator clock.
2: Assuming GUARD = 10 option selected in CONFIG_0 Configuration Word.
3: Allow for a +/- 10% tolerance on the encoder internal oscillator after calibration.
4: Assuming HEADER = 1 option selected in SEED_3 Configuration Word.

FIGURE 10-5: MANCHESTER FORMAT SUMMARY (MOD=1)

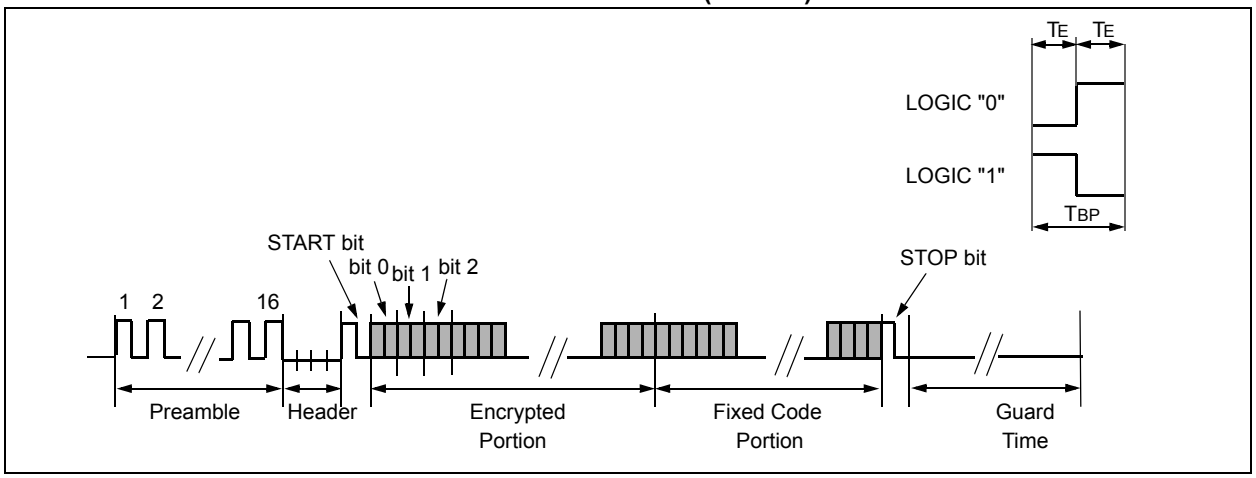


FIGURE 10-6: MANCHESTER PREAMBLE/HEADER FORMAT (MOD=1)

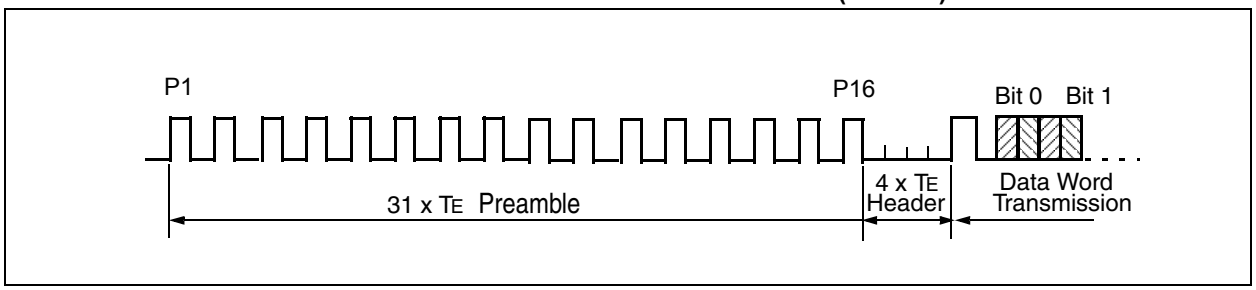


TABLE 10-5: CODE WORD TRANSMISSION TIMING PARAMETERS—MANCHESTER MODE(1,3)

VDD = +2.0V to 6.3V Industrial (I): TAMB = -40 °C to +85 °C		BSEL Value				
		11	10	01	00	
Symbol	Characteristic	Typical	Typical	Typical	Typical	Units
TE	Basic pulse element(3)	800	400	200	100	µs
TBP	Bit width	2	2	2	2	TE
TP	Preamble duration	31	31	31	31	TE
TH	Header duration	4	4	4	4	TE
TC	Data duration	138	138	138	138	TE
TG	Guard time(2)	26.8	26.4	26	25.8	ms
—	Total transmit time	166	96	61	43	ms
—	Data Rate	625	1250	2500	5000	bps

Note 1: The timing parameters are not tested but derived from the oscillator clock.
2: Assuming GUARD = 10 option selected in CONFIG_0 Configuration Word.
3: Allow for a +/- 10% tolerance on the encoder internal oscillator after calibration.

TABLE 10-6: TRANSMITTER DC CHARACTERISTICS*

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤TA ≤+85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDDRF	Supply Voltage	2.2	—	5.5	V	
	IPDRF	Power-Down Current	—	0.05	0.1	µA	RFEN = 0
	IDDRF	Supply Current	4.8	—	11.5	mA	**Note 1**
	VILRF	Input Low Voltage	-0.3	—	0.3 VSSRF	V	**Note 2**
	VIHRF	Input High Voltage	0.7 VSSRF	—	VSSRF + 0.3	V	**Note 2**
	IILRF	Input Leakage Current	-1	—	1	µA	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Depends on output power selection. See Table 6-6.

Note 2: Applies to RFEN pin.

TABLE 10-7: TRANSMITTER AC CHARACTERISTICS*

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤TA ≤+85°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	f_{xtal}	Crystal Frequency	9.69	—	15	MHz	
	$f_{transmit}$	Transmit Frequency	310	—	440	MHz	Fixed, set by f_{xtal}
	fCLKOUT	CLKOUT Frequency	2.42	—	3.75	MHz	Fixed, set by f_{xtal}
	P_o	Transmit Output Power	-12	—	+2	dBm	See Table 6-6
	fASK	ASK Data Rate	—	—	40	kbps	
	fFSK	FSK Data Rate	—	—	20	kbps	**Note 3**
	PREF	Reference Spurs (1)	—	-44	—	dBm	$f_{transmit} \pm f_{xtal}$
	PCLK	Clock Spurs (1)	—	-44	—	dBm	$f_{transmit} \pm f_{CLKOUT}$
	PHARM	Harmonic Content	—	-40	—	dBm	$2f_{transmit}$, $3f_{transmit}$, $4f_{transmit,...}$
	POFF	Spurious Output Signal	—	-60	—	dBm	Vps ≤0.1V
	PN	Phase Noise	—	-87	—	dBc/Hz	$f_{transmit}$ ± 500 kHz
	KVCO	VCO Gain	—	100	—	MHz/V	
	ICP	Charge Pump Current	—	±260	—	µA	
	VCLKOUT	Clock Voltage Swing	—	2	—	VPP	C_{load} = 5 pF
	t_{on}	Start-up Time	—	0.9	—	ms	**Note 2**

bit * These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Values dependent on PLL loop filter values.

Note 2: t_{on} equals crystal oscillator and PLL start-up time.

Note 3: Max FSK data rate requires crystal with appropriate motional parameters. See Section 6.3.

APPENDIX A: ADDITIONAL INFORMATION

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Code hopping encoder patents issued in European countries and U.S.A.

Secure learning patents issued in European countries, U.S.A. and R.S.A.

REVISION HISTORY

Revision B (June 2011)

- Updated the following sections: Development Support, The Microchip Web Site, Reader Response and rfHCS362G/362F Product Identification System
- Added new section **Appendix A**
- Minor formatting and text changes were incorporated throughout the document

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Device	Temperature Range	Package	Pattern

Device	rfHCS362G: RF Code Hopping Encoder rfHCS362F: RF Code Hopping Encoder rfHCS362GT: RF Code Hopping Encoder (Tape & Reel) rfHCS362FT: RF Code Hopping Encoder (Tape & Reel)		
Temperature Range	I	=	-40° C to+85° C
Package	SO SS	= =	300 mil SOIC 209 mil SSOP
Pattern	Special Requirements		

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