

#### **Description**

The ACE3413 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and Battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

#### **Features**

- -20V/-3.4A,  $R_{DS(ON)}=95m\Omega@V_{GS}=-4.5V$
- -20V/-2.4A,  $R_{DS(ON)}=120m\Omega@V_{GS}=-2.5V$
- -20V/-1.7A,  $R_{DS(ON)}$ =145m $\Omega$ @ $V_{GS}$ =-1.8V
- Super high density cell design for extremely low R<sub>DS(ON)</sub>
- Exceptional on-resistance and maximum DC current capability

#### **Application**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC
- LCD Display inverter

#### **Absolute Maximum Ratings**

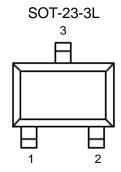
 $(T_A=25^{\circ}C$  Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	$V_{DSS}$	-20	٧	
Gate-Source Voltage	$V_{GSS}$	±12	V	
Continuous Drain Current (T <sub>J</sub> =150°C)		-3.5	Α	
T <sub>A</sub> =70°C	l <sub>D</sub>	-2.8	^	
Pulsed Drain Current	I <sub>DM</sub>	-15	Α	
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	-1.4	Α	
Power Dissipation T <sub>A</sub> =25°C	$P_{D}$	1.25	W	
Power Dissipation T <sub>A</sub> =70°C	' D	0.8		
Operating Junction Temperature	$T_J$	-55/150	$^{\circ}\!\mathbb{C}$	
Storage Temperature Range	T <sub>STG</sub>	-55/150	$^{\circ}\!\mathbb{C}$	
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	105	°C/W	

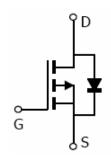




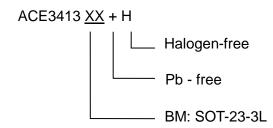
# **Packaging Type**



SOT-23-3L	Description
1	Gate
2	Source
3	Drain



# **Ordering information**



### **Electrical Characteristics**

 $(T_A=25^{\circ}C$ , Unless otherwise noted)

Parameter	Symbol	Conditions Min Typ		Тур	Max	Unit	
Static							
Drain-Source Breakdown Voltage	irce Breakdown Voltage $V_{(BR)DSS}$ $V_{GS}=0V$ , $I_D=-250uA$ -20		-20			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=-250uA$	-0.35		-0.8	V	
Gate Leakage Current	I <sub>GSS</sub>	$V_{DS}$ =0.V, $V_{GS}$ =±12V			±100	nA	
Zana Cata Valtana Duain Communi		$V_{DS}$ =-20V, $V_{GS}$ =0V			-1	uA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ =-20V, $V_{GS}$ =0V $T_J$ =55 $^{\circ}$ C			-5	uA	
On-State Drain Current	I <sub>D(ON)</sub>	$V_{DS}$ $\leq$ -5V, $V_{GS}$ =-4.5V	-6			Α	
Drain-Source On-Resistance	R <sub>DS(ON)</sub>	$V_{GS}$ =-4.5V, $I_{D}$ =-3.4A		0.076	0.095		
		$V_{GS}$ =-2.5V, $I_{D}$ =-2.4A		0.097	0.120		
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-1.7A		0.123	0.145	Ω	
		V <sub>GS</sub> =-1.25V, I <sub>D</sub> =-1.0A		0.185	0.210		
Forward Transconductance	Gfs	$V_{DS}$ =-5.0V, $I_{D}$ =-2.8A		6		S	
Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> =-1.5A, V <sub>GS</sub> =0V		-0.8	-1.2	V	
Dynamic							
Total Gate Charge	$Q_g$	\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		4.8	8		
Gate-Source Charge	$Q_{gs}$	$V_{DS}$ =-6V, $V_{GS}$ =-4.5V, $I_{D}$ $\equiv$ -2.8A		1.0		nC	
Gate-Drain Charge	$Q_{gd}$	ID=-2.0A		1.0			

2



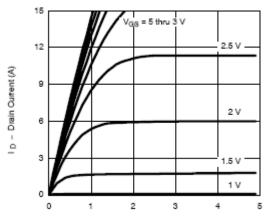
# **ACE3413**

### **P-Channel Enhancement Mode MOSFET**

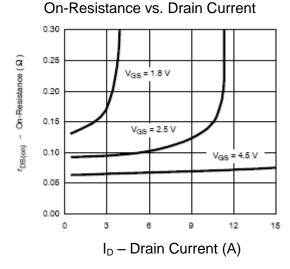
Input Capacitance	C <sub>iss</sub>	\/	485		
Output Capacitance	C <sub>oss</sub>	$V_{DS}$ =-6V, $V_{GS}$ =0V, f=1MHz	85		pF
Reverse Transfer Capacitance	$C_{rss}$	1-1101112	40		
Turn-On Time	$t_{d(on)}$	$V_{DD}$ =-6V, $R_{L}$ =6 $\Omega$ $I_{D}$ =-1.0A, $V_{GEN}$ =-4.5V $R_{O}$ =6 $\Omega$	10	16	
	t <sub>r</sub>		13	23	20
Turn-Off Time	t <sub>d(off)</sub>		18	25	ns
Turn-On Time	t <sub>f</sub>	11G 022	15	20	

# **Typical Characteristics**

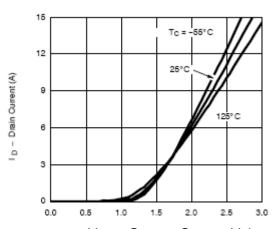
### **Output Characteristics**



V<sub>DS</sub> – Drain to Source Voltage (V)

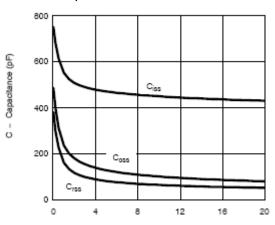


#### **Transfer Characteristics**



V<sub>GS</sub> – Gate to Source Voltage (V)

### Capacitance



V<sub>DS</sub> – Drain to Source Voltage (V)

3



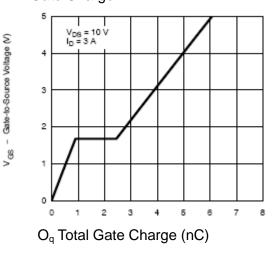
# **ACE3413**

#### P-Channel Enhancement Mode MOSFET

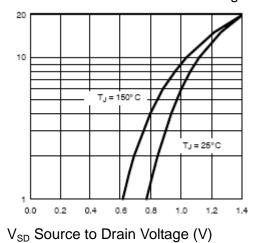
## **Typical Characteristics**

### Gate Charge

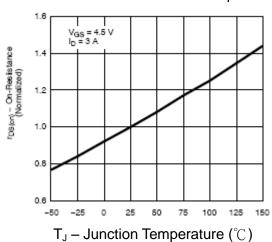
Is - Source Current (A)



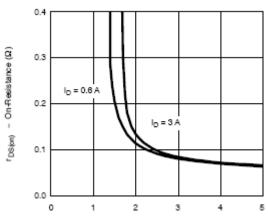
### Source-Drain Diode Forward Voltage



#### On-Resistance vs. Junction Temperature



### On-Resistance vs. Gate-to-Source Voltage



V<sub>GS</sub> – Gate to Source Voltage (V)

4





## **Typical Characteristics**

Threshold Voltage

0.4

0.3

0.2

0.1

0.1

0.1

0.2

-0.1

-0.2

-50

-25

0

25

50

75

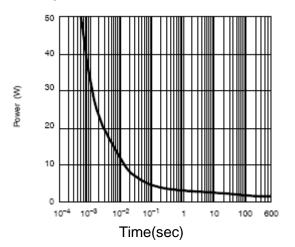
100

125

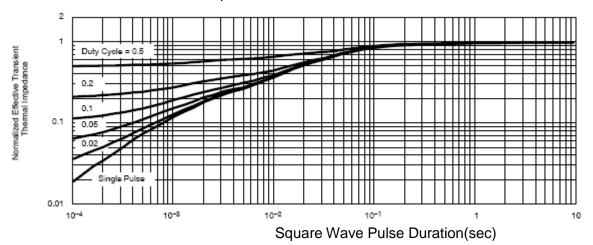
15

T<sub>J</sub> - Temperature

Single Pulse Power, Junction-To-Ambient



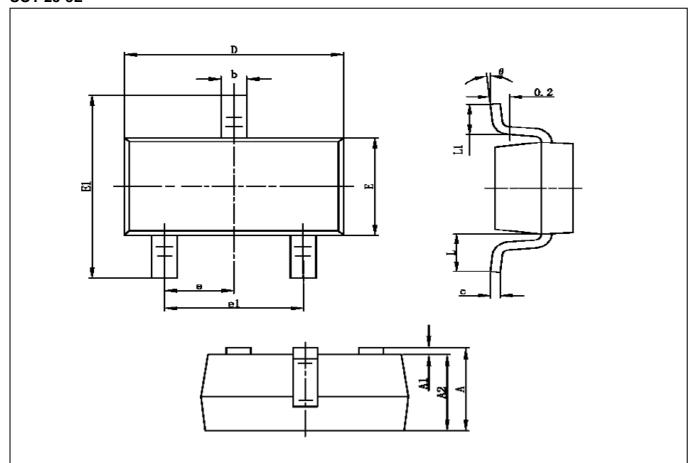
### Normalized Thermal Transient Impedance, Junction-to-Foot





# **Packing Information**

### SOT-23-3L



Cambal	Dimensions	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	1.050	1.250	0.041	0.049	
A1	0.000	0.100	0.000	0.004	
A2	1.050	1.150	0.041	0.045	
b	0.300	0.400	0.012	0.016	
С	0.100	0.200	0.004	0.008	
D	2.820	3.020	0.111	0.119	
E	1.500	1.700	0.059	0.067	
E1	2.650	2.950	0.104	0.116	
е	0.950TYP		0.037TYP		
e1	1.800	2.000	0.071	0.079	
L	0.700REF		0.028REF		
L1	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	



### ACE3413

#### P-Channel Enhancement Mode MOSFET

#### Notes

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- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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