ACE803N/ACE809N/ACE810N

Ultra Low Power Microprocessor Reset IC

Description

The ACE803N/ACE809N/ACE810N series are micro- processor (μP) supervisory circuits used to monitor the power supplies in μP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components.

These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold.

The ACE809N/810N have CMOS outputs, The ACE803N has open drain output. The ACE803N/809N have an active-low $\overline{\text{RESET}}$ output, while the ACE810N has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1.15V over the temperature range.

Features

- Precise Reset Threshold: ±2.5%
- CMOS Output(ACE809N/810N) and Open Drain Output(ACE803N)
- 140ms min Reset Pulse Width
- 3.2μA Supply Current @V_{CC}=3V
- Guaranteed Reset Valid to V_{CC} = +1.15V
- Power Supply Transient Immunity
- Operating Temperature Range: -40°C to +85°C

Application

- Computers
- Portable/Battery-Powered Equipment
- Intelligent Instruments
- Controllers

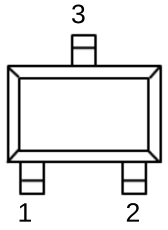
Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Terminal Voltage (With respect to GND)	V_{CC}	-0.3~6	V
	$\overline{\text{RESET}}$, RESET		
Input / Output Current	V_{CC}	20	mA
	$\overline{\text{RESET}}$, RESET		
Thermal resistance	θ_{JA}	300	℃/W
Operating Temperature	T_A	-40~85	℃
ESD Rating (HBM)		4	KV
Storage Temperature	T_S	-60 to 150	℃

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Packaging Type

SOT-23-3



SOT-23-3	Description	Function
1	GND	Ground terminal
2	$\overline{\text{RESET}}$ (ACE809N)	CMOS Output. This output remains low if V_{CC} drops below V_{RES}, and for at least 140ms after V_{CC} rises above V_{RES} + V_{HYST}
	RESET (ACE810N)	CMOS Output. This output remains high if V_{CC} drops below V_{RES}, and for at least 140ms after V_{CC} rises above V_{RES} + V_{HYST}
	$\overline{\text{RESET}}$ (ACE803N)	Open Drain Output. This output remains low if V_{CC} drops below V_{RES}, and for at least 140ms after V_{CC} rises above V_{RES} + V_{HYST}
3	Vcc	Analog Input. This pin is both the power supply to internal circuit and the voltage to be monitored

Ordering information

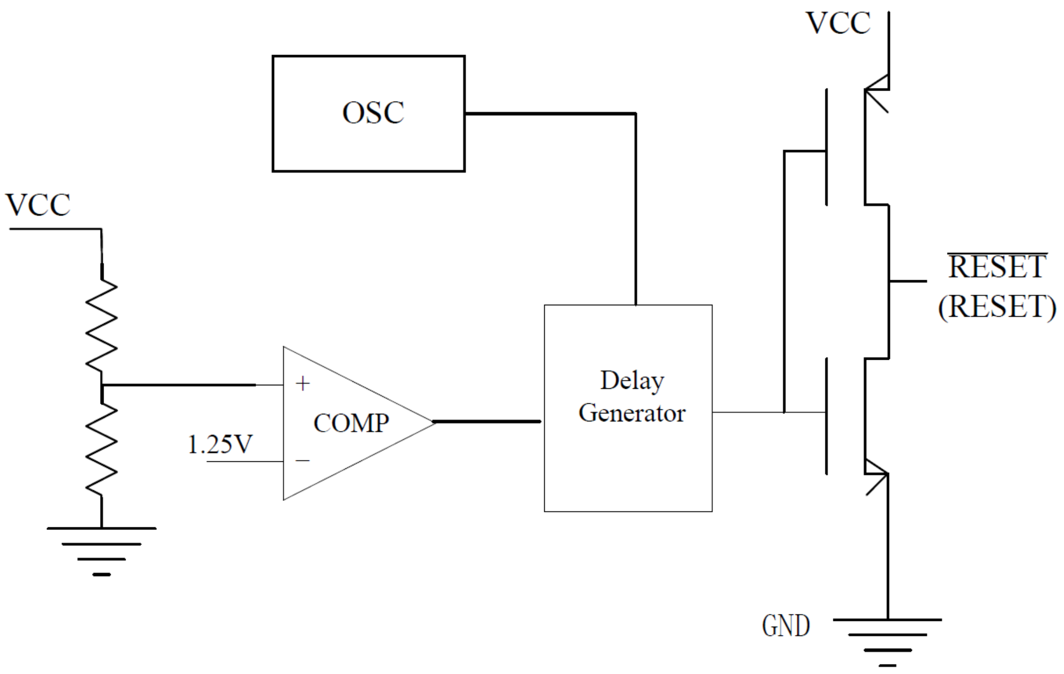
ACE803N/809N/810N X XX + H

- H: Halogen - free
- +: Pb - free
- XX: BM: SOT-23-3
- X: Voltage : L: 4.63V / M: 4.38V / J: 4.00V / T: 3.08V
  S: 2.93V / R: 2.63V

Device Function Reference Table:

Part No.	Reset threshold	Rest active Low or High	Output Type
ACE809NL	4.63V	Low	CMOS
ACE810NL		High	CMOS
ACE809NM	4.38V	Low	CMOS
ACE810NM		High	CMOS
ACE809NJ	4.00V	Low	CMOS
ACE809NT	3.08V	Low	CMOS
ACE810NT		High	CMOS
ACE809NS	2.93V	Low	CMOS
ACE810NS		High	CMOS
ACE809NR	2.63V	Low	CMOS
ACE810NR		High	CMOS
ACE803NS	2.93V	Low	Open Drain
ACE803NR	2.63V	Low	Open Drain

Block Diagram



Block Diagram For CMOS Output

Electrical Characteristics

Vcc=3V, T_A=-40℃ to 85℃, Typical values are at T_A=25℃,unless otherwise noted

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	Vcc		1.15		5.5	V
Supply Current	Icc	V_{CC}=2.0V		2.8	5.5	uA
		V_{CC}=3.0V		3.2	6	
		V_{CC}=5.0V		4.0	7.5	
Reset Threshold	V_{RES}	ACE8XXN-4.63	4.51	4.63	4.75	V
		ACE8XXN-4.38	4.25	4.38	4.50	
		ACE8XXN-4.00	3.89	4.00	4.11	
		ACE8XXN-3.08	3.00	3.08	3.15	
		ACE8XXN-2.93	2.86	2.93	3.00	
		ACE8XXN-2.63	2.56	2.63	2.70	
Reset Threshold hysteresis	V_{HYST}			0.013V_{RES}		V
V_{CC} to $\overline{RESET}$ Delay(ACE803N/ACE809N)		V_{CC} transitions from V_{RES}+0.1V to V_{RES}-0.1V		20		us
V_{CC} to RESET Delay(ACE810N)		V_{CC} transitions from V_{RES}+0.1V to V_{RES}-0.1V		20		us
RESET Output Voltage Low (ACE803N/ACE809N)	V_{OL}	$V_{RES}>V_{CC}$=2V,I_{SINK}=1.5mA			0.3	V
		$V_{RES}>V_{CC}$=3V,I_{SINK}=3.2mA				
		$V_{RES}>V_{CC}$=4V,I_{SINK}=5mA				
$\overline{RESET}$ Output Voltage High (ACE809N)	V_{OH}	$V_{RES}<V_{CC}$=3V,I_{SRC}=1.2mA	VCC-0.4			V
		$V_{RES}<V_{CC}$=4V,I_{SRC}=2mA				
		$V_{RES}<V_{CC}$=5V,I_{SRC}=2.5mA				
$\overline{RESET}$ Output Voltage Low (ACE810N)	V_{OL}	$V_{RES}<V_{CC}$=3V,I_{SINK}=3.2mA			0.3	V
		$V_{RES}<V_{CC}$=4V,I_{SINK}=5mA				
		$V_{RES}<V_{CC}$=5V,I_{SINK}=6mA				
RESET Output Voltage High (ACE810N)	V_{OH}	$V_{RES}>V_{CC}$=2V,I_{SRC}=600uA	VCC-0.4			V
		$V_{RES}>V_{CC}$=3V, I_{SRC}=1.2mA				
		$V_{RES}>V_{CC}$=4V, I_{SRC}=2mA				
Reset Pulse Width	T_{RES}		140	240	400	ms

Note : Parts are 100% production tested at 25℃. Specifications over full temperature range are guaranteed by design

Detailed Description

A microprocessor's (μP's) reset input starts the μP in a known state. The ACE803N/809N/810N series assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. The device consists of a comparator, a low current high precision voltage reference, voltage divider, output delay circuit and output driver. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The ACE809N/810N have a CMOS output stage, the ACE803N has an open drain output stage. The ACE803N/809N have an active-low $\overline{\text{RESET}}$ output, while the ACE810N has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1.15V over the temperature range.

The operation of the device can be best understood by referring to figure 3.

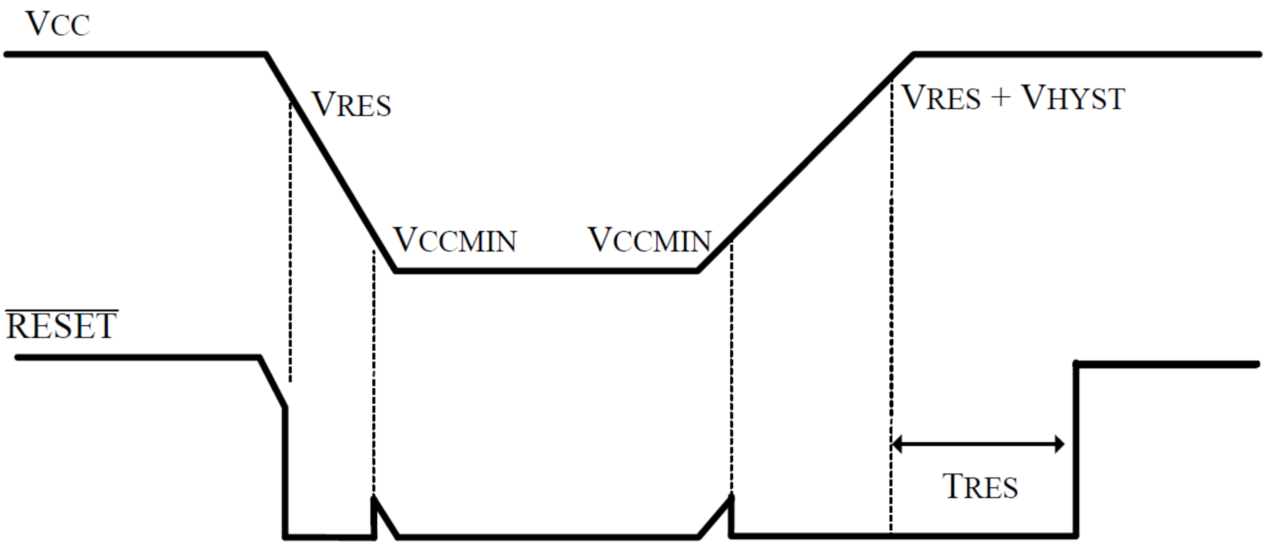


Fig. 2 Timing waveform

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the μP during power-up, power-down, and brownout conditions, the ACE803N/809N/810N series are relatively immune to short-duration negative-going V_{CC} transients (glitches). As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 10μs or less will not cause a reset pulse. A 0.1μF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Ensuring a Valid Reset Output Down to V_{CC} = 0

When V_{CC} falls below 1.15V, the ACE809N $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications, since most μP and other circuitry is inoperative with V_{CC} below 1.15V. However, in applications where $\overline{RESET}$ must be valid down to 0V, a pull-down resistor is needed from $\overline{RESET}$ pin to GND as shown in Figure 4, then $\overline{RESET}$ output will be held at low state. The resistor's value is not critical, it should be about 100KΩ, large enough not to load $\overline{RESET}$, small enough to pull $\overline{RESET}$ to ground.

A 100KΩ pull-up resistor to V_{CC} is also recommended for the ACE810N if active high RESET is required to remain valid for V_{CC} < 1.15V.

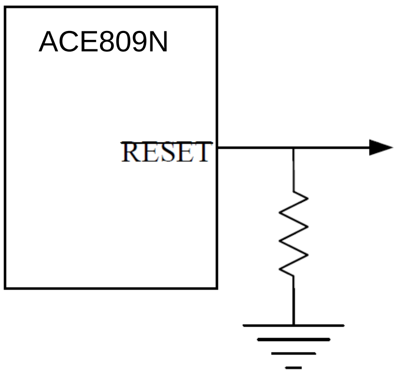
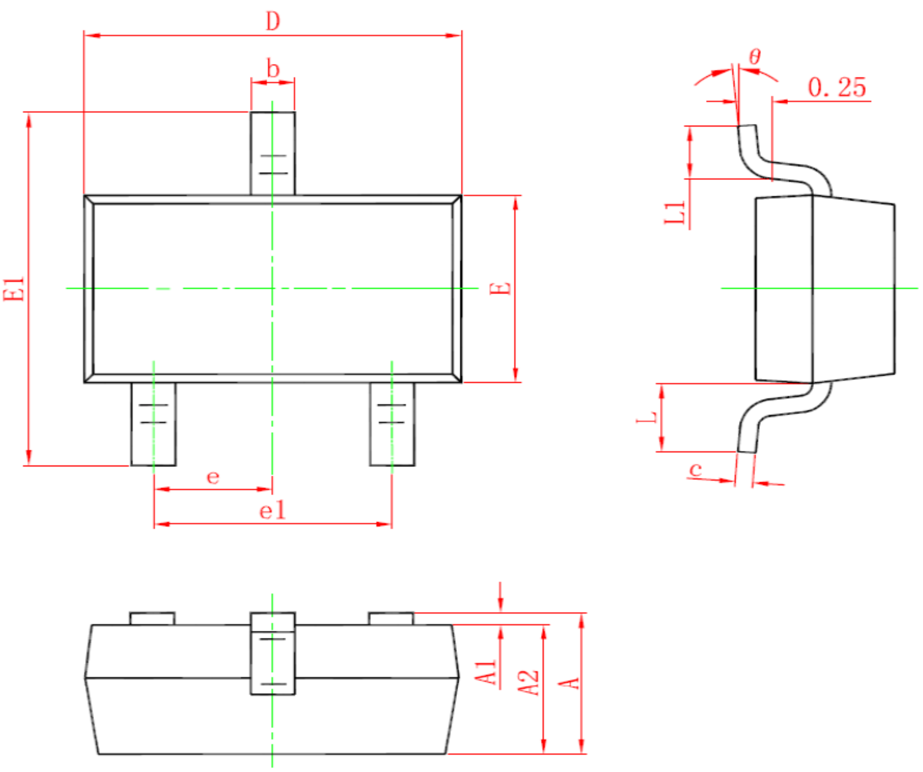


Fig. 3 RESET Valid to Ground Circuit

Packing Information

SOT-23-3



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Notes

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